

## 54ACT/74ACT573 Octal Latch with TRI-STATE® Outputs

### General Description

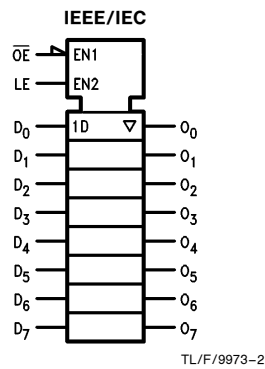
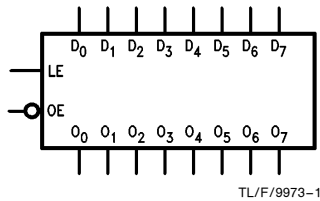
The 'ACT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( $\overline{OE}$ ) inputs.

The 'ACT573 is functionally identical to the 'ACT373 but has inputs and outputs on opposite sides.

### Features

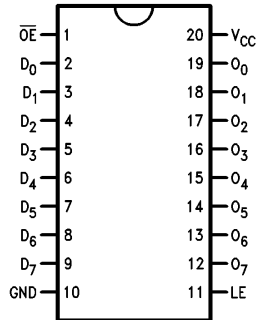
- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT373
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT573 has TTL-compatible inputs
- Standard Military Drawing (SMD)  
— 'ACT573: 5962-87664

### Logic Symbols



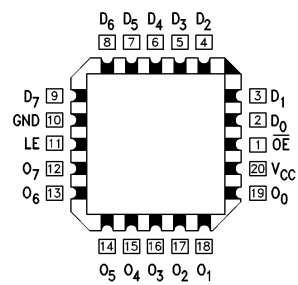
### Connection Diagrams

#### Pin Assignment for DIP, Flatpak and SOIC



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Latch Outputs

#### Pin Assignment for LCC



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## Functional Description

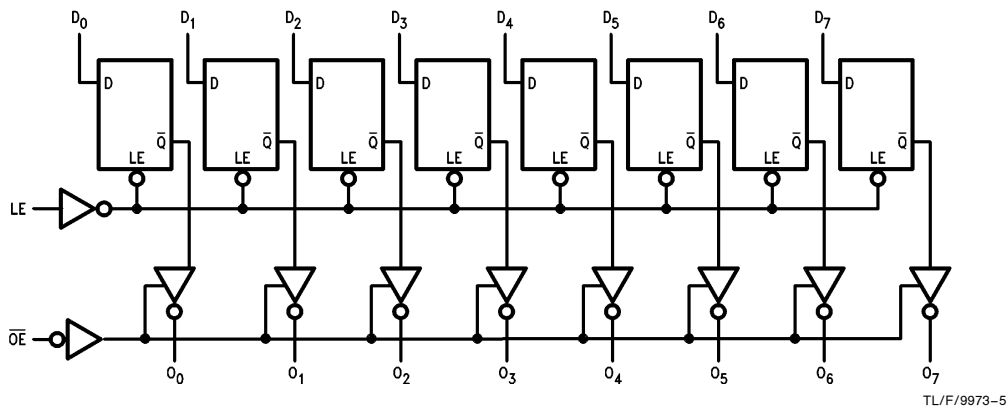
The 'ACT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are enabled. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

## Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	$O_n$
L	H	H	H
L	H	L	L
L	L	X	$O_0$
H	X	X	Z

H = HIGH Voltage  
 L = LOW Voltage  
 Z = High Impedance  
 X = Immaterial  
 $O_0$  = Previous  $O_0$  before HIGH-to-LOW transition of Latch Enable

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	-20 mA
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	-20 mA
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
CDIP	175°C
PDIP	140°C

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
'ACT	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
74ACT	-40°C to +85°C
54ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

## DC Characteristics for 'ACT Family Devices

Symbol	Parameter	$V_{CC}$ (V)	74ACT		54ACT		74ACT		Units	Conditions
			$T_A = +25^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			
			Typ	Guaranteed Limits						
$V_{IH}$	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	2.0	2.0	2.0	2.0			
$V_{IL}$	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	0.8	0.8	0.8	0.8			
$V_{OH}$	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	4.4	V	$I_{OUT} = -50 \mu\text{A}$	
		5.5	5.49	5.4	5.4	5.4	5.4			
		4.5		3.86	3.70	3.76	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$		
		5.5		4.86	4.70	4.76				
$V_{OL}$	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		5.5	0.001	0.1	0.1	0.1				
		4.5		0.36	0.50	0.44	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$		
		5.5		0.36	0.50	0.44				
$I_{IN}$	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	$V_I = V_{CC}, \text{GND}$		
$I_{OZ}$	Maximum TRI-STATE Leakage Current	5.5		$\pm 0.25$	$\pm 5.0$	$\pm 2.5$	$\mu\text{A}$	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{GND}$		

\*All outputs loaded; thresholds on input associated with output under test.

## DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	74ACT		54ACT		74ACT		Units	Conditions
			T <sub>A</sub> = +25°C		T <sub>A</sub> = -55°C to +125°C		T <sub>A</sub> = -40°C to +85°C			
			Typ	Guaranteed Limits						
I <sub>CC</sub> T	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.6		1.5		mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	† Minimum Dynamic Output Current	5.5			50		75		mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>		5.5			-50		-75		mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5		4.0	80.0		40.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND

† Maximum test duration 2.0 ms, one output loaded at a time.

**Note:** I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT			54ACT		74ACT		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay D <sub>m</sub> to O <sub>n</sub>	5.0	2.5	6.0	10.5	1.5	13.5	2.0	12.0	ns
t <sub>PHL</sub>	Propagation Delay D <sub>n</sub> to O <sub>n</sub>	5.0	2.5	6.0	10.5	1.5	13.5	2.0	12.0	ns
t <sub>PLH</sub>	Propagation Delay LE to O <sub>n</sub>	5.0	3.0	6.0	10.5	1.5	13.0	2.5	12.0	ns
t <sub>PHL</sub>	Propagation Delay LE to O <sub>n</sub>	5.0	2.5	5.5	9.5	1.5	12.0	2.0	10.5	ns
t <sub>PZH</sub>	Output Enable Time	5.0	2.0	5.5	10.0	1.5	11.5	1.5	11.0	ns
t <sub>PZL</sub>	Output Enable Time	5.0	1.5	5.5	9.5	1.5	11.0	1.5	10.5	ns
t <sub>PHZ</sub>	Output Disable Time	5.0	2.5	6.5	11.0	1.5	13.5	1.5	12.5	ns
t <sub>PLZ</sub>	Output Disable Time	5.0	1.5	5.0	8.5	1.5	10.5	1.0	9.5	ns

\*Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT	54ACT	74ACT	Units	
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF	T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Typ	Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to LE	5.0	1.5	3.0	4.5	3.5	ns
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to LE	5.0	-1.5	0	1.0	0	ns
t <sub>w</sub>	LE Pulse Width, HIGH	5.0	2.0	3.5	5.0	4.0	ns

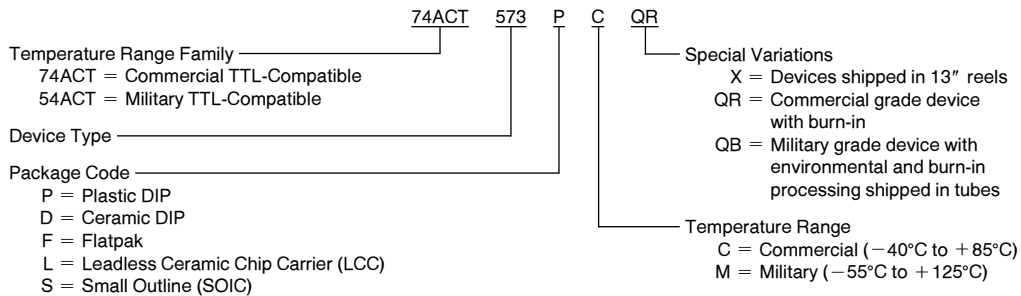
\*Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

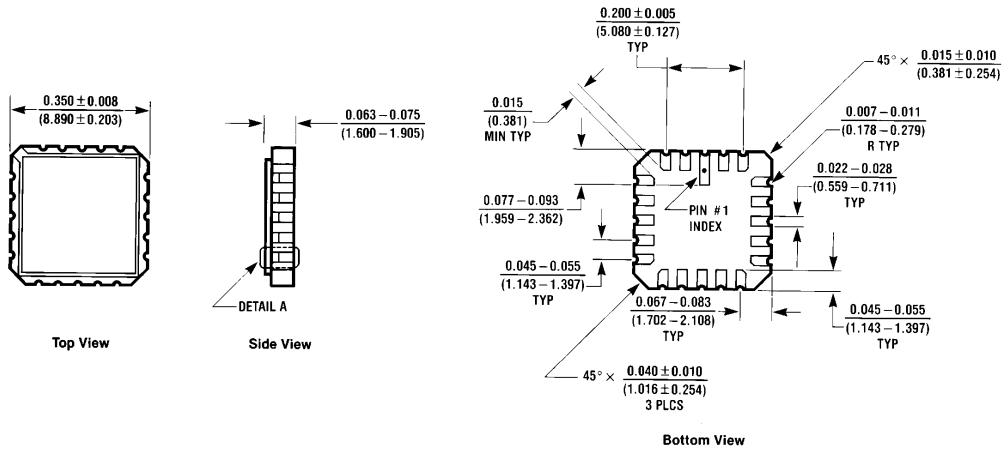
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	5.0	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	25.0	pF	V <sub>CC</sub> = 5.0V

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

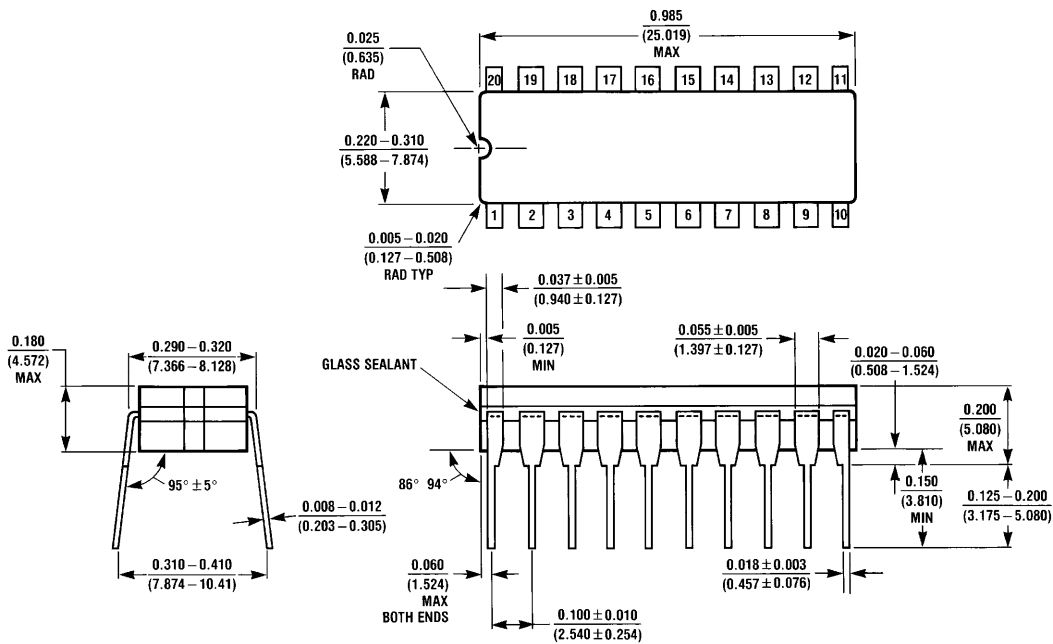


**Physical Dimensions** inches (millimeters)



E20A (REV D)

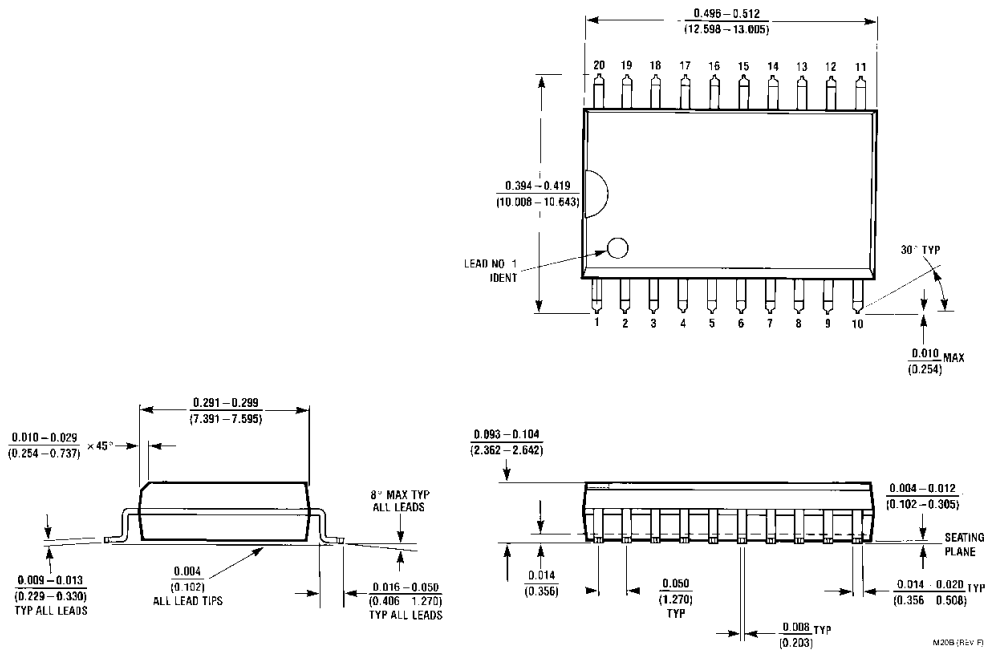
**20 Terminal Ceramic Leadless Chip Carrier (L)  
NS Package Number E20A**



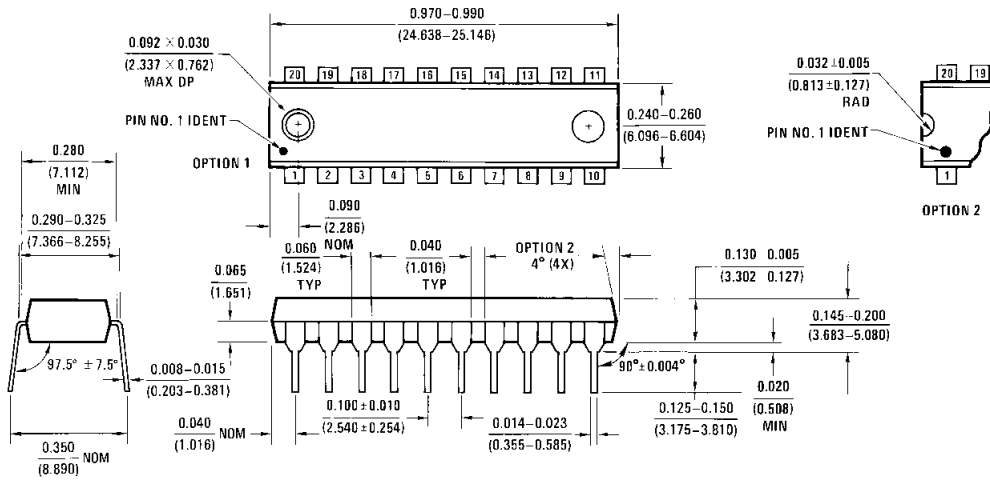
J20A (REV M)

**20-Lead Ceramic Dual-In-Line Package (D)  
NS Package Number J20A**

**Physical Dimensions** inches (millimeters) (Continued)

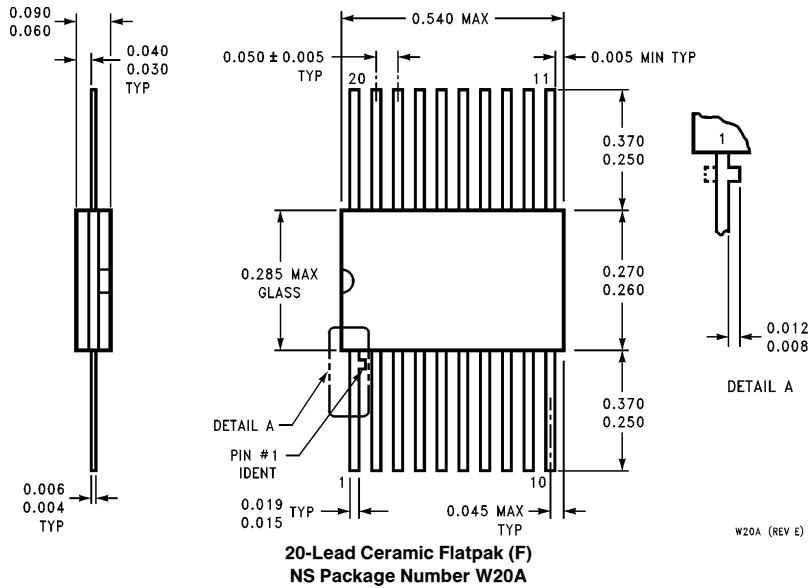


**20-Lead Small Outline Integrated Circuit (S)  
NS Package Number M20B**



**20-Lead Plastic Dual-In-Line Package (P)  
NS Package Number N20B**

**Physical Dimensions** inches (millimeters) (Continued)



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