



Title	<i>Reference Design Report for 14.5 W Standby and 300 W Main Power Supply Using HiperTFS™ TFS762HG</i>
Specification	300 VDC – 385 VDC Input; 5 V, 2.9 A (Standby) and 12 V, 25 A (Main) Outputs
Application	PC Power Supply
Author	Applications Engineering Department
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Summary and Features

- High efficiency Main and Standby converters
- Remote on/off
- Built-in main and standby undervoltage thresholds protection ensures graceful power supply start-up and shutdown
- Latching output overvoltage protection
- Integrated high-side driver
- Output short-circuit and open loop protection
- Main transformer reset protection
- Flat standby overload versus input voltage

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.powerint.com/ip.htm>.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an AC isolation transformer to the DC power supply or power factor stage used to provide the input voltage.



1 Introduction

This document is an engineering report describing a 5 V, 2.9 A Standby and a 12 V, 25 A Main power supply utilizing the TFS762HG device from the HiperTFS family. This example power supply uses a fixed DC input voltage, but in a typical application, it would be connected to a PFC boost input stage, delivering approximately 385 VDC to implement a 300 W power supply with various output voltages. A lab bench DC power supply capable of 400 VDC at 3 A or an AC input rectifier stage is required supply to the input for evaluation. It is also possible to use the power factor circuit RDK-236 to provide the regulated 385 VDC needed to power RDK-249.

Typically PC power supplies have a universal AC input power factor corrected (PFC) input stage but as the bias standby supply must operate before the PFC stage is active, the Standby output must operate with the DC equivalent of universal AC input voltages (85 VAC to 265 VAC and 100 VDC to 400 VDC).

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

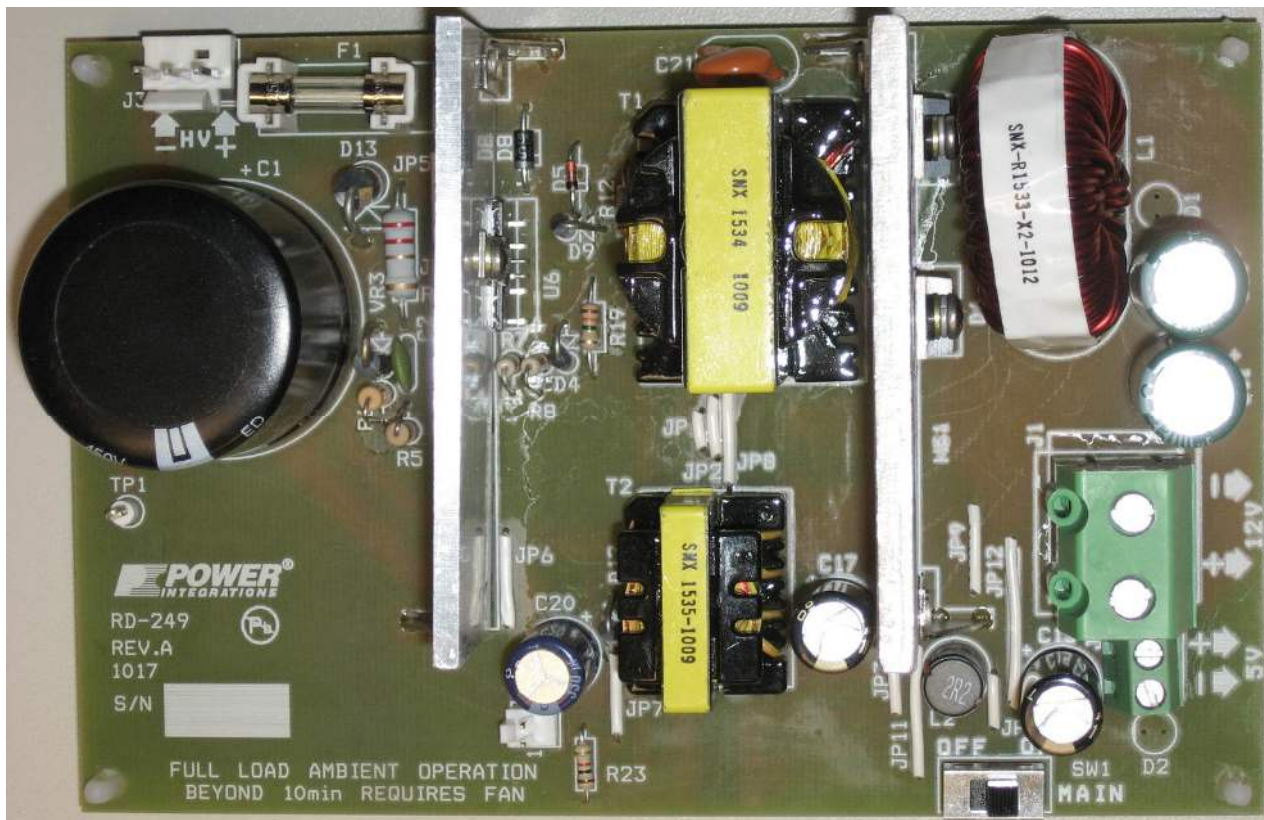


Figure 1 – Populated Circuit Board Photograph.



2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Standby only Voltage	V_{IN}	100		420	VDC	Equivalent to 85 VAC - 295 VAC
Main and Standby Voltage	V_{IN}	300	380	420	VDC	
No-load Input Power (324 VDC)	P_{IN}			0.3	W	Equivalent to 230 VAC Standby only
Output						
Output Voltage 1 (standby)	V_{OUT1}	4.75	5.00	5.25	V	$\pm 5\%$, 40 mA minimum load
Output Current 1 (standby)	I_{OUT1}	0.04	2.9	5	A	$\pm 10\%$
Output Ripple Voltage 1 (standby)	$V_{RIPPLE1}$			50	mV	20MHz bandwidth
Output Voltage 2 (main 12 V)	V_{OUT2}	11.4	12.00	12.6	V	$\pm 5\%$, 100mA minimum load
Output Current 2 (main 12 V)	I_{OUT2}	0.1	25	28.33	A	$\pm 10\%$
Output Ripple Voltage 2 (main 12 V)	$V_{RIPPLE2}$			120	mV	20 MHz bandwidth
Total Output Power 1	P_{OUT1}		14.5	20	W	For Standby only
Total Output Power 2	P_{OUT2}		300		W	For Main 12 V only
Total Output Power 3	P_{OUT3}		314.5		W	For both Main and Standby
Total Peak Output Power	P_{PEAK}		380		W	For both Main and Standby
Holdup Time	$T_{HOLD UP}$	20 ms			ms	For P_{OUT3}
Efficiency						
Main and Standby	η	86.5			%	100% Load
Standby Only	η		76		%	100% Load
Ambient Temperature	T_{AMB}	0		50	$^{\circ}\text{C}$	Forced cooling, sea level

Table 1 –Power Supply Specifications Using TFS762HG

Note 1: All measurements performed with 380 VDC input unless otherwise specified

Note 2: For output voltage tolerance and ripple see minimum/maximum allowed current

Note 3: Total peak DC output power will not exceed 365 W at 50 $^{\circ}\text{C}$ with forced cooling

Note 4: Peak Main power is 340 W (excluding Standby)

Note 5: Absolute maximum Standby power is less than 25 W (excluding Main)

Note 6: Full load operation at room temperature beyond 10 minutes requires a 30 CFM

fan



3 Schematic

Missing from this schematic are any mechanical/assembly part like mounting holes, screws, heat-sing brackets etc.

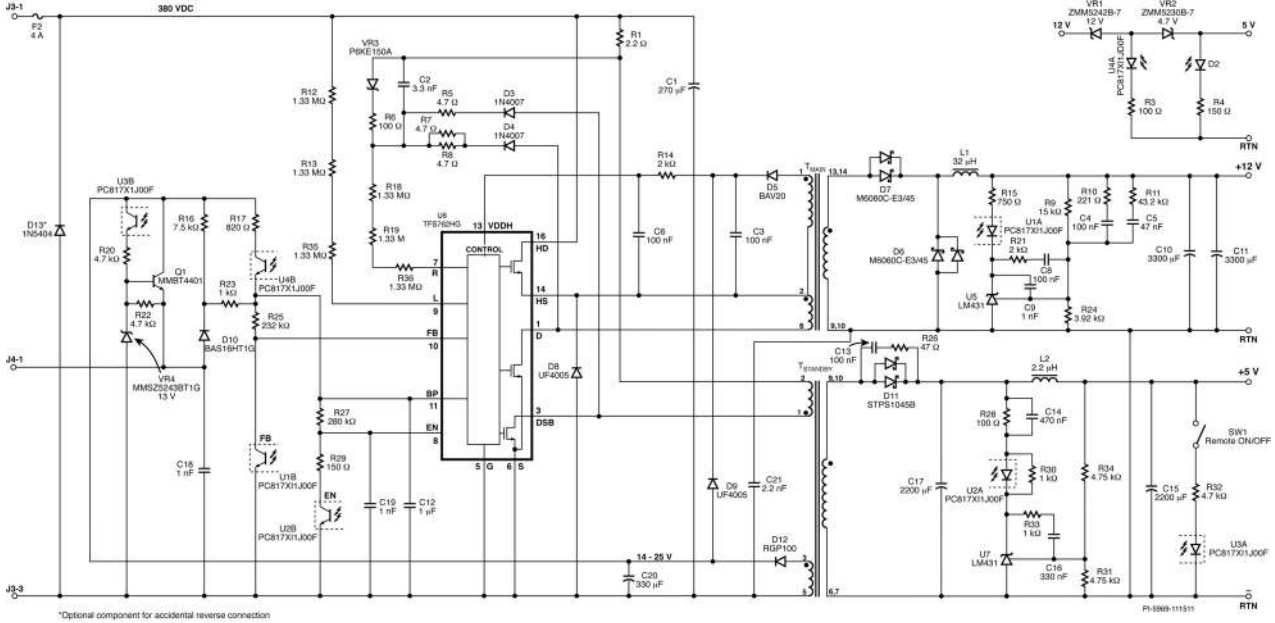


Figure 2 – Schematic.



4 Circuit Description

The HiperTFS TFS762HG cost effectively incorporates a low-side 725 V Main MOSFET, a high-side 530 V Main MOSFET and a 725 V Standby MOSFET, main and standby controllers, a high-side driver along with thermal shutdown and other fault protection and other control circuitry in a single package. The device is well suited for high power applications with both main and standby converter (such as PC power supplies). The standby operates over a wide input voltage range. The main converter is intended to accept boosted input voltage from a power-factor correction stage and normally operates over a range from 385 VDC to 300 VDC

4.1 Power Input and Filter

This circuit is designed for PC power supplies with a Main output power up to 300 W. Diode D13 provides protection against catastrophic failure in case of reverse input voltage connection which would cause fuse F1 to open. Capacitor C1 is the bulk energy storage element providing energy for at least 20 ms at full load from 385 VDC initial input voltage.

4.2 Primary Side

Components C2, R1, R6 and VR3 form a turn-off clamping circuit that limits the drain voltage of U6 for both the standby drain and the drain of the low-side Main Drain of the forward converter. Zener VR3 provides a defined clamp voltage and maintains a maximum voltage (150 V) on clamp capacitor C2. Most of the leakage and magnetizing energy is returned back to converter due to the slow recovery aspect of the general recovery diodes D3 and D4. Shared reset/leakage spike clamp between Main and Standby reduces component count. The Standby is connected via diode D3 and resistor R5 and the Main section is connected through D8 and D4 together with R7 and R8. During the reset time, the Main section is connected to a substantially higher reset voltage than V_{IN} , hence the Main operating duty cycle of the Main converter can operate above 50% which lowers RMS switch currents without penalizing holdup time.

The BYPASS (BP) pin along with C12 provides a decoupled operating voltage for the HiperTFS controller. At start-up the bypass capacitor is charged from an internal device current source. When the BP pin voltage reaches 5.8 V the standby converter will begin switching and both the +5 V standby output and primary-side bias voltage will begin to rise. The output of the bias/auxiliary supply winding is rectified by diode D12 and filtered by capacitor C20. Output of the bias winding is used to supply power via resistor R16 to the HiperTFS BP pin during standby only operation. Additional current is provided by Q1 and D10 by the primary bias supply when remote-on switch SW1 activates U3A and U3B and commands Q1 into an ON state. In a complete PC power supply application, this voltage is used to supply bias to the PFC controller through J4 connector. The value of R16 is selected to maintain the minimum 700 μ A required into BP pin to inhibit the internal HiperTFS high voltage current source and thus reduce no-load consumption. Capacitor C12 connected to the BP pin of U6 provides decoupling for the internally



regulated 5.85 V supply. Zener diode VR4 provides a voltage reference for Q1 to regulate the emitter voltage to 12.4 V for a stable 6 mA into BP pin.

The ENABLE (EN) pin is the feedback pin for the Standby controller section. Prior to the start-up a resistor R27 connected from EN to BP can be detected to select one of several internal current limits for Standby section. FEEDBACK (FB) pin resistor R25 can also be used to select one of three Main current limits at start-up in the same manner as the EN pin. Four different resistor values can be used for R27 to select one of the four internal current limit configurations for the Standby section, and three different values for R25 to select one of the three current limit configurations for the Main section. The circuit presented here uses R27 (280 k Ω) for a standby I_{LIM} of 650 mA and R25 for a Main I_{LIM} of 3.5 A.

The FB pin provides feedback for the Main converter. An increase in current sink from FB pin to ground will lead to a reduction in the operating duty cycle.

Diode D9 is used to provide the initial power for the bootstrap charging C3 and C6 during start-up. During this time the high-side MOSFET HS pin is briefly pulled to Source for 12 ms. Once the main converter begins switching after the initial 12 ms bootstrap delay, diode D5 is used to provide the internal nominal power for the high-side section from the Main transformer support winding, pins 1 and 2. The normal voltage on C6 during normal operation is shunt regulated to approximately 12 V. It is necessary to insure at all times a minimum of 13 V on C3.

Resistors R18, R19, and R36 are used to translate the maximum available OFF time reset voltage into a current for the R pin and compare with the L pin current to compute the maximum allowable duty cycle to prevent saturation and also determines the maximum allowable duty factor as a function of peak on-time flux.

The LINE-SENSE (L) pin provides an input bulk voltage line-sense function. This information is used by the under-voltage and over-voltage detection circuits for both the Main and standby sections. This pin can also be pulled down to SOURCE to implement a remote-ON/OFF of both the Standby and Main supplies simultaneously. Resistors R12, R13, and R35 are used to translate the input voltage into a current for L pin.

4.3 Output Rectification

For the Standby section, output rectification is provided by diode D11. A low ESR capacitor, C17, provides filtering with low ripple. Inductor L2 and capacitor C15 form a post-filter to further reduce switching ripple and noise in the output.

For the Main section diode D7 rectifies during Main on-time and diode D6 is the catch diode to provide a current discharge path for the output inductor, L1, during the Main off-time. Inductor L1 together with capacitors C10 and C11 form an output filter out switching output ripple and noise.



4.4 Output Feedback

For the Standby section, resistor R34 and R31 form a network divider. The output voltage of the power supply is divided and fed to the input terminal of error amplifier U7. The cathode terminal voltage of U2A is controlled by the amplifier inside U7 to maintain the divider voltage to 2.5 V +/-2%. Change in cathode terminal voltage results in a change of the current through optocoupler diode inside U2A, which in turn changes the current through the transistor inside U2B. Capacitor C19 provides strong noise rejection for the EN pin. When the current sinking from the EN pin exceeds the EN pin threshold current, the next switching cycle is inhibited, and when the output voltage falls below the feedback threshold, a conduction cycle is allowed to occur. By adjusting the number of enabled cycles, output regulation is maintained. As the load reduces, the number of enabled cycles decreases lowering the effective switching frequency and scales the switching losses with load. This provides almost constant efficiency down to very light loads, ideal for meeting energy efficiency requirements.

For the Main section, resistors R9 and R24 are employed to provide the DC reference for the U5 error amplifier. In a similar manner, U5 controls the optocoupler U1 used to adjust the operating duty cycle through the current sink from the FB pin with the main difference being the FB pin current controls the duty cycle of the main converter in a linear manner versus the whole cycle on/off control of the standby converter.

4.5 Output Overvoltage Protection

The output OV protection for both Main and Standby is provided through optocoupler U4. If the feedback loop is broken or for any other internal or external reason, the output voltage increases over the maximum allowed limit, VR1 and/or VR2 are used to activate the protection circuit built around U4. When the output of U4B turns on, the current flow into the BP pin exceeds the latching shutdown threshold current of 15 mA. This will trigger the latching shutdown feature of HiperTFS and the device stops switching, protecting the output. The latching condition disables switching until the latch is reset with source current into the L pin below 10 μ A.



5 PCB Layout

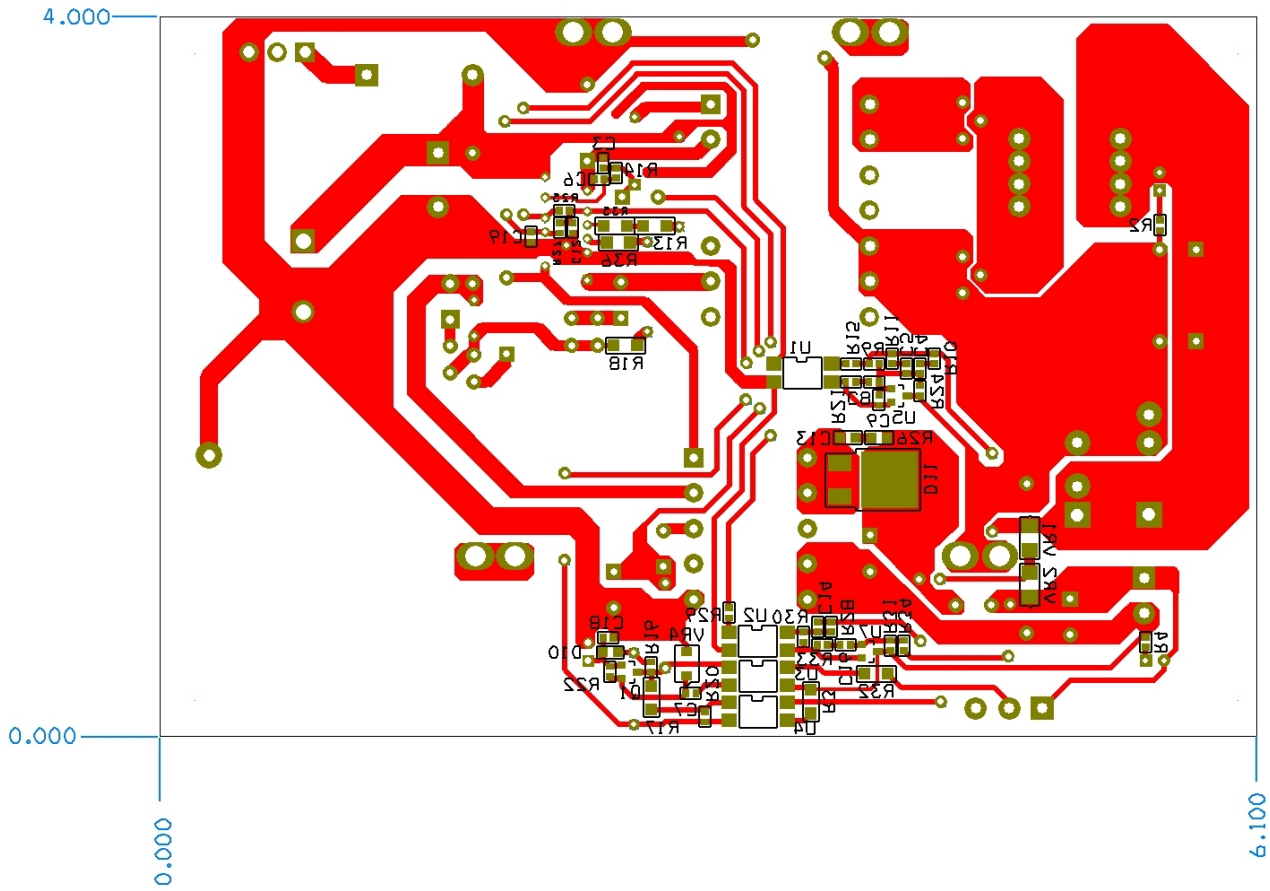


Figure 3 – Printed Circuit Layout, Bottom Side.



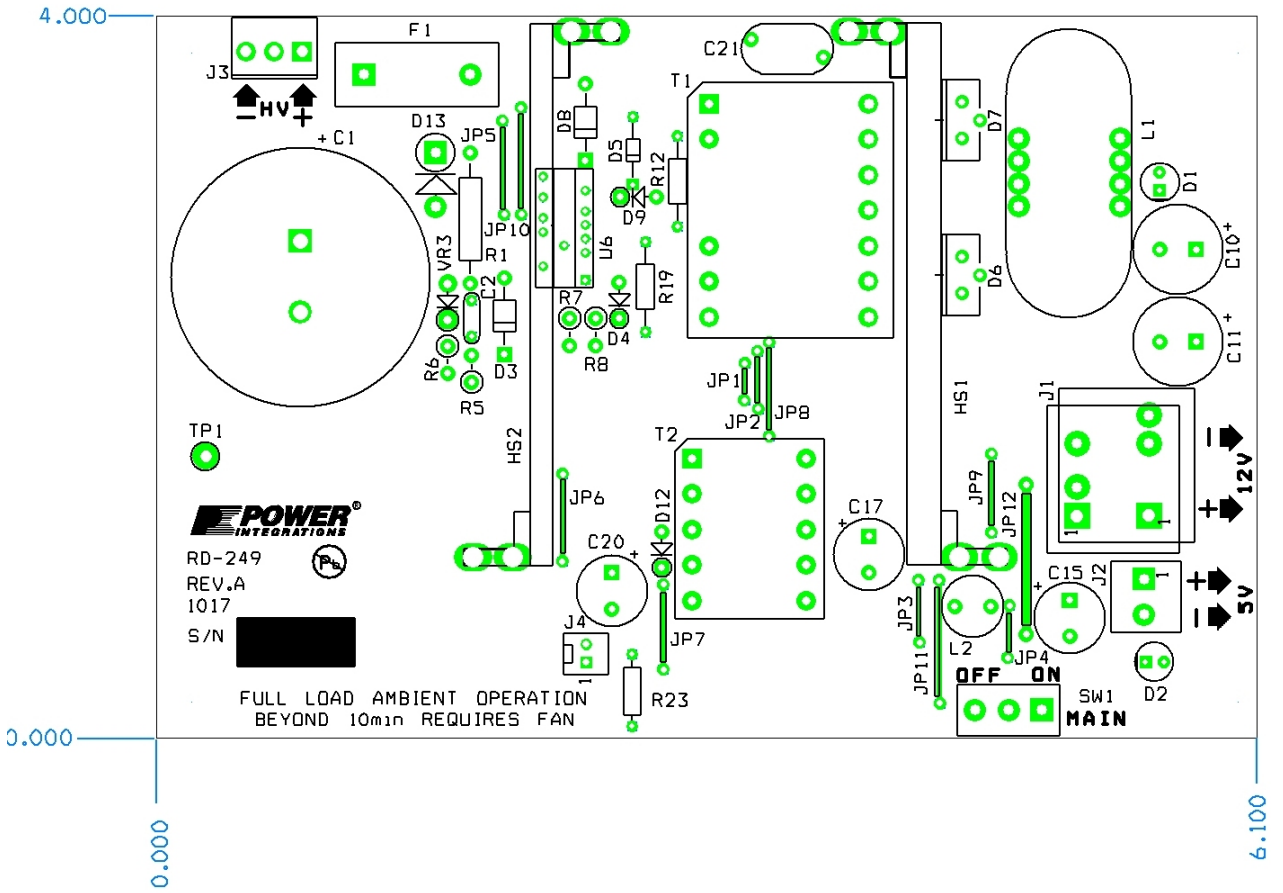


Figure 4 – Printed Circuit Layout, Top Side.



6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	270 μ F, 450 V, Electrolytic, (35 x 35)	EET-ED2W271EA	Panasonic
2	1	C2	3.3 nF, 1 kV, Disc Ceramic	NCD332M1KVZ5U	NIC
3	4	C3 C4 C6 C8	100 nF 25 V, Ceramic, X7R, 0603	ECJ-1VB1E104K	Panasonic
4	1	C5	47 nF 16 V, Ceramic, X7R, 0603	ECJ-1VB1C473K	Panasonic
5	1	C7	470 pF 50 V, Ceramic, X7R, 0603	ECJ-1VC1H471J	Panasonic
6	3	C9 C18 C19	1000 pF, 100 V, Ceramic, COG, 0603	C1608C0G2A102J	TDK
7	2	C10 C11	3300 μ F, 16 V, Electrolytic, Very Low ESR, 15 m Ω , (12.5 x 35)	EKZE160ELL332MK35S	Nippon Chemi-Con
8	1	C12	1 μ F, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
9	1	C13	1 nF, 100 V, Ceramic, X7R, 0805	ECJ-2VB2A102K	Panasonic
10	1	C14	470 nF, 50 V, Ceramic, Y5G, 0603	C1608Y5V1H474Z	TDK
11	2	C15 C17	2200 μ F, 10 V, Electrolytic, Low ESR, (10 x 25)	10MCZ1000M10X25	Rubycon
12	1	C16	330 nF, 16 V, Ceramic, Y5G, 0603	ECJ-1VF1C334Z	Panasonic
13	1	C20	330 μ F, 35 V, Electrolytic, Low ESR, 68 m Ω , (10 x 16)	ELXZ350ELL331MJ16S	Nippon Chemi-Con
14	1	C21	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
15	1	D1	LED, Yellow, 5 mm, 585 nm, 30 mcd	SSL-LX5093YD	Lumex Opto
16	1	D2	LED, Green, 5 mm, 565 nm, 30 mcd	SSL-LX5093GD	Lumex Opto
17	2	D3 D4	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
18	1	D5	200 V, 200 mA, Fast Switching, 50 ns, DO-35	BAV20	Vishay
19	2	D6 D7	60 V, 60 A, Dual Schottky, TO-220AB	M6060C-E3/45	Vishay
20	2	D8 D9	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
21	1	D10	75 V, 200 mA, Rectifier, SOD323	BAS16HT1G	ON Semi
22	1	D11	45 V, 10 A, Schottky Low Drop, SMD, DPAK	STPS1045B-TR	ST
23	1	D12	50 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4001-E3	Vishay
24	1	D13	OBS non RoHS use 15-00796-00. 400 V, 3 A, Rectifier, DO-201AD	1N5404	Vishay
25	1	ESIP CLIP1	Heatsink Hardware, Edge Clip xxN (xx lbs) 14.33 mm L x 6.35 mm W	TRK-24	Kang Tang Hardware
26	1	F1	FUSEHOLDER OPEN 5 X 20 MM PC MNT	64900001039	Wickmann
27	1	F2	6.3 A, 250 V, Fast, 5 mm x 20 mm, Cartridge	021706.3HXP	Littlefuse
28	1	GREASE1	Thermal Grease, Silicone, 5 oz Tube	CT40-5	ITW Chemtronics
29	2	HEATSINK BRACKET RIGHT1 HEATSINK BRACKET RIGHT2	Bracket, Heatsink, Right		Custom
30	2	HEATSINK BRACKET3 HEATSINK BRACKET4	Bracket, Heatsink, Left		Custom
31	2	HS PAD1 HS PAD2	HEATSINK PAD, TO-220, Sil-Pad 1000	1009-58	Bergpuist
32	1	HS1	HEATSINK, RDK249-Diode-Hsink, Alum 5052, 3.00" L x 1.650" W x 0.187" Thk	61-00041-00	Custom



33	1	HS2	HEATSINK, RDK249-eSIP-Hsink, Alum 5052, 3.00" L x 1.650" W x 0.125" Thk	61-00042-00	Custom
34	1	J1	2 Position (1 x 2) header, 10.16 mm (0.400) pitch, Vertical	1706785	Phoenix Contact
35	1	J1_OPTIO	2 Position (1 x 2) header, 10.16 mm (0.400) pitch, Vertical	39910-0102	Molex
36	1	J2	2 Position (1 x 2) header, 5 mm (0.196) pitch, Vertical	1715022	Phoenix Contact
37	1	J3	CONN HEADER 3POS (1x3).156 VERT TIN	26-64-4030	Molex
38	1	J4	2 Position (1 x 2) header, 0.1 pitch, Vertical	22-23-2021	Molex
39	1	JP1	Wire Jumper, Insulated, 22 AWG, 0.2 in	C2004-12-02	Gen Cable
40	3	JP2 JP3 JP4	Wire Jumper, Insulated, 22 AWG, 0.3 in	C2004-12-02	Gen Cable
41	5	JP5 JP6 JP7 JP8 JP9	Wire Jumper, Insulated, 22 AWG, 0.5 in	C2004-12-02	Gen Cable
42	2	JP10 JP11	Wire Jumper, Insulated, 22 AWG, 0.7 in	C2004-12-02	Gen Cable
43	1	JP12	Wire Jumper, Insulated, 22 AWG, 0.8 in	C2004-12-02	Gen Cable
44	1	JP13	0 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
45	1	L1	32 μ H,xA, Power Iron Toroid, 8P	SNX-R1533	Santronics USA
46	1	L2	2.2 μ H, 6.0 A	RFB0807-2R2L	Coilcraft
47	4	POST-CRKT_BRD_6-32_HEX1-4	Post, Circuit Board, Female, Hex, 6-32, snap, 0.375L, Nylon	561-0375A	Eagle Hardware
48	1	Q1	NPN, Small Signal BJT, GP SS, 40 V, 0.6 A, SOT-23	MMBT4401LT1G	On Semi
49	1	R1	2.2 Ω , 5%, 1 W, Metal Film, Fusible	NFR0100002208JR500	Vishay
50	1	R2	470 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ471V	Panasonic
51	1	R3	100 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-3GEYJ101V	Panasonic
52	2	R4 R29	150 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ151V	Panasonic
53	3	R5 R7 R8	4.7 Ω , 5%, 1/2 W, Carbon Film	CFR-50JB-4R7	Yageo
54	1	R6	100 Ω , 5%, 1/2 W, Carbon Film	CFR-50JB-100R	Yageo
55	1	R9	15 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ153V	Panasonic
56	1	R10	221 Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2210V	Panasonic
57	1	R11	43.2 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4322V	Panasonic
58	2	R12 R19	1.33 M Ω , 1%, 1/4 W, Metal Film	271-1.33M/REEL-RC	Xicon
59	4	R13 R18 R35 R36	1.33 M Ω , 1%, 1/4 W, Thick Film, 1206	MCR18EZH1334	Rohm
60	1	R14	2 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ202V	Panasonic
61	1	R15	750 Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF7500V	Panasonic
62	1	R16	7.5 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF7501V	Panasonic
63	1	R17	820 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ821V	Panasonic
64	2	R20 R22	4.7 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ472V	Panasonic
65	1	R21	2 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2001V	Panasonic
66	1	R23	1 k Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-1K0	Yageo
67	1	R24	3.92 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3921V	Panasonic
68	1	R25	232 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2323V	Panasonic
69	1	R26	200 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ201V	Panasonic
70	1	R27	280 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2803V	Panasonic
71	1	R28	100 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
72	2	R30 R33	1 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic



73	2	R31 R34	4.75 k Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4751V	Panasonic
74	1	R32	4.7 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ472V	Panasonic
75	4	RIVET1 RIVET2 RIVET3 RIVET4	Rivet, Al, .093 Dia x 0.187 (3/16) L, 100 Deg Countersunk, soft, 1100-F Aluminum		Olander
76	4	RIVET5 RIVET6 RIVET7 RIVET8	Rivet, Al, .093 Dia x 0.250 (1/4) L, 100 Deg Countersunk, soft, 1100-F Aluminum		Olander
77	1	SCREW1	SCREW MACHINE PHIL 4-40 X 1/4 SS	PMSSS 440 0025 PH	Building Fasteners
78	2	SCREW2 SCREW3	SCREW MACHINE PHIL 4-40 X 5/16 SS	PMSSS 440 0031 PH	Building Fasteners
79	1	SW1	SLIDE MINI SPDT PC MNT AU	1101M2S3CBE2	ITT Ind/C&Kdiv
80	1	T1	Custom Transformer, Vertical, 14 pins Bobbin	SNX-R1534 YC-3508	Santronics USA Ying Chin
81	1	T2	Custom Transformer, Vertical, 10 Pins Bobbin	SNX-R1535 YW-360-02B	Santronics USA Yih-Hwa
82	1	TP1	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
83	4	U1 U2 U3 U4	Optocoupler, TRAN OUT 4-SMD	PC817XI1J00F	Sharp
84	2	U5 U7	OBS see 45-00144-00 2.495 V Shunt Regulator IC, 2%, -40 to 85C, SOT23	LM431AIM	National Semiconductor
85	1	U6	TFS762HG, ESIP16/12	TFS762HG	Power Integrations
86	1	VR1	12 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5242B-7	Diodes Inc
87	1	VR2	4.7 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5230B-7	Diodes Inc
88	1	VR3	150 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE150A	LittleFuse
89	1	VR4	13 V, 5%, 500 mW, SOD-123	MMSZ5243BT1G	ON Semi
90	3	WASHER 1, 2, 3	Washer, Lk, #4 SS	4NSLWS	Olander
91	2	WASHER 4, 5	Washer FLAT #4 SS	FWSS 004	Building Fasteners
92	2	WASHER 6, 7	Washer, Shoulder, Nylon, #4	3049	Keystone



7 Standby Transformer Specification

7.1 Electrical Diagram

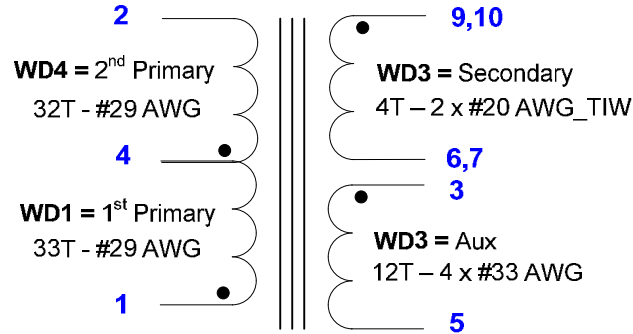


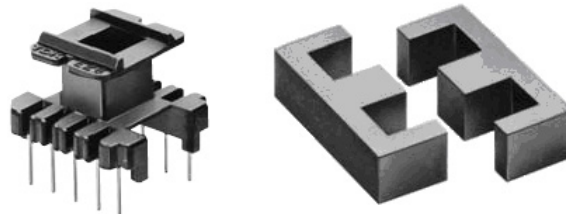
Figure 5 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-5 to pins 6-10	3000 VAC
Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz, 0.4 V _{RMS}	850 μH, ±10%
Resonant Frequency	Pins 1-2, all other windings open	2.15 MHz Min
Leakage Inductance	Pins 1-2, with secondary pins shorted, measured at 100 kHz, 0.4 V _{RMS}	18 μH Max

7.3 Materials

Item	Description
[1]	Core: TDK EE25 part #: PC40EE25.4-Z
[2]	Bobbin: EE25, Vertical, 10 pins, (5/5), Yhi Hwa part #: YW-360-02B
[3]	Magnet wire: #29 AWG
[4]	Magnet wire: #33 AWG
[5]	Magnet wire: #20 AWG Triple Insulated Wire
[6]	Tape: 3M 1298 Polyester Film, 2 mils thick, 10.8 mm wide
[7]	Varnish



7.4 Transformer Build Diagram

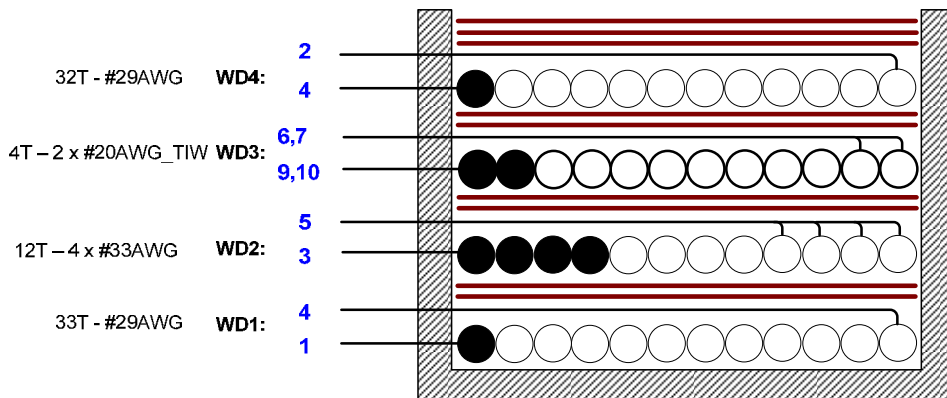


Figure 6 – Transformer Build Diagram.

7.5 Transformer Construction

Winding Preparation	Position the bobbin on the mandrel such that the pin side is on the left side of bobbin mandrel. Winding direction is clock-wise direction
WD1: 1st Primary	Start at pin 1, wind 33 turns of wire item [3] from left to right with tight tension in one layer, at the last turn bring the wire back to the left and terminate at pin 4
Insulation	2 layers of tape item [6]
WD2: Auxiliary	Start at pin 3, wind 12 quad-filar turns of wire item [4] from left to right also with tight tension in one layer, at the last turn bring the wire back to the left and terminate at pin 5
Insulation	2 layers of tape item [6]
WD3: Secondary	Start at pin 9, 10 wind 4 bi-filar turns of wire item [5] from left to right also with tight tension in one layer, at the last turn bring the wire back to the left and terminate at pin 6, 7
Insulation	2 layers of tape item [6]
WD4: 2nd Primary	Start at pin 4, wind 32 turns of wire item [3] from right to left with tight tension in one layer, at the last turn bring the wire back to the right and terminate at pin 2
Insulation	3 layers of tape item [6]
Finish	Assemble, grind the cores to get 2.15 mH and secure with tape. Varnish [7]



8 Main Transformer Specification

8.1 Electrical Diagram

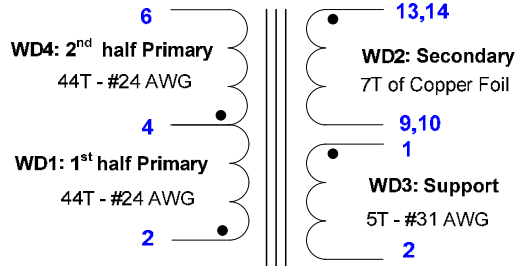


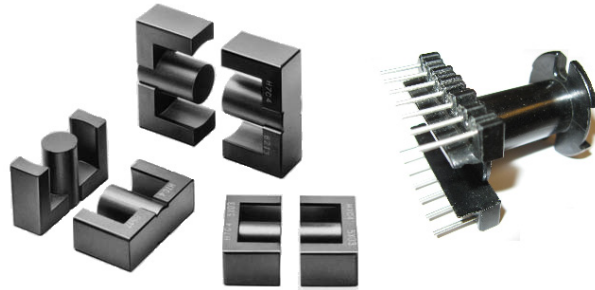
Figure 7 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-7 to pins 8-14	3000 VAC
Primary Inductance	Pins 2-6, all other open, measured at 50 kHz, 0.4 V _{RMS}	23 mH, ±25%
Resonant Frequency	Pins 2-6, all other open	200 kHz (Min.)
Primary Leakage	Pins 2-6, with pins 8-14 shorted, measured at 50 kHz, 0.4 V _{RMS}	25 μH (Max.)

8.3 Materials

Item	Description
[1]	Core: TDK part #:PC40HEER35-Z
[2]	Bobbin: EER35, Vertical, 14 pins, (7/7), YingChin part #: YC-3508
[3]	Magnet wire: #24 AWG Heavy Nyleze (Solderable Polyurethane-Nylon, Class 130°C Type B)
[4]	Magnet wire: #31 AWG Heavy Nyleze (Solderable Polyurethane-Nylon, Class 130°C Type B)
[5]	Copper Foil: 8 mils thick (see Fig. 3)
[6]	Tape: 3M 1298 Polyester Film, 2 mil thick, 25.5 mm wide
[7]	Tape: 3M 1298 Polyester Film, 2 mil thick, 36.0 mm wide
[8]	Tape: 3M 44 Margin tape (cream), 3.0 mm wide
[9]	Tape: 3M 44 Margin tape (cream), 6.0 mm wide
[10]	Varnish



8.4 Transformer Build Diagram

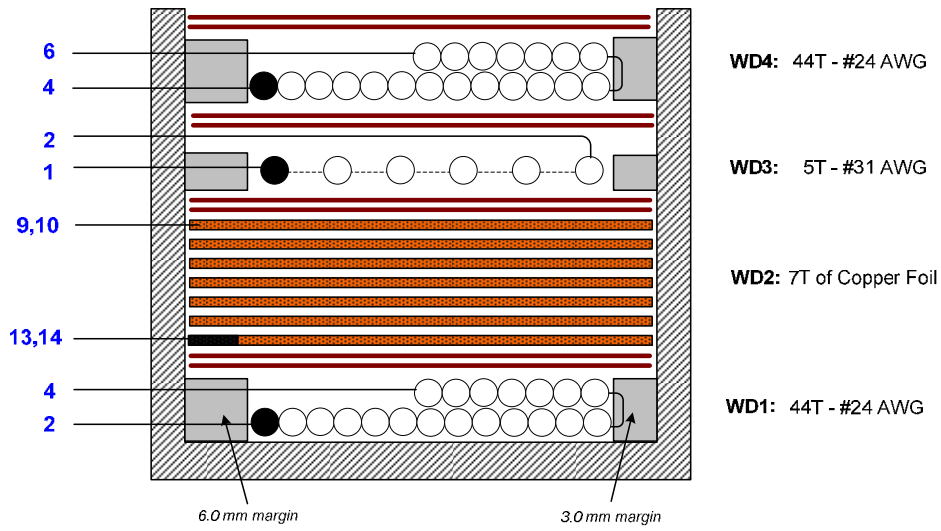


Figure 8 – Transformer Build Diagram.

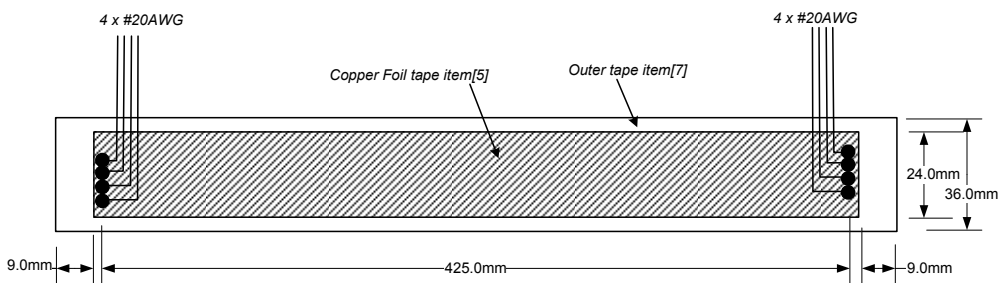


Figure 9 – Copper Foil Preparation.



8.5 Transformer Construction

Winding Preparation	Position the bobbin on the mandrel such that the pin side is on the left side of bobbin mandrel. Winding direction is clock-wise direction
Margin Tape	Place margin tape 6.0 mm item [9] for the left side and 3.0 mm item [8] for the right side matching with height of WD1
WD1: 1st Half Primary	Start at pin 2, wind 44 turns of wire item [3] from left to right and right to left in 1 ½ layers and terminate at pin 4
Insulation	2 layers of tape item [6]
Copper Foil	Prepare the copper foil as in above figure
WD2: Secondary	Use copper foil item [5], start at pins 13, 14, wind 7 turns with tight tension and end at pins 9, 10
Insulation	2 layers of tape item [6]
Margin Tape	Place margin tape 6.0mm item [9] for the left side and 3.0mm item [8] for the right side matching with height of WD3
WD3: Support	Start at pin 1, wind 5 turns item [4] from left to right, at the last turn bring the wire back to the left to terminate at pin 2
Insulation	2 layers of tape item [6]
Margin Tape	Place margin tape 6.0 mm item [9] for the left side and 3.0 mm item [8] for the right side matching with height of WD4
WD4: 2nd Half Primary	Start at pin 4, wind 44 turns of wire item [3] from left to right and right to left in 1 ½ layers and terminate at pin 6
Insulation	2 layers of tape item [6]
Finish	Assemble and secure the cores with tape. Varnish item [7]



9 Main Output Inductor Specification

9.1 Electrical Diagram

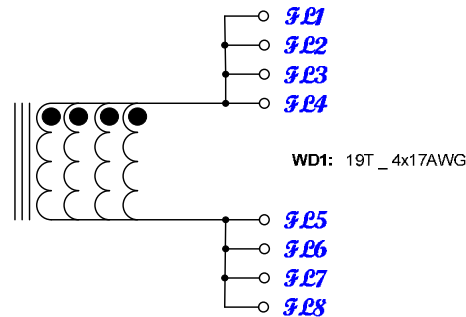


Figure 10 – Inductor Electrical Diagram.

9.2 Electrical Specifications

Core Effective Inductance		AL = 95 nH/N ²
Inductance (LCM)	Pins 1-2 measured at 100 kHz	35.8 μH ±10%

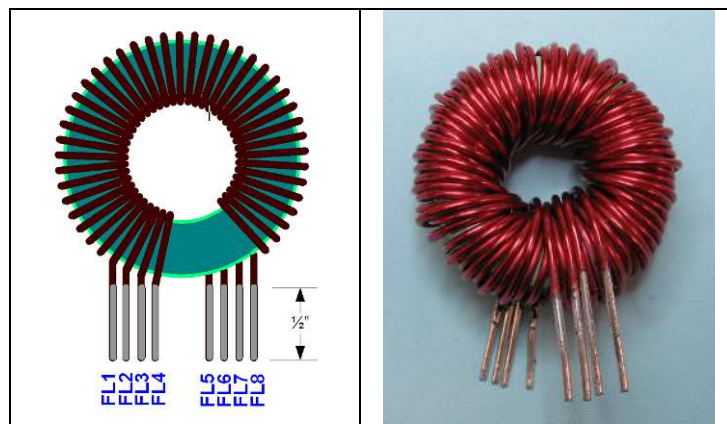
9.3 Materials

Item	Description
[1]	Toroid: Micrometals, part#: T132-52
[2]	Magnet Wire: #17 AWG, solderable double coated

9.4 Winding Instructions

- Use 4 wires of item [2] about 100 cm long, wind 19 turns in ~2 layers firmly and in one direction. Start with FL1, FL2, FL3, FL4, end with FL5, FL6, FL7, FL8, and leave ~ 1/2" long.
- Tin all leads ~1/2"

9.5 Inductor Illustrations



10 Transformer Design Spreadsheet

(Note – Output current is made 4.20 A in the spreadsheet to account for load on the auxiliary output)

HiperTFS_Two-switch_Forward_092110 ; Rev.1.04; Copyright Power Integrations 2010	INPUT	INFO	OUTPUT	UNIT	HiperTFS_092110 Two-switch Forward Transformer Design Spreadsheet
HiperTFS MAIN OUTPUT (TWO-SWITCH FORWARD STAGE) OUTPUT VOLTAGE AND CURRENT					
VMAIN	12.00			V	Main output voltage
IMAIN	25.00			A	Main output current
VOUT2				V	Output2 voltage
IOUT2				A	Output2 current
POST REGULATED OUTPUT					
Post Regulator	NONE	<i>Info</i>			!!!! Info. No Selection for post-regulator - select 'NONE' if not using post-regulator
V_SOURCE				V	Select source of input voltage for post regulator
VOUT3			0.0	V	Enter postregulator output voltage
IOUT3			0.0	A	Enter post regulator output current
n_PR			1		Enter postregulator efficiency (Buck only)
COUPLED-INDUCTOR (LOW POWER) DERIVED OUTPUT					
VOUT4	12.00			V	Coupled-Inductor derived (low power) output voltage (typically -12 V)
IOUT4	0.10			A	Coupled-Inductor derived (low power) output current
POUT(Main)			301.2	W	Total output power (Main converter)
POUT_PEAK(Main)	340.00		340.0	W	Peak Output power(Main converter). If there is no peak power requirement enter value equal to continuous power
POUT(Standby)			10.3	W	Continuous output power from Standby power supply
POUT_PEAK(Standby)			14.5	W	Peak output power from Standby section
POUT(System Total)			311.5	W	Total system continuous output power
POUT_PEAK(System Total)				W	Total system peak output power
VBIAS	17.00			V	DC bias voltage from main transformer aux winding
INPUT VOLTAGE AND UV/OV					
CIN			269.92	uF	Input Capacitance. To increase CMIN, increase T_HOLDUP
T_HOLDUP			20.00	ms	Holdup time
VMIN			300	V	Minimum input voltage to guarantee output regulation
VNOM			380	V	Nominal input voltage
VMAX			420	V	Maximum DC input voltage
UV / OV / UVOV		min	max		
VUV OFF		236.0	287.9	V	Minimum undervoltage On-Off threshold
VUV ON		300.0	344.7	V	Maximum undervoltage Off-On threshold (turn-on)
VOV ON		480.4	-	V	Minimum overvoltage Off-On threshold
VOV OFF		664.5	-	V	Minimum overvoltage On-Off threshold (turn-off)
RR			4.00	M-ohm	R pin resistor
RL	4		4.00	M-ohm	Line Sense resistor value (L-pin) - goal seek (VUV OFF) for std 1% resistor series
ENTER DEVICE VARIABLES					
Device	TFS762				Selected HiperTFS device
Chosen Device			TFS762		
ILIMIT_MIN			3.25	A	Device current limit (Minimum)
ILIMIT_TYP			3.50	A	Device current limit (Typical)
ILIMIT_MAX			3.75	A	Device current limit (Maximum)
fSMIN			61500	Hz	Device switching frequency (Minimum)
fS			66000	Hz	Device switching frequency (Typical)



fSMAX			70500	Hz	Device switching frequency (Maximum)
KI	1.0		1.0		Select Current limit factor (KI=1.0 for default ILIMIT, or select KI=0.8 or KI=0.6)
R(FB)			232.0	k-ohms	Feedback Pin Resistor value
ILIMIT SELECT			3.25	A	Selected current limit
RDS(ON)			3.05	ohms	Rds(on) at 100°C
DVNOM_GOAL	0.448		0.45		Target duty cycle at nominal input voltage (VNOM)
VDS			5.28	V	HiperTFS average on-state Drain to Source Voltage
Clamp Selection	CLAMP TO RAIL				Select either "CLAMP TO RAIL" (default) or "CLAMP TO GND"
VCLAMP	150.00		150.00	V	Asymmetric Clamp Voltage
VDSOP			570.00	V	Maximum HiperTFS Drain voltage (at VOVOFF_MAX)
DIODE Vf SELECTION					
VDMAIN			0.5	V	Main output diodes forward voltage drop
VDOUT2			0.5	V	Secondary output diodes forward voltage drop
VDOUT3			0.5	V	3rd output diodes forward voltage drop
VDB			0.7	V	Bias diode forward voltage drop
TRANSFORMER CORE SELECTION					
Core Type	EER35				Selected core type
<i>Core</i>		EER35		P/N:	PC40EER35-Z
<i>Bobbin</i>		EER35	BOBBIN	P/N:	BEER-35-1116CPH
AE			1.07	cm ²	Core Effective Cross Sectional Area
LE			9.08	cm	Core Effective Path Length
AL			2770	nH/T ²	Ungapped Core Effective Inductance
BW			26.1	mm	Bobbin Physical Winding Width
M			4.5	mm	Bobbin safety margin tape width (2 * M = Total Margin)
LG MAX			0.002	mm	Maximum zero gap tolerance, default 2um
L			3.00		Transformer primary layers (split primary recommended)
NMAIN			7.0		Main rounded turns
NS2			0.0		Vout2 rounded secondary turns (Independent windings)
NBIAS			5		VBIAS rounded turns (forward bias winding)
VOUT2 ACTUAL			0.0	V	Approximate Output2 voltage of with NS2 = 0 turns (AC stacked secondary)
VBIAS_ACTUAL			16.3	V	Approximate Forward Bias Winding Voltage at VMIN with NB = 5 turns
TRANSFORMER DESIGN PARAMETERS					
NP			88		Primary rounded turns
BM_MAX			1791	Gauss	Max positive operating flux density at minimum switching frequency
BM PK-PK			2714	Gauss	Max peak-peak operating flux density at minimum switching frequency
BP_MAX			2321	Gauss	Max positive flux density at Vmax (limited by DVMAX clamp)
BP PK-PK			3516	Gauss	Max peak-peak flux density at Vmax (limited by DVMAX clamp)
LP MIN			20.60	mHenries	Minimum primary magnetizing inductance (assumes LG MAX=2um)
IMAG			0.123	A	Peak magnetizing current at minimum input voltage
OD_P			0.58	mm	Primary wire outer diameter
AWG_P			23	AWG	Primary Wire Gauge (rounded to maximum AWG value)
DUTY CYCLE VALUES (REGULATION)					
DVMIN			0.57		Duty cycle at minimum DC input voltage
DVNOM			0.45		Duty cycle at nominal DC input voltage
DVMAX			0.40		Duty cycle at maximum DC input voltage



DOVOFF_MIN			0.25		Duty cycle at over-voltage DC input voltage(DOVOFF_MIN)
MAXIMUM DUTY CYCLE VALUES					
DMAX_UVOFF_MIN			0.62		Max duty cycle clamp at VUVOFF_MIN
DMAX_VMIN			0.60		Max duty clamp cycle at VMIN
DMAX_VNOM			0.58		Max duty clamp cycle at VNOM
DMAX_VMAX			0.52		Max duty clamp cycle at VMAX
DMAX_OVOFFMIN			0.33		Max duty clamp cycle at VOVOFF_MAX
CURRENT WAVESHAPe PARAMETERS					
IP			2.39	A	Maximum peak primary current at maximum DC input voltage
IP_PEAK			2.69	A	Peak primary current at Peak Output Power and max DC input voltage
IPRMS(NOM)			1.38	A	Nominal primary RMS current at nominal DC input voltage
OUTPUT INDUCTOR OUTPUT PARAMETERS					
KDI_ACTUAL			0.27		Current ripple factor of combined Main and Output2 outputs
Core Type	Pow Iron		Pow Iron		Select core type
Core	T132-52(O.D)=33)		T132-52(O.D)=33)		Coupled Inductor - Core size
AE			80.5	mm^2	Core Effective Cross Sectional Area
LE			79.6	mm	Core Effective Path Length
AL			95.0	nH/T^2	Ungapped Core Effective Inductance
BW			55.9	mm	Bobbin Physical Winding Width
VE			6410.0	mm^3	
Powder cores (Sendust and Powdered Iron) Cores					
MUR			75.0		Relative permeability of material
H			64.9	AT/cm	Magnetic field strength
MUR_RATIO			0.48		Percent of permeability as compared to permeability at H = 0 AT/cm
LMAIN_ACTUAL			16.4	uH	Estimated inductance of main output at full load
LMAIN_0bias			34.3	uH	Estimated inductance of main output with 0 DC bias
LOUT2			0.0	uH	Estimated inductance of auxilliary output at full load
BM_IND			2919.0	Gauss	DC component of flux density
BAC_IND			402.8	Gauss	AC component of flux density
Turns					
INDUCTOR TURNS MULTIPLIER	2.7		2.7		Multiplier factor between main number of turns in transformer and inductor (default value = 3)
NMAIN_INDUCTOR			19.0		Main output inductor number of turns
NOUT2_INDUCTOR			0.0		Output 2 inductor number of turns
NOUT4_INDUCTOR			12.0		Bias output inductor number of turns (for bias or control circuit VDD supply)
Ferrite Cores					
LMAIN_ACTUAL			N/A	uH	Estimated inductance of main output
LOUT2			N/A	uH	Estimated inductance of aux output
LG			N/A	mm	Gap length of inductor cores
Target BM			N/A	Gauss	Target maximum flux density
BM_IND			N/A	Gauss	Estimated maximum operating flux density
BAC_IND			N/A	Gauss	AC flux density
Turns					
NMAIN_INDUCTOR			N/A		Main output inductor number of turns
NAUX_INDUCTOR			N/A		Aux output inductor number of turns
N_BIAS			N/A		Aux output inductor number of turns
Wire Parameters					
Total number of layers			1.06		Total number of layers for chosen toroid
IRMS_MAIN			25.0	A	RMS current through main inductor windings
IRMS_AUX			0.0	A	RMS current through aux winding
AWG_MAIN			15.0	AWG	Main inductor winding wire gauge
OD_MAIN			1.5	mm	Main winding wire gauge outer diameter



FILAR_MAIN			2.0		Number of parallel strands for main output
RDC_MAIN			4.3	mohm	Reisistance of wire for main inductor winding
AC Resistance Ratio (Main)			4.0		Ratio of total resistance (AC + DC) to the DC resistance (using Dowell curves)
CMA_MAIN			260.5	CMA	Cir mils per amp for main inductor winding
J_MAIN			13.6	A/mm^2	Current density in main inductor winding
AWG_AUX			0.0	AWG	Aux winding wire gauge
OD_MAIN			N/A	mm	Auxilliary winding wire gauge outer diameter
FILAR_AUX			2.0		Number of parallel strands for aux output
RDC_AUX			0.0	mohm	Reisistance of wire for aux inductor winding
AC Resistance Ratio (Aux)			0.00		Ratio of total resistance (AC + DC) to the DC resistance (using Dowell curves)
CMA_AUX		Info	0.0	CMA	!!! Info. Low CMA may cause overheating. Verify acceptable temperature rise
J_AUX			0.0	A/mm^2	Current density in auxilliary winding
Estimated Power Loss					
PCOPPER_MAIN			2.7	W	Copper loss in main inductor winding
PCOPPER_AUX			0.0	W	Copper loss in aux inductor windigs
PCORE			2.2	W	Total core loss
PTOTAL			4.9	W	Total losses in output choke
SECONDARY OUTPUT PARAMETERS					
ISFWRMS			18.99	A	Max. fwd sec. RMS current (at DVNOM)
ISFWD2RMS			0.00	A	Max. fwd sec. RMS current (at DVNOM)
ISCATHRMS			21.16	A	Max. catch sec. RMS current (at DVNOM)
ISCATCH2RMS			0.00	A	Max. catch sec. RMS current (at DVNOM)
IDAVMAINF			14.18	A	Maximum average current, Main rectifier (single device rating)
IDAVMAINC			14.92	A	Maximum average current, Main rectifier (single device rating)
IDAVOUT2F			0.00	A	Maximum average current, Main rectifier (single device rating)
IDAVOUT2C			0.00	A	Maximum average current, Main rectifier (single device rating)
IRMSMAIN			1.98	A	Maximum RMS current, Main output capacitor
IRMSOUT2			0.00	A	Maximum RMS current, Out2 output capacitor
	% Derating				
VPIVMAINF	100%		45.3	V	Main Forward Diode peak-inverse voltage (at VDSOP)
VPIVMAINC	100%		33.4	V	Main Catch Diode peak-inverse voltage (at VOVOFF_MAX)
VPIVOUT2F	100%		0.0	V	Output2 Forward Diode peak-inverse voltage (at VDSOP)
VPIVOUT2C	100%		0.0	V	Output2 Catch Diode peak-inverse voltage (at VOVOFF_MAX)
VPIVB	100%		32.4	V	Bias output rectifier peak-inverse voltage (at VDSOP)
HiperTFS STANDBY SECTION (FLYBACK STAGE)					
ENTER APPLICATION VARIABLES					
VACMIN	85			V	Minimum AC Input Voltage
VACMAX	265			V	Maximum AC Input Voltage
fL	50			Hz	AC Mains Frequency
VO_SB	5.00			V	Output Voltage (at continuous power)
IO_SB	2.00			A	Power Supply Output Current (corresponding to peak power)
IO_SB_PK	2.90				
POUT_SB			10	W	Continuous Output Power
POUT_SB_TOTAL			10.32	W	Total Standby power (Includes Bias winding power)
POUT_SB_PK			14.7	W	Peak Standby Output Power



n	0.70				Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z	0.50				Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC	3.00			ms	Bridge Rectifier Conduction Time Estimate
ENTER HiperTFS STANDBY VARIABLES					
Select Current Limit	STD		Standard Current Limit		Enter "LOW" for low current limit, "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIM_MIN			0.605	A	Minimum Current Limit
ILIM_TYP			0.650	A	Typical Current Limit
ILIM_MAX			0.696	A	Maximum Current Limit
R(EN)			280.0	k-ohms	Enable pin resistor
fSmin			124000	Hz	Minimum Device Switching Frequency
I ² fmin			50.19	A ² kHz	I ² f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	90.00		90	V	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10	V	HiperTFS Standby On State Drain to Source Voltage
VD_SB			0.5	V	Output Winding Diode Forward Voltage Drop
KP			0.71		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.36		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB			16.00	V	Bias Winding Voltage
IB			20.00	mA	Bias winding Load current
PB			0.32	W	Bias winding power
VDB			0.70	V	Bias Winding Diode Forward Voltage Drop
NB			9.11		Bias Winding Number of Turns
VZOV			22.00	V	Over Voltage Protection zener diode voltage.
UVLO VARIABLES					
RLS			4.00	M-Ohms	Line sense resistor (from Main converter section)
V_UV_ACTUAL			102	V	Typical DC start-up voltage
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE25	EE25	EE25		Enter Transformer Core
Core		EE25		P/N:	PC40EE25-Z
Bobbin		EE25 BOBBIN		P/N:	EE25 BOBBIN
AE			0.404	cm ²	Core Effective Cross Sectional Area
LE			7.34	cm	Core Effective Path Length
AL			1420	nH/T ²	Ungapped Core Effective Inductance
BW			10.2	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			2		Number of Primary Layers
NS_SB			3		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN_SB			115.65	V	Minimum DC Input Voltage
VMAX_SB			374.77	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX_SB			0.46		Duty Ratio at full load, minimum primary inductance and minimum input voltage
I _{AVG}			0.20	A	Average Primary Current
I _{P_SB}			0.60	A	Minimum Peak Primary Current
I _{R_SB}			0.43	A	Primary Ripple Current
I _{RMS_SB}			0.32	A	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP_SB			841.65	uH	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 765 uH



LP_TOLERANCE			10	%	Primary inductance tolerance
NP_SB			49		Primary Winding Number of Turns
ALG			349	nH/T^2	Gapped Core Effective Inductance
BM			2952	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			1050	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			2053		Relative Permeability of Ungapped Core
LG			0.11	mm	Gap Length (Lg > 0.1 mm)
BWE			20.4	mm	Effective Bobbin Width
OD			0.42	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.35	mm	Bare conductor diameter
AWG			28	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			161	Cmils	Bare conductor effective area in circular mils
CMA		<i>Info</i>	506	Cmils/Amp	CAN DECREASE CMA < 500 (decrease L(primary layers),increase NS,use smaller Core)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			9.89	A	Peak Secondary Current
ISRMS			5.65	A	Secondary RMS Current
IRIPPLE			5.29	A	Output Capacitor RMS Ripple Current
CMS			1131	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			19	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			584	V	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
PIVS			28	V	Output Rectifier Maximum Peak Inverse Voltage



11 Performance Data

All measurements are performed at the PCB connector at room temperature and 380 VDC input. For standby measurements, DC input voltage was adjusted to match the equivalent AC voltage.

11.1 Main and Standby Efficiency

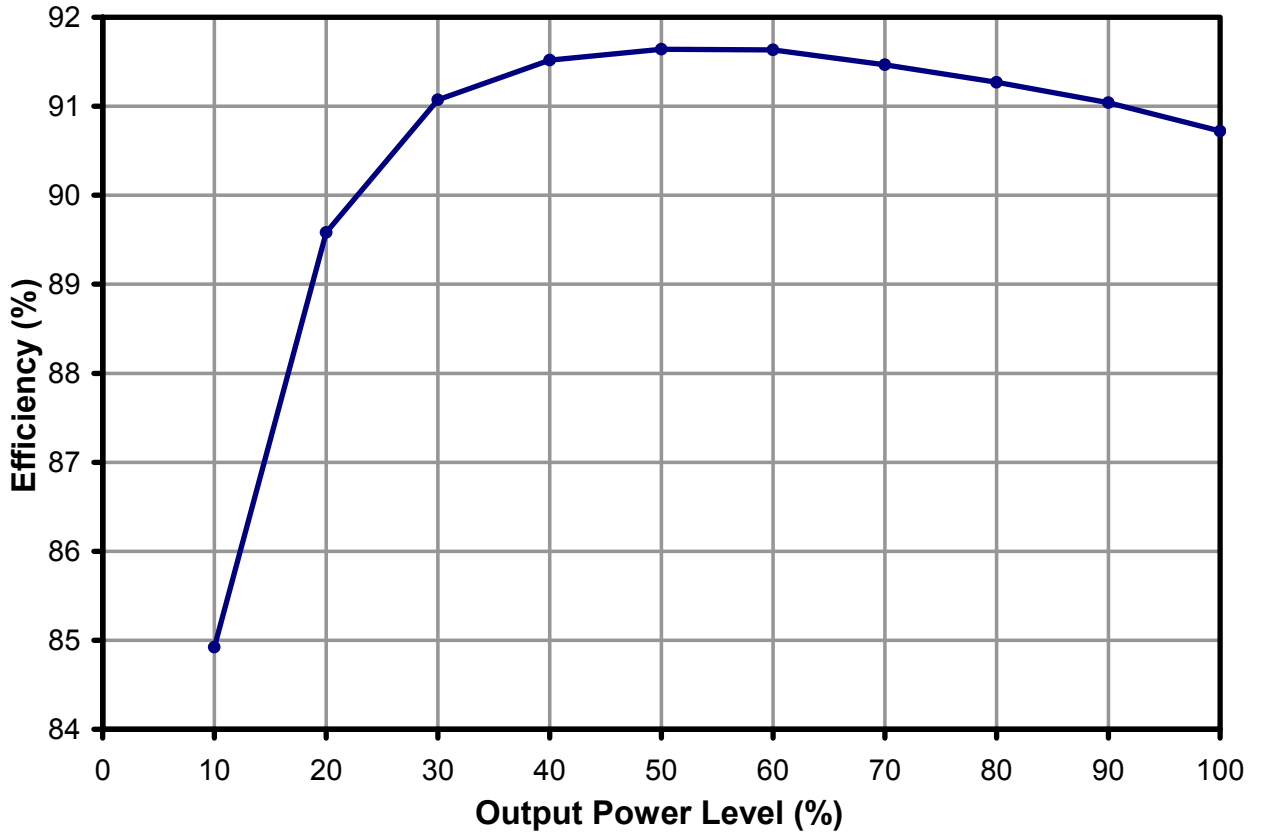


Figure 11 – Main and Standby Efficiency [%], Room Temperature, Forced Cooling.



11.2 Full Power Standby Efficiency vs. Equivalent AC Input Voltage

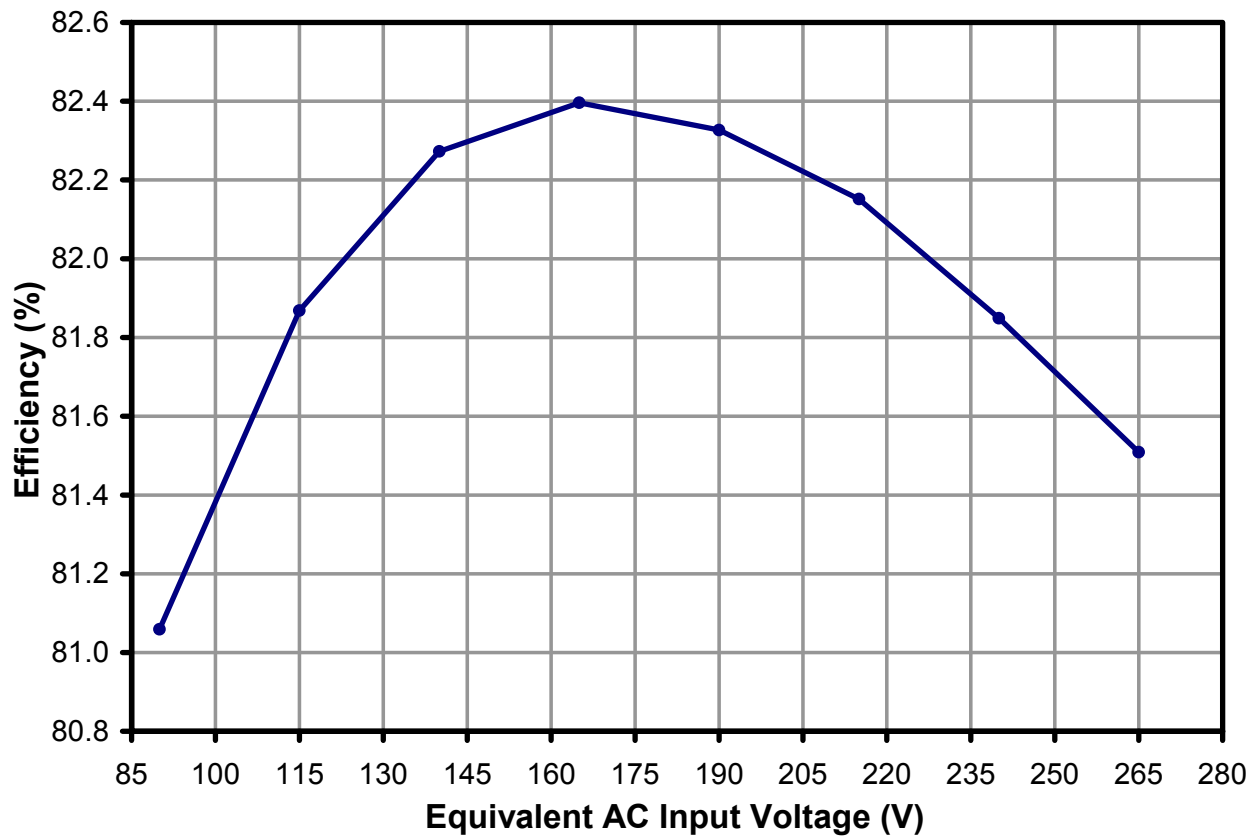


Figure 12 – Full Power Standby Efficiency [%] vs. AC Input Voltage [V] at Room Temperature



11.3 Standby Efficiency vs. Output Power

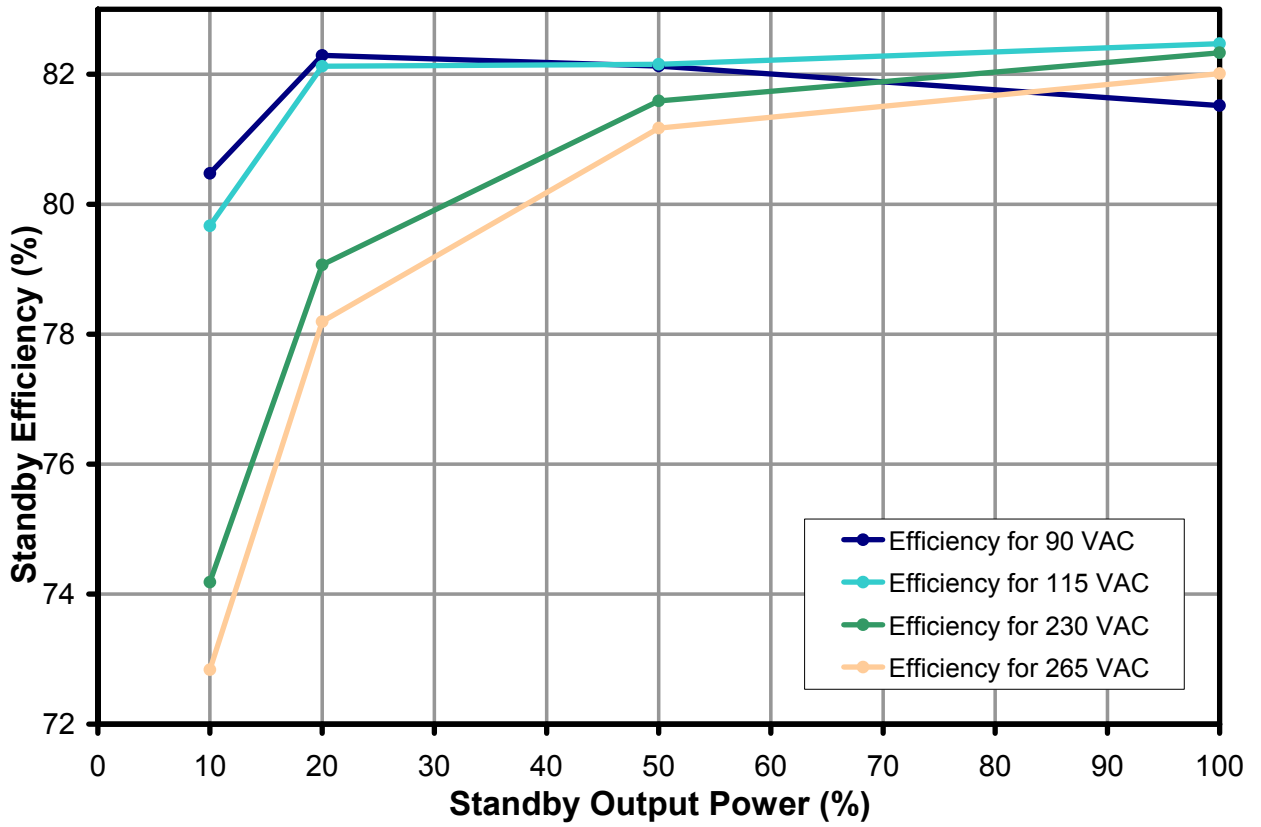


Figure 13 – Standby Efficiency [%], at Room Temperature and Equivalent AC Input Voltage.



11.4 Standby Only No-Load Input Power

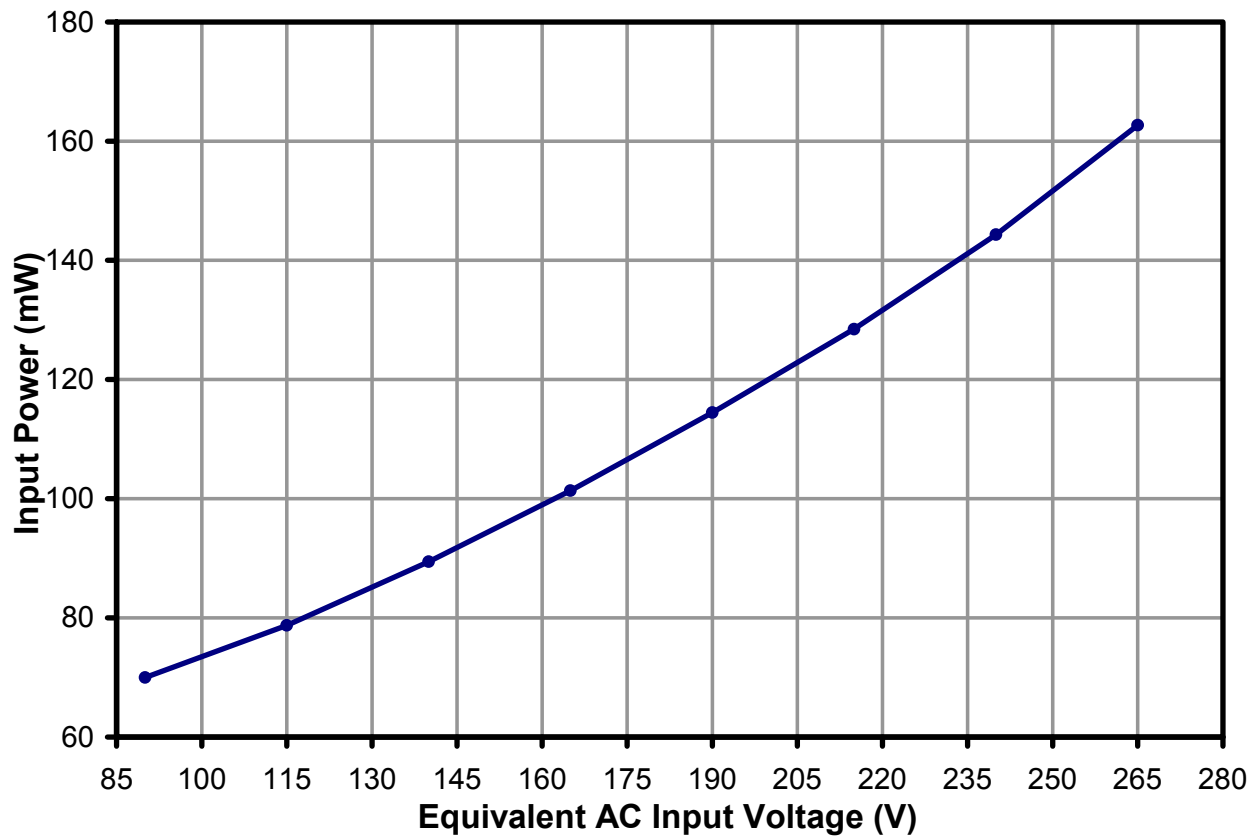


Figure 14 – Input Power [mW] vs. Input Line Voltage [V], for Zero Standby Load at Room Temperature.



11.5 Main and Standby Voltage Regulation

11.5.1 Main Load Regulation

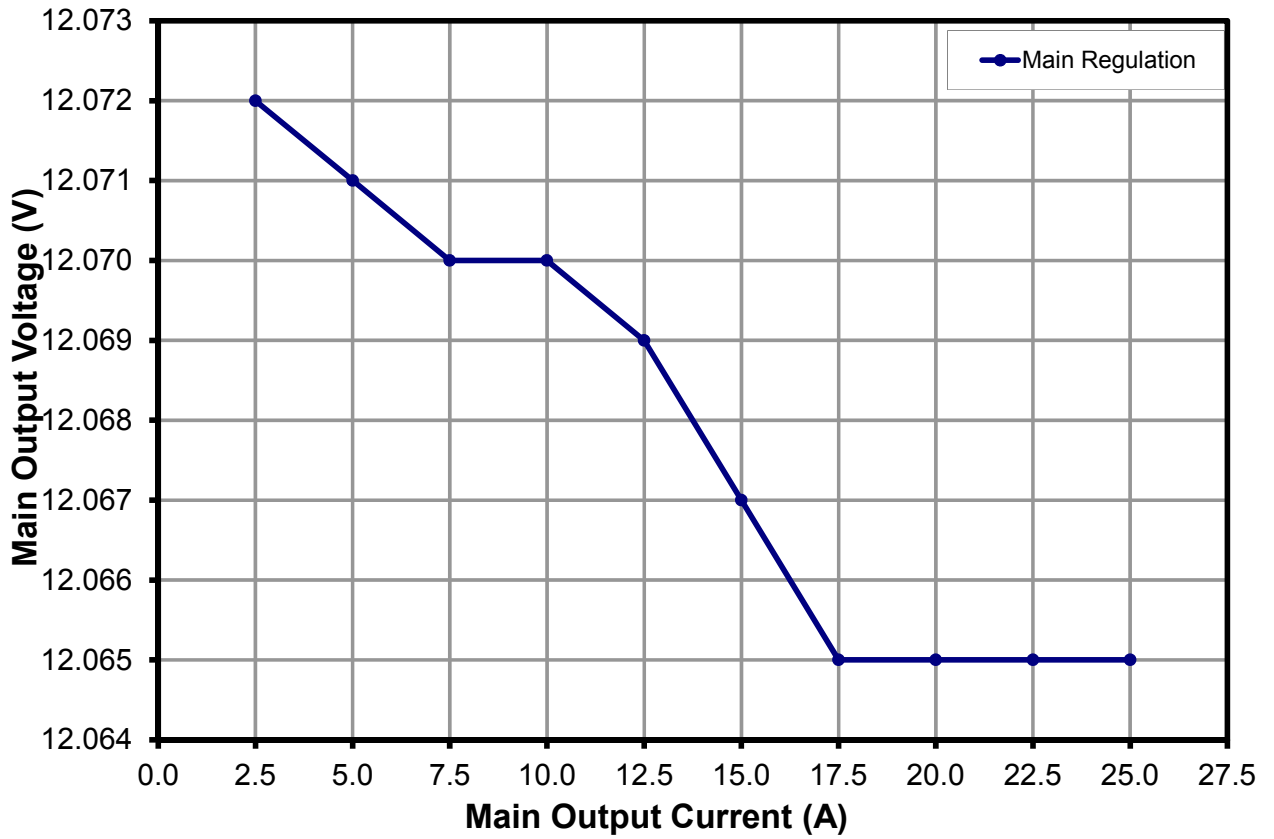


Figure 15 – Main Load Regulation, at Room Temperature and 380 VDC Input Voltage.



11.5.2 Standby Load Regulation at Equivalent AC Input Voltages

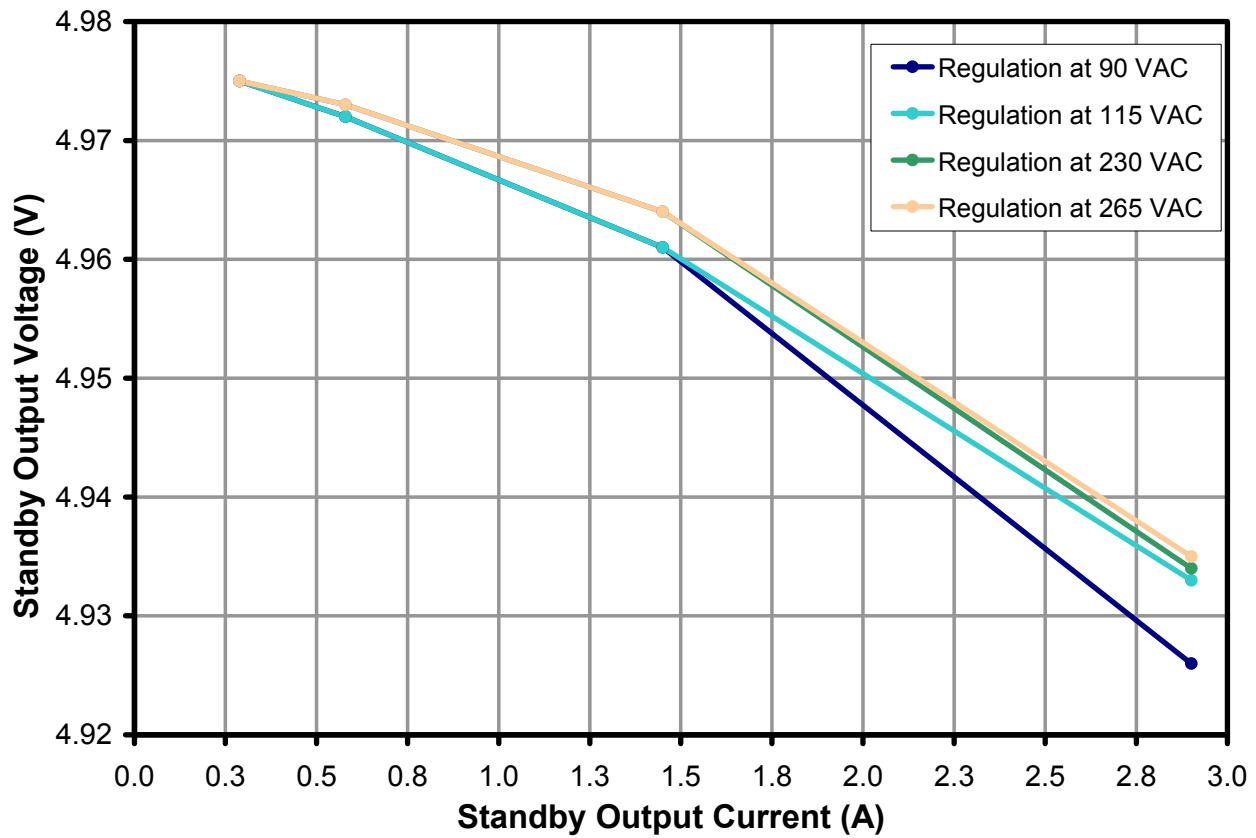


Figure 16 – Standby Load Regulation, at Room Temperature and Equivalent AC Input Voltage.



11.5.3 Standby Line Regulation at Full Power

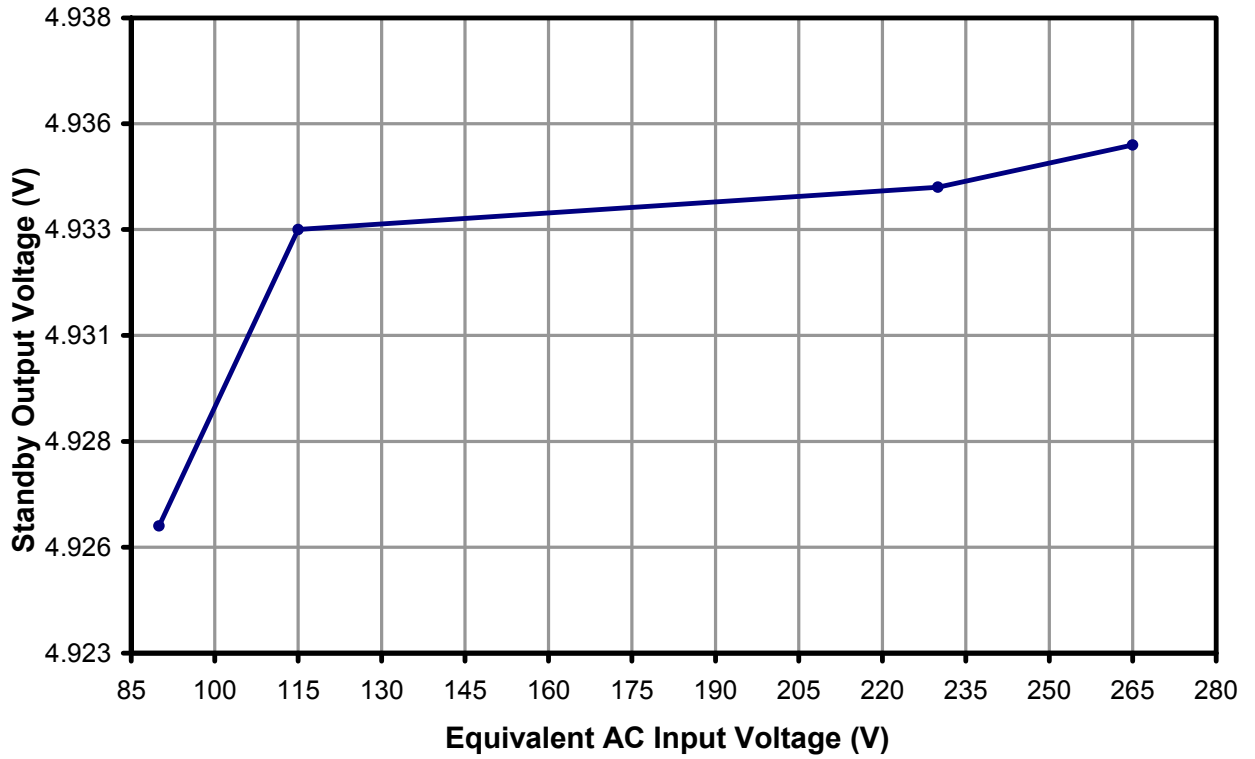


Figure 17 – Line Regulation, at Room Temperature, Full Load.



12 Thermal Performance

Full output power operation at room temperature is allowed only for operation time under 10 minutes. It is required to provide forced air cooling for operation at full power for more than 10 minutes or for over-power tests.

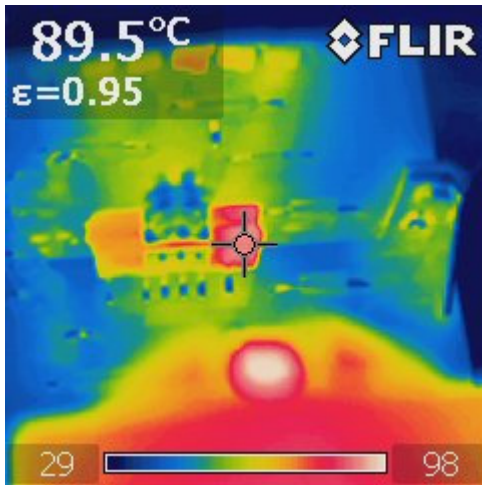


Figure 18 – HiperTFS Device Temperature.

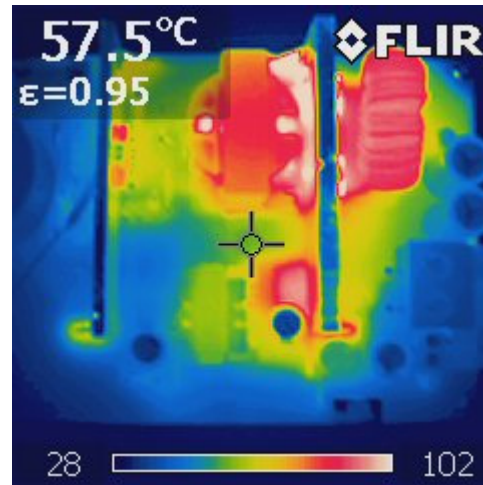


Figure 19 – Board Thermal Image.

In case of power components replacement it is important to insure a clean and smooth surfaces for heat-sink mechanical assembly with thermal conductive grease between any surface in contact, even for the isolation pad.

13 Waveforms

13.1 Main Drain Voltage and Current, Normal Operation, Full Power

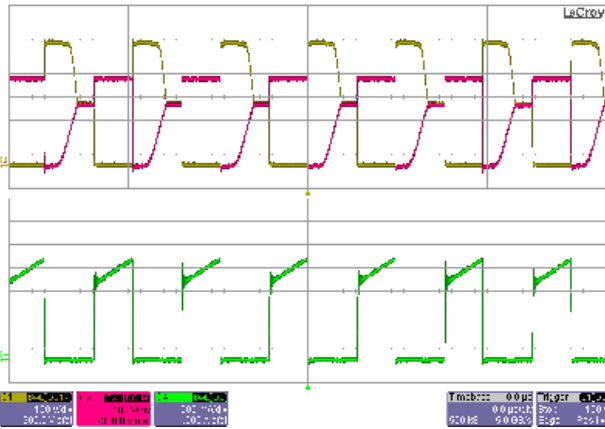


Figure 20 – Input Voltage: 380 VDC
 Upper: Main Upper MOSFET (Red) V_{SOURCE} , 100 V / div.
 Upper: Main Lower MOSFET (Gold) V_{DRAIN} , 100 V / div.
 Lower: Main I_{DRAIN} , 500 mA, 10 μ s / div.

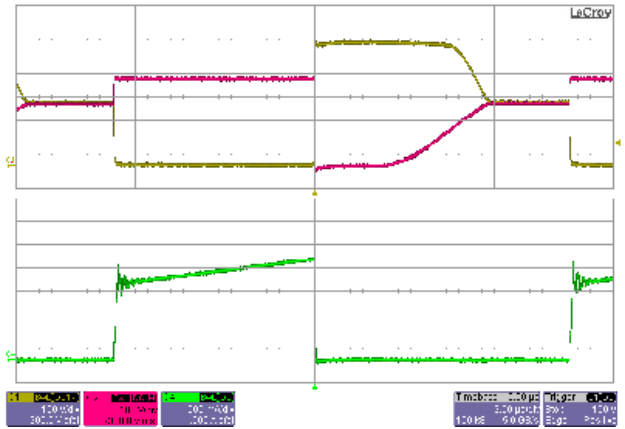


Figure 21 – Input Voltage: 380 VDC
 Upper: Main Upper MOSFET (Red) V_{SOURCE} , 100 V / div.
 Upper: Main Lower MOSFET (Gold) V_{DRAIN} , 100 V / div.
 Lower: Main I_{DRAIN} , 500 mA, 2 μ s / div.



13.2 Standby Drain Voltage and Current, Normal Operation, Full Power

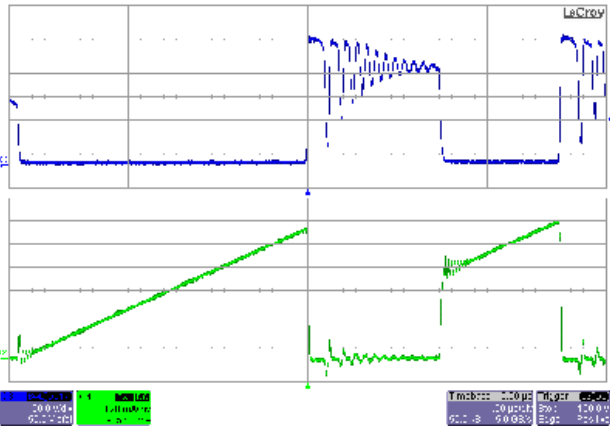


Figure 22 – Input Voltage: 127 VDC
 Upper: Standby V_{DRAIN} , 50 V / div.
 Lower: Standby I_{DRAIN} , 120 mA, 1 μ s / div.

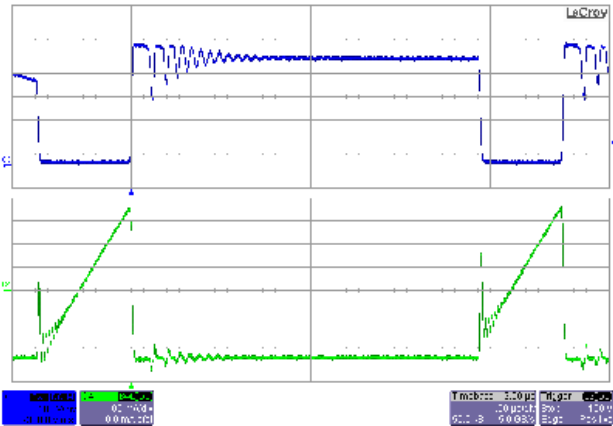


Figure 23 – Input Voltage: 380 VDC
 Upper: Standby V_{DRAIN} , 100 V / div.
 Lower: Standby I_{DRAIN} , 100 mA, 1 μ s / div.

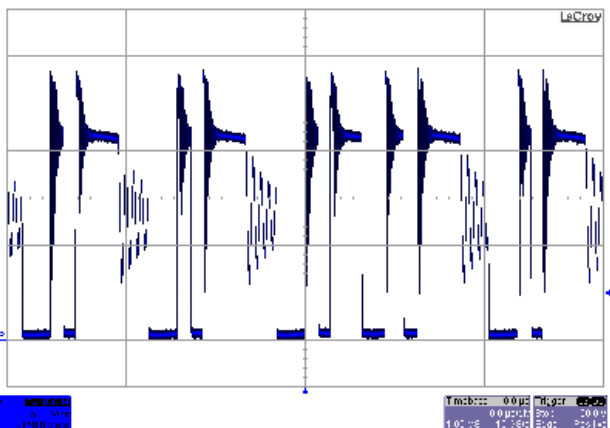


Figure 24 – Input Voltage: 127 VDC
 Standby V_{DRAIN} , 50 V / div., 10 μ s / div.

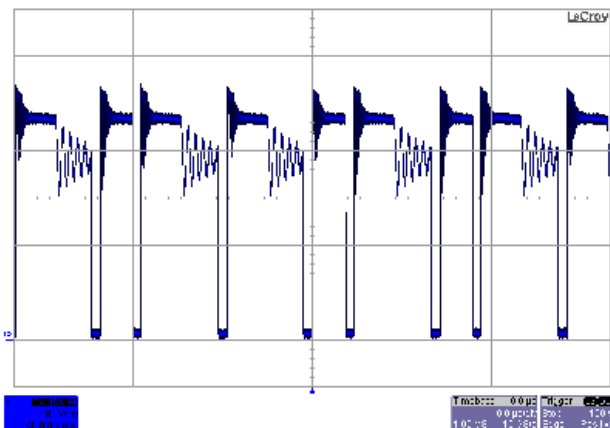


Figure 25 – 380 VDC
 Standby V_{DRAIN} , 100 V / div., 10 μ s / div.



13.3 Standby Drain Current and Output Voltage Start-Up Profile

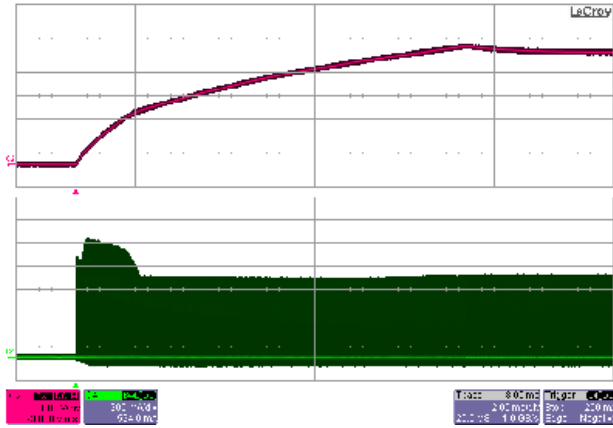


Figure 26 – Full Load: 127 VDC Input Voltage.
 Upper: V_{STBY} , 1 V / div.
 Lower: Standby I_{DRAIN} , 200 mA, 2 ms / div.

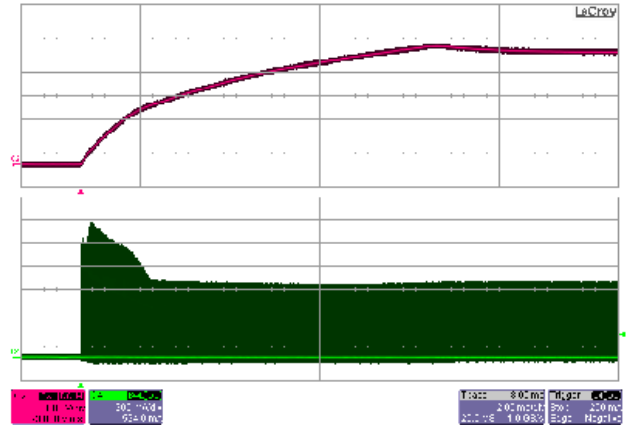


Figure 27 – Full Load: 380 VDC Input Voltage.
 Upper: V_{STBY} , 1V / div.
 Lower: Standby I_{DRAIN} , 200 mA, 2 ms / div.

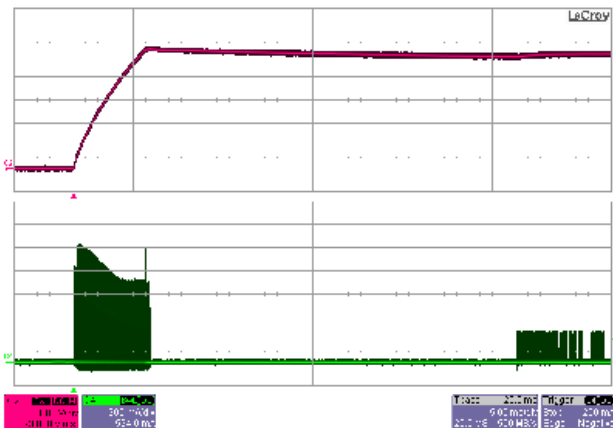


Figure 28 – No-load at 127 VDC Input Voltage
 Upper: V_{STBY} , 1 V / div.
 Lower: Standby I_{DRAIN} , 200 mA, 5 ms / div.

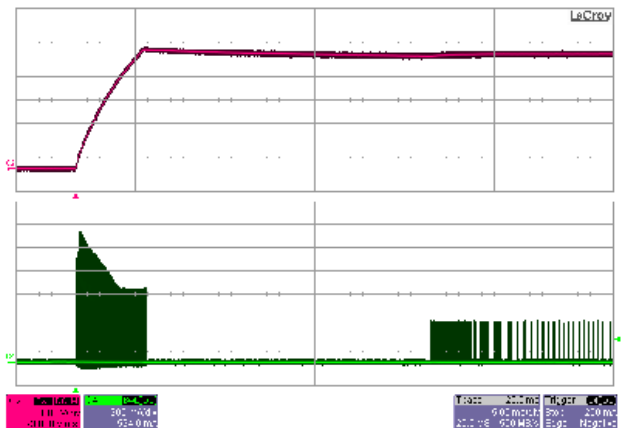


Figure 29 – No-load at 380 VDC Input Voltage
 Upper: V_{STBY} , 1 V / div.
 Lower: Standby I_{DRAIN} , 200 mA, 5 ms / div.



13.4 Main Drain Current, and Main and Standby Output Voltage Start-Up Profile

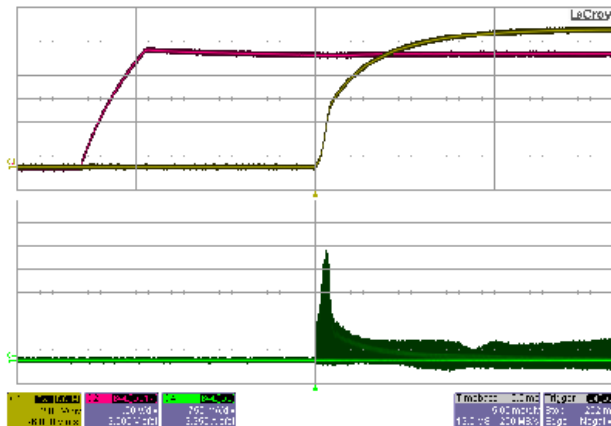


Figure 30 – No-load: 380 VDC Input Voltage.
 Upper (Red): V_{STBY} , 1 V / div.
 Upper (Yellow): V_{MAIN} , 2 V / div.
 Lower: Main I_{DRAIN} , 750 mA, 5 ms / div.

For this test the DC input voltage was applied with remote-ON/OFF switch in ON position.

13.5 Main Output Voltage Remote-ON Start-Up Profile

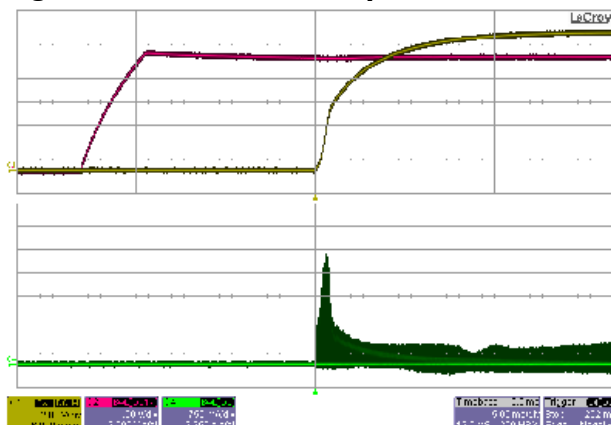


Figure 31 – No-load: 380 VDC Input Voltage.
 Upper (Red): V_{STBY} , 1 V / div.
 Upper (Yellow): V_{MAIN} , 2 V / div.
 Lower: Main I_{DRAIN} , 750 mA, 5 ms / div.



13.6 Main or Standby OV Shutdown

In order to activate the Standby or Main Overvoltage Protection Circuit for testing purpose, the recommended procedure is to temporarily short-circuit the input side of the respective optocouplers: U1A for the Main section or U2A for the Standby section. Without proper signal, the feedback loop will be forced to maximize the control signal and the Main or the Standby output voltage will increase all the way up to the shut-down limit. This overvoltage trigger condition will force the current into the BP pin to exceed the threshold limit and the internal HiperTFS controller to lock-out in a disabled state. For resetting the lock-out condition, the input voltage must be removed to allow the voltage on the BP pin to be discharged.

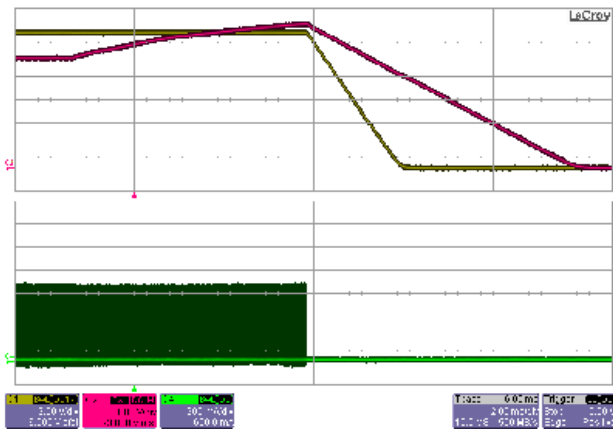


Figure 32 – Standby OV Protection.
 Upper (Red): V_{STBY} , 1 V / div.
 Upper (Yellow): V_{MAIN} , 2 V / div.
 Lower: Standby I_{DRAIN} , 200 mA, 2 ms / div.

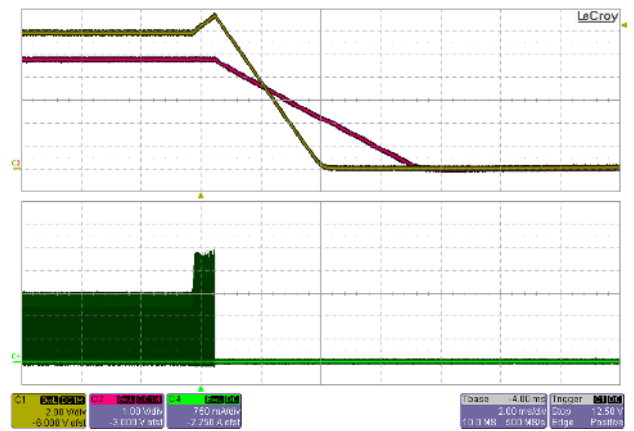


Figure 33 – Main OV Protection.
 Upper (Red): V_{STBY} , 1 V / div.
 Upper (Yellow): V_{MAIN} , 2 V / div.
 Lower: Main I_{DRAIN} , 750 mA, 2 ms / div.



13.7 Full Power Hold-Up Time

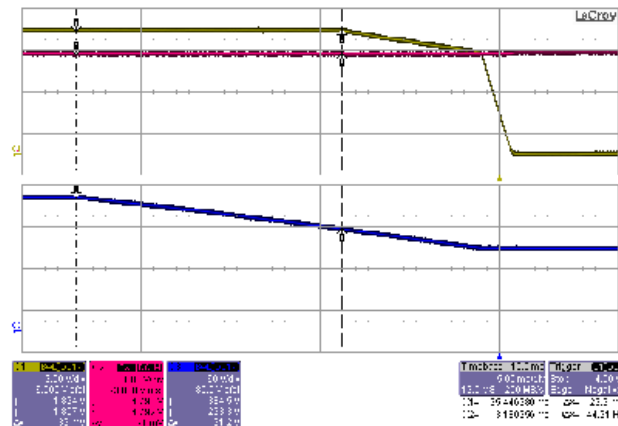


Figure 34 – Maximum Hold-Up Time = 22.3 ms
 Upper (Yellow): V_{MAIN}, 2 V / div.
 Upper (Red): V_{STBY}, 1 V / div.
 Lower: Input VDC, 60 V, 5 ms / div.

After turning OFF the input voltage, the full output power Hold-Up Time from 385 VDC down to 300 VDC is 20.8 ms. Maximum Hold-Up time (before 12 V Main output losing regulation, starting from 385 VDC input) is 22.3 ms.

13.8 Standby Auto-Restart

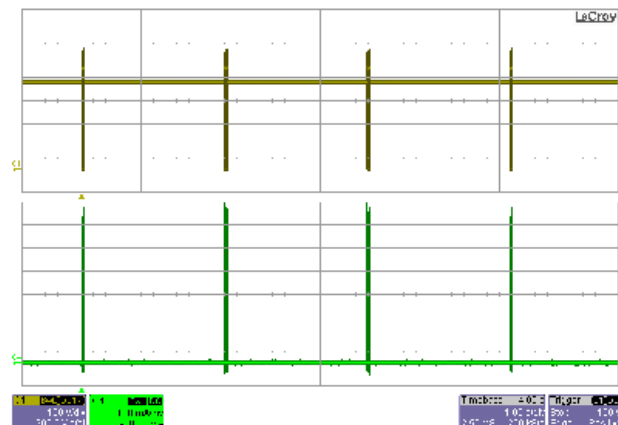


Figure 35 – Maximum Hold-Up Time = 22.3 ms
 Upper: Standby V_{DRAIN}, 100 V / div.
 Lower: Standby I_{DRAIN}, 100 mA, 1 s / div.

Overloading the standby output with 6 A for 380 VDC input shows repeated restart attempts every 2.3 s followed by a quick shutdown.



13.9 Main and Standby Full Power Output Short-Circuit

For short-circuit testing the recommended procedure is to use MOSFETs like IXYS IXFN180N25T or equivalent devices with high current capability connected to both Main and Standby outputs. In Short-Circuit mode only the output connectors and cable wires will have any significant resistivity. The unit will withstand short-circuit conditions without any permanent damage, and the outputs will go back to normal after the fault condition is removed. The Standby controller will try a restart cycle any time when the restart conditions are satisfied.

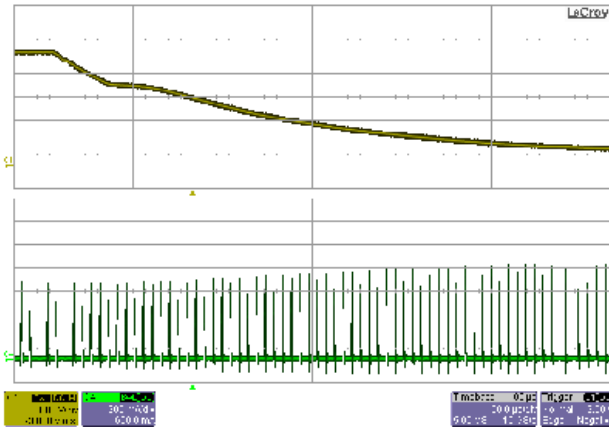


Figure 36 – Standby Output Short-Circuit.
 Upper: V_{STBY} , 1 V / div.
 Lower: Standby I_{DRAIN} , 200 mA, 50 μ s / div.

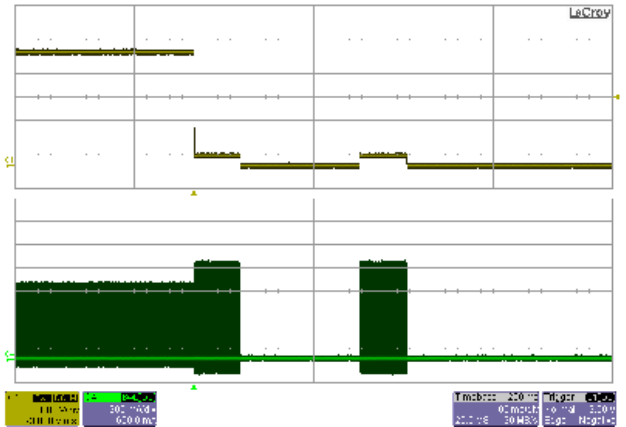


Figure 37 – Standby Output Short-Circuit.
 Upper: V_{STBY} , 1 V / div.
 Lower: Standby I_{DRAIN} , 200 mA, 100 ms / div.

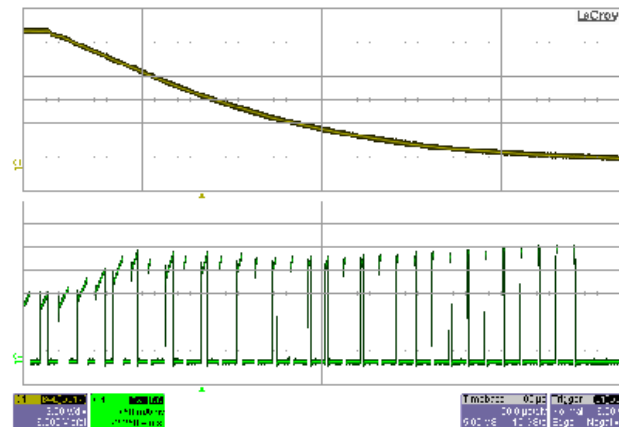


Figure 38 – Main Output Short-Circuit.
 Upper: V_{MAIN} , 2 V / div.
 Lower: Main I_{DRAIN} , 750 mA, 50 μ s / div.

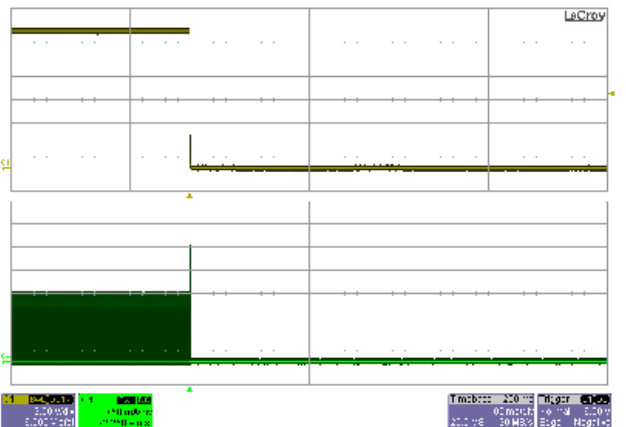


Figure 39 – Main Output Short-Circuit.
 Upper: V_{MAIN} , 2 V / div.
 Lower: Main I_{DRAIN} , 750 mA, 100 ms / div.



13.10 Main Remote-ON/OFF

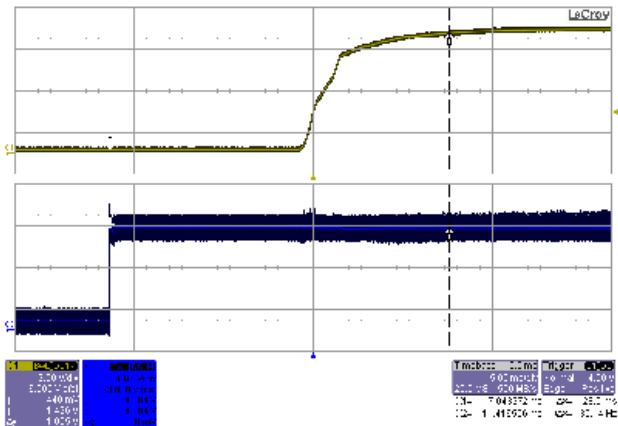


Figure 40 – Main Remote-ON: 385 VDC = 28.5 ms.
 Upper: V_{MAIN} , 2 V / div.
 Lower: Remote-ON, 1 V, 5 ms / div.

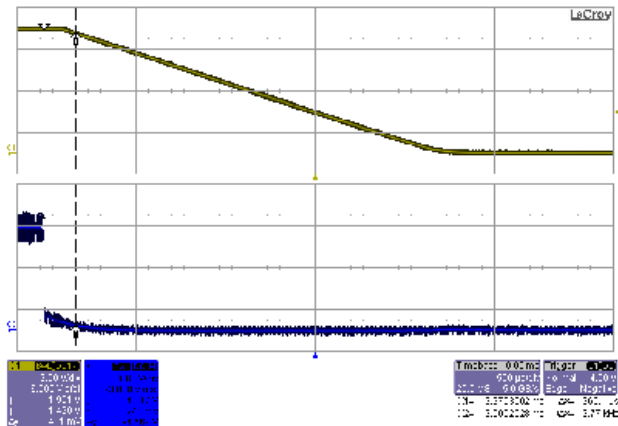


Figure 41 – Main Remote-OFF: 385 VDC = 265 μ s.
 Upper: V_{MAIN} , 2 V / div.
 Lower: Remote-OFF, 1 V, 5 ms / div.

Main Remote-ON start-up time is measured between Remote-ON/OFF signal going in ON state and Main 12 V output reaching 11.5 V, and it is 28.5 ms. Main Remote-OFF shut-down time is measured from Remote-ON/OFF signal going in OFF state and Main 12 V output going down to 11.5 V, and it is 265 μ s.



13.11 Output Ripple Measurements

13.11.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in the figures below.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 1.0 μF /50V aluminum electrolytic. **The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).**

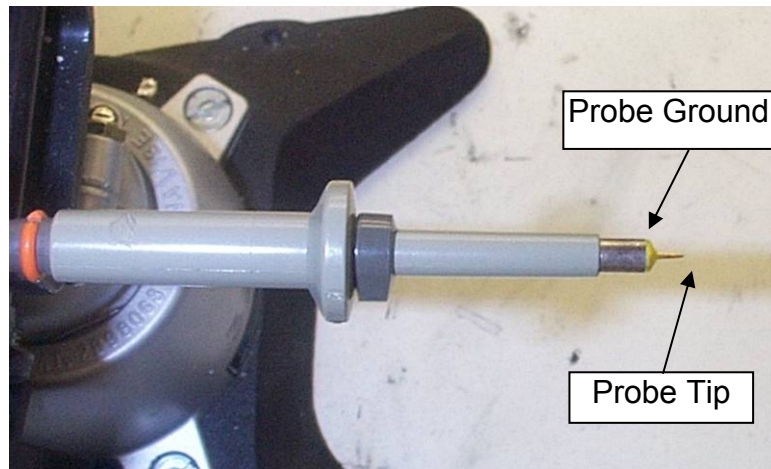


Figure 42 – Oscilloscope Probe Prepared for Ripple Measurement.
(End Cap and Ground Lead Removed)

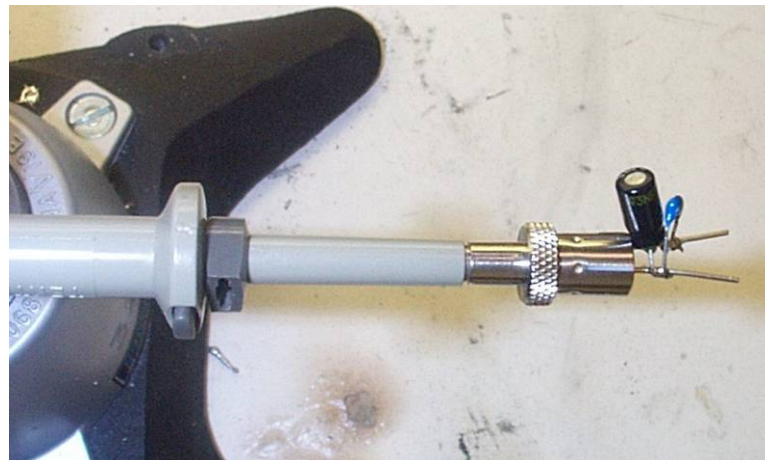


Figure 43 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter.
(Modified for ripple measurement, and two parallel decoupling capacitors added)

13.11.2 Measurement Results

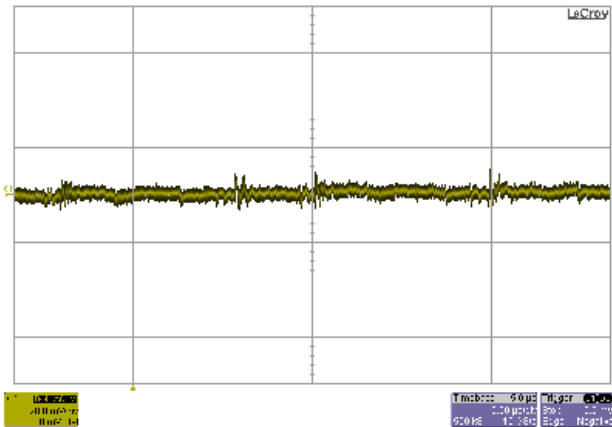


Figure 44 – Standby Output Ripple: 380 VDC
 V_{STBY} , 20 mV / div., 5 μ s / div. (Full Load)

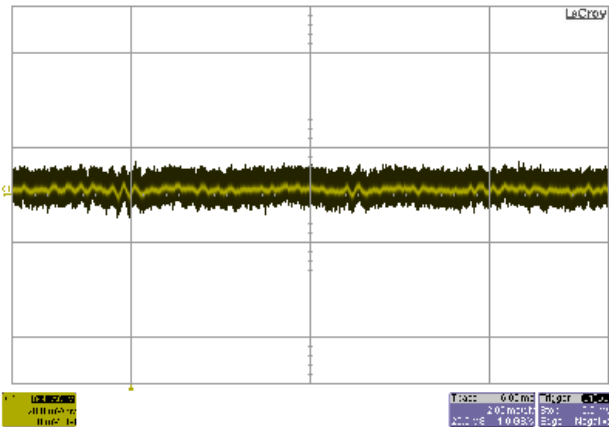


Figure 45 – Standby Output Ripple: 380 VDC.
 V_{STBY} , 20 mV / div., 2 ms / div. (Full Load)

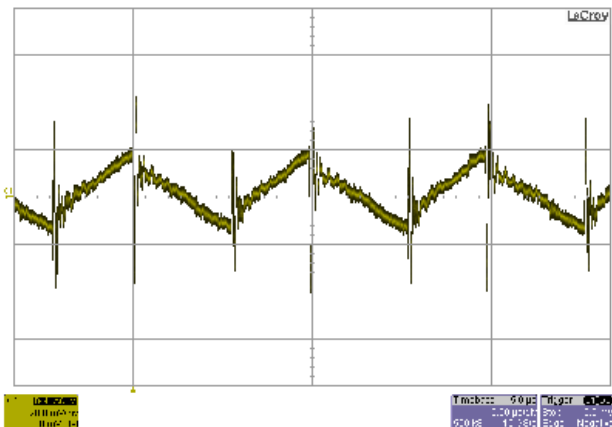


Figure 46 – Main Output Ripple: 380 VDC
 V_{MAIN} , 20 mV / div., 5 μ s / div. (Full Load)

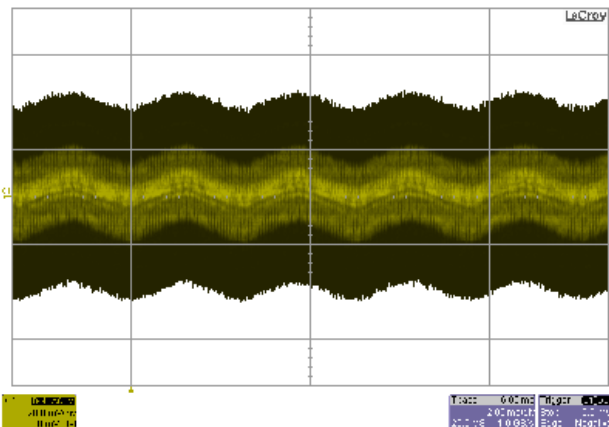


Figure 47 – Main Output Ripple: 380 VDC
 V_{MAIN} , 20 mV / div., 2 ms / div. (Full Load)



13.12 Main and Standby Load Transient Response

The waveform shows the instantaneous output voltage for 33% to 66% step load change. The voltage step change is under 50 mV for Standby output and under 150 mV for Main output. For the Standby test the Main output was off, for the Main test the Standby output was loaded at 50%.

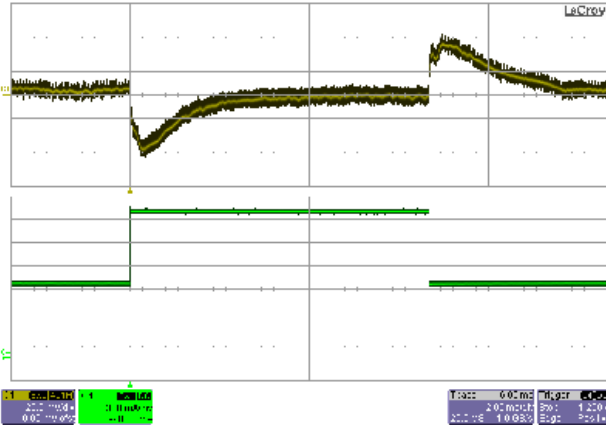


Figure 48 – Standby Step Load: 380 VDC
 Upper: V_{STBY} , 20 mV / div.
 Lower: Standby I_{OUT} , 300 mA, 2ms / div.

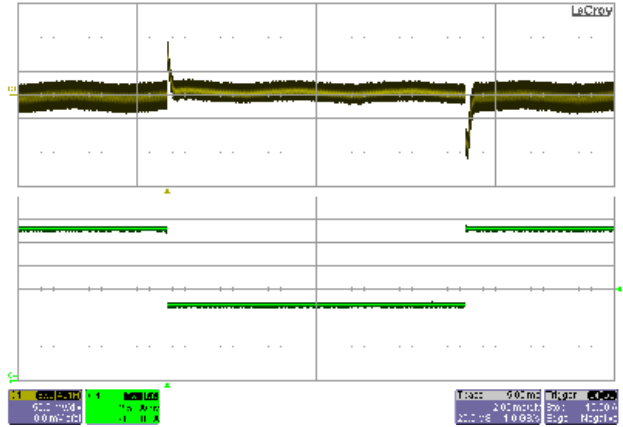


Figure 49 – Main Step Load: 380 VDC
 Upper: V_{MAIN} , 50 mV / div.
 Lower: Main I_{OUT} , 2.5 A, 2 ms / div.



14 Design Notes:

1. Pay extra attention when mounting the TFS762HG and the eSIP clip. TFS762HG must be placed flush with the PCB, as close as possible. There must be at least 2 mm clearance between clip and TFS762HG edge to avoid short-circuit from exposed metallic ends to mounting clip.
2. For convenience, two LED footprints are provided for optional visual control. All no-load tests must be completed without LEDs.
3. J1_OPTIO is provided at schematic and BOM level as an alternative option only.



15 Revision History

Date	Author	Revision	Description and changes	Reviewed
09-Nov-10	AN	1.0	Initial Release	Apps & Mktg
16-Nov-11	KM	1.1	Updated BOM and Schematic	



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