Synchronous Regulator, TINYBOOST®, 2.5 MHz

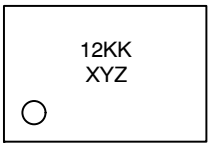
FAN48695

ON Semiconductor®

www.onsemi.com

WLCSP9
CASE 567VH

MARKING DIAGRAM



12	= Alphanumeric Device Code (See Ordering Information for specific device marking)
KK	= Lot Run Number
X	= Alphabetical Year Code
Y	= 2−weeks Date Code
Z	= Assembly Plant Code

Description

The FAN48695 is a low−power boost regulator designed to provide a regulated output voltage from a single cell Lithium or Li−Ion battery. The device maintains output voltage regulation within the recommended operating conditions. The combination of built−in power transistors, synchronous rectification and low supply current make the FAN48695 ideal for battery−powered applications.

The FAN48695 is available in a 9−bump, 0.4 mm pitch, Wafer−Level Chip Scale Package (WLCSP).

Features

- Input Voltage Range: 2.5 V to 5.5 V
- 1 A Load Capability
- PFM / PWM for high efficiency
- 2.5 MHz Fixed Frequency PWM Operation
- Synchronous Rectification
- Reverse Current Blocking
- Automatic Pass−Through Operation
- Forced Pass−Through Mode
- Over Temperature Protection
- Over Current Protection
- Under Voltage Protection
- 3 Stage Soft Start
- These Devices are Pb−Free and are RoHS Compliant

Applications

- NFC/USB/Power Amp
- Cell Phones, Smart Phones, Portable Instruments

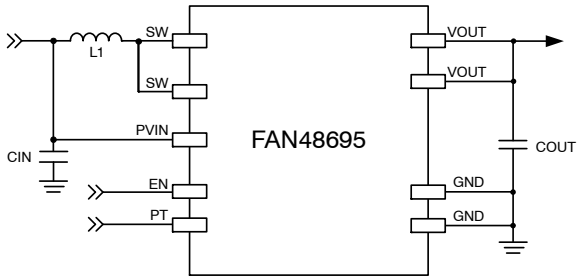


Figure 1. Typical Application

Table 1. ORDERING INFORMATION

Part Number	V_{OUT} *	Operating Temperature Range	Package	Packing†	Device Marking
FAN48695UC190X	5.0 V	−40°C to 85°C	9−Bump, 0.4 mm Pitch, WLCSP Package	3000 / Tape & Reel	2G

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
*Additional Output voltage options are available upon request.

Block Diagram

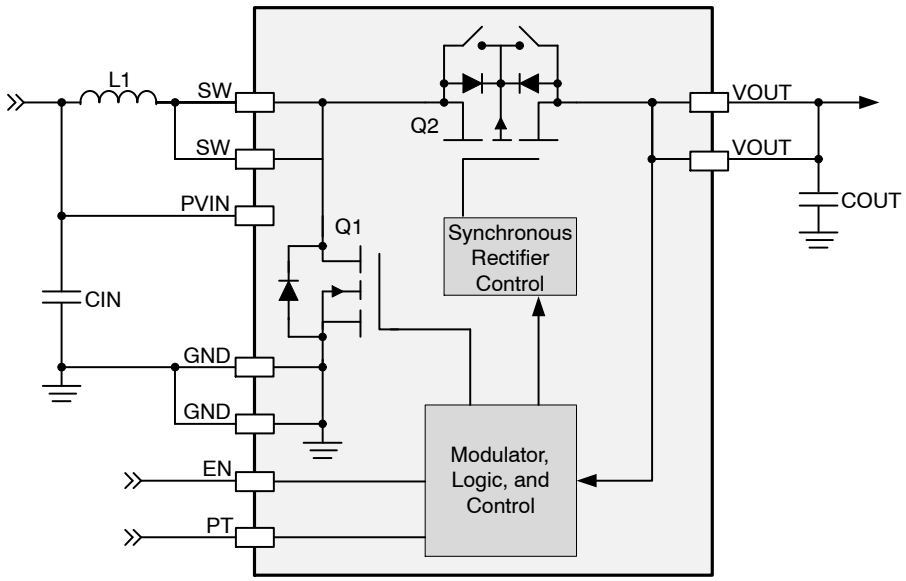


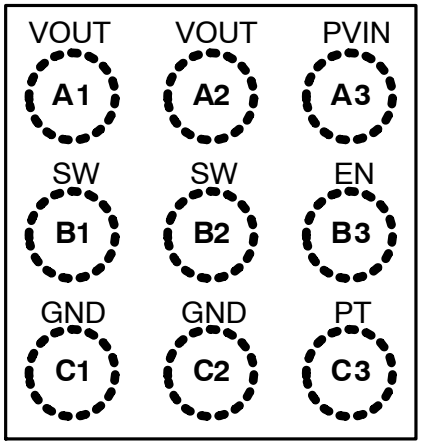
Figure 2. IC Block Diagram

Table 2. RECOMMENDED EXTERNAL COMPONENTS

REF	Description	Part Number
C_{IN}	10 μF, 6.3 V, 20%, X5R, 0402	Murata GRM155R60J106ME15
L1	1 μH / I_{SAT} = 3.6 A / I_{RAT} = 2.7 A / R_{DC} = 57 mΩ	Murata DFE201610E−1R0M
C_{OUT}	22 μF, 10 V, 20%, X5R, 0603	Murata GRM187R61A226ME15

NOTE: For improved ripple performance, additional output capacitance can be added.

Pin Configuration



Top View

Figure 3. WLCSP

Table 3. PIN DEFINITIONS

Pin	Name	Description
A1	VOUT	Output Voltage: Output of Boost Regulator. Connect C_{OUT} to this pin using the lowest impedance trace possible.
A2		
A3	PVIN	Input Voltage: Input power source for Boost Regulator. Connect C_{IN} directly to this pin using the lowest impedance trace possible.
B1	SW	Switching Node: Connect L1 to this pin.
B2		
B3	EN	Enable: A logic HIGH enables the device. A logic LOW disables the device.
C1	GND	Ground: Power and signal ground reference for the IC. C_{IN} and C_{OUT} should be connected to this pin using the lowest impedance trace possible.
C2		
C3	PT	Pass−Through: A logic HIGH will place the device in Forced Pass−Through mode.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Units
V_{IN}	Input Voltage	PVIN pin	−0.3	6.0	V
V_{OUT}	Output Voltage	VOUT pin	−0.3	6.0	V
V_{SW}	Continuous Switch Node Voltage	SW pin	−0.3	6.5	V
V_{CTRL}	Control Voltage	EN and PT pins	−0.3	(Note 1)	V
ESD	Electrostatic Discharge Protection Level	Human Body Model	2.0		kV
		Charged Device Model	1.0		kV
T_J	Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Soldering Temperature (10 Seconds)			+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Lesser of 6 V or V_{IN} + 0.3 V.

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Supply Voltage Range	PV_{IN}	2.5		5.5	V
L	Inductor			1.0		μH
C_{IN}	Input Capacitance			10		μF
C_{OUT}	Output Capacitance (Note 2)		3.5	22		μF
I_{OUT}	Output Current (Note 3)	$PV_{IN} \geq 2.8$ V	1000			mA
T_A	Operating Ambient Temperature		−40		+85	°C
T_J	Junction Temperature		−40		+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. The effective capacitance (CEFF) of small, high−value, ceramic capacitors will decrease as bias voltage increases. The effects of bias voltage (DC bias characteristics), tolerance, and temperature must be considered.
3. Refer to Figure 17 in Application Information Section.

Table 6. THERMAL PROPERTIES

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance	50	°C/W

NOTE: Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with two−layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

Table 7. ELECTRICAL SPECIFICATIONS (Note 4)

Minimum and maximum values are at PV_{IN} = 2.5 to 5.5 V and $PV_{IN} < V_{OUT}$ − 300 mV, EN = 1.8 V, PT = 0 V, T_A = −40°C to +85°C unless otherwise specified. Typical values are at T_A = 25°C, PV_{IN} = 3.8 V, EN = 1.8 V, PT = 0 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLIES						
I_{Q_PFM}	Quiescent Current	No Load, Non Switching, $PV_{IN} \le V_{OUT}$ − 300 mV		27	40	μA
I_{Q_APT}	Auto Pass−Through Operating IQ	No Load, PV_{IN} = 5.5 V		40	60	μA
I_{Q_FPT}	Forced Pass−Through Mode Operating Current	No Load, PV_{IN} = 3.8 V, PT = 1.8 V		9	15	μA
I_{SD}	Shutdown Current	EN = 0 V		3	8	μA
V_{UVLO_R}	Under−Voltage Lockout Threshold	Rising PV_{IN}	2.10	2.15	2.20	V
V_{UVLO_F}	Under−Voltage Lockout Threshold	Falling PV_{IN}	2.00	2.05	2.10	V
OUTPUT VOLTAGE ACCURACY						
V_{O_ACC}	Regulated Output Voltage	PV_{IN} = 3.8 V, No Load (PFM Mode)	4.884	5.035	5.186	V
		PV_{IN} = 3.8 V, I_{LOAD} = 200 mA (PWM Mode)	4.900	5.000	5.100	V
REGULATOR						
F_{SW}	PWM Switching Frequency	PV_{IN} = 3.8 V	2.25	2.50	2.75	MHz
RDS_{ON_P}	PMOS Resistance, SW to VOUT			55	100	mΩ
RDS_{ON_N}	NMOS Resistance, SW to PGND			55	100	mΩ
I_{SW_LIM}	Inductor Peak Current Limit		2.34	2.63	2.84	A
LIN1	First Stage Linear Soft Start Input Current Limit	V_{OUT} = 2.0 V		280		mA
LIN2	Linear Soft Start Input Current Limit	V_{OUT} = 2.0 V		600		mA
T_{SD}	Thermal Shutdown Threshold	I_{LOAD} = 10 mA		145		°C
T_{HYS}	Thermal Shutdown Hysteresis			28		°C
LOGIC PINS (EN, PT)						
V_{IL}	Logic Low threshold				0.4	V
V_{IH}	Logic High threshold		1.2			V
R_{PD}	Pull−Down Resistance	Logic Low state only		300		kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Specifications in the Electrical Characteristics table reflect open−loop, steady−state data.

TYPICAL CHARACTERISTICS

Unless otherwise specified, circuit of Figure 1 using recommended external components and layout, T_A = 25°C, PV_{IN} = 3.8 V, EN = 1.8 V.

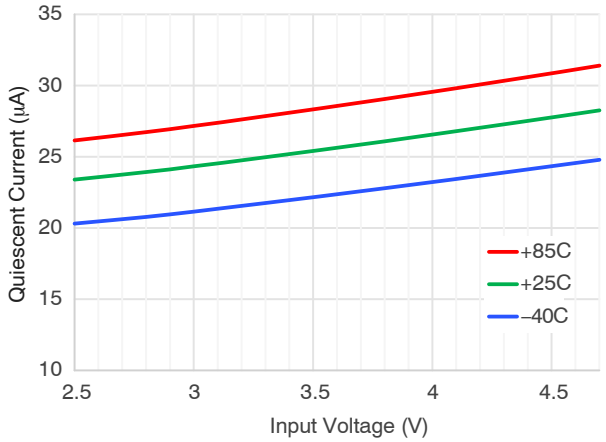


Figure 4. Quiescent Current (Non−Switching) vs. Input Voltage

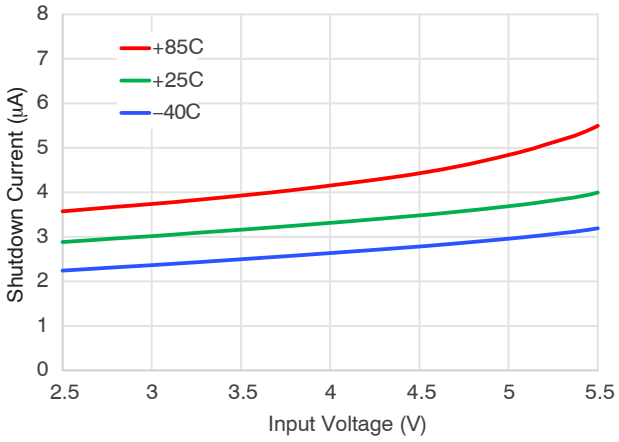


Figure 5. Shutdown Current vs. Input Voltage

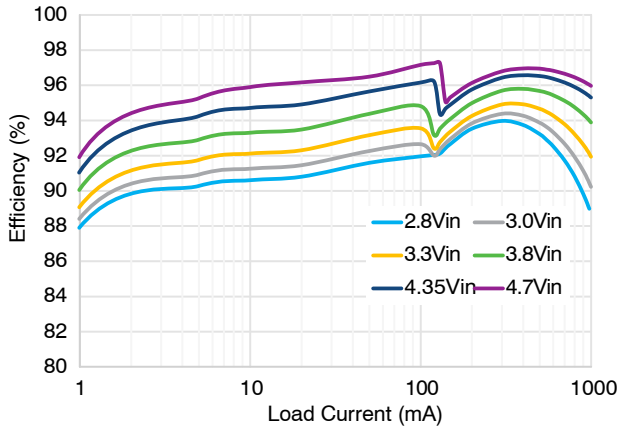


Figure 6. Efficiency vs. Load Current and Input Voltage, L = DFE201610E−1R0M

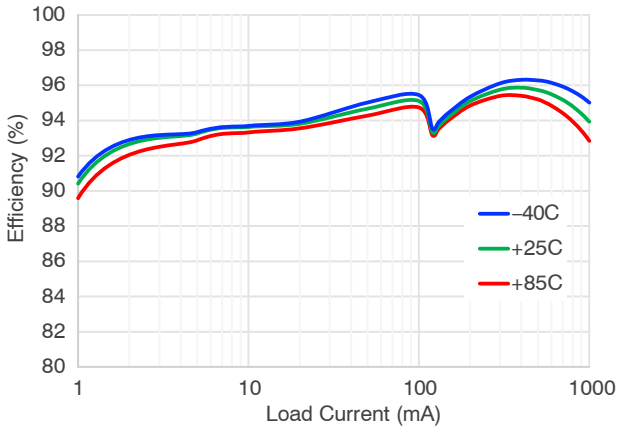


Figure 7. Efficiency vs. Load Current and Temperature, L = DFE201610E−1R0M

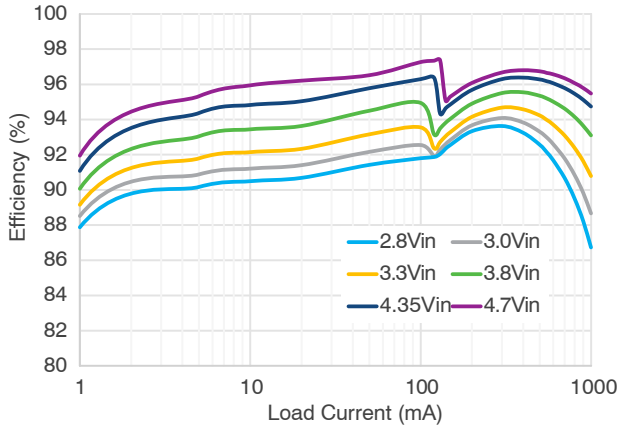


Figure 8. Efficiency vs. Load Current and Input Voltage, L = DFE201610R−H−1R0M

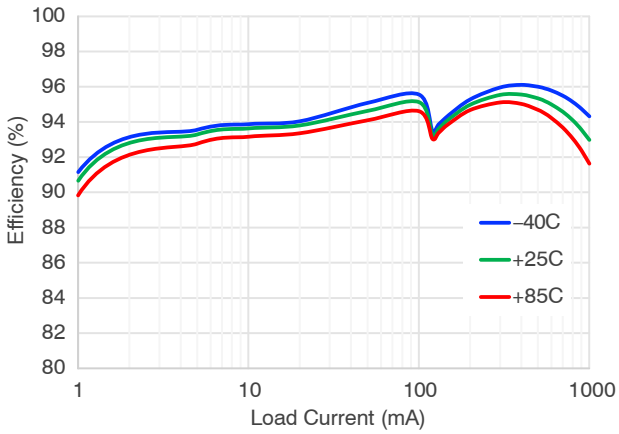


Figure 9. Efficiency vs. Load Current and Temperature, L = DFE201610R−H−1R0M

TYPICAL CHARACTERISTICS

Unless otherwise specified, circuit of Figure 1 using recommended external components and layout, T_A = 25°C, PV_{IN} = 3.8 V, EN = 1.8 V.

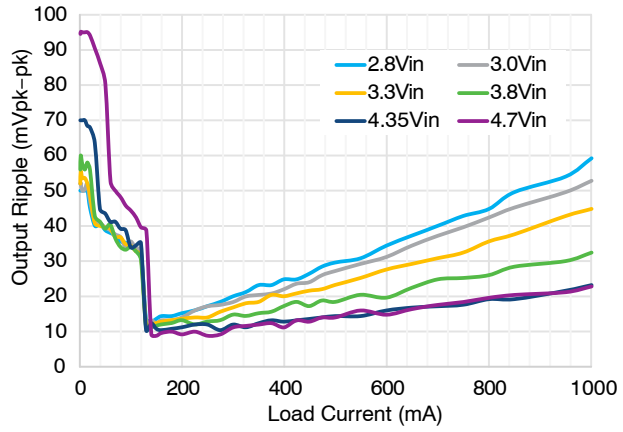


Figure 10. Output Ripple vs. Load Current

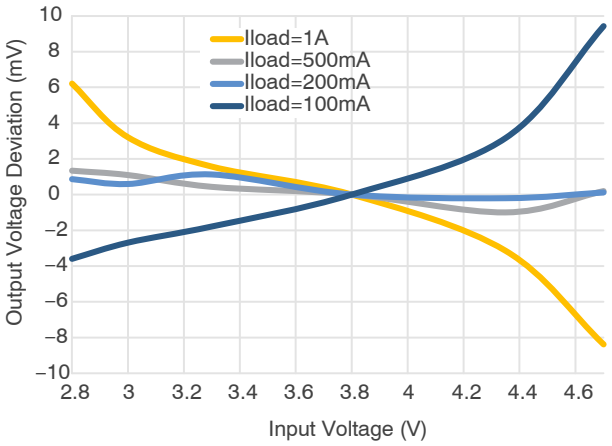


Figure 11. Line Regulation, Deviation from 3.8 PV_{IN} Measurement

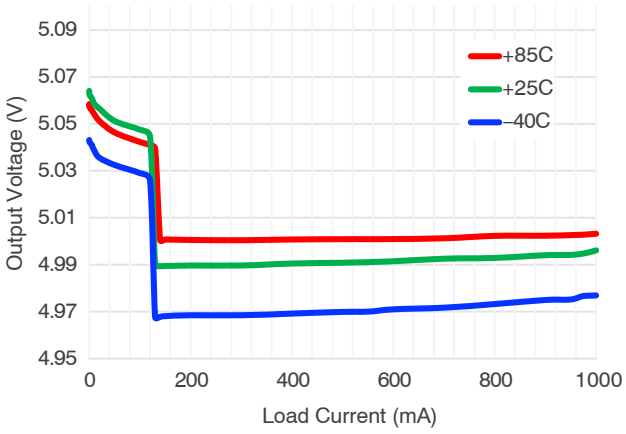


Figure 12. Load Regulation

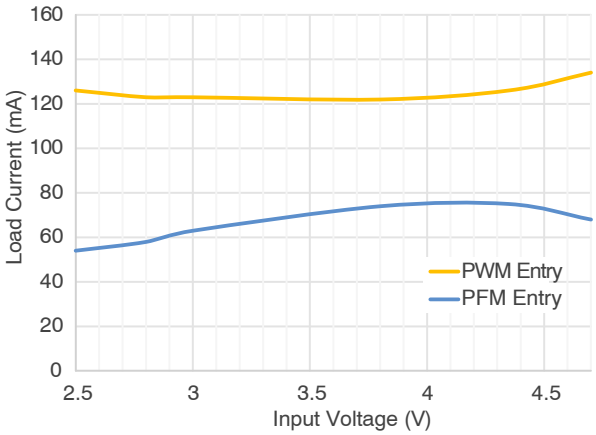


Figure 13. PWM/PFM Entry Thresholds vs. Input Voltage

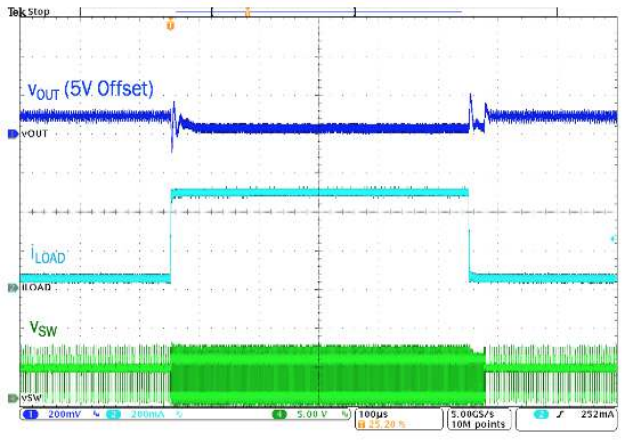


Figure 14. Load Transient, 50 mA ↔ 500 mA, 1 μs Edge

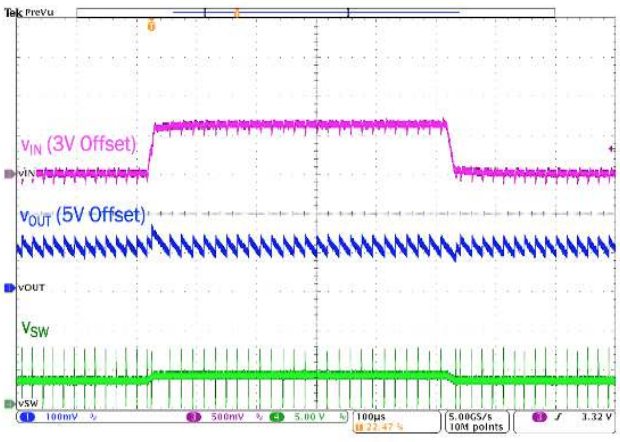


Figure 15. Line Transient, 3.0 V ↔ 3.6 V, 10 μs Edge, 10 mA Load

TYPICAL CHARACTERISTICS

Unless otherwise specified, circuit of Figure 1 using recommended external components and layout, T_A = 25°C, PV_{IN} = 3.8 V, EN = 1.8 V.

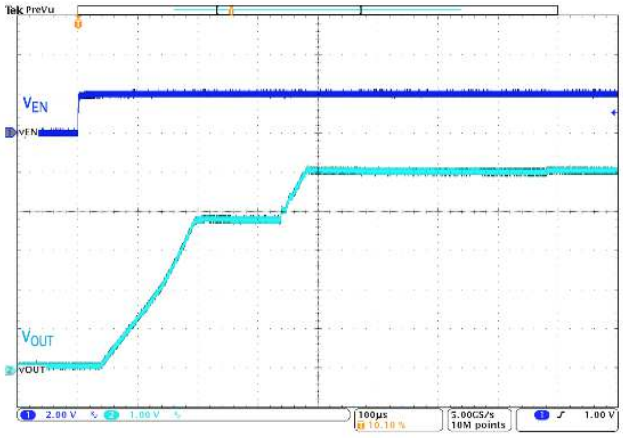


Figure 16. Start−Up into 50 Ω Load

APPLICATION INFORMATION

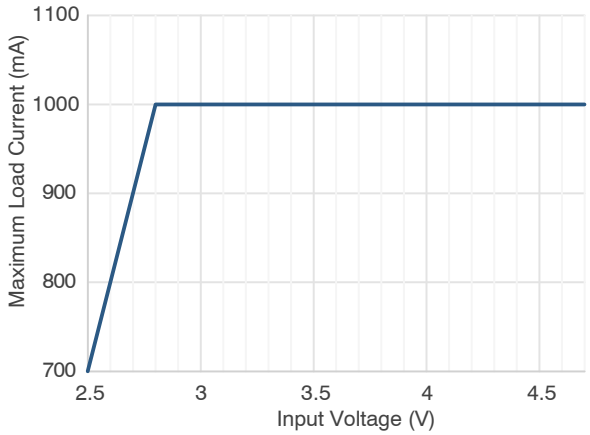


Figure 17. Load Capability vs. Input Voltage

Operation Description

The FAN48695 is a low−power boost regulator designed to provide a regulated output voltage from a single cell Lithium or Li−Ion battery. It maintains the output in regulation within the devices recommended operating conditions. For higher efficiency at low load conditions, the device will transition into PFM Mode.

Automatic Pass−Through Mode will occur during boost Mode if the input voltage rises close to or above the desired output voltage. Additionally, the device can be put into Forced Pass−Through Mode when boosting the output is not required by setting the PT pin to HIGH.

Startup Description

The FAN48695 can startup in either Boost Mode or Forced Pass−Through (FPT) Mode. Both modes use a two stage linear soft−start to limit inrush currents from the source.

Linear Soft−Start State

An internal fixed current source of LIN1 is applied to V_{OUT} for up to 500 μs. If V_{OUT} does not reach V_{IN} − 300 mV within 500 μsec, the current source is increased to LIN2 for up to an additional 1 ms.

Boost Mode:

- If any time during the Linear Soft−Start State V_{OUT} charges up to V_{IN} − 300 mV, the fixed current source will be disabled and the device then proceeds to the Switching Soft−Start State.
- If V_{OUT} fails to charge up to V_{IN} − 300 mV by the end of LIN2, the fixed current source is disabled, a fault condition is declared, and the device waits 20 ms to attempt an automatic restart.

FPT Mode:

- If V_{OUT} charges up to V_{IN}, Forced Pass−Through Mode is achieved.
- If V_{OUT} fails to charge up to V_{IN} by the end of LIN2, the fixed current source is disabled, a fault condition is declared, and the device waits 20 ms to attempt an automatic restart.

Switching Soft−Start State

The regulator begins switching in PFM operation with I_{SW_LIM} set to one−quarter its normal value until V_{OUT} reaches its target voltage or 100 μs has elapsed. The device will then transition to BOOST Mode with I_{SW_LIM} returned to its typical value.

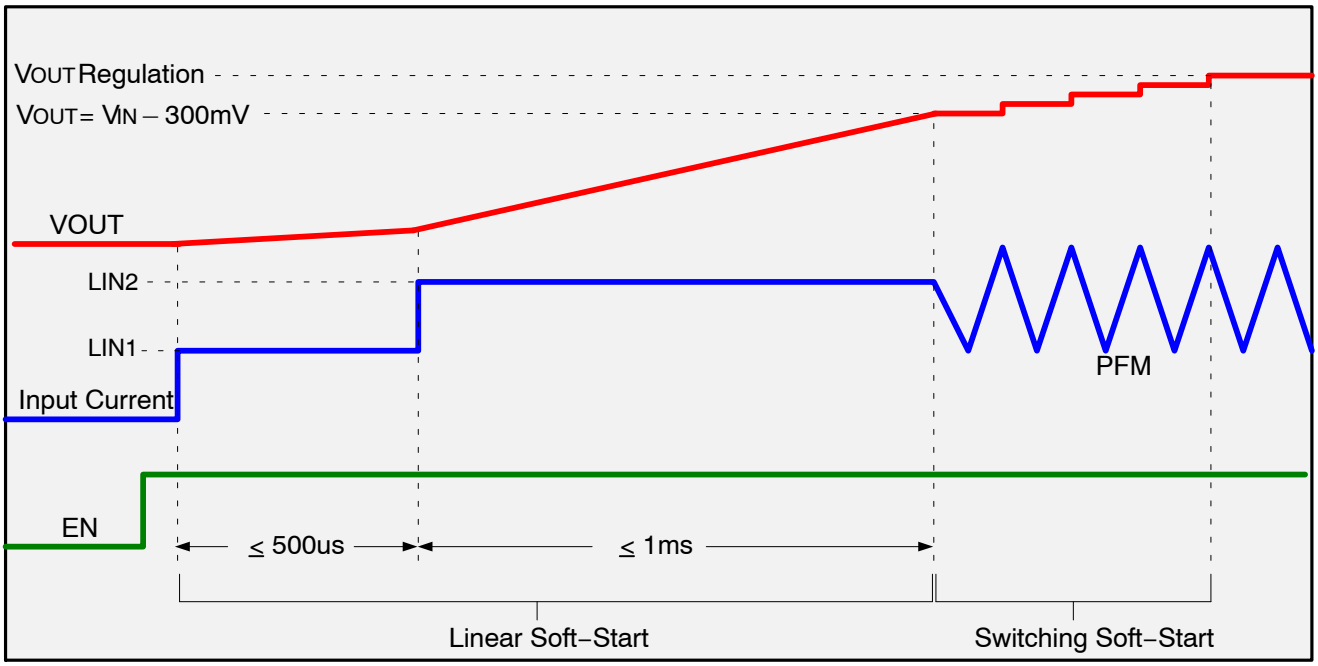


Figure 18. Boost Mode Startup

Shutdown Description

The boost can be disabled by asserting the EN pin low. The output (VOUT) will discharge into the prevailing load.

Modes of Operation

Boost PWM Mode

During PWM mode, the boost regulates the output using a fixed switching frequency of ~2.5 MHz. As the load increases, the inductor current will have an increasing DC offset. The period of when the V_{SW} (voltage at switching node) signal is low, will grow as the battery voltage in a mobile device decays.

Boost PFM Mode

The FAN48695 has PFM operation which improves efficiency at light loads. The device operates in PFM when the load current falls below approximately 80 mA. In PFM mode, the average output voltage is regulated higher than the average PWM output voltage to improve transient dips.

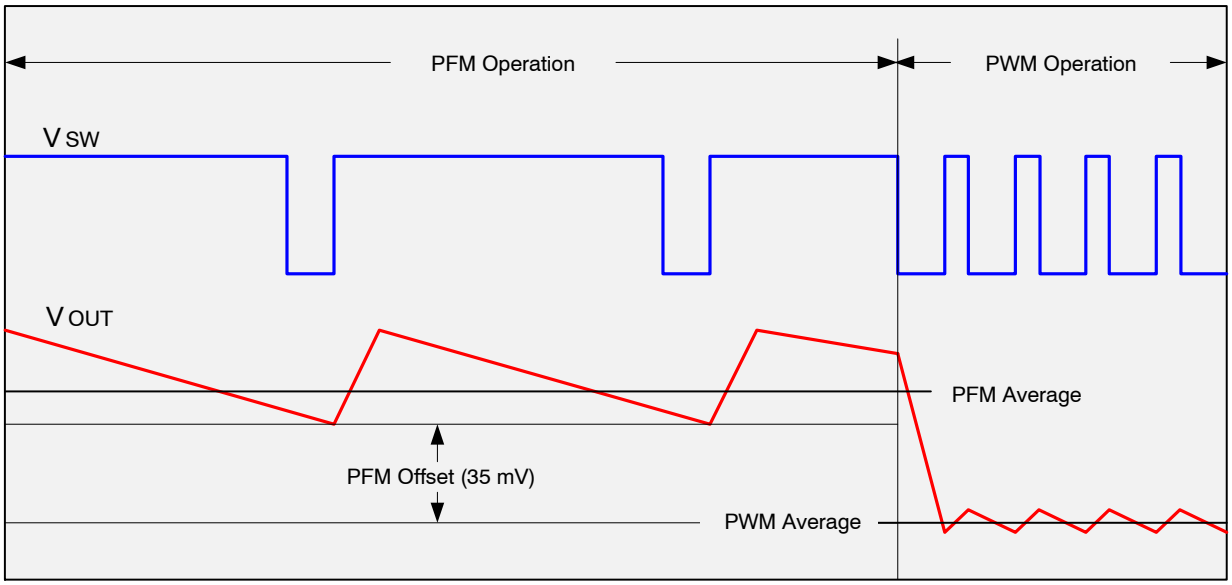


Figure 19. Boost Mode Operation

Automatic Pass−Through Operation

In normal operation, the device automatically transitions from Boost Mode to Pass−Through Operation if V_{IN} is more than the boost target voltage minus 250 mV for ≥5 μsec. In Pass−Through Mode, the device has a low impedance path between V_{IN} and V_{OUT} (RDS_{ON_P} + L_{DCR}). The device will automatically exit Pass−Through Mode when V_{IN} is 350 mV less than the target boost voltage.

Forced Pass−Through Mode

When the PT pin is set to a logic HIGH and EN=HIGH, Forced Pass−Through mode occurs. In Pass−Through Mode, the device has a low impedance path between V_{IN} and V_{OUT} (RDS_{ON_P} + L_{DCR}).

Protection Features

V_{OUT} Fault

If the output voltage is pulled down to 300 mV below V_{IN} by a heavy load, the device will fault to protect itself, the source, and the load.

Soft Start Fault

Refer to the Start−up section for additional detail. If the device fails to drive the output up to V_{IN} − 300 mV within 1.5 ms the device will fault due to sensing a heavy load. If the device is unable to bring the output up to regulation within 100 μs after exiting the linear charging phases, the device will fault. In either case, the device will attempt a restart 20 ms later.

Current Limit (OCP)

FAN48695 has a current limit feature which protects itself, the inductor, and load during overload conditions. When the inductor peak current limit is reached and held for 2 ms, the device enters fault state.

During an output overload condition, if V_{OUT} falls 300 mV below V_{IN} the device enters fault state without waiting 2 ms.

In fault state, Q2 is completely opened to prevent current flow between PVIN and VOUT, in either direction. The device will attempt an automatic restart every 20 ms.

Automatic Pass−Through Mode Protection

During Automatic Pass−Through Mode, the device is short−circuit protected. If the voltage difference between V_{IN} and V_{OUT} exceed more than 350 mV for ≤10 μs, a fault is declared. The part will automatically attempt a restart every 20ms until the short condition ceases.

Forced Pass−Through Mode Protection

In Forced Pass−Through Mode, fault protection occurs when V_{OUT} is dragged below V_{IN} − 450 mV. The device will automatically attempt a restart every 20 ms.

Thermal Shutdown (TSD)

When the die temperature increases, due to a high load condition and/or a rising ambient temperature, the output switching is disabled until the die temperature falls to the hysteresis threshold. The junction temperature at which the thermal shutdown activates is nominally T_{SD} with T_{HYS} hysteresis.

Under−Voltage Lockout (UVLO)

If the EN pin is HIGH, once rising V_{IN} reaches V_{UVLO_R}, the part will begin the Soft Start process. When falling V_{IN} reaches V_{UVLO_F}, the output will go to a high Z state and the output voltage will decay into the prevailing load.

External Component Selection

Refer to Table 2: Recommended External Components.

Output Capacitance (C_{OUT})

It is recommended to use the output capacitor shown in the Recommended External Components table. If a different component is chosen, it is important that its effective capacitance is equal to or greater than that of the recommended component. See the Recommended Operating Conditions table for details. For better ripple performance, additional output capacitance can be added.

Output Voltage Ripple

Output voltage ripple is inversely proportional to C_{OUT}. During t_{ON}, when the boost switch is on, all load current is supplied by C_{OUT}.

$$V_{RIPPLE(P-P)} = t_{ON} \cdot \frac{I_{LOAD}}{C_{OUT}} \quad \text{(eq. 1)}$$

And

$$t_{ON} = t_{SW} \cdot D = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad \text{(eq. 2)}$$

therefore:

$$V_{RIPPLE(P-P)} = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \cdot \frac{I_{LOAD}}{C_{OUT}} \quad \text{(eq. 3)}$$

$$t_{SW} = \frac{1}{f_{SW}} \quad \text{(eq. 4)}$$

For better ripple performance, more output capacitance can be added.

Input Capacitance (C_{IN})

The 10uF ceramic 0402 input capacitor should be placed as close as possible between the PV_{IN} pin and GND to minimize the parasitic inductance.

NOTE: The effective capacitance value decreases as V_{IN} increases due to DC bias effects. A high quality capacitor with ample voltage rating should be used for C_{IN}.

Inductor (L1)

The FAN48695 employs peak current limiting and there is a finite amount of time between when the peak current is detected and when the switch turns off. During overload conditions, peak currents will be safely limited to I_{SW_LIM} when using a properly rated inductor. Saturation effects should be considered during inductor selection.

Layout Guideline

The Recommended Layout shows all components on the top layer, top copper in RED and bottom copper in BLUE. For thermal reasons, it is recommended to maximize the pour area for all planes other than SW.

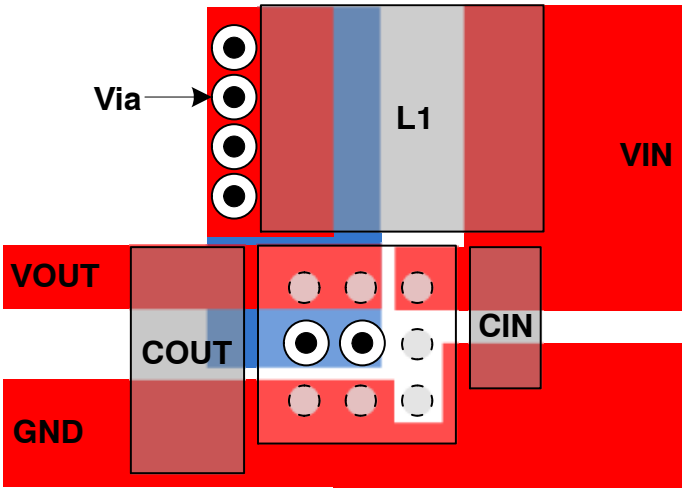
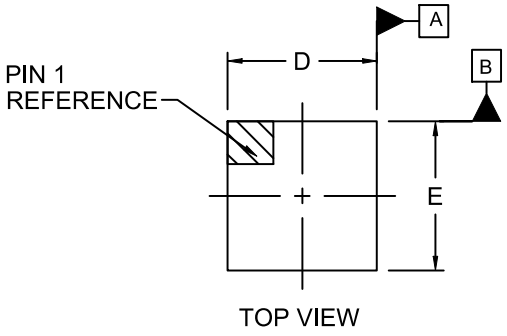


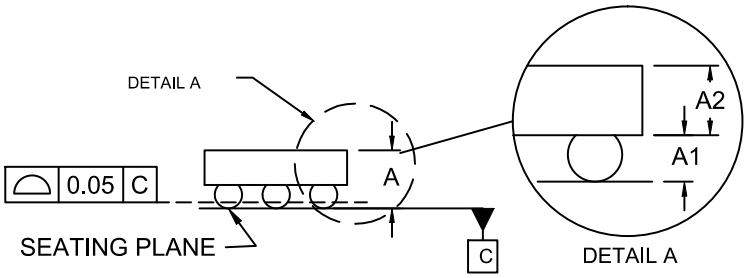
Figure 20. Recommended Layout

WLCSP9, 1.365x1.315x0.586
CASE 567VH
ISSUE O

DATE 03 NOV 2017



TOP VIEW

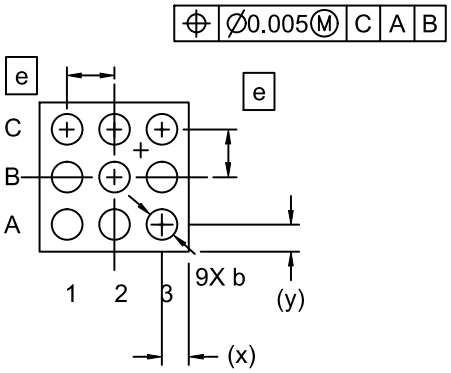


SIDE VIEW

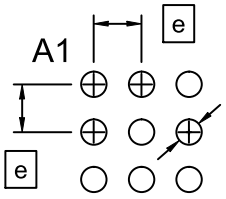
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.548	0.586	0.624
A1	0.188	0.208	0.228
A2	0.360	0.378	0.396
b	0.240	0.260	0.280
D	1.335	1.365	1.395
E	1.285	1.315	1.345
e	0.40 BSC		
x	0.268	0.283	0.298
y	0.243	0.258	0.273



BOTTOM VIEW



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