BDX Series Evaluation Board User Manual

Bellnix Ver. 1.0

Model Name: BDX12-EVM-01 to 08

1. Product Introduction

This is an evaluation board for BDX12-1.0S100RM and BDX12-1.0S50R0S. Output voltage and each setting value, such as sequence etc. can be changed and can get information of input voltage and output current etc. via PMBus serial communication interface. By using USB-PMBusEVM-03 (sold separately), this product can be controlled via PC.

2. Related Documents

To use this evaluation board, we have the following related documents to support your operation. If you need them, please contact with Bellnix sales dept.

1. Data sheet: BDX series
2. Application note for BDX series: Parallel and dual output operation

3. Specification

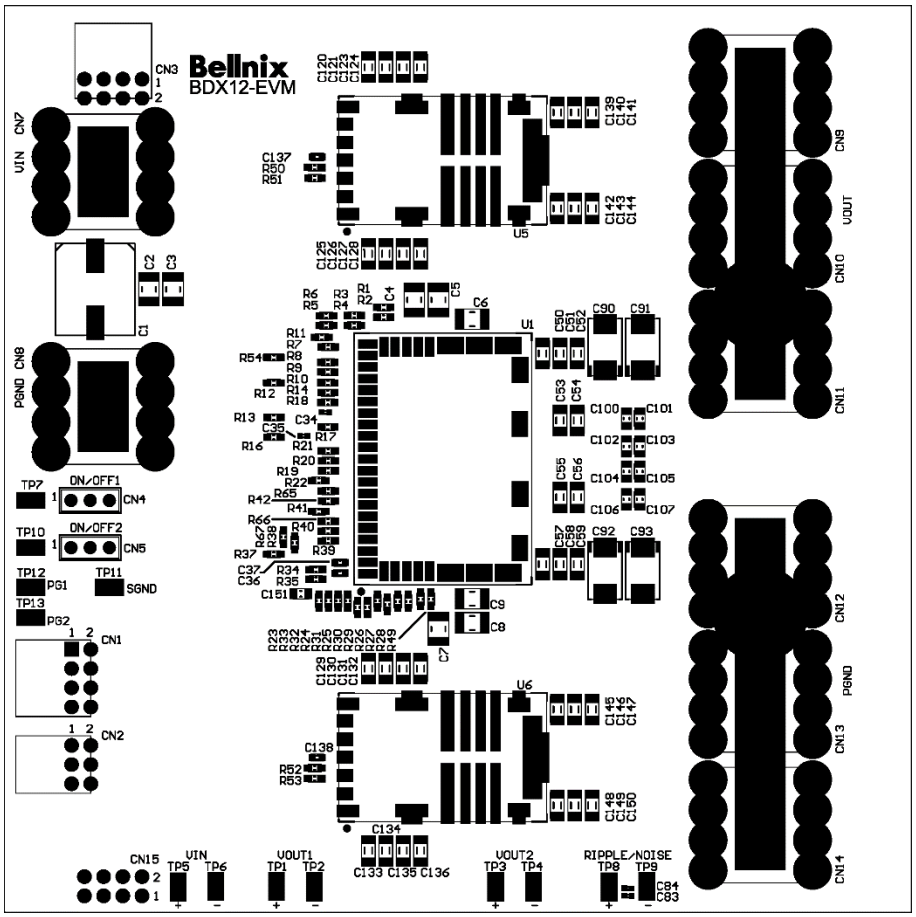
Please refer to Table 1: Electrical spec., Figure 1: PWB layout and Table 3: Pin assignments. The outline of each board are shown in Table 2. For the parts mounted on each board, please refer to the attached “BDX series Evaluation Board Components Table”.

Table 1 Electrical spec.

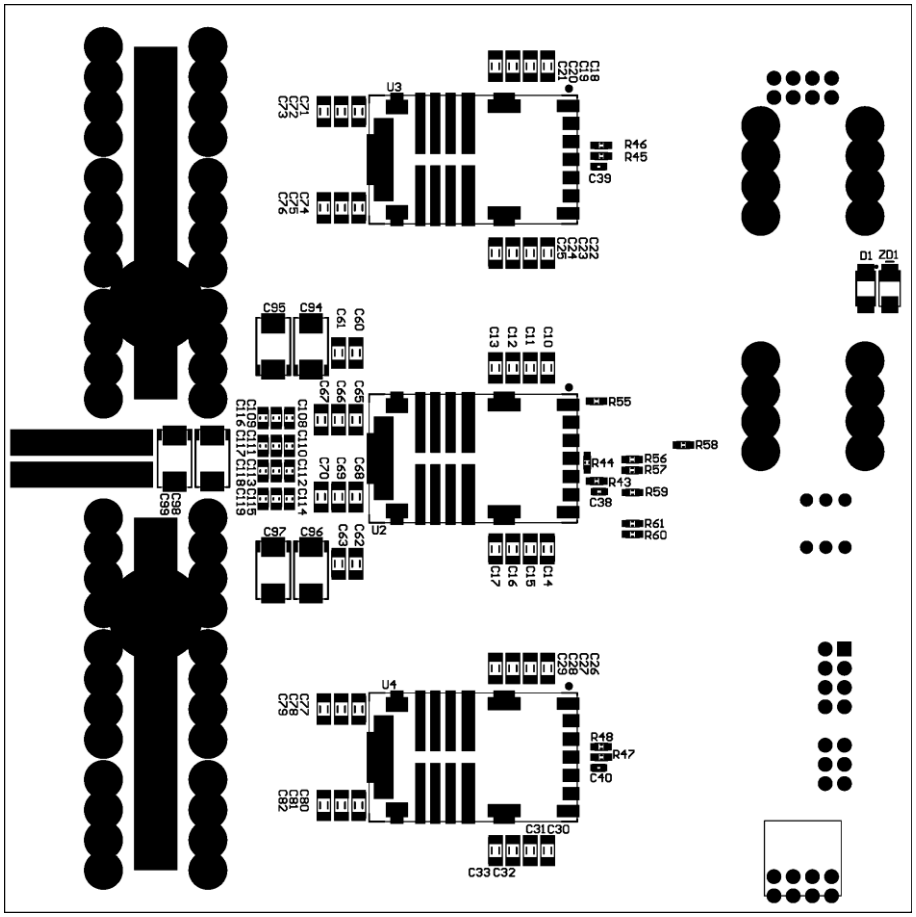
Operating Input Voltage range	8V to 14V
Default Preset Output Voltage	1.0V
Rated Output Voltage	1.0V
Output Current	See Table 2
Output Voltage range	0.5 to 1.2V
Overcurrent protection	Operates at 105% or above (auto restart type)
Serial communication method	PMBus Specification Revision 1.3, AVSBus compliant
External Dimensions	See Figure 2

Table 2 Outline of each board

Model name	Outline	Output current	ASSY No.
BDX12-EVM-01	BDX12-1.0S100RM Single operation board	0 to 100A	01
BDX12-EVM-02	BDX12-1.0S100RM × 1unit // BDX12-1.0S50R0S × 1unit Parallel operation board	0 to 150A	02
BDX12-EVM-03	BDX12-1.0S100RM × 1unit // BDX12-1.0S50R0S × 2units Parallel operation board	0 to 200A	03
BDX12-EVM-04	BDX12-1.0S100RM × 1unit // BDX12-1.0S50R0S × 3units Parallel operation board	0 to 250A	04
BDX12-EVM-05	BDX12-1.0S100RM × 1unit // BDX12-1.0S50R0S × 4units Parallel operation board	0 to 300A	05
BDX12-EVM-06	BDX12-1.0S100RM × 1unit // BDX12-1.0S50R0S × 5units Parallel operation board	0 to 350A	06
BDX12-EVM-07	BDX12-1.0S50R0S Dual output (VOUT2) board (For operation BDX12-EVM-08 is required)	0 to 50A	07
BDX12-EVM-08	BDX12-1.0S100RM board is for operating BDX12-EVM-07	0 to 100A	08

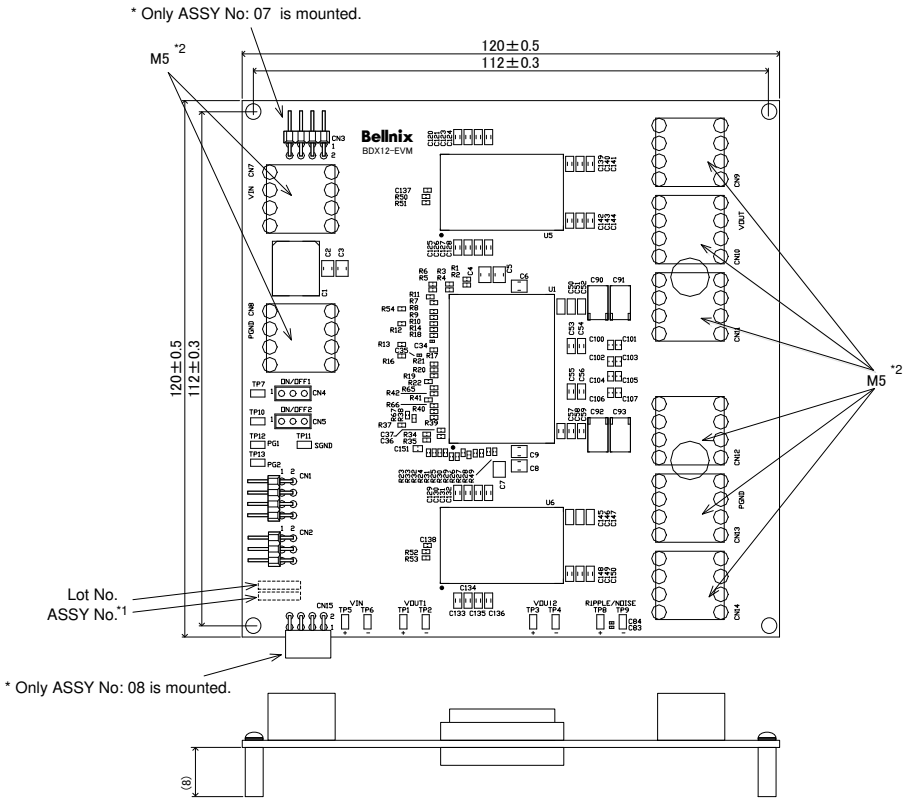


(Top View)



(Bottom View)

Figure 1 PWB Layout



*1 Refer to Table 2.
*2 (+)Round head screw P=4 (spring washer + small washer built in) 5×10 FeNi

Figure 2 External dimensions

Table 3 Pin assignment

Pin	Explanation
CN1	PMBus input/output pin (Male)
CN2	AVSBus input/output pin (Male)
CN3	Parallel input/output pin (Male)
CN4	ON/OFF1 (VOUT1) control pin
CN5	ON/OFF2 (VOUT2) control pin
CN7	Input power pin (+)
CN8	Input power pin (-)
CN9 to 11	Load connection pin (+)
CN12 to 14	Load connection pin (-)
CN15	Parallel input/output pin (Female)
TP1	Output voltage (VOUT1) measurement pin(+)
TP2	Output voltage (VOUT1) measurement pin (-)
TP3	Output voltage (VOUT2) measurement pin (+)
TP4	Output voltage (VOUT2) measurement pin (-)
TP5	Input voltage measurement pin (+)
TP6	Input voltage measurement pin (-)
TP7	Voltage measurement pin of ON/OFF1 pin *SGND pin shall be referred.
TP8	Confirmation pin of Ripple noise wave form (+)
TP9	Confirmation pin of Ripple noise wave form (-)
TP10	Voltage measurement pin of ON/OFF2 pin *SGND pin shall be referred.
TP11	SGND pin
TP12	Confirmation pin of P-Good1 (VOUT1) signal *SGND pin shall be referred.
TP13	Confirmation pin of P-Good2 (VOUT2) signal *SGND pin shall be referred.

4. Handling Method

4-1. Connection

Connect DC power supply, load, voltmeter and USB-PMBusEVM-03 (or an equivalent PMBus/AVSBus master device) according to Figure 3 or Figure 4.

CN1 pin assignment	
1, 3, 4, 5, 7	SGND
2	SDA
6	SCL
8	SALRT

CN2 pin assignment	
1	AVS_CLK
2	AVS_SDA
3	AVS_MDA
4	SGND
5	AVS_VDDIO
6	NC

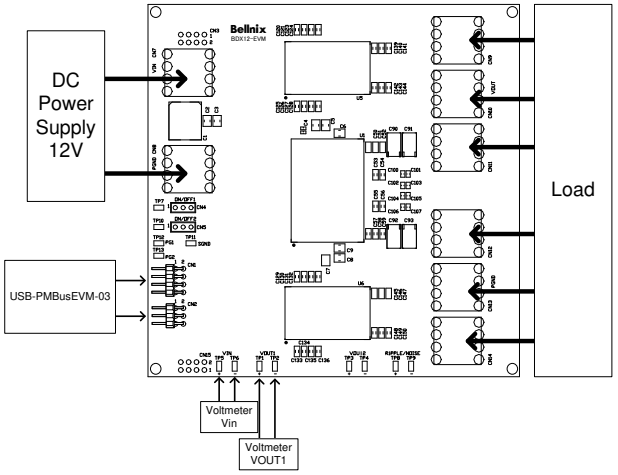


Figure 3 Connection method (BDX12-EVM-01 to 06)

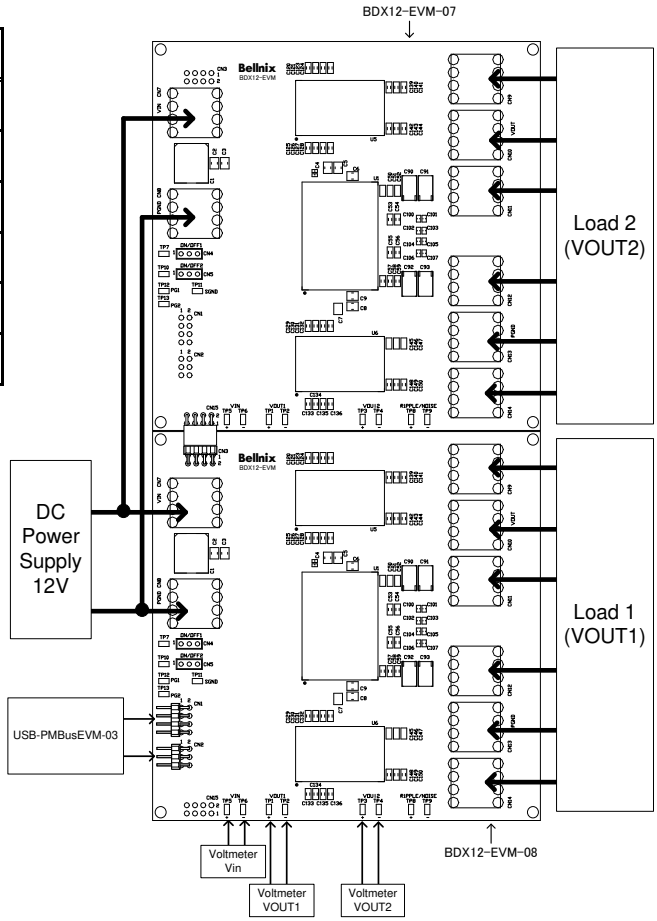


Figure 4 Connection method (BDX12-EVM-07, 08)

Note1: Wire between the input power - board and the load - board in order to lower the impedance.
Note2: If the line impedance between the input power - board gets high, the input voltage of the converter (U1 to U6) may become unstable. In that case, mount a capacitor which has appropriate capacity to operate stable input voltage to C1, C2 and C3.

5. Function List

The function, default setting and the setting change method are mentioned as Table 4.

Table 4 Function List

Function	Default setting	Setting change method
Device address setting	1011 101b	By the setting resistor R49
ON/OFF pin setting	ON	By CN4, CN5, JP1 and JP2
ON/OFF control operation setting	ON/OFF pin : enabled Serial communication: disabled	Based on serial communication
Output voltage limit	1.2V	Based on serial communication
Output voltage setting	1.0V	Based on serial communication
Output voltage trimming setting	0V	Based on serial communication
Margin voltage setting	High：1.2V Low：0.5V	Based on serial communication
Switching margin voltage	Margin OFF	Based on serial communication
Turn-on delay setting	0.2ms	Based on serial communication
Turn-on rise setting	1ms	Based on serial communication
Turn-off delay setting	0ms	Based on serial communication
P-Good signal output	Yes	Based on serial communication
Remote sensing	Yes	—
Output overvoltage protection	1.35V	Based on serial communication
Output undervoltage detection	0V	Based on serial communication
Output overcurrent protection	Operates at 105% or above (auto restart type)	
Undervoltage lock out	Start-up: 7.5V typ. Stop: 6.8V typ.	—
Read STATUS register	Yes	—
Clear STATUS resister	Yes	—
Input voltage monitor	Yes	—
Output voltage monitor	Yes	—
Output current monitor	Yes	—
Storing/restoring the setting value	Yes	—

Note: Refer to BDX series data sheet for enable PMBus or AVSBus commands.

5-1. ON/OFF Function

As shown in Table 5, the ON/OFF of the output can be controlled by replacing the jump socket (JP1, JP2) of CN4, CN5.

Table 5 ON/OFF Function

CN4, CN5	Output	Default setting
Short between pin 1 - 2	ON	●
Short between pin 2 - 3	OFF	

5-2. Device Address Setup

The device address can be set by the address setting resistor R49. Table 6 shows the resistor value and the device addresses.

Table 6 Device address setup

Device address	Rsa [Ω]	Device address	Rsa [Ω]
1100 000	0	1010 000	1500
1100 001	180	1010 001	1800
1100 100	330	1010 100	2200
1100 101	470	1010 101	2700
1000 000	680	1011 000	3300
1000 001	820	1011 001	3900
1000 100	1000	1011 100	4700
1000 101	1200	1011 101	5600 (default setting)

5-3. Output Voltage Setup

Output voltage can be changed in the range between 0.5 to 1.2V via serial communication. The default preset output voltage is 1.0V. Output voltage needs to be changed by serial communication. Refer to BDX series data sheet for output voltage setups.

5-4. P-Good Output

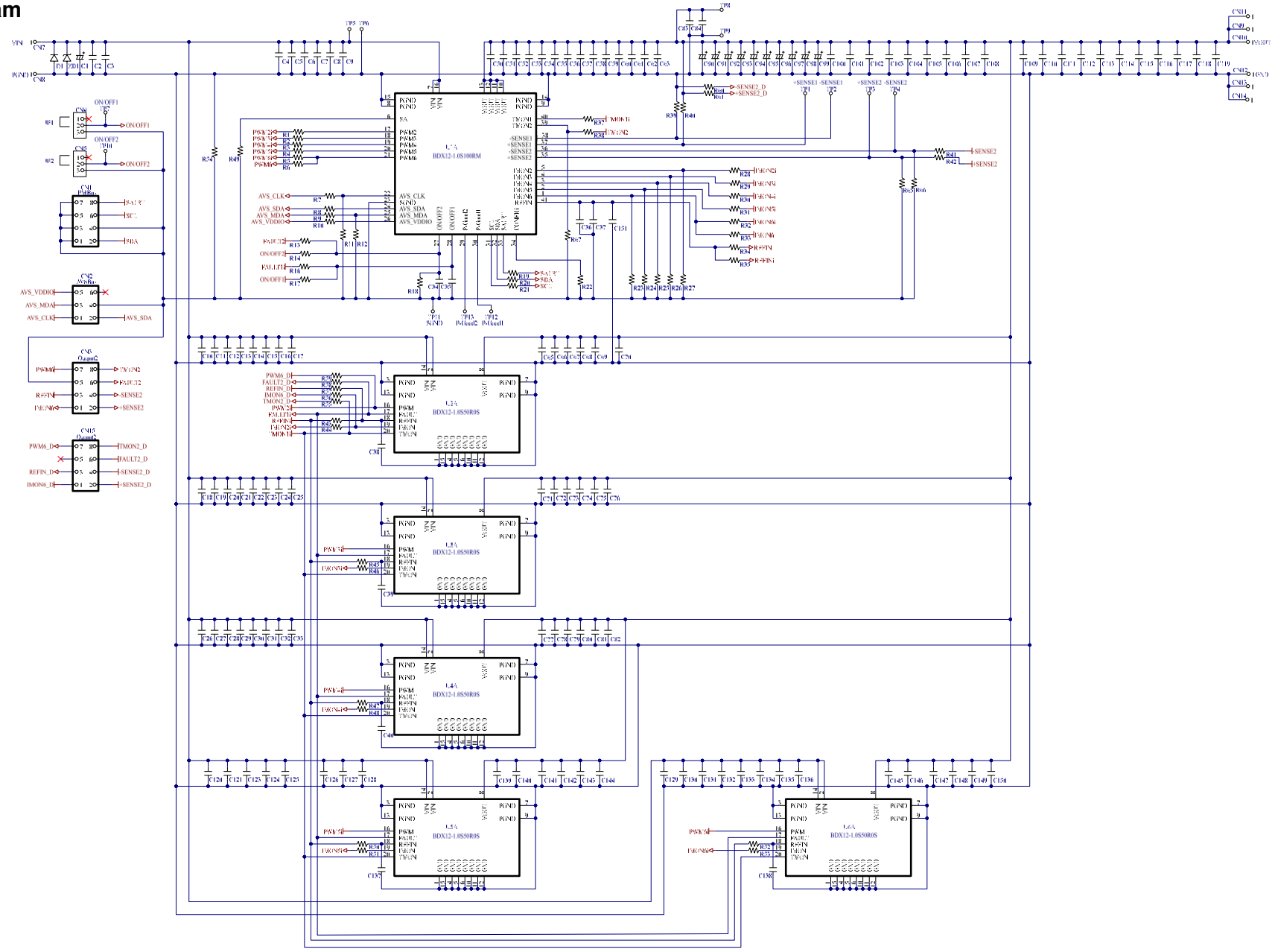
P-Good1 and P-Good2 pins allow monitoring the status of VOUT1 and VOUT2 respectively.

P-Goodx pin outputs High when the converter is performing the assumed regulation, and Low when it is under the following conditions.

-When the output is set to OFF by ON/OFFx pin or PMBus communication
-During turn-on delay
-During turn-on rise
-When protection function such as overcurrent protection, under voltage lock out, output overvoltage protection etc. are in operation.

Note 1: P-Goodx pin may output High when input voltage turn-on up to operation starting voltage.

6. Circuit Diagram



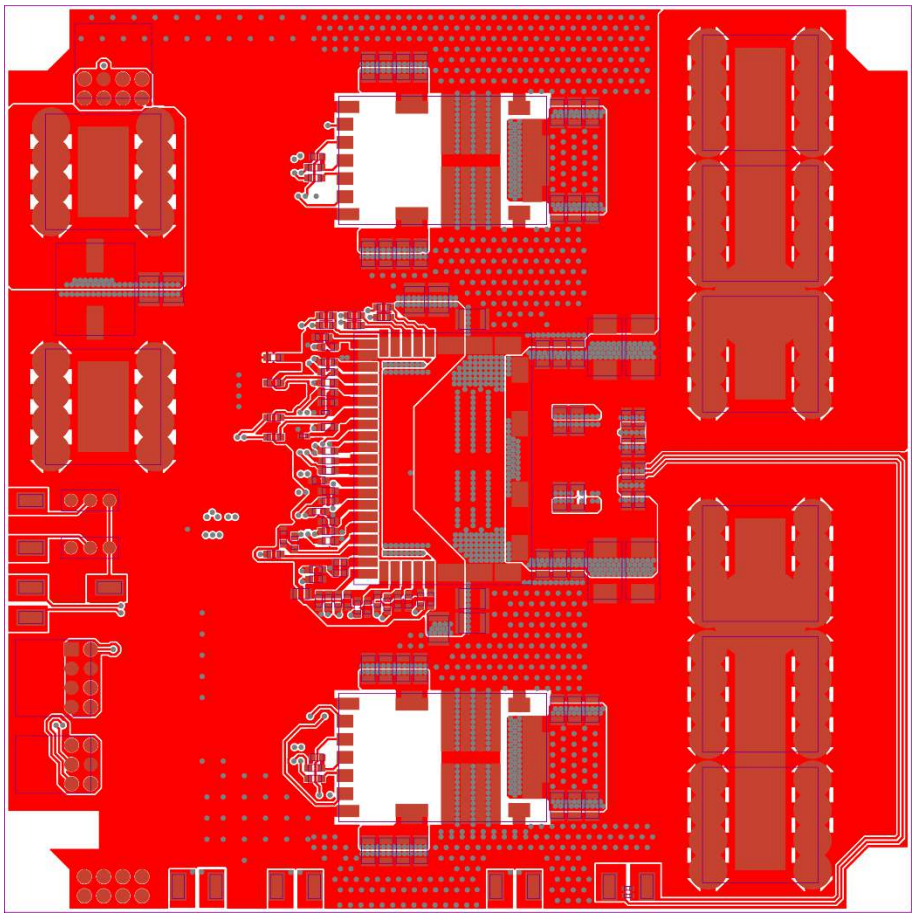
7. Pattern Layout Description

The product name will be abbreviated as follows.

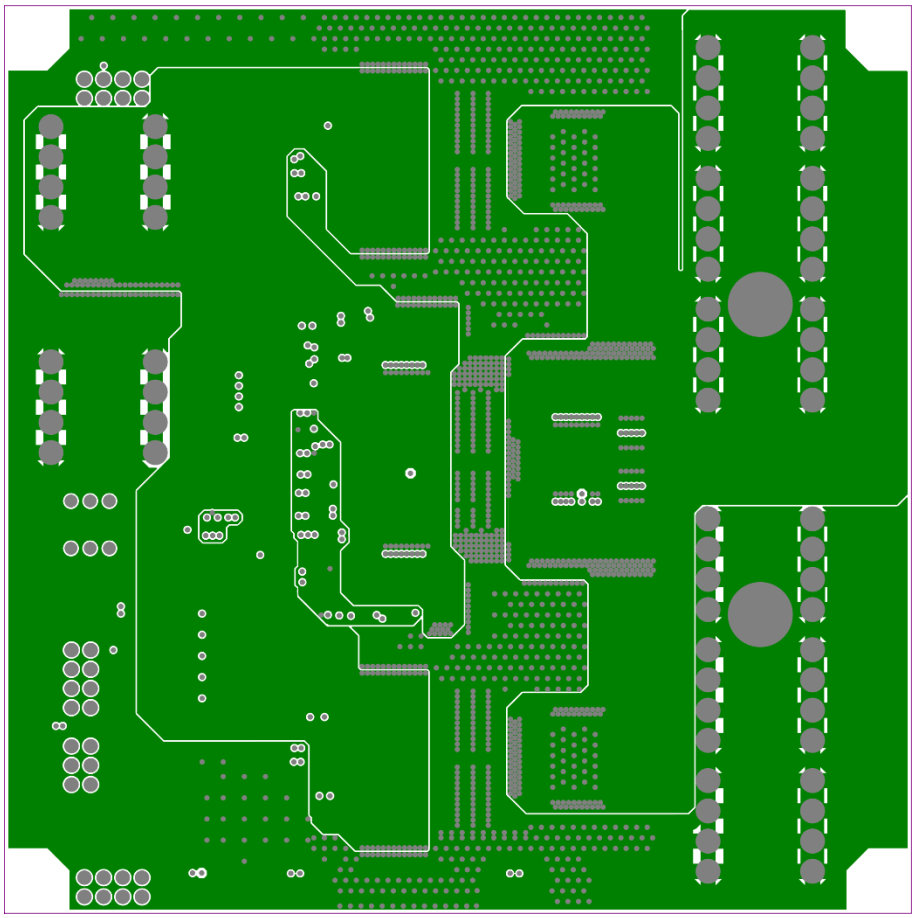
BDX12-1.0S100RM: BDX-100M
BDX12-1.0S50R0S: BDX-50S

7-1. Pattern Diagram

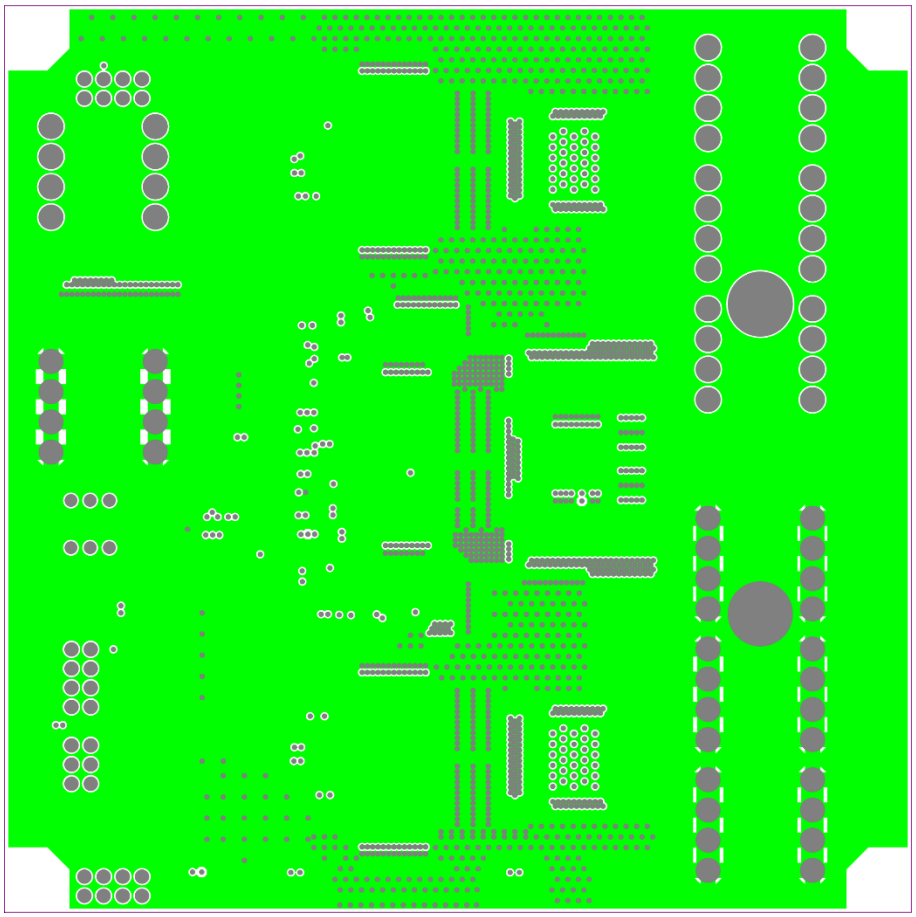
Please refer to the following pages.



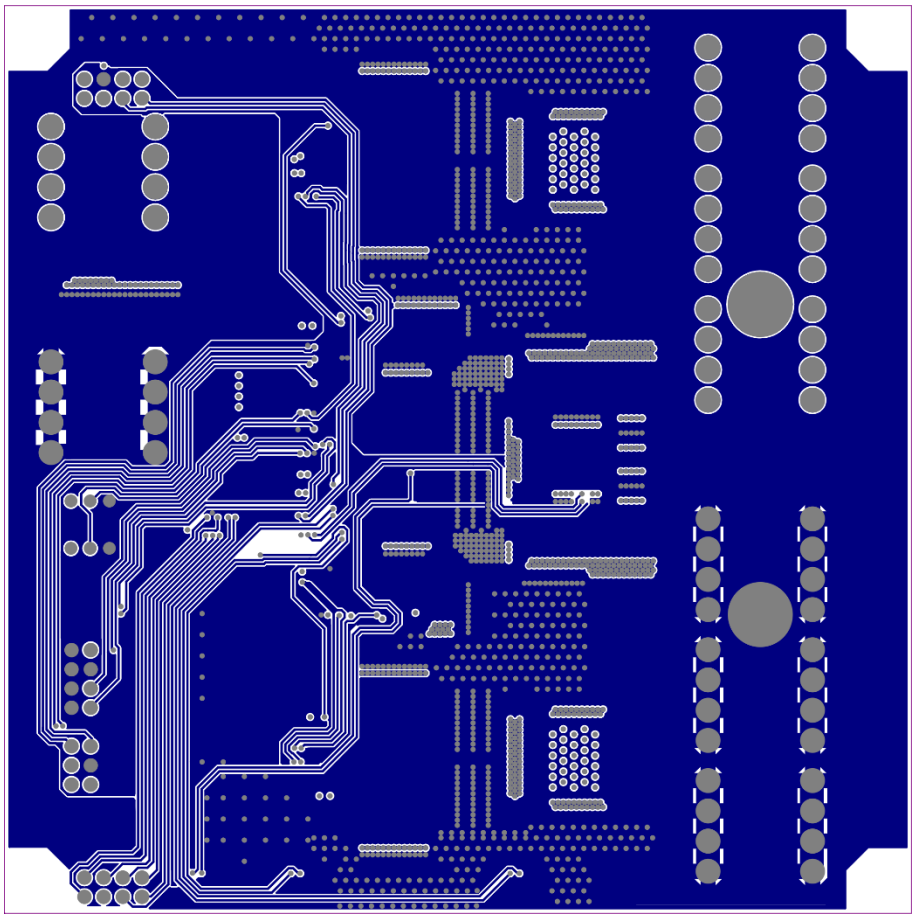
Surface- First layer (Top View)



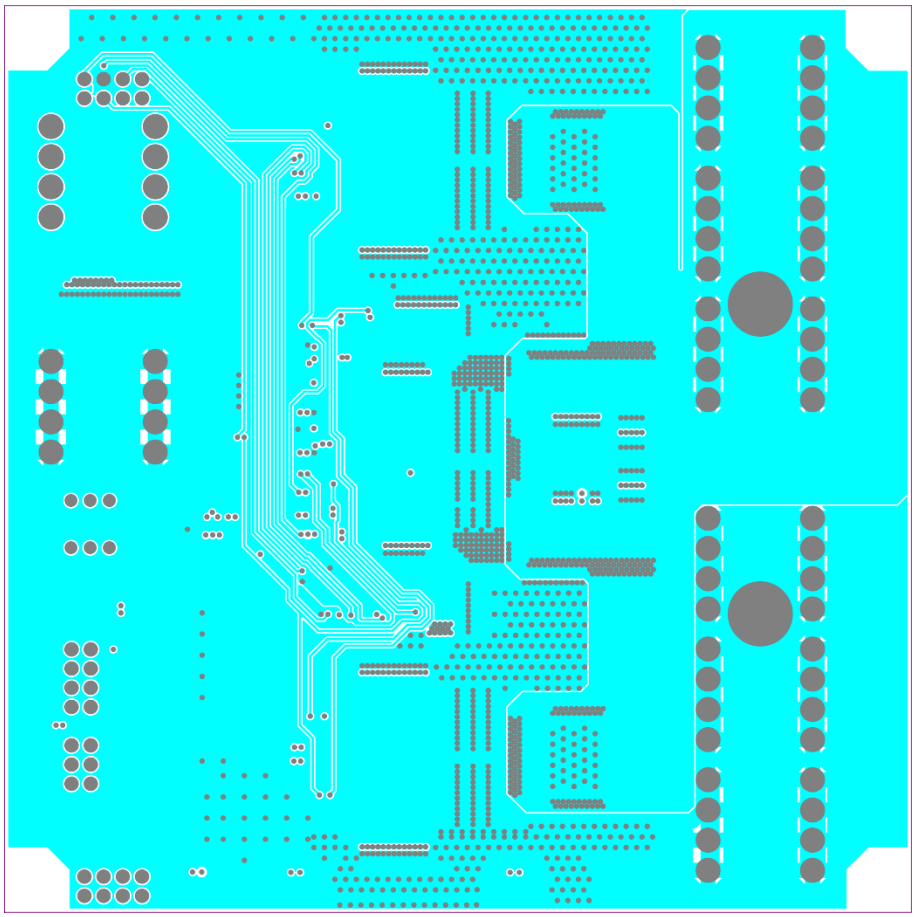
Inner layer- Second layer (Top View)



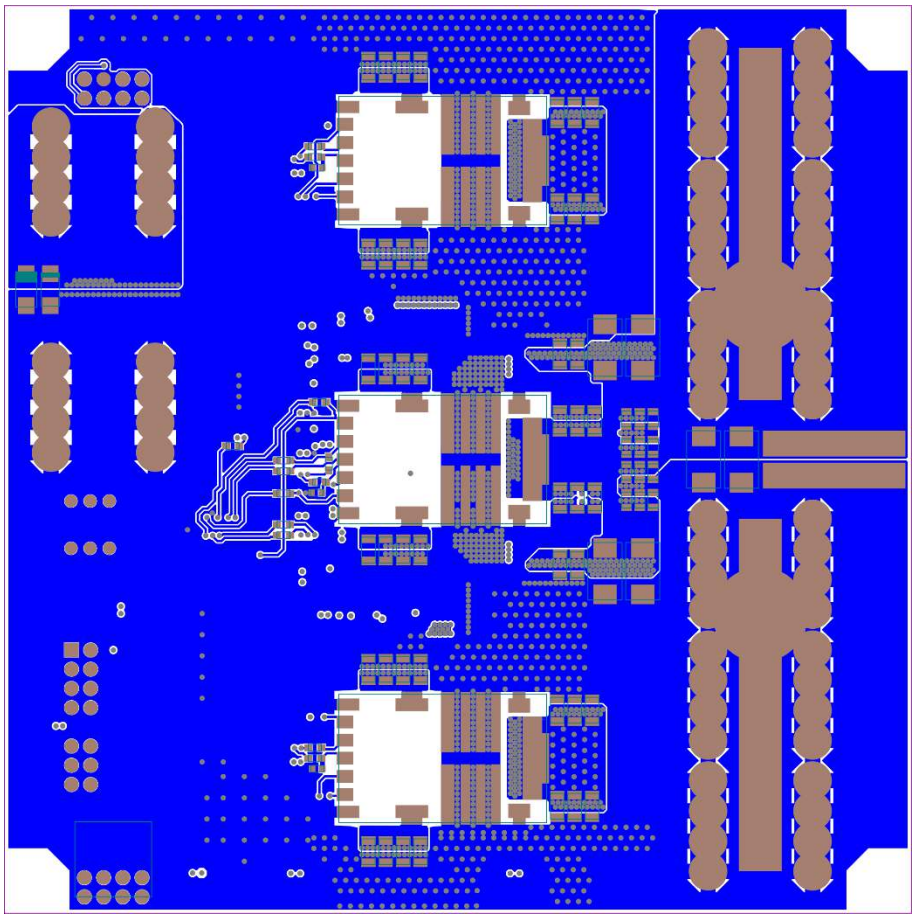
Inner layer- Third layer (Top View)



Inner layer- Fourth layer (Top View)



Inner layer- Fifth layer (Top View)



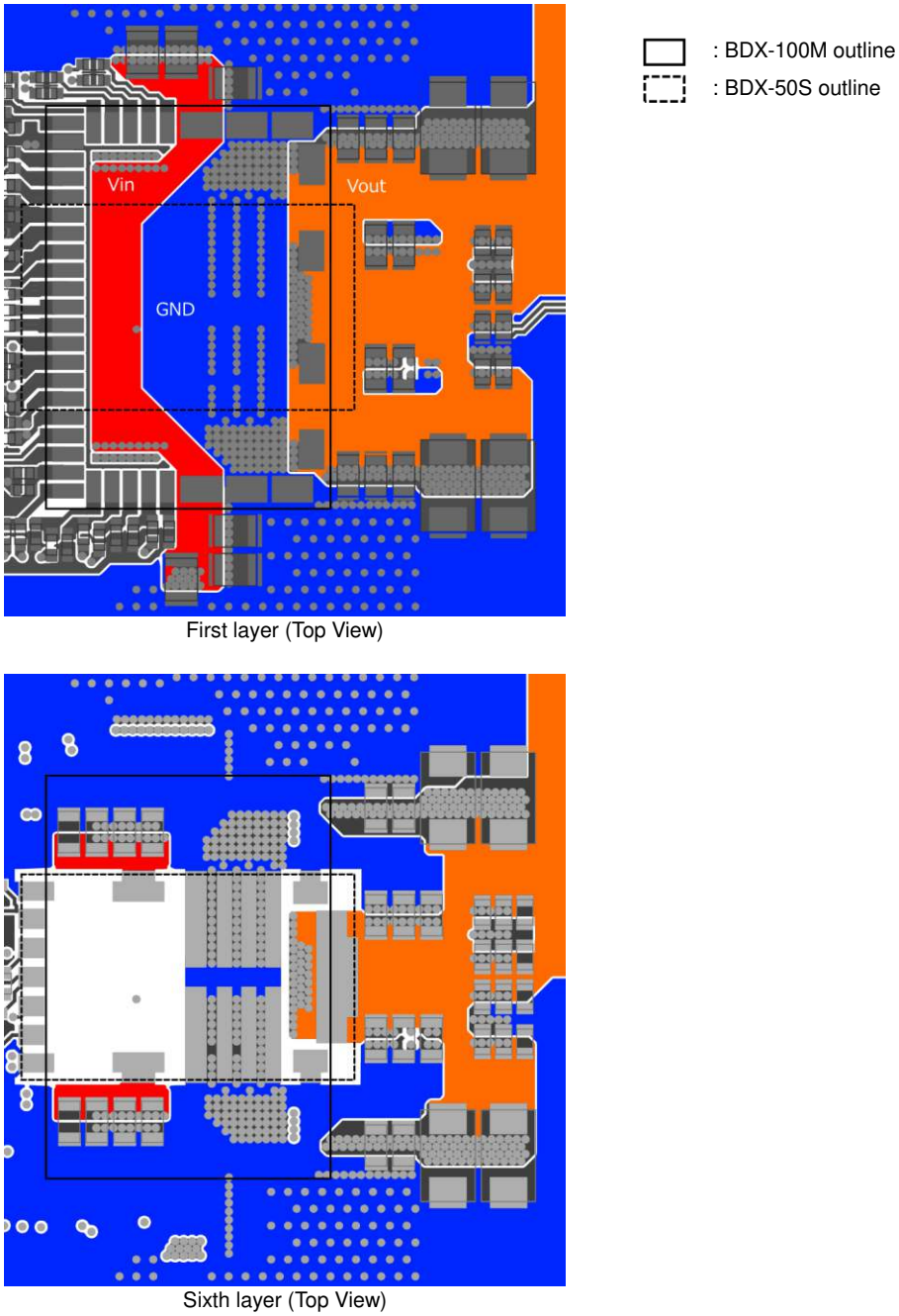
Back side- Sixth layer (Top View)

7-2. Layout Description

7-2-1. Power Line

When performing parallel operation, it is necessary to layout so that the line impedance between BDX12-1.0S100RM and BDX12-1.0S50R0S is as low as possible so that the current balance does not collapse. VIN, PGND and VOUT pins of BDX12-1.0S100RM and BDX12-1.0S50R0S are placed in line symmetry to facilitate parallel connection.

When placing BDX12-1.0S50R0S on the back side of BDX12-1.0S100RM, it is recommended to match the positions of the VOUT and GND pins especially where large current flows, as shown in Figure 5.



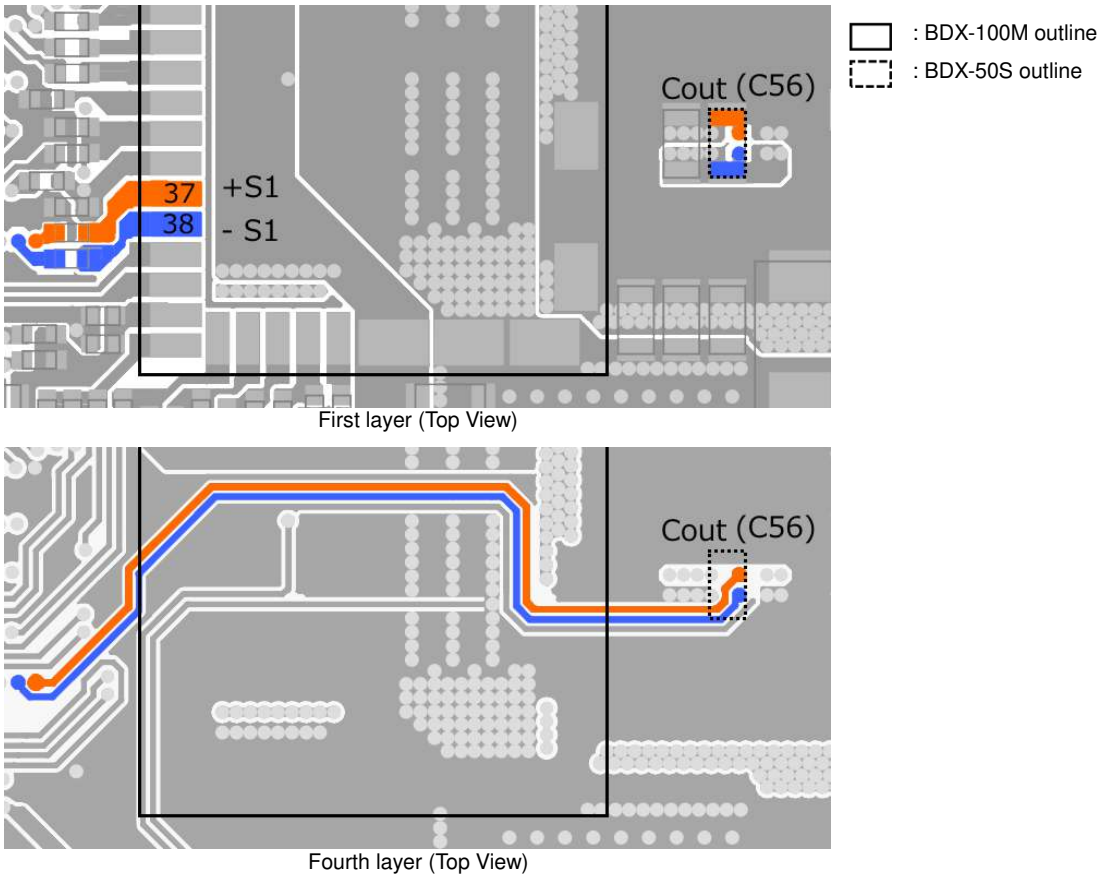
First layer (Top View)

Sixth layer (Top View)

Figure 5 Power Line Layout Enlarged View

7-2-2. SENSE Line

SENSE line (the line from +SENSE1, -SENSE1 pin to the both sides of Cout) is related to the feedback loop. Since the SENSE line is sensitive to noise, do not route the wiring long as much as possible and wire it in parallel. (Figure 6)



First layer (Top View)

Fourth layer (Top View)

Figure 6 SENSE Line Layout Enlarged View

7-2-3. IMON-REFIN Line

IMON-REFIN line (the line from IMONx and REFIN pin of BDX-100M to IMON and REFIN pin of BDX12-50S) is strongly related to the feedback loop and current monitor accuracy. Since the IMON-REFIN line is sensitive to noise, do not route the wiring long as much as possible as and wire it in parallel, as shown in Figure 7.

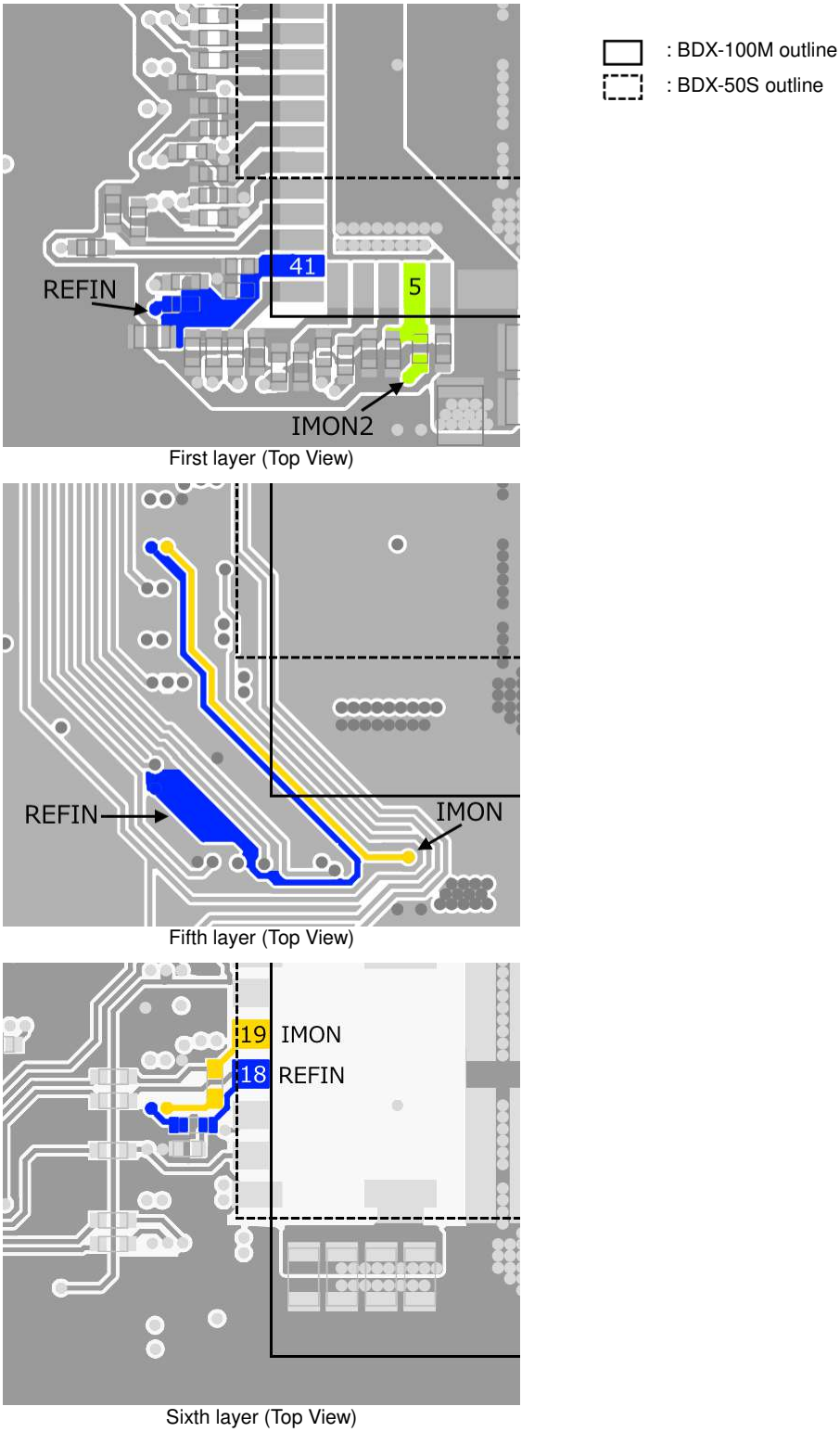
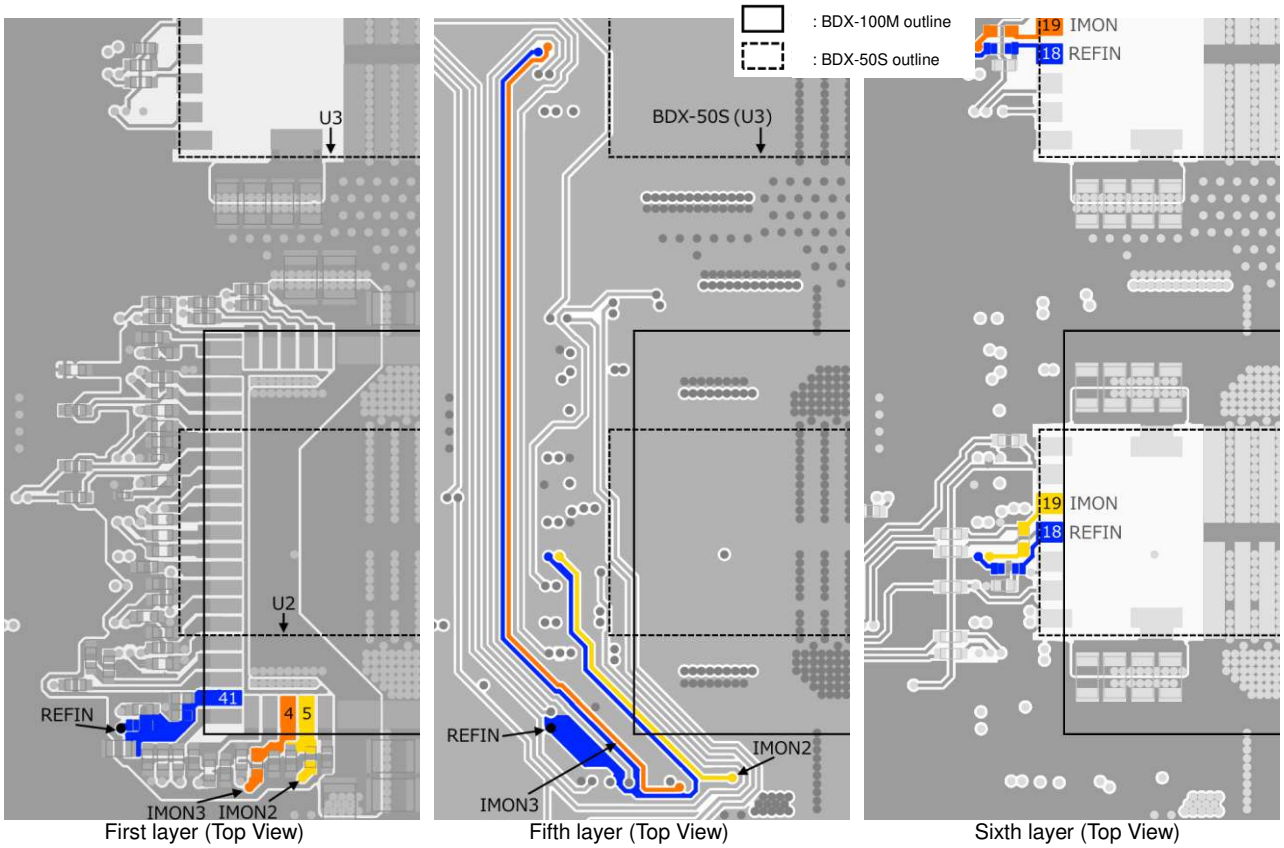


Figure 7 IMON-REFIN Line Layout Enlarged View (1)

When connecting BDX-100M and multiple BDX-50S units, branch off REFIN in the vicinity of BDX-100M and wire IMON and REFIN in parallel, as shown in Figure 8.



First layer (Top View) Fifth layer (Top View) Sixth layer (Top View)

Figure 8 IMON-REFIN Line Layout Enlarged View (2)

8. BOM

To view a BOM list, please click the URL below.

http://www.bellnix.com/pdf/BDX12-EVM_BOM.pdf