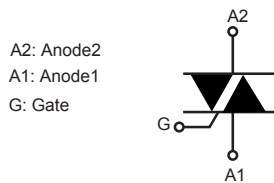
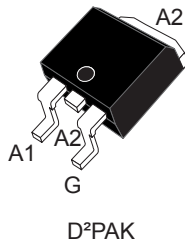


12 A - 800 V logic level T-series Triac in D²PAK


Product status link

[T1210T-8G](#)

Product summary

| | |
|-------------------|-------|
| $I_{T(RMS)}$ | 12 A |
| V_{DRM}/V_{RRM} | 800 V |
| V_{DSM}/V_{RSM} | 900 V |
| I_{GT} | 10 mA |

Features

- 150 °C maximum junction temperature
- Three quadrants
- High commutation on resistive loads
- Surge capability V_{DSM} , $V_{RSM} = 900$ V
- Benefits:
 - Easy direct control by MCU thanks to low 10 mA I_{GT}
 - Increase of thermal margin due to extended working T_j up to 150 °C
 - Ability to turn off resistive surges of 28 A

Applications

- General purpose AC line load switching
- Small home appliances with resistive loads
- Hybrid relays
- Inrush current limiting circuits
- Overvoltage crowbar protection

Description

The SMD T1210T-8G Triac can be used for the on/off or phase angle control function in general purpose AC switching with resistive loads. A Logic level T-series Triac, the T1210T-8G can be controlled directly from an MCU with a simplified circuit.

T-series triacs are optimized for high EMI constraints. The surface mount D²PAK package enables compact SMT designs for automated manufacturing.

D²PAK package's molding compound resin is halogen-free and meets UL94 flammability standard level V0.

Package environmentally friendly [Ecopack2](#) graded (RoHS and Halogen Free compliance).

1 Characteristics

Table 1. Absolute maximum ratings (limiting values), $T_j = 25\text{ °C}$ unless otherwise specified

| Symbol | Parameter | | Value | Unit |
|-------------------|--|--|-------------|-------------|
| V_{DRM}/V_{RRM} | Repetitive peak off-state voltage (50-60 Hz) | $T_j = 125\text{ °C}$ | 800 | V |
| | | $T_j = 150\text{ °C}$ | 600 | V |
| V_{DSM}/V_{RSM} | Non Repetitive peak off-state voltage | $t_p = 10\text{ ms}$, $T_j = 25\text{ °C}$ | 900 | V |
| $I_{T(RMS)}$ | RMS on-state current (full sine wave) | $T_c = 131\text{ °C}$ | 12 | A |
| I_{TSM} | Non repetitive surge peak on-state current (full cycle, T_j initial = 25 °C) | $t = 16.7\text{ ms}$ | 105 | A |
| | | $t = 20\text{ ms}$ | 100 | |
| I^2t | I^2t value for fusing | $t_p = 10\text{ ms}$ | 66 | A^2s |
| di/dt | Critical rate of rise of on-state current, $I_G = 2 \times I_{GT}$, $tr \leq 100\text{ ns}$ | $f = 100\text{ Hz}$ | 100 | $A/\mu s$ |
| I_{GM} | Peak gate current | $t_p = 20\text{ }\mu s$, | 4 | A |
| V_{GM} | Peak Gate Voltage | $T_j = 150\text{ °C}$ | 5 | V |
| $P_{G(AV)}$ | Average gate power dissipation | $T_j = 150\text{ °C}$ | 1 | W |
| T_{stg} | Storage junction temperature range | | -40 to +150 | $^{\circ}C$ |
| T_j | Operating junction temperature range | | -40 to +150 | $^{\circ}C$ |

Table 2. Electrical characteristics ($T_j = 25\text{ °C}$, unless otherwise specified)

| Symbol | Test conditions | Quadrants; T_j | | Value | Unit |
|-------------------|---|-----------------------|------|-------|-----------|
| $I_{GT}^{(1)}$ | $V_D = 12\text{ V}$, $R_L = 30\text{ }\Omega$ | I - II - III | Max. | 10 | mA |
| V_{GT} | $V_D = 12\text{ V}$, $R_L = 30\text{ }\Omega$ | I - II - III | Max. | 1 | V |
| V_{GD} | $V_D = 800\text{ V}$, $R_L = 3.3\text{ k}\Omega$ $T_j = 125\text{ °C}$ | I - II - III | Min. | 0.15 | V |
| I_L | $I_G = 1.2 \times I_{GT}$ | I - III | Max. | 30 | mA |
| | $I_G = 1.2 \times I_{GT}$ | II | Max. | 35 | mA |
| $I_H^{(2)}$ | $I_T = 500\text{ mA}$, gate open | | Max. | 25 | mA |
| $dV/dt^{(2)}$ | $V_D = 536\text{ V}$, gate open | $T_j = 125\text{ °C}$ | Min. | 200 | $V/\mu s$ |
| | $V_D = 402\text{ V}$, gate open | $T_j = 150\text{ °C}$ | Min. | 150 | $V/\mu s$ |
| $(di/dt)_c^{(2)}$ | $(dV/dt)_c = 0.1\text{ V}/\mu s$ | $T_j = 125\text{ °C}$ | Min. | 20 | A/ms |
| | | $T_j = 150\text{ °C}$ | | 14.4 | |
| | $(dV/dt)_c = 10\text{ V}/\mu s$ | $T_j = 125\text{ °C}$ | Min. | 6 | A/ms |
| | | $T_j = 150\text{ °C}$ | | 3.8 | |

1. Minimum I_{GT} is guaranteed at 5% of $I_{GT\text{ max}}$
2. For both polarities of A2 referenced to A1.

Table 3. Static characteristics

| Symbol | Test conditions | T_j | | Value | Unit |
|-------------------|--|--------|------|-------|------|
| $V_{TM}^{(1)}$ | $I_T = 16.9\text{ A}$, $t_p = 380\ \mu\text{s}$ | 25 °C | Max. | 1.55 | V |
| $V_{TO}^{(1)}$ | Threshold on-state voltage | 150 °C | Max. | 0.81 | V |
| $R_D^{(1)}$ | Dynamic resistance | 150 °C | Max. | 40 | mΩ |
| I_{DRM}/I_{RRM} | $V_{DRM} = V_{RRM} = 800\text{ V}$ | 25 °C | Max. | 7.5 | μA |
| | | 125°C | | 1.0 | mA |
| | $V_{DRM} = V_{RRM} = 600\text{ V}$ | 150 °C | Max. | 3.3 | mA |

1. For both polarities of A2 referenced to A1.

Table 4. Thermal resistance

| Symbol | Parameter | | | Value | Unit |
|---------------|--|--------------------|------|-------|------|
| $R_{th(j-c)}$ | Junction to case (AC) | D ² PAK | Max. | 1.3 | °C/W |
| $R_{th(j-a)}$ | Junction to ambient ($S_{CU}^{(1)} = 2\text{ cm}^2$) | | Typ. | 45 | °C/W |

1. S_{cu} : copper pad surface under tab, 35 μm copper thickness on FR4 PCB.

1.1 Characteristics (curves)

Figure 1. Maximum power dissipation versus on-state RMS current

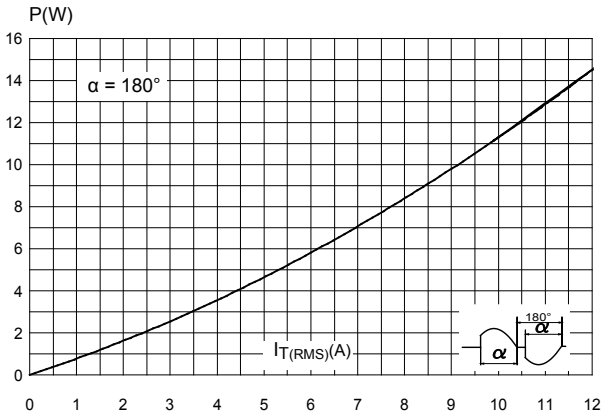


Figure 2. On-state RMS current versus case temperature

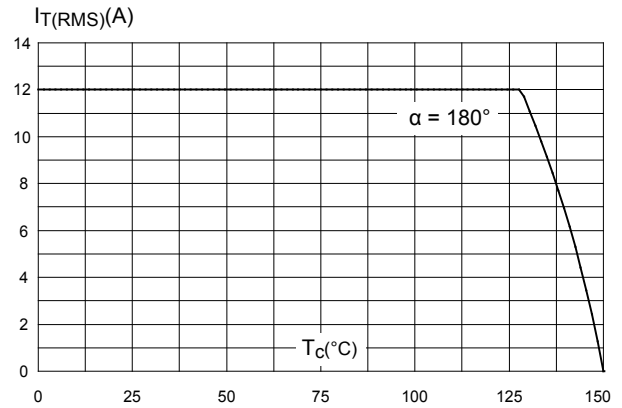


Figure 3. On-state RMS current versus ambient temperature (free air convection)

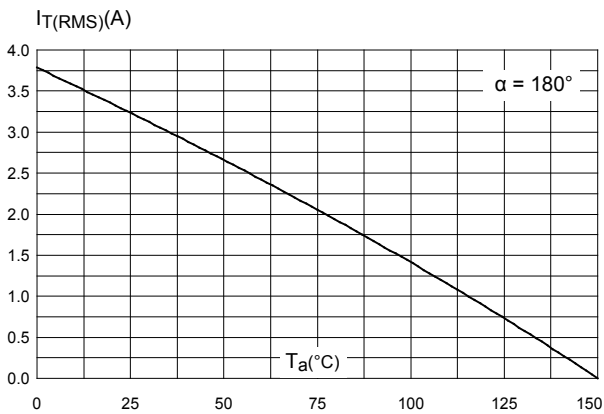


Figure 4. Relative variation of thermal impedance versus pulse duration

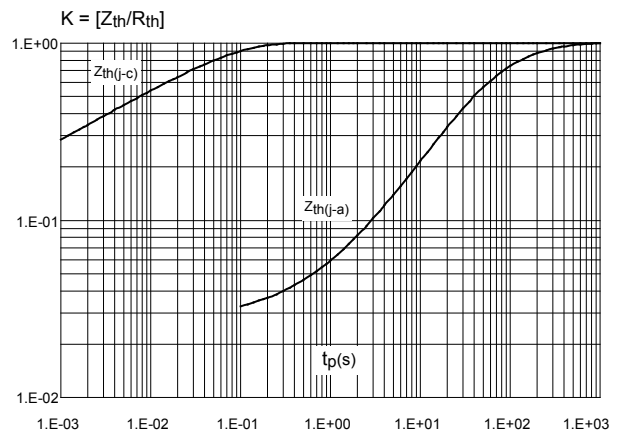


Figure 5. Relative variation of gate trigger voltage and current versus junction temperature (typical values)

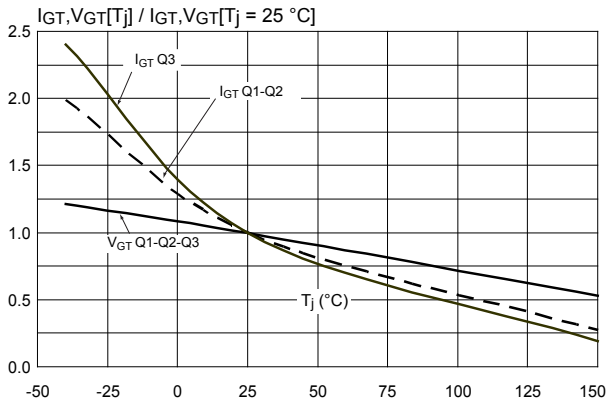


Figure 6. Relative variation of holding current and latching current versus junction temperature (typical values)

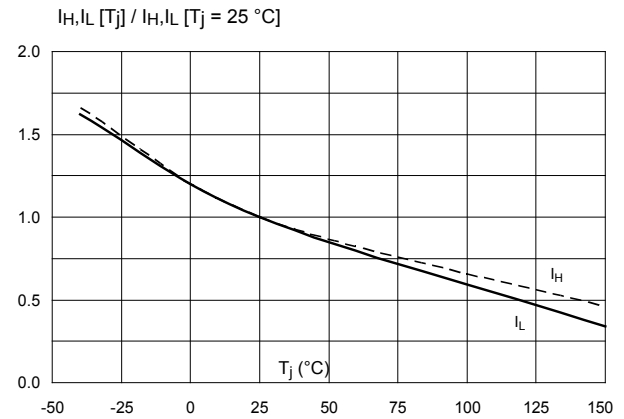


Figure 7. Surge peak on-state current versus number of cycles

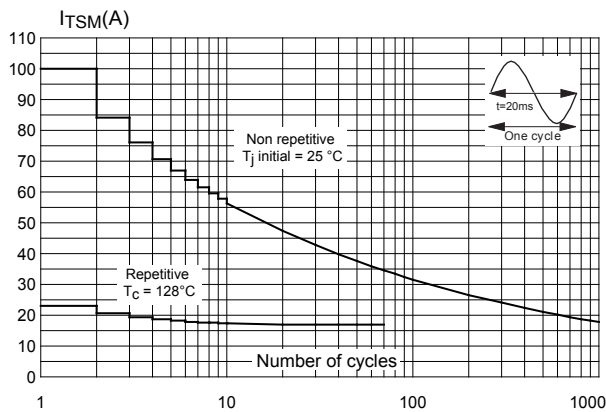


Figure 8. Non repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms

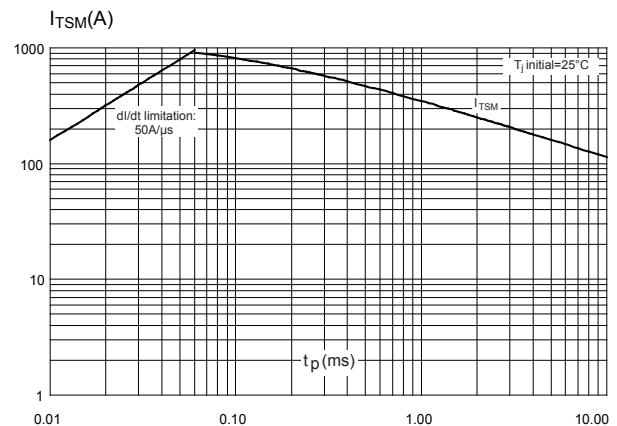


Figure 9. On-state characteristics (maximum values)

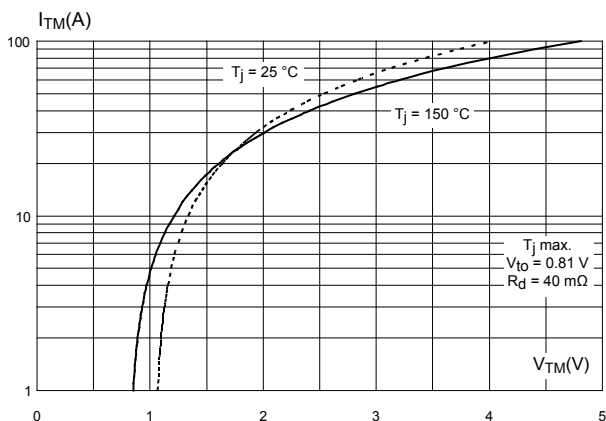


Figure 10. Relative variation of critical rate of decrease of main voltage versus junction temperature

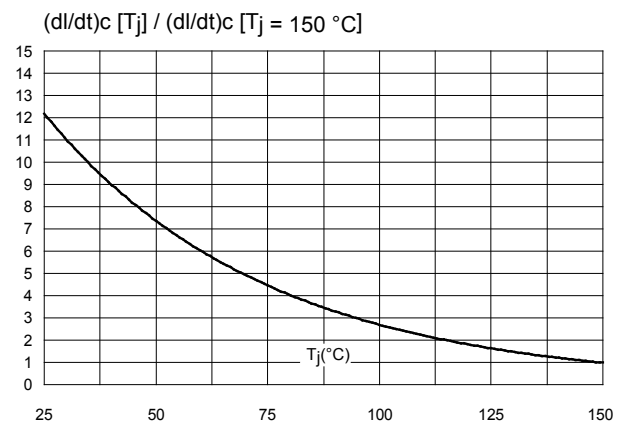


Figure 11. Relative variation of critical rate of decrease of main current versus reapplied dV/dt (typical values)

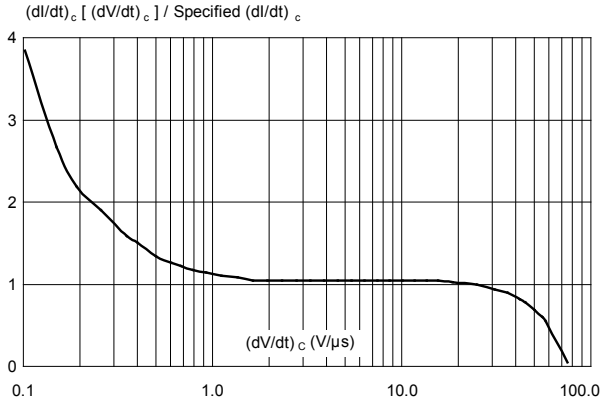


Figure 12. Relative variation of static dV/dt immunity versus junction temperature

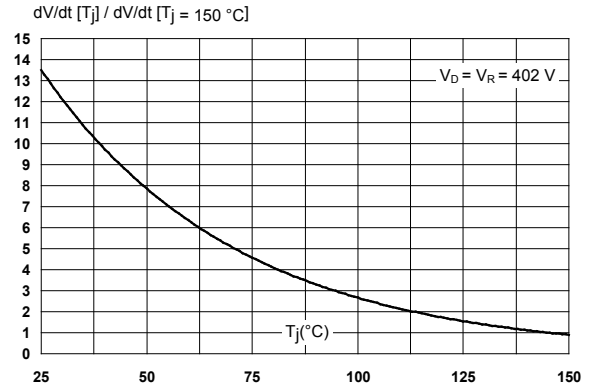


Figure 13. Relative variation of leakage current versus junction temperature for different values of blocking voltage (typical values)

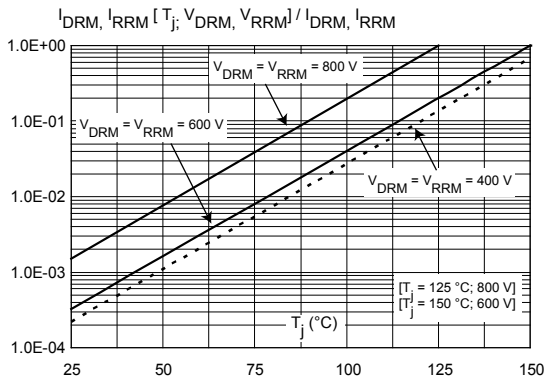
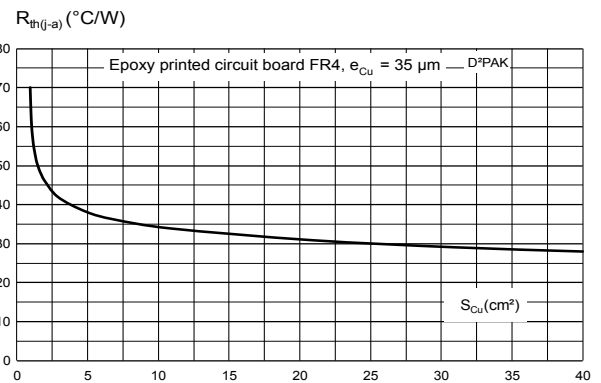


Figure 14. Thermal resistance junction to ambient versus copper surface under tab



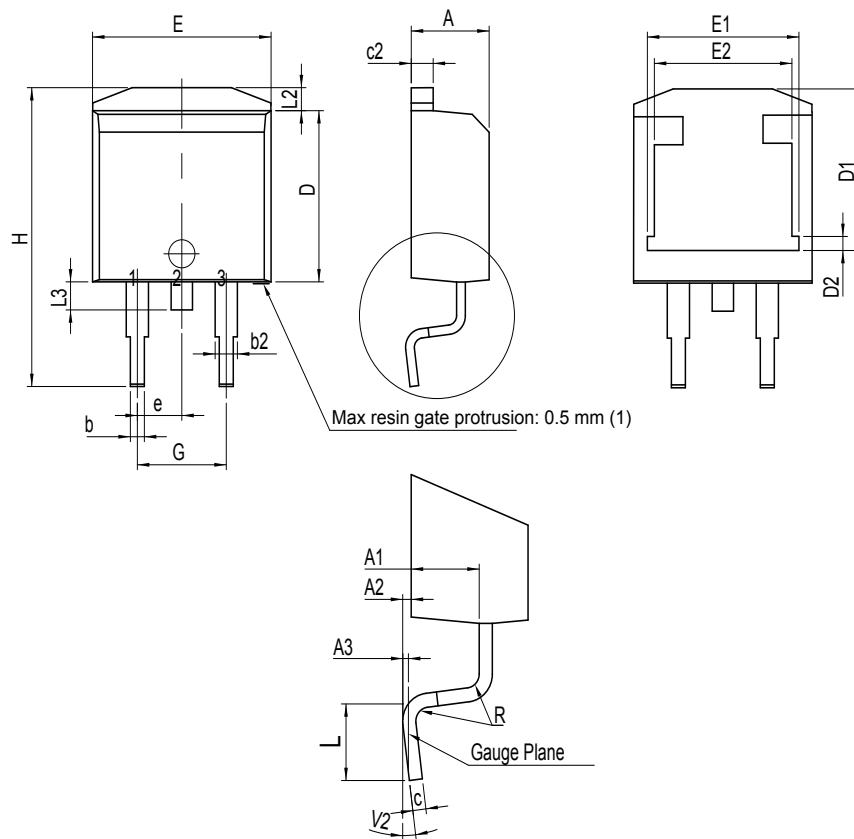
2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 D²PAK package information

- **ECOPACK2** compliant
- Lead-free package leads finishing
- Molding compound resin is halogen-free and meets UL standard level V0

Figure 15. D²PAK package outline



(1) Resin gate is accepted in each of position shown on the drawing, or their symmetrical.

Table 5. D²PAK package mechanical data

| Ref. | Dimensions | | | | | |
|-------------------|-------------|------|-------|-----------------------|--------|--------|
| | Millimeters | | | Inches ⁽¹⁾ | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 4.30 | | 4.60 | 0.1693 | | 0.1811 |
| A1 | 2.49 | | 2.69 | 0.0980 | | 0.1059 |
| A2 | 0.03 | | 0.23 | 0.0012 | | 0.0091 |
| A3 | | 0.25 | | | 0.0098 | |
| b | 0.70 | | 0.93 | 0.0276 | | 0.0366 |
| b2 | 1.25 | | 1.7 | 0.0492 | | 0.0669 |
| c | 0.45 | | 0.60 | 0.0177 | | 0.0236 |
| c2 | 1.21 | | 1.36 | 0.0476 | | 0.0535 |
| D | 8.95 | | 9.35 | 0.3524 | | 0.3681 |
| D1 | 7.50 | | 8.00 | 0.2953 | | 0.3150 |
| D2 | 1.30 | | 1.70 | 0.0512 | | 0.0669 |
| e | | 2.54 | | | 0.1 | |
| E | 10.00 | | 10.28 | 0.3937 | | 0.4047 |
| E1 | 8.30 | | 8.70 | 0.3268 | | 0.3425 |
| E2 | 6.85 | | 7.25 | 0.2697 | | 0.2854 |
| G | 4.88 | | 5.28 | 0.1921 | | 0.2079 |
| H | 15 | | 15.85 | 0.5906 | | 0.6240 |
| L | 1.78 | | 2.28 | 0.0701 | | 0.0898 |
| L2 | 1.19 | | 1.40 | 0.0468 | | 0.0551 |
| L3 | 1.40 | | 1.75 | 0.0551 | | 0.0689 |
| R | | 0.40 | | | 0.0157 | |
| V2 ⁽²⁾ | 0° | | 8° | 0° | | 8° |

1. Dimensions in inches are given for reference only

2. Degrees

Figure 16. D²PAK recommended footprint (dimensions are in mm)

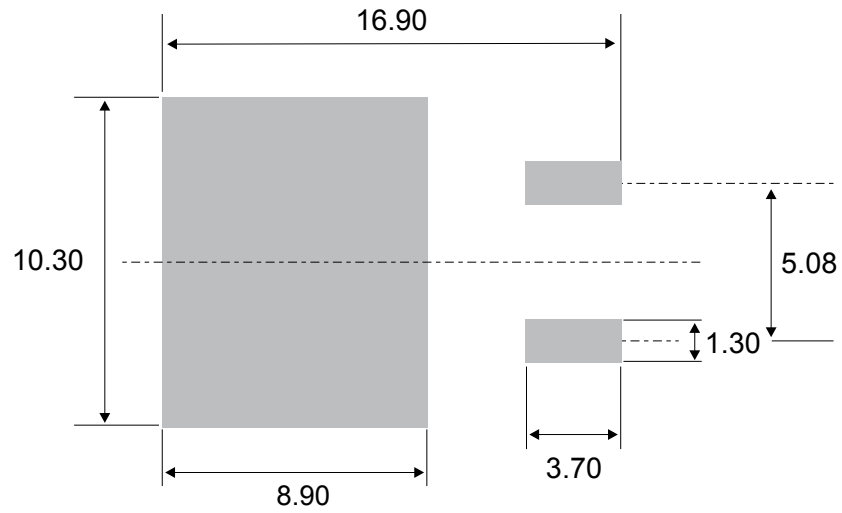
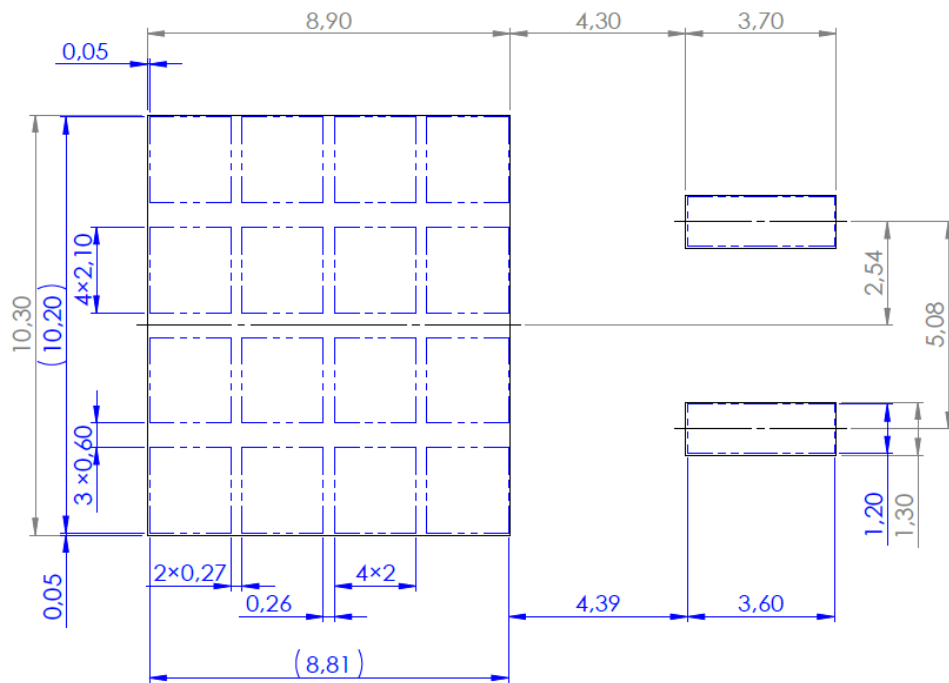


Figure 17. D²PAK stencil definitions (dimensions are in mm)



3 Ordering information

Figure 18. Ordering information scheme

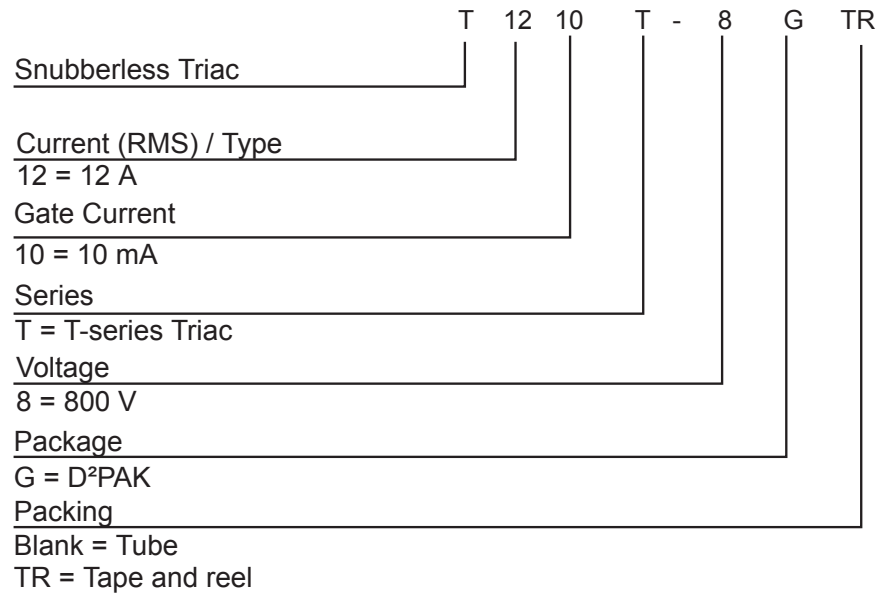


Table 6. Ordering information

| Order code | Marking | Package | Weight | Base qty. | Delivery mode |
|--------------|-----------|--------------------|--------|-----------|---------------|
| T1210T-8G-TR | T1210T-8G | D ² PAK | 1.6 g | 1000 | Tape and reel |
| T1210T-8G | | | | 50 | Tube |

Revision history

Table 7. Document revision history

| Date | Version | Changes |
|-------------|---------|---|
| 05-Aug-2019 | 1 | Initial release. |
| 01-Oct-2019 | 2 | Updated Table 1. Absolute maximum ratings (limiting values), $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified and Table 4. Thermal resistance. |
| 29-Oct-2020 | 3 | Updated Table 5. D ² PAK package mechanical data. Minor text changes. |

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