

Features

- Four differential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- Supports the following output frequencies: 156.25MHz, 125MHz, 62.5MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.23ps (typical)
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (12kHz – 20MHz): 0.28ps (typical)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free packages

Description

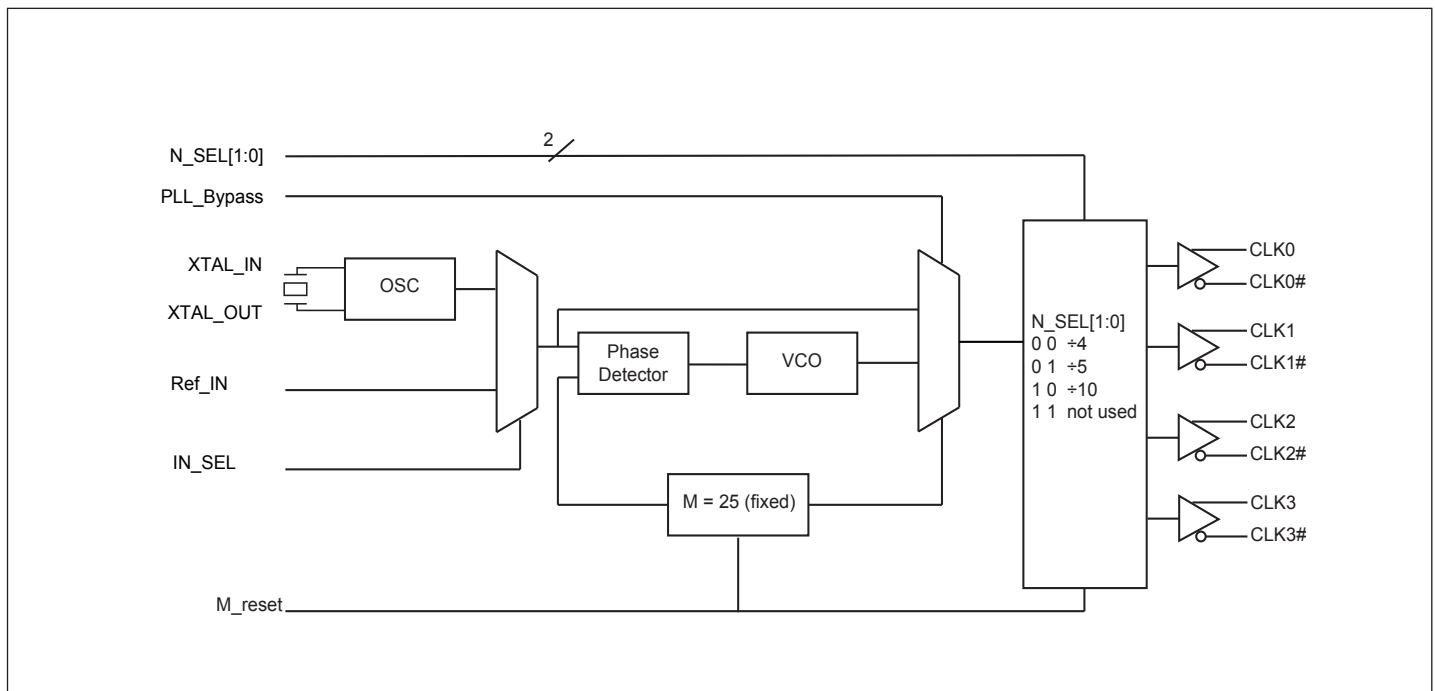
The PI6LC48P0401 is a 4-output LVPECL synthesizer optimized to generate Ethernet reference clock frequencies and is a member of Pericom's HiFlex family of high performance clock solutions. Using a 25MHz crystal, the following frequencies can be generated based on the settings of 2 frequency select pins (N_SEL[1:0]): 156.25MHz, 125MHz, 62.5MHz.

The PI6LC48P0401 uses Pericom's proprietary low phase noise VCO technology and can achieve less than 1ps typical rms phase jitter, so it is ideal for Ethernet interface in all kind of systems.

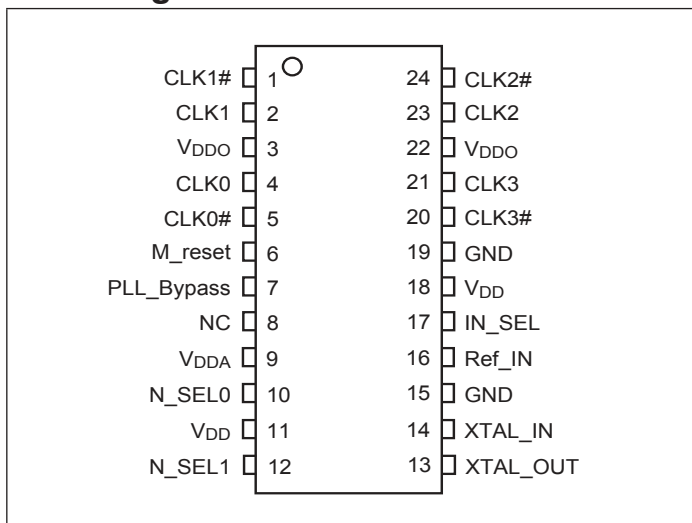
Applications

- Networking systems

Block Diagram



Pin Configuration



Pinout Table

| Pin No. | Pin Name | I/O Type | | Description |
|---------|-------------------|----------------|----------|--|
| 1, 2 | CLK1#, CLK1 | Output | | LVPECL Output Clock 1 |
| 3, 22 | V _{DDO} | Power | | Output supply pins |
| 4, 5 | CLK0, CLK0# | Output | | LVPECL Output Clock 0 |
| 6 | M_reset | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and outputs are enabled. |
| 7 | PLL_Bypass | Input | Pulldown | Selects either the PLL or the active input reference to be routed to the output dividers. When LOW, selects PLL (PLL enable). When HIGH, selects the reference clock (PLL bypass). |
| 8 | NC | | | Not connected |
| 9 | V _{DDA} | Power | | Analog power supply |
| 10, 12 | N_SEL0, N_SEL1 | Input | Pulldown | Frequency select pins |
| 11, 18 | V _{DD} | Power | | Core power supply |
| 13, 14 | XTAL_OUT, XTAL_IN | Output / Input | | Parallel resonant crystal interface. XTAL_OUT is the output, and XTAL_IN is the input. |
| 15, 19 | GND | Power | | Ground |
| 16 | Ref_IN | Input | Pulldown | CMOS reference clock input |
| 17 | IN_SEL | Input | Pulldown | Selects between the single-ended Ref_IN or crystal interface as the PLL reference source. When HIGH, selects Ref_IN. When LOW selects XTAL inputs. |
| 20, 21 | CLK3#, CLK3 | Output | | LVPECL Output Clock 3 |
| 23, 24 | CLK2, CLK2# | Output | | LVPECL Output Clock 2 |

Frequency Select Function Table

| Inputs | | | | | Output Frequency (MHz) (25MHz Reference) |
|--------|--------|--------------|--------------|----------------|---|
| N_SEL1 | N_SEL0 | M Div. Value | N Div. Value | M/N Div. Value | |
| 0 | 0 | 25 | 4 | 6.25 | 156.25 |
| 0 | 1 | 25 | 5 | 5 | 125 |
| 1 | 0 | 25 | 10 | 2.5 | 62.5 |
| 1 | 1 | 25 | Not Used | | Not Used |

Typical Crystal Requirement

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

Recommended Crystal Specification

Pericom recommends:

- a) FL2500047, SMD 3.2x2.5(4P), 25MHz, CL=18pF, +/-20ppm, <http://www.pericom.com/pdf/datasheets/se/FL.pdf>
- b) FY2500091, SMD 5x3.2(4P), 25MHz, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

Maximum Ratings (Over operating free-air temperature range)

| | |
|---|-----------------|
| Storage Temperature..... | -65°C to +155°C |
| Ambient Temperature with Power Applied..... | -40°C to +85°C |
| 3.3V Analog Supply Voltage..... | -0.5 to +3.6V |
| ESD Protection (HBM) | 2000V |

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Specifications
Power Supply DC Characterisitcs, ($T_A = -40$ to 85°C)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------|-----------------------|------------------------------|-------|-----|-------|-------|
| V _{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V _{DDA} | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V _{DDO} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I _{GND} | Power Supply Current | | | | 130 | mA |
| I _{DDA} | Analog Supply Current | Included in I _{GND} | | | 30 | mA |

Power Supply DC Characterisitcs, ($T_A = -40$ to 85°C)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------|-----------------------|------------------------------|-------|-----|-------|-------|
| V _{DD} | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V _{DDA} | Analog Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V _{DDO} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I _{GND} | Power Supply Current | | | | 125 | mA |
| I _{DDA} | Analog Supply Current | Included in I _{GND} | | | 30 | mA |

LVC MOS/LVTTL DC Characterisitcs, ($T_A = -40$ to 85°C)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------------|-------------------------|---|------|-----|-----------------------|-------|
| V _{IH} | Input High Voltage | V _{DD} = 3.3V ± 5% | 2 | | V _{DD} + 0.3 | V |
| | | V _{DD} = 2.5V ± 5% | 1.7 | | V _{DD} + 0.3 | V |
| V _{IL} | Input Low Voltage | V _{DD} = 3.3V ± 5% | -0.3 | | 0.8 | V |
| | | V _{DD} = 2.5V ± 5% | -0.3 | | 0.7 | V |
| I _{IH} | Input High Current | Ref_IN, M_reset, N_SEL[0:1], PLL_Bypass, IN_SEL, V _{DD} = V _{IN} = 3.465V | | | 150 | μA |
| I _{IL} | Input Low Current | Ref_IN, M_reset, N_SEL[0:1], PLL_Bypass, IN_SEL, V _{DD} = V _{IN} = 0V | -5 | | | μA |
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULL-DOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

LVPECL DC Characteristics, ($V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40$ to $85^\circ C$)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------------|------------------------------------|------------------------|-----|-----|-----|-------|
| V _{OH} | Output High Voltage ⁽¹⁾ | V _{DD} = 3.3V | 1.9 | | 2.4 | V |
| | | V _{DD} = 2.5V | 1.1 | | 1.6 | |
| V _{OL} | Output Low Voltage ⁽¹⁾ | V _{DD} = 3.3V | 1.2 | | 1.6 | V |
| | | V _{DD} = 2.5V | 0.4 | | 0.8 | |

Note: 1. LVPECL Termination: Source 150ohm to GND and 100ohm across CLK and CLK#.

AC Electrical Characteristics

LVPECL Termination: Source 150ohm to GND and using 0.01uF ac-coupled to 50ohm to GND

AC Characteristics, ($V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40$ to $85^\circ C$)

| Symbol | Parameter | Condition | Min. | Typ. | Max | Units |
|---------------------------------|---|-------------------------------|------|------|-----|-------|
| f _{OUT} | Output Frequency Range | N_SEL[1:0] = 00 | 140 | | 170 | MHz |
| | | N_SEL[1:0] = 01 | 112 | | 136 | MHz |
| | | N_SEL[1:0] = 10 | 56 | | 68 | MHz |
| t _{sk(o)} | Output Skew ^(1,2) | | | | 120 | ps |
| t _{jit(Ø)} | RMS Phase Jitter, (Random) ⁽³⁾ | 156.25MHz, (1.875MHz - 20MHz) | | 0.23 | | ps |
| | | 156.25MHz, (12kHz - 20MHz) | | 0.28 | | ps |
| | | 125MHz, (1.875MHz - 20MHz) | | 0.14 | | ps |
| | | 125MHz, (12kHz - 20MHz) | | 0.32 | | ps |
| | | 62.5MHz, (637kHz - 10MHz) | | 0.29 | | ps |
| | | 62.5MHz, (12kHz - 10MHz) | | 0.47 | | ps |
| t _R / t _F | Output Rise/Fall Time | 20% to 80% | | | 400 | ps |
| odc | Output Duty Cycle | | 48 | | 52 | % |

Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Note1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

Note2: This parameter is defined in accordance with JEDEC Standard 65.

Note3: Please refer to the Phase Noise Plots.

AC Characterisitcs, ($V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40$ to $85^\circ C$)

| Symbol | Parameter | Condition | Min. | Typ. | Max | Units |
|---------------------------------|---|-------------------------------|------|------|-----|-------|
| f _{OUT} | Output Frequency Range | N_SEL[1:0] = 00 | 140 | | 170 | MHz |
| | | N_SEL[1:0] = 01 | 112 | | 136 | MHz |
| | | N_SEL[1:0] = 10 | 56 | | 68 | MHz |
| t _{sk(o)} | Output Skew ^(1, 2) | | | | 120 | ps |
| t _{jit(Ø)} | RMS Phase Jitter, (Random) ⁽³⁾ | 156.25MHz, (1.875MHz - 20MHz) | | 0.21 | | ps |
| | | 156.25MHz, (12kHz - 20MHz) | | 0.28 | | ps |
| | | 125MHz, (1.875MHz - 20MHz) | | 0.14 | | ps |
| | | 125MHz, (12kHz - 20MHz) | | 0.32 | | ps |
| | | 62.5MHz, (637kHz - 10MHz) | | 0.28 | | ps |
| | | 62.5MHz, (12kHz - 10MHz) | | 0.47 | | ps |
| t _R / t _F | Output Rise/Fall Time | 20% to 80% | | | 400 | ps |
| odc | Output Duty Cycle | | 48 | | 52 | % |

Note: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

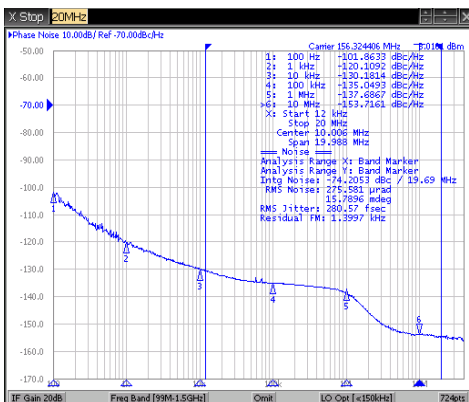
Note1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

Note2: This parameter is defined in accordance with JEDEC Standard 65.

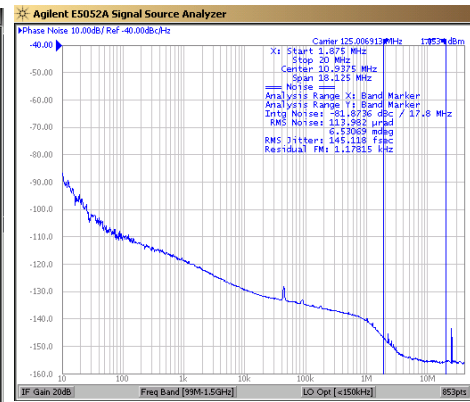
Note3: Please refer to the Phase Noise Plots.

Phase Noise Plot

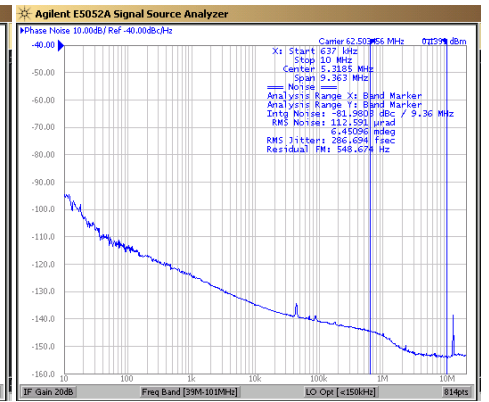
156.25MHz



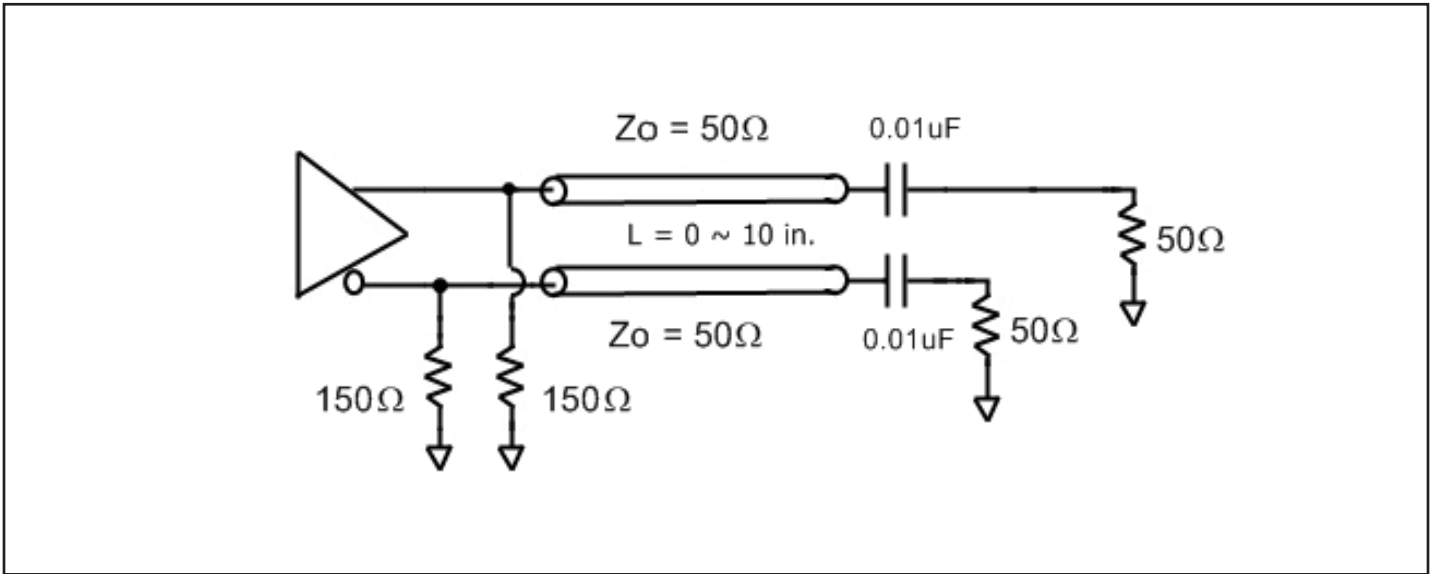
125MHz



62.5MHz

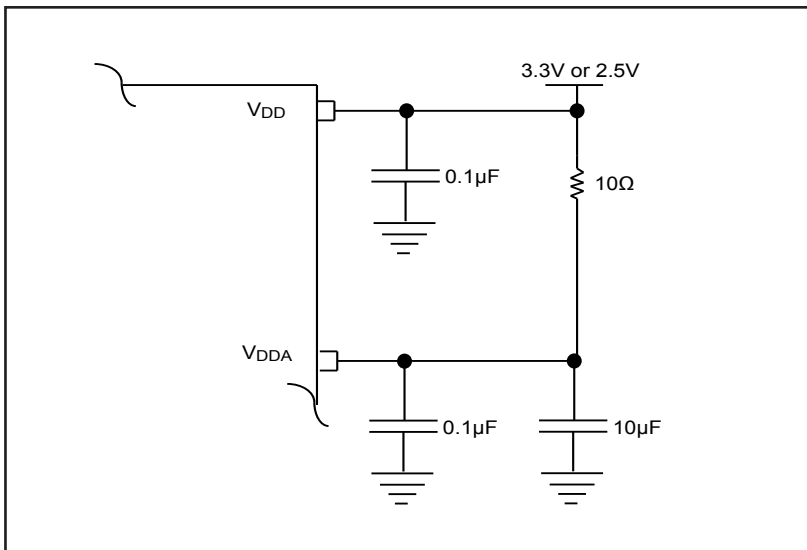


LVPECL Test Circuit



Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48P0401 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.1μF bypass capacitors should be used for each pin. Figure below illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10μF bypass capacitor be connected to the V_{DDA} pin.



Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. A 1kΩ resistor can be tied from XTAL_IN to ground for additional protection.

Ref_IN Input:

For applications not requiring the use of the clock, it can be left floating. A 1kΩ resistor tied from the Ref_IN to ground can provide additional protection.

LVC MOS Control Pins:

All control pins have internal pulldowns; A 1kΩ resistor tied from each control pin to ground can provide additional protection.

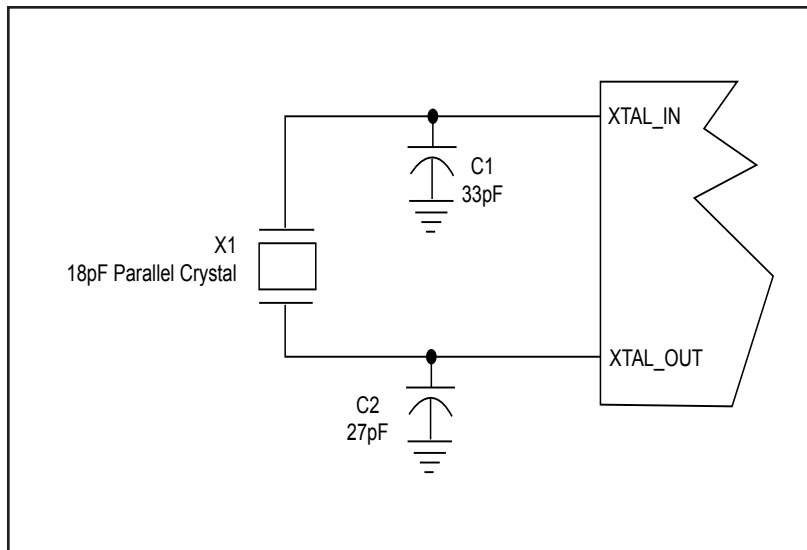
Outputs:

LVPECL Outputs:

All unused LVPECL outputs can be left floating.

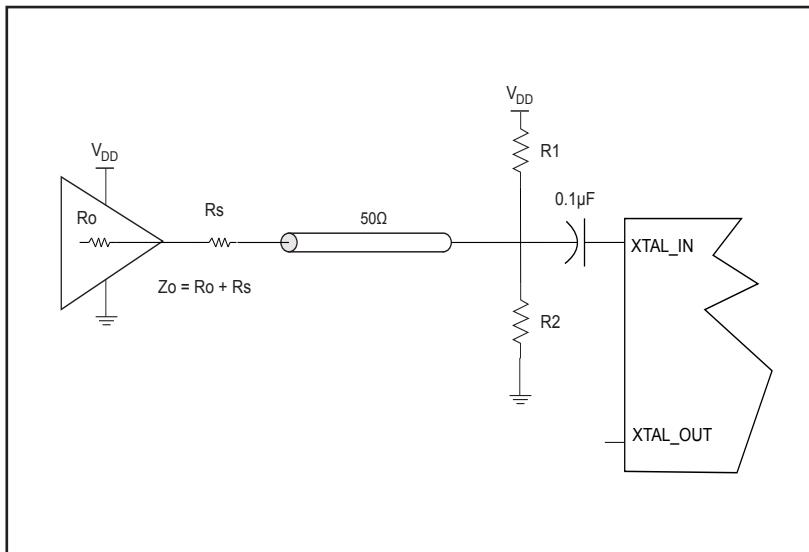
Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

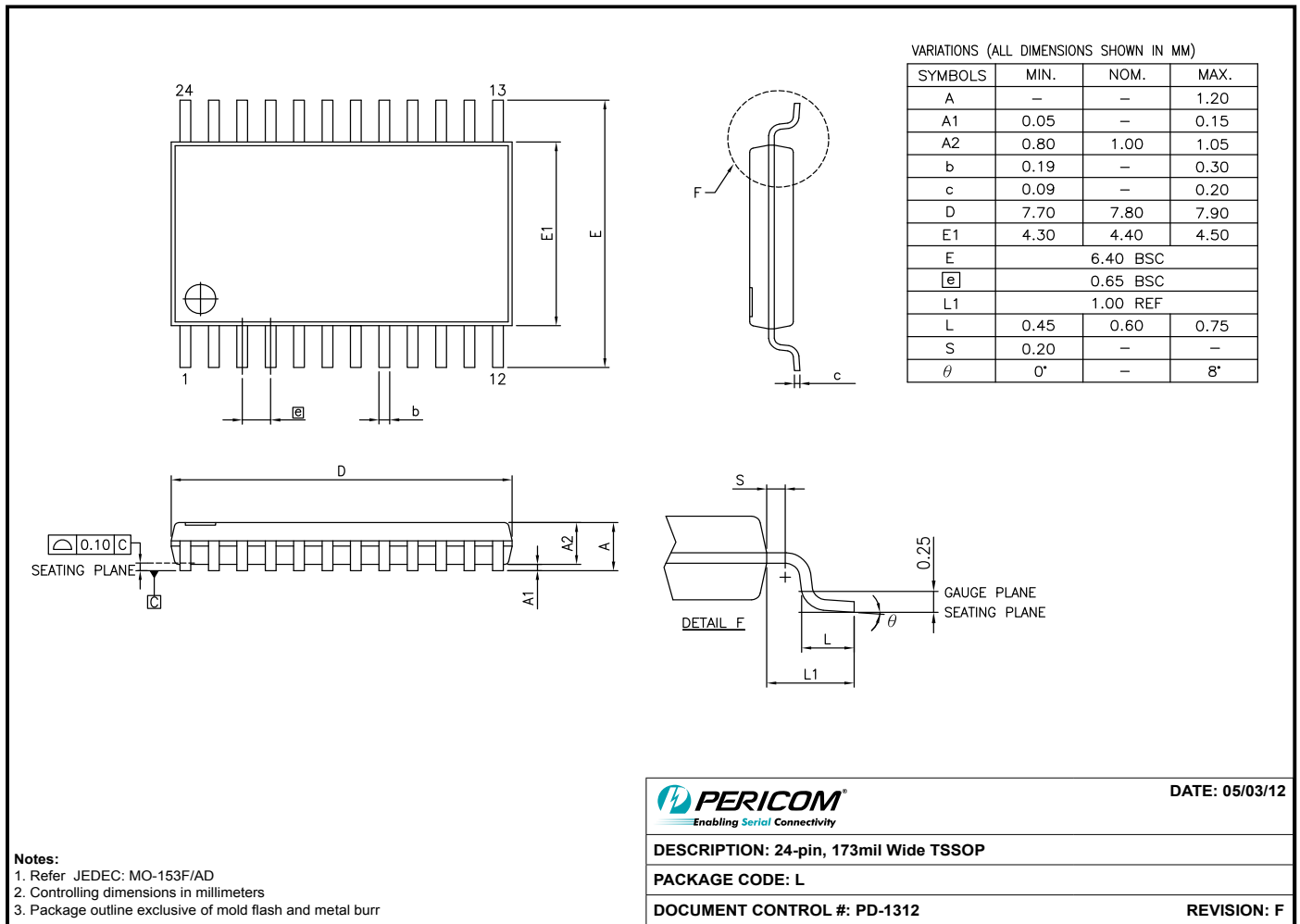


LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω . This can also be accomplished by removing R_1 and making R_2 50Ω . By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.



Packaging Mechanical: 24-Contact TSSOP (L)



12-0374

Ordering Information

| Ordering Code | Packaging Type | Package Description | Operating Temperature |
|-----------------|----------------|-------------------------------|-----------------------|
| PI6LC48P0401LE | L | Pb-free & Green, 24-pin TSSOP | Commercial |
| PI6LC48P0401LIE | L | Pb-free & Green, 24-pin TSSOP | Industrial |

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging