MAX98371

Digital Input Class D Speaker Amplifier with Dynamic Headroom Tracking

General Description

The MAX98371 is a high-efficiency, mono Class D audio amplifier featuring Dynamic Headroom Tracking (DHT). DHT automatically optimizes the headroom available to the Class D amplifier as the power supply voltage varies, due to sudden transients and declining battery life to maintain a consistent listening experience. A wide 5.5V to 18V supply range allows the device to reach 19W into an 8Ω load.

The MAX98371's flexible digital audio interface (DAI) supports I²S, Left-Justified, and TDM formats. The digital audio interface accepts 32kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz sample rates with 16-/24-/32-bit data supported for all data formats. In TDM mode, the device can support up to 16 channels of audio data. A unique clocking structure eliminates the need for an external MCLK signal that is typically needed for PCM communication. This reduces pin count and simplifys board layout.

Active Emissions Limiting (AEL) with edge rate control minimizes EMI, and eliminates the need for output filtering found in traditional Class D devices.

An 8-bit PVDD supply voltage ADC enables the Dynamic Headroom Tracking circuit. DHT optimizes audio program peak behavior as the supply voltage varies and provides flexible user-defined parameters.

Thermal foldback protection ensures robust behavior when the thermal limits of the device are exercised. The circuit can be enabled to automatically reduce the output power above a user specified temperature. This allows for uninterrupted music playback even at high ambient temperatures. Traditional thermal protection is also available in addition to robust overcurrent protection.

All MAX98371 control is performed using a standard 2-wire, I²C interface. One of sixteen slave addresses can be selected through two, four-level address pins. The IC is available in a 0.4mm pitch, 30-bump WLP package. It is specified over the extended, -40°C to +85°C temperature range.

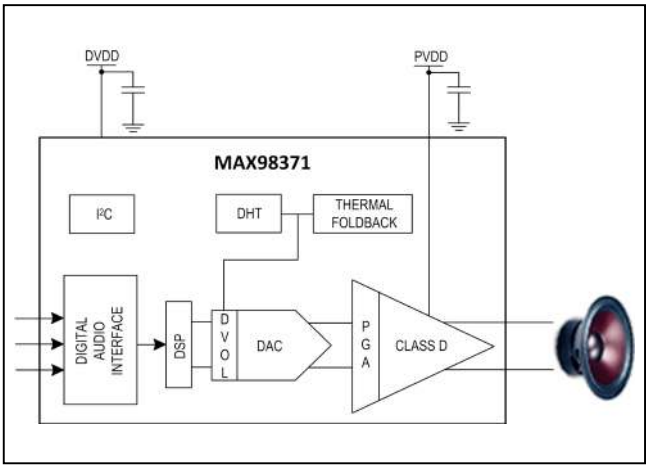
Applications

- Tablets
- Notebook Computers
- Soundbars

Benefits and Features

- Wide Supply Range (5.5V to 18V)
- Dynamic Headroom Tracking Maintains a Consistent Listening Experience
- Integrated Thermal Foldback Allows Robust Operation in a WLP Package
- Remote Output Sensing Allows Up to 20dB THD+N Improvement When Ferrites Are Used
- Class D Edge Rate Control Enables Filterless Operation
- 110dB A-Weighted Dynamic Range
- Output Power at 1% THD+N:
  - 15.7W into 8Ω, V_{PVDD} = 17V
  - 13.2W into 4Ω, V_{PVDD} = 12V
- Output Power at 10% THD+N
  - 19W into 8Ω, V_{PVDD} = 17V
  - 15.8W into 4Ω, V_{PVDD} = 12V
- Speaker Amplifier Efficiency
  - 91% at 10W into 8Ω, V_{PVDD} = 12V
  - 81% at 15W into 4Ω, V_{PVDD} = 12V
- Extensive Click-and-Pop Suppression
- Space Saving, 30-Bump WLP Package (2.1mm x 2.6mm x 0.6mm, 0.4mm Pitch)

Simplified Block Diagram



Ordering Information ***appears at end of data sheet.***

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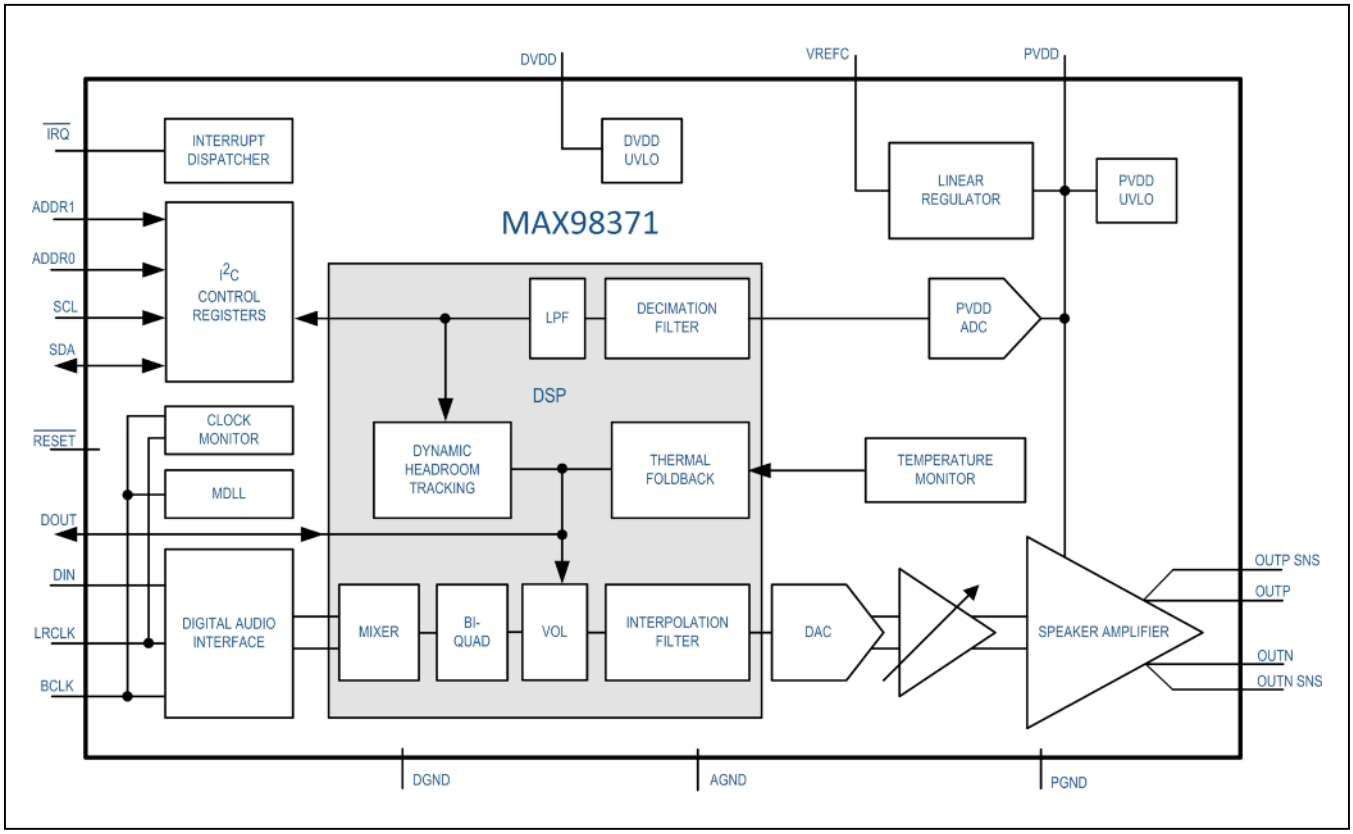


Absolute Maximum Ratings

PVDD to PGND ..... -0.3V to 20V
OUT_ to PGND ..... -0.3V to (V_{PVDD} + 0.3V)
V_{REFC} to AGND ..... -0.3V to 2.2V
DVDD to DGND ..... -0.3V to 2.2V
SDA, SCL, ADDR_, $\overline{IRQ}$ to DGND ..... -0.3V to 2.2V
BCLK, LRCLK, DIN, $\overline{RESET}$ to DGND ..... -0.3V to (V_{DVDD} + 0.3V)
AGND, DGND to PGND ..... -0.1V to 0.1V

Short-Circuit Duration
Between OUTP, OUTN and PGND or PVDD ..... Continuous
Between OUTP and OUTN ..... Continuous
Continuous Power Dissipation (T_A = +70°C) for Multilayer Board (derate 27mW/°C above +70°C) 1.9W
Junction Temperature ..... 150°C
Operating Temperature Range ..... -40°C to 85°C
Storage Temperature Range ..... -65°C to 150°C
Soldering Temperature (reflow) ..... 260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 37°C/W
Junction-to-Board Thermal Resistance (θ_{JB}) ..... 33.4°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{PVDD} = 12V, V_{DVDD} = $\overline{RESET}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Power Supply Voltage Range	V_{PVDD}			5.5		18	V
	V_{DVDD}			1.14		1.98	
VREFC Regulator Output	V_{REFC}				2.0		V
PVDD Under Voltage Lockout	PVDD UVLO			3.65	4.3	4.75	V
DVDD Under Voltage Lockout	DVDD UVLO				0.75		V
Quiescent Current	I_{Q_PVDD}	SPK_SWCLK = 0	472kHz		8.4	12	mA
		SPK_SWCLK = 1	330kHz		7		
Quiescent Current	I_{Q_DVDD}				1.5	2.5	mA
Software Shutdown Supply Current	I_{SHDN_SW}	All DAI pins pulled low, T_A = 25°C	I_{PVDD}			10	µA
			I_{DVDD}			10	
Hardware Shutdown Supply Current	I_{SHDN_HW}	$\overline{RESET}$ =0V, T_A = 25°C	I_{PVDD}			5	µA
			I_{DVDD}			1	
Turn-On Time	t_{ON}	From SW_EN bit set to full operation	Volume ramping disabled		10		ms
			Volume ramping enabled		30		

Electrical Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = $\overline{RESET}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Turn-Off Time	t_{OFF}	From SW_EN bit cleared to Shutdown	Volume ramping disabled		10		ms
			Volume ramping enabled		30		
DIGITAL FILTER CHARACTERISICS (LRCLK < 50kHz) (Note 5)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff			0.43 x f_S		Hz
		-3dB cutoff			0.47 x f_S		
		-6.02dB cutoff			0.5 x f_S		
Passband Ripple		f < f_{PLP}		-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}					0.58 x f_S	Hz
Stopband Attenuation		f > f_{SLP}		60			dB
DIGITAL FILTER CHARACTERISICS (LRCLK > 50kHz) (Note 5)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff			0.24 x f_S		Hz
		-3dB cutoff			0.31 x f_S		
Passband Ripple		f < f_{PLP}		-0.1		0.1	dB
Stopband Cutoff	f_{SLP}					0.417 x f_S	Hz
Stopband Attenuation		f > f_{SLP}		60			dB
DIGITAL HIGHPASS FILTER CHARACTERISTICS							
DC Attenuation (Note 5)				80			dB
DC Blocking Cutoff Frequency (Note 5)		Across all sample rates	DACHPF = 0x1			2	Hz
High Pass Cutoff Frequency		Across all sample rates	DACHPF = 0x2		50		Hz
			DACHPF = 0x3		100		
			DACHPF = 0x4		200		
			DACHPF = 0x5		400		
			DACHPF = 0x6		800		
SPEAKER AMPLIFIER ELECTRICAL CHARACTERISTICS							
DIGITAL VOLUME CONTROL							
Digital Volume (max)		DVOL[6:0] = 0x00			0		dB
Digital Volume (min)		DVOL[6:0] = 0x7E			-63		dB
Volume Control Step Size					0.5		dB
Output Offset Voltage	VOS	T_A = 25°C			±1	±5	mV
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second, digital audio inputs have zero-code input	Into shutdown		-66		dBV
			Out of shutdown		-60		

Electrical Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = $\overline{RESET}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Dynamic Range	DR	V_{PVDD} = 17V, Z_L = 8Ω + 33µH, measured using the EIAJ method, -60dBFS 1kHz output signal, referenced to 1% output power	A-weighted		110		dB
Integrated Output Noise	e_N	Z_L = 8Ω + 33µH	A-weighted		35		μV_{RMS}
			Unweighted		72		
Output Power	P_{OUT}	THD+N ≤ 1%, f = 1kHz	Z_L = 8Ω + 33µH		8.2		W
			Z_L = 8Ω + 33µH, V_{PVDD} = 17V		15.7		
			Z_L = 4Ω + 33µH		13.2		
		THD+N ≤ 10%, f = 1kHz	Z_L = 8Ω + 33µH		10.2		
			Z_L = 8Ω + 33µH, V_{PVDD} = 17V		19		
			Z_L = 4Ω + 33µH		15.8		
Efficiency	η_{SPK}	f = 1kHz	P_{OUT} = 10W, Z_L = 8Ω + 33µH		91		%
			P_{OUT} = 15W, Z_L = 4Ω + 33µH		81		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz	P_{OUT} = 4W, Z_L = 8Ω + 33µH		0.02		%
			P_{OUT} = 8W, Z_L = 4Ω + 33µH		0.03		
		f = Up to 6kHz	P_{OUT} = 4W, Z_L = 8Ω + 33µH		0.1		
			P_{OUT} = 8W, Z_L = 4Ω + 33µH		0.2		
Maximum Frequency Response Deviation		Maximum deviation above and below 1kHz reference			0.2		dB
Gain Error	A_{VERROR}	f =1kHz, V_O = 2.828V_{RMS}		-0.5		+0.5	dB
Maximum Channel-to-Channel Phase Error (Note 3)		Output phase shift between multiple devices from 20Hz to 20kHz, across all sample rates and DAI operating modes			1		deg

Electrical Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = $\overline{RESET}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
PVDD Power Supply Rejection Ratio	PSRR		V_{PVDD} = 5.5V to 18V		85		dB
			f =20Hz to 10kHz, V_{RIPPLE} = 100mV_{P-P}		75		
			f =10kHz to 20kHz, V_{RIPPLE} = 100mV_{P-P}		60		
DVDD Power Supply Rejection Ratio	PSRR		f = 1kHz, V_{RIPPLE} = 50mV_{P-P}		100		
Output Switching Frequency	f_S	Constant across all sample rates	SPK_SWCLK = 0		472		kHz
			SPK_SWCLK = 1		330		kHz
Output Stage On-Resistance	R_{ON}	PMOS + NMOS			0.425		Ω
Current Limit	I_{LIM}	Z_L = 8Ω + 33µH or Z_L = 4Ω + 33µH		4.5	6.0		A
THERMAL FOLDBACK							
Attack Time					10		µs
Attenuation Slope		THRM_SLOPE[1:0] = 0x0			0.5		dB/°C
		THRM_SLOPE[1:0] = 0x1			1		
		THRM_SLOPE[1:0] = 0x2			2		
Max Attenuation					12		dB
Release Time		THRM_REL[1:0] = 0x0			3		ms/dB
		THRM_REL[1:0] = 0x3			300		
THERMAL SHUTDOWN							
Trigger Point		(Note 3)		140	150	160	°C
Hysteresis					20		°C
PVDD ADC ELECTRICAL CHARACTERISTICS							
Resolution					8		Bits
Absolute Error					1.2		LSB
ADC Voltage Range				5.35		18.15	V
ADC Lowpass Filter Cutoff Frequency		-3dB limit			0.0875 x fS		Hz

Electrical Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = $\overline{RESET}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
ADC Lowpass Filter Stopband Frequency		-40dB limit			0.167 x f_S		Hz
ADC Programmable Lowpass Filter		PVDD_ADC_BW[1:0] = 0x1			2		Hz
		PVDD_ADC_BW[1:0] = 0x2			20		
		PVDD_ADC_BW[1:0] = 0x3			200		
DIGITAL I/O CHARACTERISTICS							
DIN, BCLK, LRCLK, ADDR_, $\overline{RESET}$							
Input Voltage High	V_{IH}			0.7 x V_{DVDD}			V
Input Voltage Low	V_{IL}					0.3 x V_{DVDD}	V
Input Leakage Current	I_{IH}, I_{IL}			-1		+1	µA
Input Capacitance	C_{IN}				3		pF
INPUT (SDA, SCL)							
Input Voltage High	V_{IH}			0.7 x V_{DVDD}			V
Input Voltage Low	V_{IL}					0.3 x V_{DVDD}	V
Input Hysteresis	V_{HYS}				200		mV
Input Capacitance	C_{IN}				3		pF
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C, input high		-1		+1	µA
OUTPUT (SDA, $\overline{IRQ}$)							
Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
Output Current	I_{OL}				13		mA
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS							
GLOBAL							
LRCLK Frequency Range	f_{LRCLK}	All DAI operating modes		32		96	kHz
Word Length		All DAI operating modes			16		bits
					24		
					32		
BCLK Duty Cycle				45		55	%
Maximum BCLK/LRCLK Input Jitter		Maximum jitter with minimal performance degradation	RMS jitter below 40kHz		0.5		ns
			RMS jitter above 40kHz		0.9		

Electrical Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = $\overline{RESET}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
PCM MODE (I^2S, LEFT-JUSTIFIED)						
LRCLK Duty Cycle			45		55	%
LRCLK to BCLK Active Edge Setup Time	$t_{SYNCSET}$		10			ns
LRCLK to BCLK Active Edge Hold Time	$t_{SYNCHOLD}$		10			ns
DIN to BCLK Active Edge Setup Time	t_{SETUP}		10			ns
DIN to BCLK Active Edge Hold Time	t_{HOLD}		10			ns
BCLK Period (Note 3)	t_{BCLK}		160			ns
BCLK Frequency (Note 3)	f_{BCLK}				6.25	MHz
				f_S x 32		
				f_S x 48		
				f_S x 64		
TDM MODE						
LRCLK Pulse Width	PW_{LRCLK}	Measured in number of BCLK cycles			511	cycles
DIN Frame Delay after LRCLK Edge		Measured in number of BCLK cycles	0		2	cycles
BCLK Period (Note 3)	t_{BCLK}		20			ns
BCLK Frequency (Note 3)	f_{BCLK}	All TDM operating modes			50	MHz

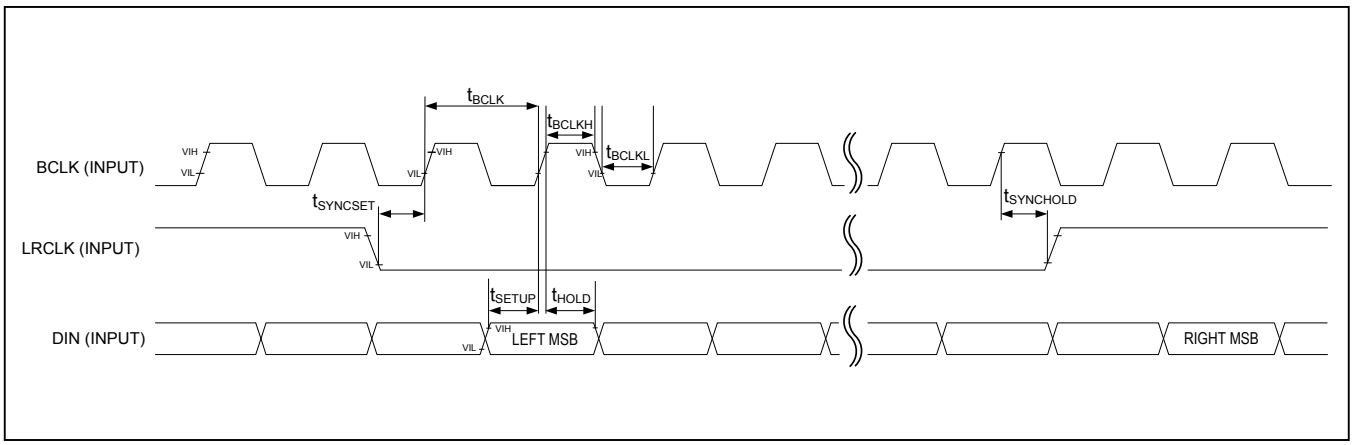


Figure 1. I²S Audio Interface Timing Diagram

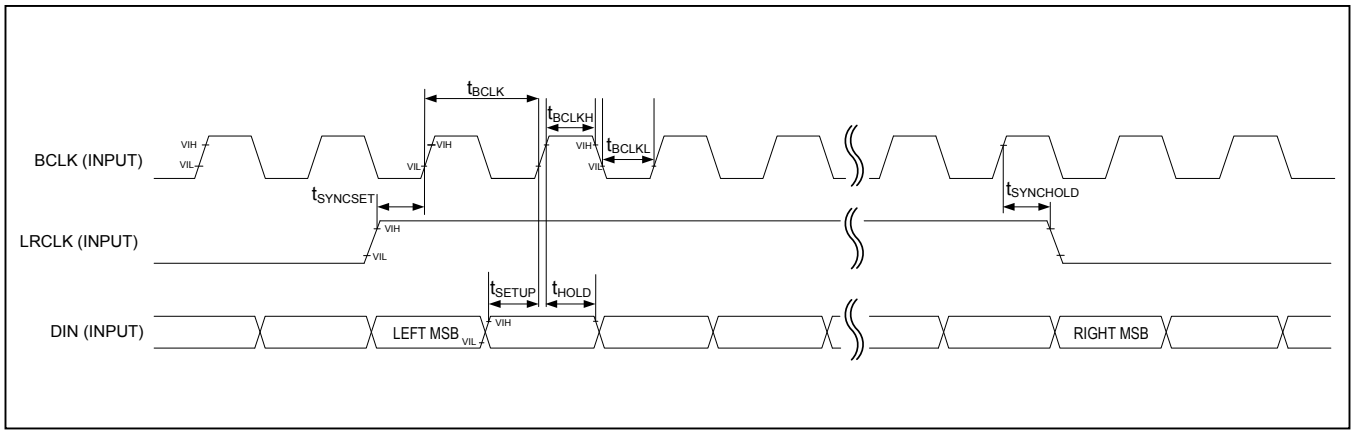


Figure 2. Left-Justified Audio Interface Timing Diagram

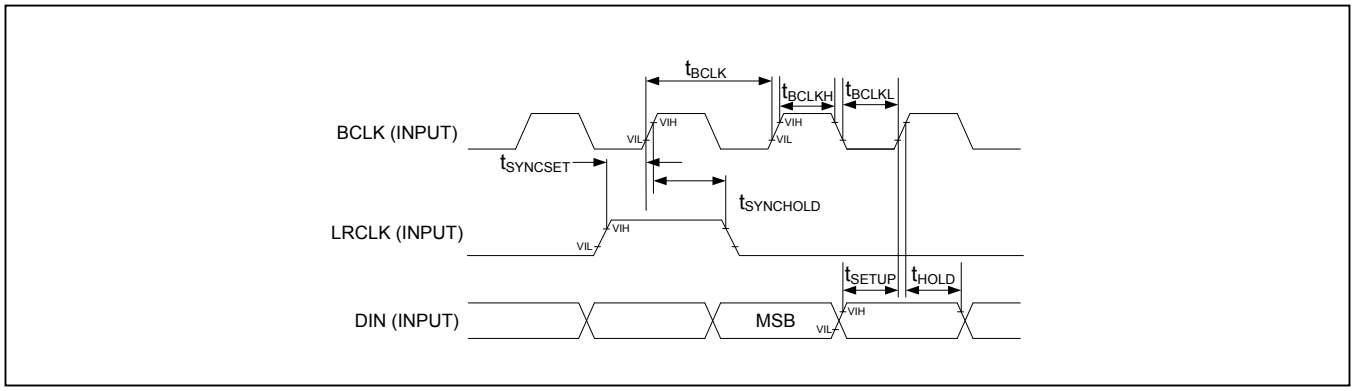


Figure 3.TDM Audio Interface Timing Diagrams

I²C Timing Characteristics

(V_{PVDD} = 12V, V_{DVDD} = $\overline{RESET}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, CV_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING CHARACTERISTICS						
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time (Note 4)	t_R		20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time (Note 4)	t_F		20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F		20		250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

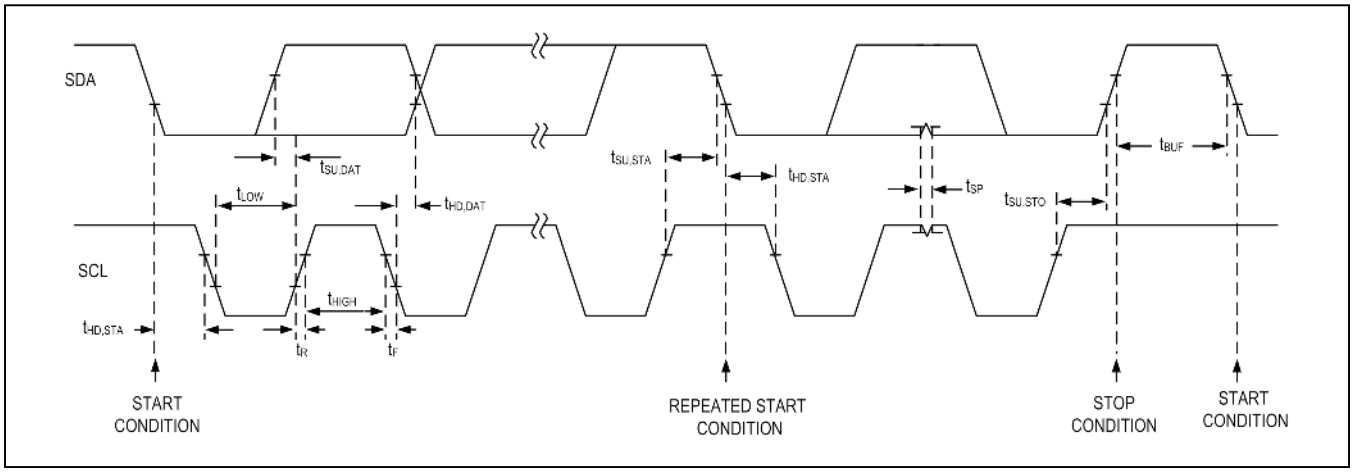


Figure 4. I²C Interface Timing Diagram

Power Consumption

(V_{PVDD} = 12V, V_{DVDD} = $\overline{RESET}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, CV_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

CONDITION	I_{PVDD} (mA)	P_{PVDD} (mW)	I_{DVDD} (mA)	P_{DVDD} (mW)	P_{TOTAL} (mW)
f_{SPK}=330kHz					
PCM to SPK	7.0	84.0	1.3	2.3	86.3
PCM to SPK, DHT	7.3	88.0	1.8	3.3	91.3
PCM to SPK, LMTR	7.0	84.0	1.8	3.2	87.2
f_{SPK}=472kHz					
PCM to SPK,	8.4	100.8	1.3	2.3	103.1
PCM to SPK, DHT	8.8	105.6	1.8	3.3	108.9
PCM to SPK, LMTR	8.5	101.5	1.8	3.2	104.7
f_{SPK}=472kHz AND PVDD = 17V					
PCM to SPK	9.3	157.7	1.3	2.3	160.0
PCM to SPK, DHT	6.6	163.0	1.8	3.3	166.6
PCM to SPK, LMTR	6.0	157.1	1.8	3.2	160.3

Note 2: 100% production tested at T_A = +25C. Specifications over temperature limits are guaranteed by design. Typical values are based on 1 sigma characterization data, unless otherwise noted.

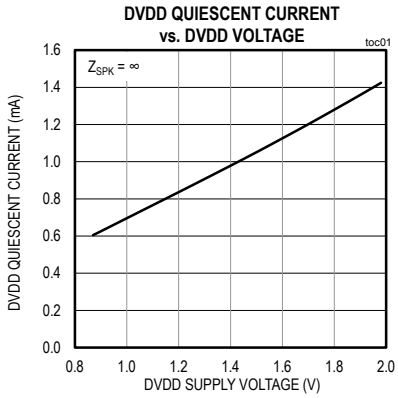
Note 3: Minimums and/or maximum limits shown are design targets and not 100% production tested. Characterization data is provided to validate device performance.

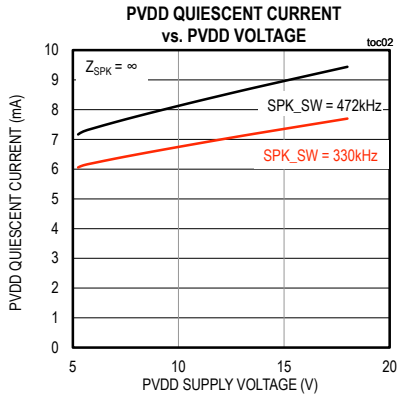
Note 4: C_B in pF.

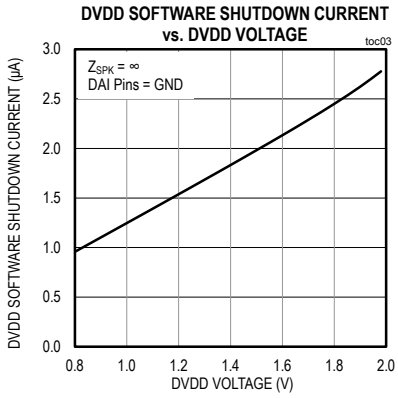
Note 5: Digital filter performance is invariant over temperature and production tested at T_A = +25C.

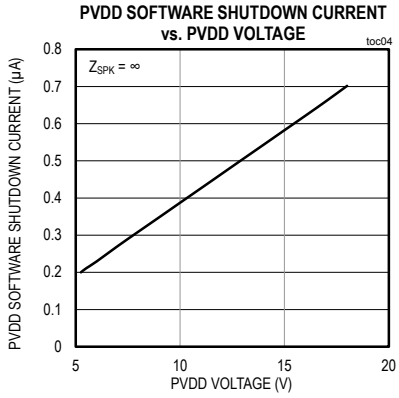
Typical Operating Characteristics

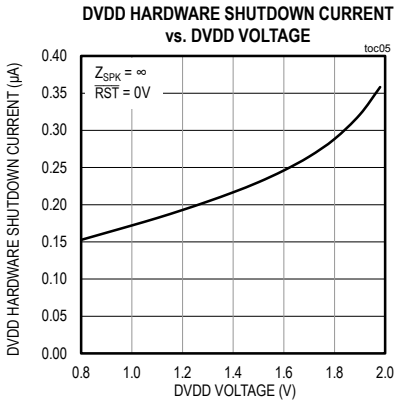
(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

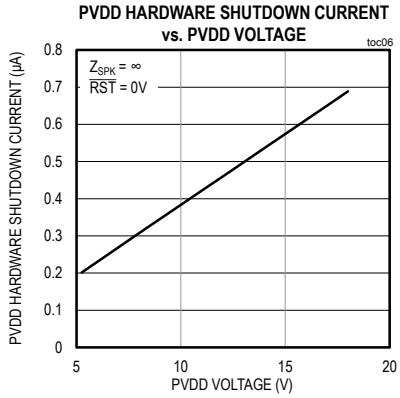








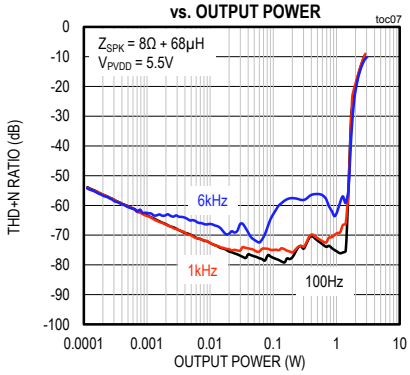




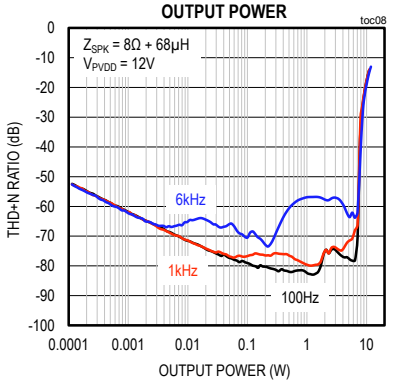
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

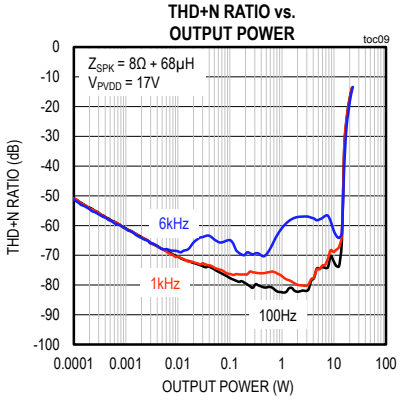
THD+N RATIO vs. OUTPUT POWER



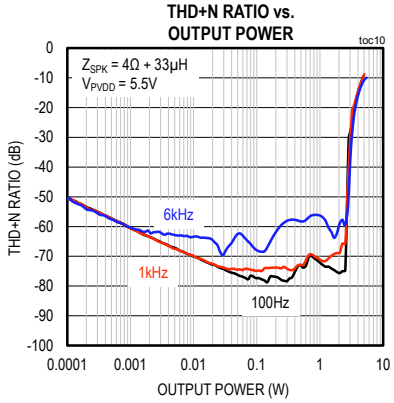
THD+N RATIO vs. OUTPUT POWER



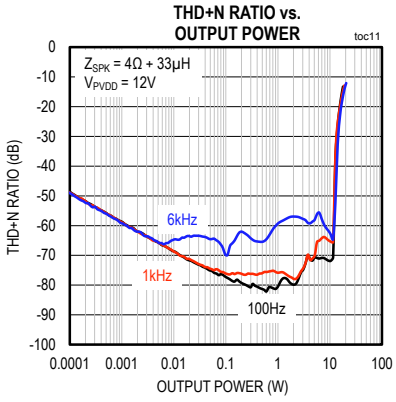
THD+N RATIO vs. OUTPUT POWER



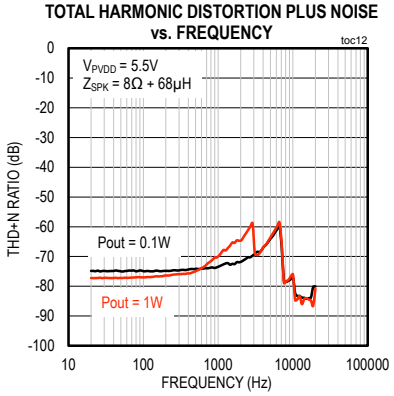
THD+N RATIO vs. OUTPUT POWER



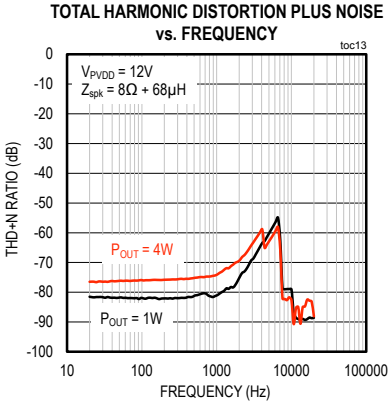
THD+N RATIO vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



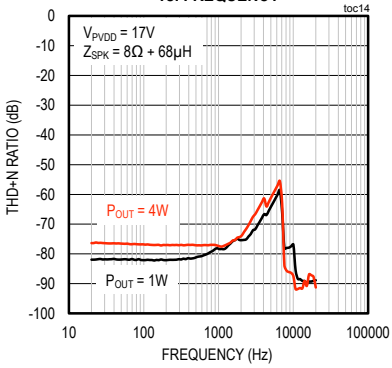
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



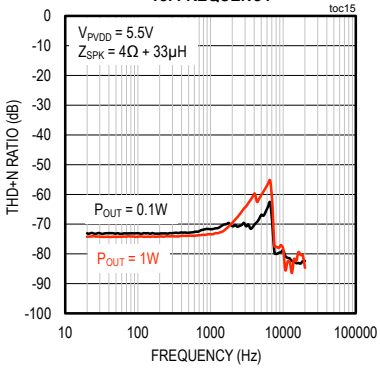
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

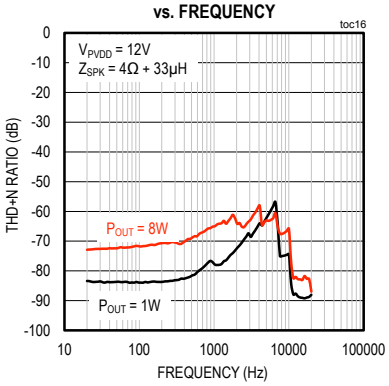
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



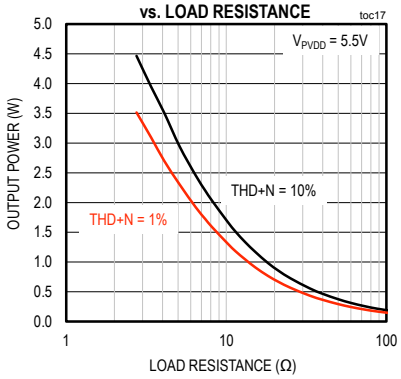
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



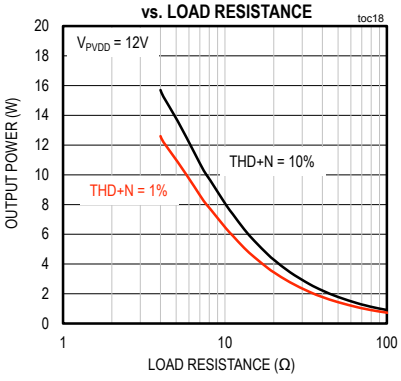
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



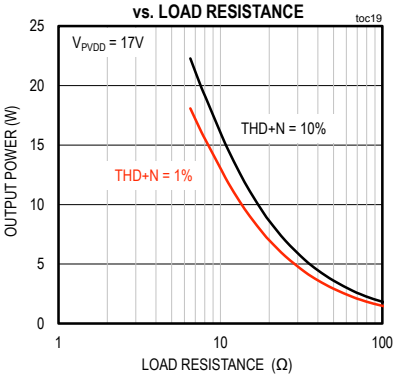
OUTPUT POWER vs. LOAD RESISTANCE



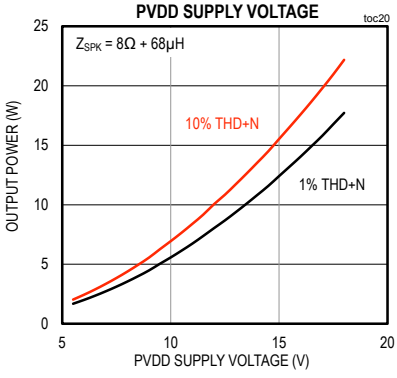
OUTPUT POWER vs. LOAD RESISTANCE



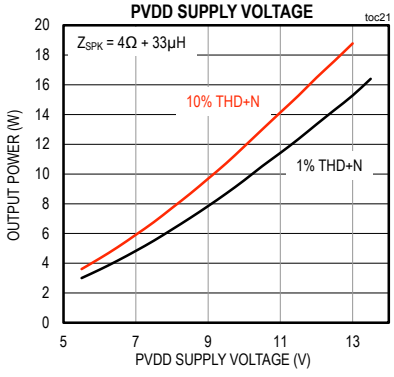
OUTPUT POWER vs. LOAD RESISTANCE



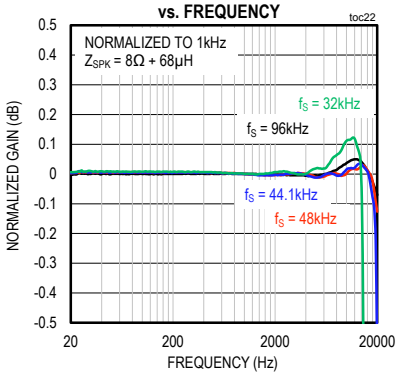
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



OUTPUT POWER vs. PVDD SUPPLY VOLTAGE

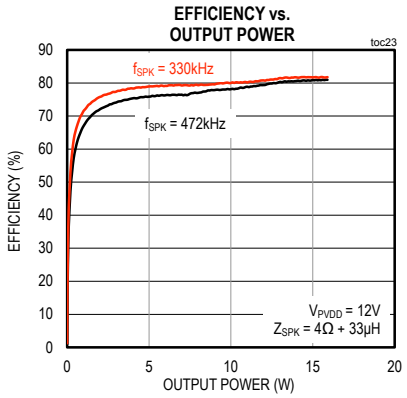


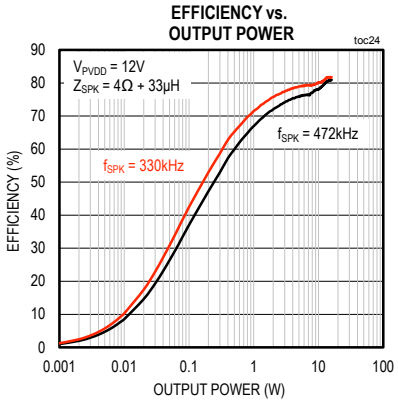
NORMALIZED GAIN vs. FREQUENCY

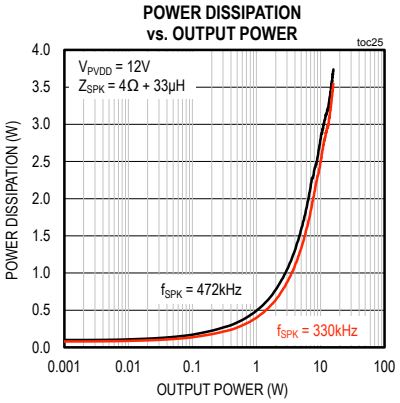


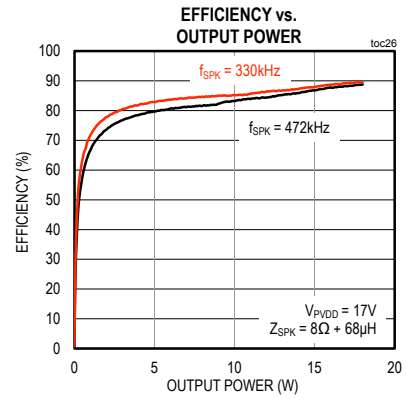
Typical Operating Characteristics (continued)

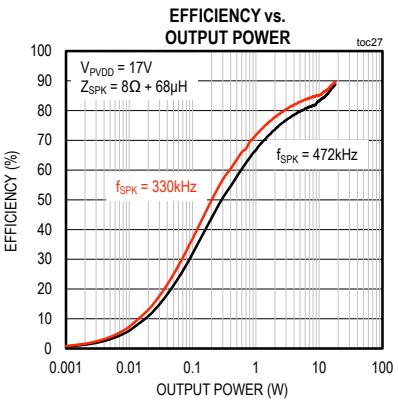
(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

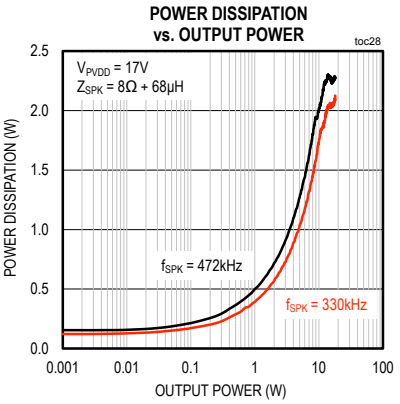


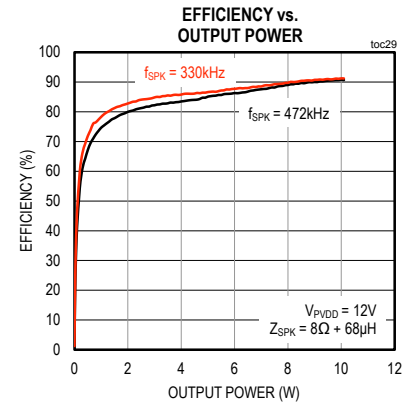


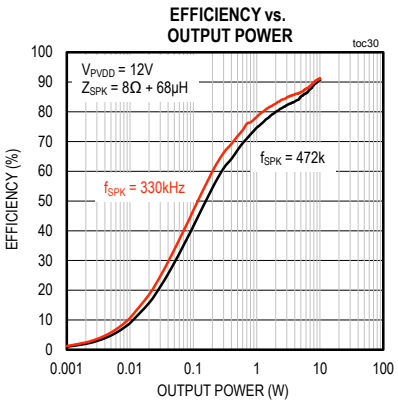


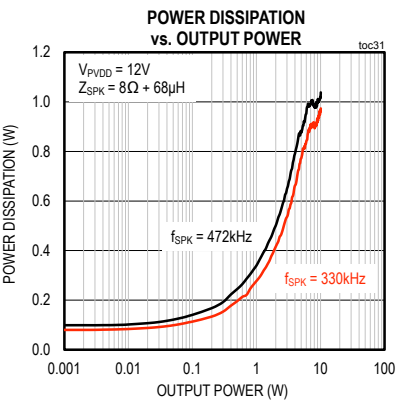








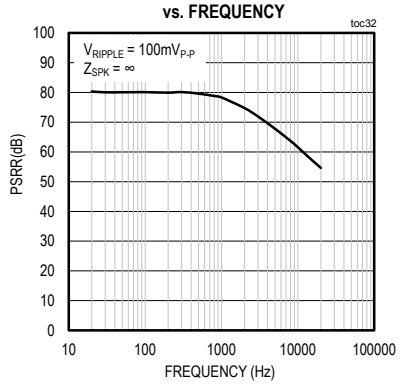




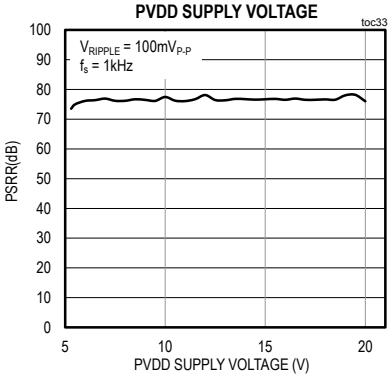
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

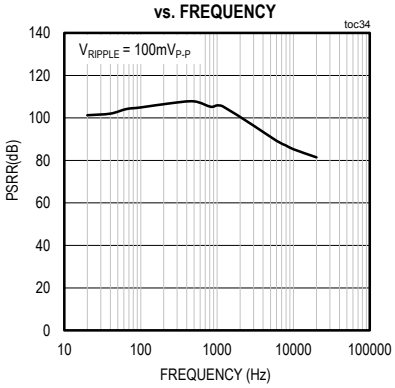
PVDD POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



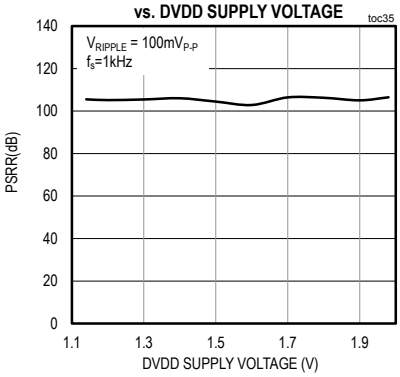
POWER-SUPPLY REJECTION RATIO vs. PVDD SUPPLY VOLTAGE



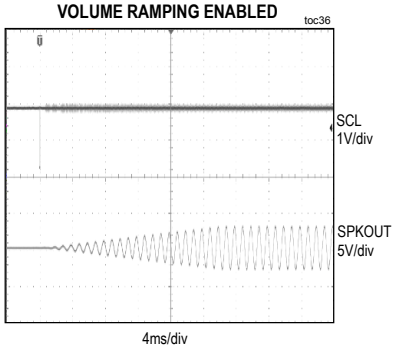
DVDD POWER SUPPLY REJECTION RATIO vs. FREQUENCY



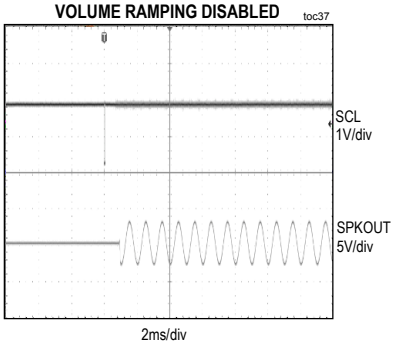
POWER SUPPLY REJECTION RATIO vs. DVDD SUPPLY VOLTAGE



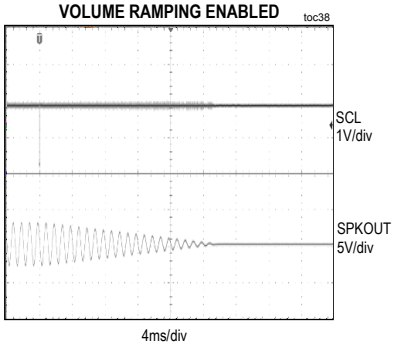
SOFTWARE ENABLE TURN ON RESPONSE VOLUME RAMPING ENABLED



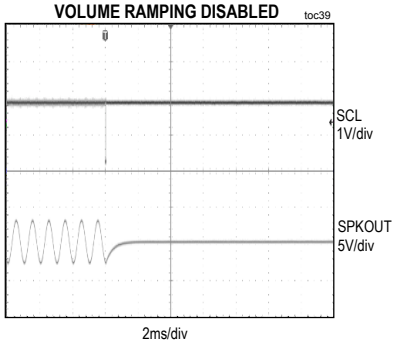
SOFTWARE ENABLE TURN-ON RESPONSE VOLUME RAMPING DISABLED



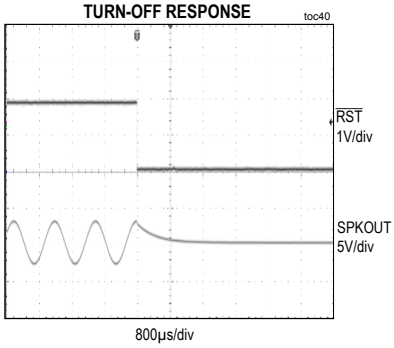
SOFTWARE DISABLE TURN-OFF RESPONSE VOLUME RAMPING ENABLED



SOFTWARE DISABLE TURN-OFF RESPONSE VOLUME RAMPING DISABLED

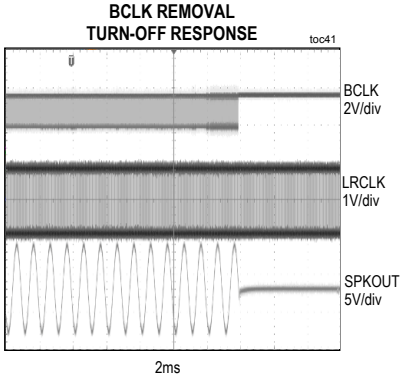


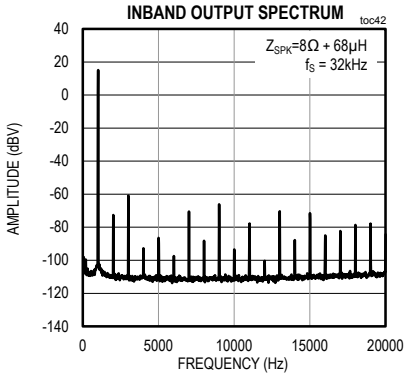
HARDWARE RESET TURN-OFF RESPONSE

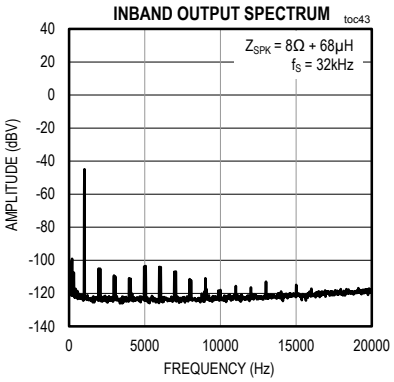


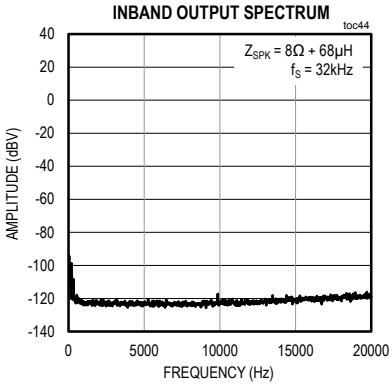
Typical Operating Characteristics (continued)

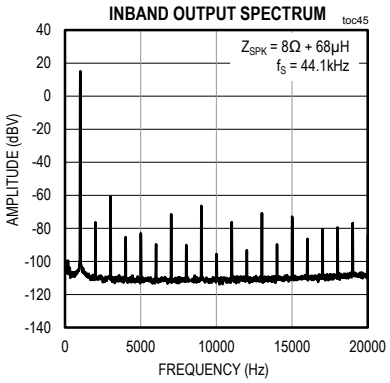
(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

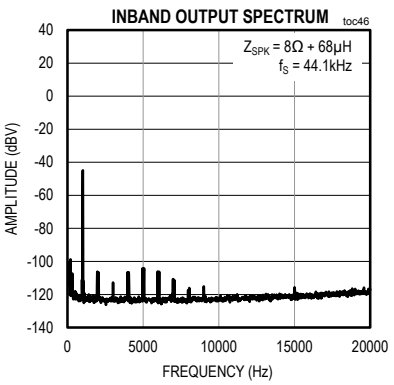


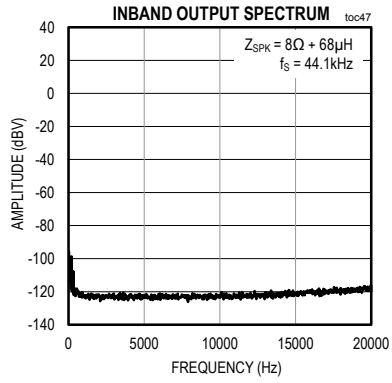


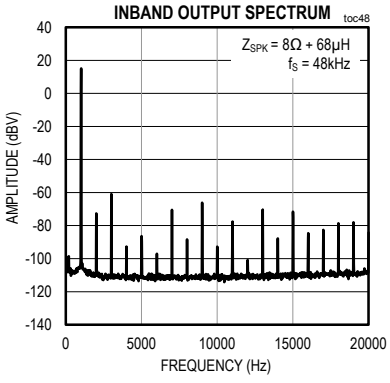


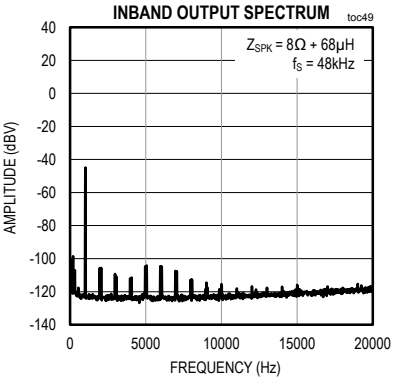






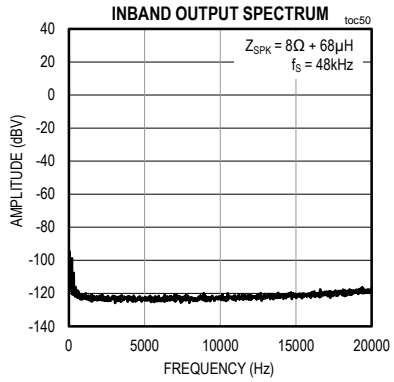


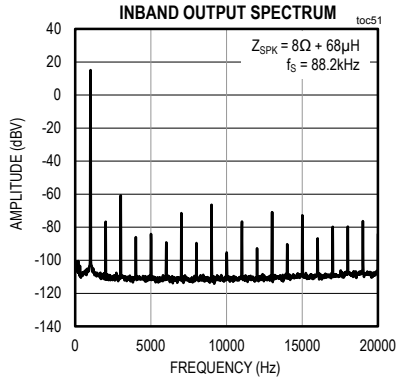


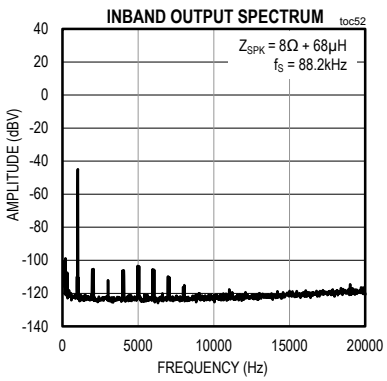


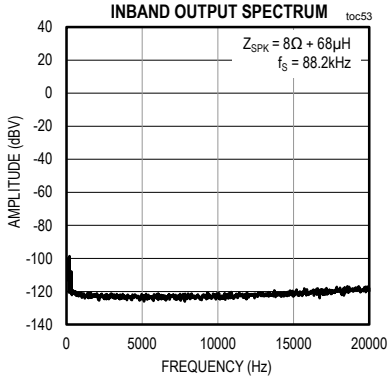
Typical Operating Characteristics (continued)

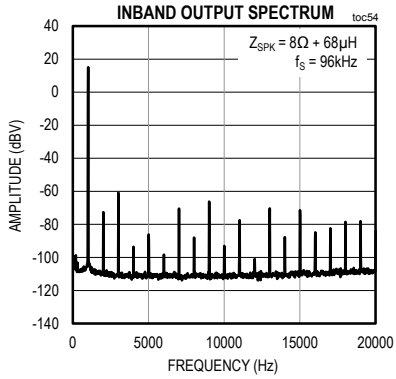
(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

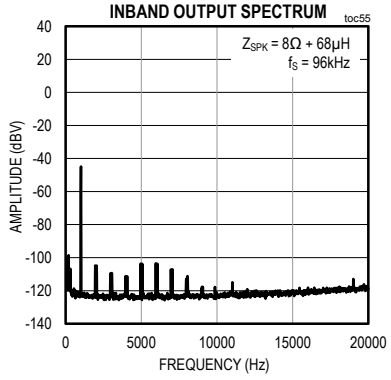


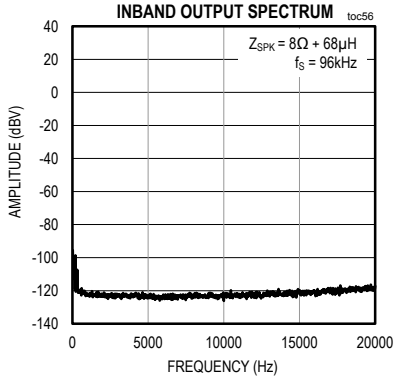




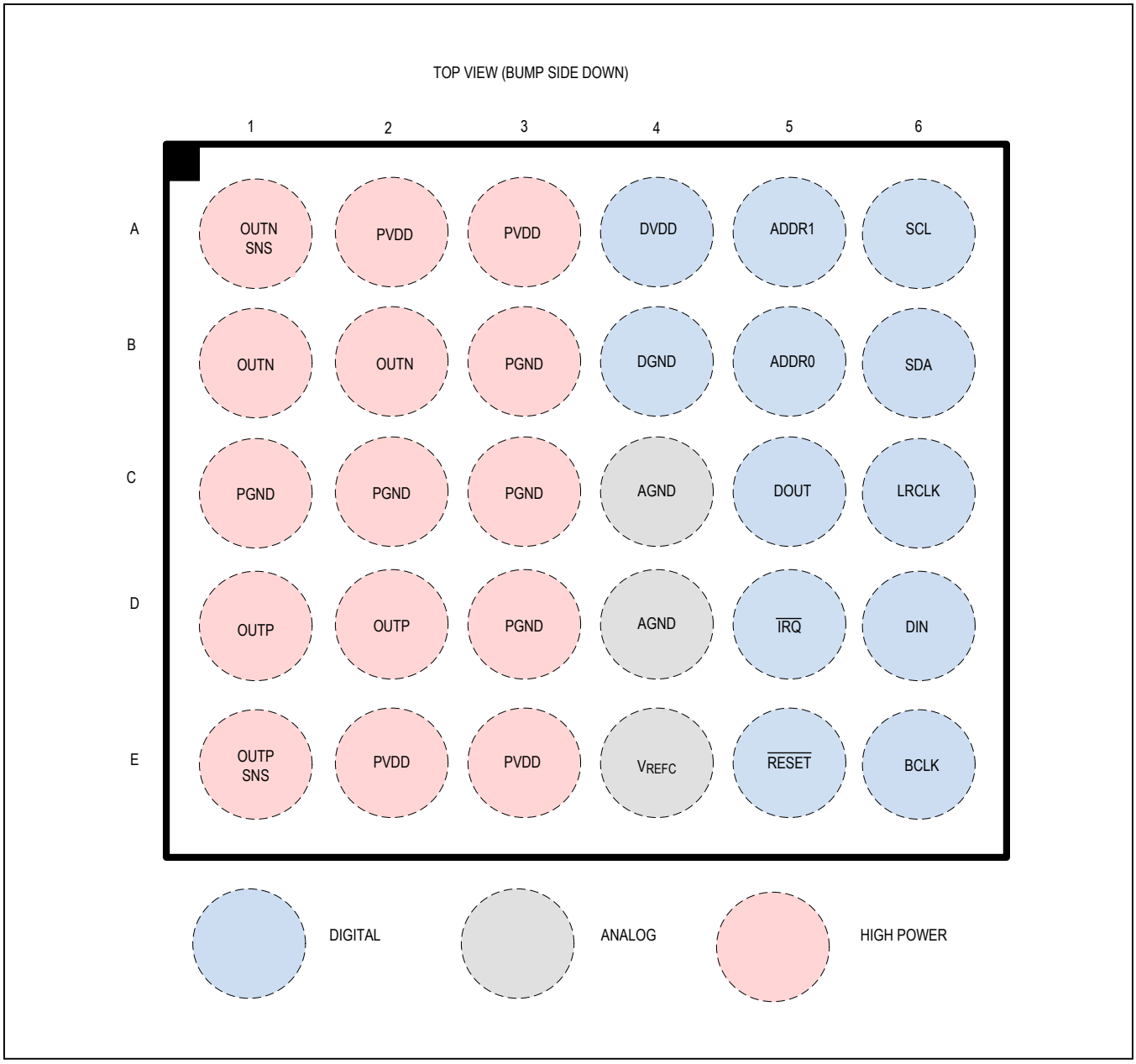








Pin Configurations



Pin Description

BUMP	NAME	SUPPLY RAIL	FUNCTION
A1	OUTNSNS	PVDD	Negative Speaker Amplifier Output Sense. If not used, connect to OUTN.
A2, A3 E2, E3	PVDD	—	Speaker Amplifier Power Supply. Bypass each bump pair to PGND with a 10µF and a 0.1µF, and a single 220µF per device.
A4	DVDD	—	Digital Core, Digital Audio Interface, and I²C Control Power Supply. Bypass to DGND with a 1µF.
A5	ADDR1	DVDD	Four-Level I²C Slave Address Select Input. See the *Slave Address Selection* section for additional information (Table 40).
A6	SCL	DVDD	I²C Control Clock Input
B1, B2	OUTN	PVDD	Negative Speaker Amplifier Output
B3,C1-C3, D3	PGND	—	Speaker Amplifier Ground
B4	DGND	—	Digital Ground
B5	ADDR0	DVDD	Four-Level I²C Slave Address Select Input. See the *Slave Address Selection* section for additional information (Table 40).
B6	SDA	DVDD	I²C Control Data Input/Output
C4, D4	AGND	—	Analog Ground
C5	DOUT	DVDD	Bidirectional ICC Link Data
C6	LRCLK	DVDD	DAI Left/Right Clock Input. LRCLK is the audio sample rate clock and determines whether audio data is routed to the left or right channel. In TDM mode, LRCLK is a frame sync pulse with programmable width.
D1, D2	OUTP	PVDD	Positive Speaker Amplifier Output
D5	$\overline{\text{IRQ}}$	DVDD	Hardware Interrupt Output. $\overline{\text{IRQ}}$ can be programmed to pull low when individual bits in the flag registers change value. Connect a 10kΩ pullup resistor for full output swing.
D6	DIN	DVDD	DAI Audio Data Input
E1	OUTPSNS	PVDD	Positive Speaker Amplifier Output Sense. If not used, connect to OUTP.
E4	VREFC	PVDD	Internal Regulator Decoupling Point. Bypass to AGND with a 1µF.
E5	$\overline{\text{RESET}}$	DVDD	Active-Low Hardware Reset. Drive low to place the device into low power reset mode and reset the device registers to their power-on-reset (POR) states.
E6	BCLK	DVDD	DAI Bit Clock Input

Detailed Description

The MAX98371 is a high-efficiency mono Class D audio amplifier that features thermal foldback protection and ADCs for sensing battery supply voltage and onboard temperature.

The MAX98371 can operate over a wide range of supply voltage (PVDD), and has extensive on-board digital signal processing to enable Dynamic Headroom Tracking (DHT). This feature automatically adjusts the output signal to fit into the available supply voltage range. The DHT can be completely bypassed for operation with fixed, regulated supply voltages.

Maxim's Active Emissions Limiting (AEL) edge rate and overshoot control circuitry, together with Class D modulation minimize the electromagnetic interference (EMI) traditionally associated with Class D amplifiers. In systems that use less than 18 inches of speaker cable, an output filter is unnecessary to meet standard EMI limits.

Two ADCs monitor PVDD supply voltage and die temperature. The PVDD supply voltage value can be read using the I²C interface. The temperature ADC can be read back through I²C, however, accurate readings only occur after the die temperature exceeds 100°C.

The DAI supports I²S, Left-Justified, and TDM formatted data at the following sample rates: 32kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz. Audio bit depths of 16, 24, and 32 bits are supported for input data. The DAI operates from BCLK to allow the device to function without MCLK.

Thermal foldback allows the device to smoothly attenuate the audio output in an effort to prevent destructive thermal behavior. Above a set threshold, the gain of the replay path reduces at a (user programmable) dB/°C rate to a 12dB maximum attenuation. Thermal monitoring capabilities alert the host when die temperature has triggered the thermal foldback circuit, or is approaching the maximum operating temperature. If maximum die temperature is exceeded, the device shuts down to protect itself. Short-circuit protection ensures that accidental shorts or high-current events do not cause damage to the IC.

Device status is communicated to the host through a hardware interrupt ($\overline{IRQ}$) and status registers accessible through the I²C interface.

The MAX98371 is fully programmable through the I²C interface. ADDR0, ADDR1 connections select one of sixteen I²C slave addresses. Shutdown mode is directly controlled through the I²C interface, or a hardware shutdown can be asserted through the $\overline{RESET}$ pin.

Table 1. MAX98371 Control Register Map

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT1	BIT 0	
INTERRUPTS											
0x01	INTERRUPT STATUS 0	R	—	—	THRMFB_ STATUS	—	THRM WRN_ STATUS	—	THRM SHDN_ STATUS	—	0x00
0x02	INTERRUPT STATUS 1	R	—	ICCOVC_ STATUS	LMTRACT_ STATUS	INVAL SLOT_ STATUS	DHTACT_ STATUS	SPK CURNT_ STATUS	PVDD OVFL_ STATUS	PVDD UVLO_ STATUS	0x00
0x03	INTERRUPT STATE 0	R	—	—	THRMFB_ END_ STATE	THRMFB_ BGN_ STATE	THRM WRN_END _STATE	THRM WRN_BGN _STATE	THRM SHDN_END _STATE	THRM SHDN_BGN _STATE	0x00
0x04	INTERRUPT STATE 1	R	—	ICCOVC_ STATE	LMTRACT_ STATE	INVAL SLOT_ STATE	DHTACT_ STATE	SPK CURNT_ STATE	PVDD OVFL_ STATE	PVDD UVLO_ STATE	0x00
0x05	INTERRUPT FLAG 0	R/W	—	—	THRMFB_ END_ FLAG	THRMFB_ BGN_ FLAG	THRM WRN_END_ FLAG	THRM WRN_BGN _FLAG	THRM SHDN_ END_ FLAG	THRM SHDN_ BGN_ FLAG	0x00

Table 1. MAX98371 Control Register Map (continued)

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT1	BIT 0	
0x06	INTERRUPT FLAG 1	R/W	—	ICCOVC_ FLAG	LMTRACT_ FLAG	INVAL SLOT_ FLAG	DHTACT_ FLAG	SPK CURNT_ FLAG	PVDD OVFL_ FLAG	PVDD UVLO_ FLAG	0x00
0x07	INTERRUPT ENABLES 0	R/W	—	—	THRMFB_ END_ EN	THRMFB_ BGN_ EN	THRM WRN_ END_ EN	THRM WRN_ BGN_ EN	THRM SHDN_ END_ EN	THRM SHDN_ BGN_ EN	0x00
0x08	INTERRUPT ENABLES 1	R/W	—	ICCOVC_ EN	LMTRACT_ EN	INVAL SLOT_ EN	DHTACT_ EN	SPK CURNT_ EN	PVDD OVFL_ EN	PVDD UVLO_ EN	0x00
0x09	INTERRUPT CLEARS 0	W	—	—	THRMFB_ END_CLR	THRMFB_ BGN_ CLR	THRM WRN_ END_ CLR	THRM WRN_ BGN_ CLR	THRM SHDN_ END_ CLR	THRM SHDN_ BGN_ CLR	0x00
0x0A	INTERRUPT CLEARS 1	W	—	ICCOVC_ CLR	LMTRACT_ CLR	INVAL SLOT_ CLR	DHTACT_ CLR	SPK CURNT_ CLR	PVDD OVFL_CLR	PVDD UVLO_ CLR	0x00
PCM CONFIGURATION											
0x10	PCM CLOCK SETUP	R/W	—	—	—	—	BSEL[3:0]				0x06
0x11	PCM SAMPLE RATE SETUP	R/W	—	—	—	—	SPK_SR[3:0]				0x08
0x14	PCM MODE CONFIG	R/W	CHANSZ[1:0]		FORMAT[2:0]			BCLEDGE	CHANSEL	—	0x80
0x15	PCM RX ENABLES A	R/W	RX_ CH7_EN	RX_ CH6_EN	RX_ CH5_EN	RX_ CH4_EN	RX_ CH3_EN	RX_ CH2_EN	RX_ CH1_EN	RX_ CH0_EN	0x00
0x16	PCM RX ENABLES B	R/W	RX_ CH15_EN	RX_ CH14_EN	RX_ CH13_EN	RX_ CH12_EN	RX_ CH11_EN	RX_ CH10_EN	RX_ CH9_EN	RX_ CH8_EN	0x00
0x18	MONOMIX CHANNEL SOURCE	R/W	DMONOMIX_CH1_SOURCE[3:0]				DMONOMIX_CH0_SOURCE[3:0]				0x00
0x19	MONOMIX CHANNEL SOURCE	R/W	—	—	—	—	—	—	DMONOMIX_CFG[1:0]		0x00
DIGITAL FILTER PARAMETERS											
0x1C	DIGITAL FILTER	R/W	PVDD_FILT _TO_LMTR	PVDD_FILT _TO_DHT	PVDD_ADC_BW[1:0]		—	DACHPF[2:0]			0x00
0x1D	DAC BQ B0	R/W	DAC_BQ_B0[23:16]								0x00
0x1E		R/W	DAC_BQ_B0[15:8]								0x00
0x1F		R/W	DAC_BQ_B0[7:0]								0x00
0x20	DAC BQ B1	R/W	DAC_BQ_B1[23:16]								0x00
0x21		R/W	DAC_BQ_B1[15:8]								0x00
0x22		R/W	DAC_BQ_B1[7:0]								0x00
0x23	DAC BQ B2	R/W	DAC_BQ_B2[23:16]								0x00
0x24		R/W	DAC_BQ_B2[15:8]								0x00
0x25		R/W	DAC_BQ_B2[7:0]								0x00

Table 1. MAX98371 Control Register Map (continued)

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT1	BIT 0	
0x26	DAC BQ A0	R/W	DAC_BQ_A0[23:16]								0x00
0x27		R/W	DAC_BQ_A0[15:8]								0x00
0x28		R/W	DAC_BQ_A0[7:0]								0x00
0x29	DAC BQ A1	R/W	DAC_BQ_A1[23:16]								0x00
0x2A		R/W	DAC_BQ_A1[15:8]								0x00
0x2B		R/W	DAC_BQ_A1[7:0]								0x00
0x2D	DIGITAL VOLUME CONTROL	R/W	DVOL_ RAMP_BYP	DVOL[6:0]							0x00
0x2E	PATH GAIN	R/W	DPGA_CLIP[3:0]				SPK_GAIN_MAX[3:0]				0x0B
DYNAMIC GAIN PARAMETERS											
0x31	DHT ROTATION POINT	R/W	SPK_GAIN_MIN[3:0]				DHT_VROT_PNT[3:0]				0x00
0x32	DHT ATTACK	R/W	—	—	—	DHT_ATK_STEP[1:0]		DHT_ATK_RATE[2:0]			0x18
0x33	DHT RELEASE	R/W	—	—	—	DHT_REL_STEP[1:0]		DHT_REL_RATE[2:0]			0x00
0x34	PVDD ADC MEASUREMENT	R	PVDD_ADC[7:0]								0x00
0x36	THERMAL FOLDBACK	R/W	THRM_HOLD[1:0]		—	—	THRM_REL[1:0]		THRM_SLOPE[1:0]		0x00
0x37	THERMAL ADC MEASUREMENT	R	—	—	THRM_ADC_MEAS[5:0]						0x00
0x38	THERMAL FOLDBACK MIN TEMP	R/W	—	—	THRM_MIN_TEMP[5:0]						0x00
0x39	THERMAL FOLDBACK LOW PASS FILTER	R/W	—	—	—	—	—	THRM_FILT_SEL[2:0]			0x00
0x3A	PCM2 RXDHT ENABLES A	R/W	RXDHT_ CH7_EN	RXDHT_ CH6_EN	RXDHT_ CH5_EN	RXDHT_ CH4_EN	RXDHT_ CH3_EN	RXDHT_ CH2_EN	RXDHT_ CH1_EN	RXDHT_ CH0_EN	0x00
0x3B	PCM2 RXDHT ENABLES B	R/W	RXDHT_ CH15_EN	RXDHT_ CH14_EN	RXDHT_ CH13_EN	RXDHT_ CH12_EN	RXDHT_ CH11_EN	RXDHT_ CH10_EN	RXDHT_ CH9_EN	RXDHT_ CH8_EN	0x00
0x3C	PCM2 RXTHM ENABLES A	R/W	RXTHM_ CH7_EN	RXTHM_ CH6_EN	RXTHM_ CH5_EN	RXTHM_ CH4_EN	RXTHM_ CH3_EN	RXTHM_ CH2_EN	RXTHM_ CH1_EN	RXTHM_ CH0_EN	0x00
0x3D	PCM2 RXTHM ENABLES B	R/W	RXTHM_ CH15_EN	RXTHM_ CH14_EN	RXTHM_ CH13_EN	RXTHM_ CH12_EN	RXTHM_ CH11_EN	RXTHM_ CH10_EN	RXTHM_ CH9_EN	RXTHM_ CH8_EN	0x00
0x3E	PCM2 TX \ ENABLES A	R/W	TX_ CH7_EN	TX_ CH6_EN	TX_ CH5_EN	TX_ CH4_EN	TX_ CH3_EN	TX_ CH2_EN	TX_ CH1_EN	TX_ CH0_EN	0x00

Table 1. MAX98371 Control Register Map (continued)

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT1	BIT 0	
0x3F	PCM2 TX ENABLES A	R/W	TX_ CH15_EN	TX_ CH14_EN	TX_ CH13_EN	TX_ CH12_EN	TX_ CH11_EN	TX_ CH10_EN	TX_ CH9_EN	TX_ CH8_EN	0x00
0x40	PCM2 DATA ORDER SELECT	R/W	—	—	—	—	DRIVE_ MODE	—	—	—	0x00
0x41	PCM2 HiZ MANUAL MODE	R/W	—	—	—	—	—	—	TX_ EXTRA_ HIZ	—	0x00
0x42	PCM2 TX HiZ ENABLES A	R/W	TX_ CH7_HIZ	TX_ CH6_HIZ	TX_ CH5_HIZ	TX_ CH4_HIZ	TX_ CH3_HIZ	TX_ CH2_HIZ	TX_ CH1_HIZ	TX_ CH0_HIZ	0x00
0x43	PCM2 TX HiZ ENABLES B	R/W	TX_ CH15_HIZ	TX_ CH14_HIZ	TX_ CH13_HIZ	TX_ CH12_HIZ	TX_ CH11_HIZ	TX_ CH10_HIZ	TX_ CH9_HIZ	TX_ CH8_HIZ	0x00
ENABLES											
0x4A	SPEAKER ENABLE	R/W	SPK_ SWCLK	—	—	—	SPK_EDGE[1:0]		—	SPK_EN	0x00
0x4B	DYNAMIC GAIN ENABLES	R/W	—	—	—	—	—	PVADC_EN	LMTR_EN	DHT_EN	0x00
0x4C	THERMAL FOLDBACK ENABLE	R/W	—	—	—	—	—	—	—	THERM_ FB_EN	0x00
0x4D	RESTART BEHAVIOR	R/W	—	—	—	—	CMON_ AUTO_ RESTART	CMON_ ENA	OVC_ SEL	TSHDN_ AUTO_ RESTART	0x00
0x4E	ICC LINK ENABLE	R/W	—	—	—	—	—	—	THM_ LINK_EN	DHT_ LINK_EN	0x00
0x50	GLOBAL ENABLE	R/W	—	—	—	—	—	—	—	EN	0x00
0x51	SOFTWARE RESET	W	—	—	—	—	—	—	—	RST	0x00
0x55	LIMITER ATTACK AND RELEASE	R/W	—	—	LMTR_REL_RATE[2:0]			LMTR_ATK_RATE[2:0]			0x00
0x58	LIMITER THRESHOLD SELECT	R/W	—	—	—	—	—	—	LMTR_TH_SEL[1:0]		0x00
0x59	LIMITER MANUAL THRESHOLD	R/W	—	—	—	LMTR_THC[4:0]					0x00
0x5C	ICC PAD CONTROL	R/W	—	ICC_OC_ ENA	ICC_ DOUTEN_ EXTFF	ICC_ DOUT_ EXTFF	ICC_PAD_CTRL[3:0]				0x00
0xFF	REV ID	R	REVID[7:0]								0x43

Interrupts

The MAX98371 supports programmable interrupts for sending feedback to the host about events that have occurred on-chip. Table 2 lists the available interrupt sources. Interrupts are output on $\overline{IRQ}$, an active low open-drain output.

Status

Each interrupt source has one bit to indicate the realtime STATUS of the source. This bit is read-only.

State

Each interrupt source has a STATE bit that is set whenever a rising edge occurs on the associated STATUS bit regardless of the state of the associated ENABLE bit. This bit is read-only.

Flag

Each interrupt source has a FLAG bit to indicate that a rising edge has occurred on the associated STATUS bit and the associated ENABLE bit is set. This bit is read-only.

Enable

Each interrupt source has an ENABLE bit to indicate that the associated FLAG bit is set whenever the STATE bit is set. This bit is read/write.

Clear

Each interrupt has a CLEAR bit that clears the associated STATE and FLAG bits when a 1 is written. Writing a 0 has no effect. This bit is write-only.

Table 2. Interrupt Sources

NAME	DESCRIPTION
Overtemperature Begin Event	Indicates when the die overtemperature threshold has been exceeded.
Overtemperature End Event	Indicates when the die overtemperature threshold is no longer exceeded including 20°C of hysteresis.
Thermal Warning Begin Event	Indicates when the thermal warning threshold has been exceeded.
Thermal Warning End Event	Indicates that the die temperature was previously above the thermal warning threshold and has now dropped below the threshold.
Speaker Current Event	Indicates when the speaker amplifier current limit has been exceeded.
Invalid Slot Event	Indicates that a slot has been selected that is not available due to one or more of the following reasons: The (number of bits per channel) x (channels per frame) does not allow for the selected slot (I^2S mode only). The number of BCLK cycles per frame does not allow for the selected slot (TDM mode only).
Thermal Foldback Event	Indicates that the Thermal Foldback Limiter is operating in the attack or release phase.
Thermal Foldback End Event	Indicates that the die temperature was previously above the thermal threshold and has now dropped below the threshold.
V_{PVDD} Overflow Event	Indicates that the V_{PVDD} supply voltage has reached the V_{PVDD} ADC's maximum input level.
PVDD UVLO Event	Indicates that PVDD has dropped below the minimum allowed voltage.
DHT Active Event	Indicates that the DHT circuit is applying compression to the signal.
Limiter Active Event	Indicates that the limiter circuit is applying a hard limit (infinite compression) to the signal.
ICC Overcurrent Event	Indicates that an overcurrent event is in progress on DOUT.

Table 3. Interrupt Registers

Interrupt Status0
Interrupt Status bits reflect real-time fault conditions. If the fault condition is less than 3-4 LRCLK cycles, the Live Status bit holds high for 3–4 LRCLK cycles.

ADDRESS	BIT	NAME	DESCRIPTION
$0x0_1$	7	0	Unused: Read back is 0.
	6	0	Unused: Read back is 0.
	5	THERMFB_STATUS	**Die Thermal Foldback Status** 0: The die temperature is below the thermal warning threshold. 1: The die temperature is above the thermal warning threshold and the signal is being dynamically attenuated.
	4	0	Unused: Read back 0.
	3	THERMWRN_STATUS	**Die Overtemperature Warning Status** 0: The die temperature is below the thermal warning threshold. 1: The die temperature is above the thermal warning threshold.
	2	0	Unused: Read back is 0.
	1	THERMSHDN_STATUS	**Die Overtemperature Status** 0: The die temperature is below the maximum die temperature. 1: The die temperature exceeds the maximum die temperature.
	0	0	Unused: Read back 0.

Table 3. Interrupt Registers (continued)

Interrupt Status1
Interrupt Status bits reflect real-time fault conditions. If the fault condition is less than 3–4 LRCLK cycles, the Live Status bit holds high for 3–4 LRCLK cycles.

ADDRESS	BIT	NAME	DESCRIPTION
0x02	7	0	Unused: Read back is 0.
	6	ICCOVC_STATUS	**ICC Overcurrent Status** 0: No overcurrent event on the DOUT is in progress. 1: Overcurrent event on the DOUT is in progress.
	5	LMTRACT_STATUS	**Limiter Active Status** 0: Limiter is not active. 1: Limiter is active.
	4	INVALSLOT_STATUS	**Invalid Slot Status** 0: Slot is valid. 1: Slot is invalid, one or more possible error conditions apply: a. The (number of bits per channel) * (channels per frame) does not allow for the selected slot. (I2S mode only) b. The number of BCLK cycles per frame does not allow for the selected slot.(TDM mode only).
	3	DHTACT_STATUS	**DHT Active Status** 0: Dynamic Headroom Tracking is not attacking or releasing. 1: Dynamic Headroom Tracking is active and is attacking or releasing.
	2	SPKCURNT_STATUS	**Speaker Overcurrent Status** 0: Speaker current is below the current limit. 1: Speaker current is above the current limit.
	1	PVDDOVFL_STATUS	**PVDD Supply Voltage Monitor Overflow Status** 0: The PVDD supply voltage is below the PVDD ADC's maximum input level. 1: The PVDD supply voltage has exceeded the PVDD ADC's maximum input level
	0	PVDDUVLO_STATUS	**PVDD Supply Voltage Undervoltage Status** 0: The PVDD supply voltage is above the PVDD UVLO level. 1: The PVDD supply voltage is below the PVDD UVLO threshold, and the speaker outputs are disabled.

Table 3. Interrupt Registers (continued)

Interrupt State 0			
ADDRESS	**BIT**	**NAME**	**DESCRIPTION**
0x03	7	0	Unused: Read back is 0.
	6	0	Unused: Read back is 0.
	5	THERMFB_END_STATE	**Die Thermal Foldback State End Event** 0: No falling edge on thermal foldback status is detected. 1: A falling edge on thermal foldback status is detected. **Note:** Write a 1 to THERMFB_END_CLR to reset
	4	THERMFB_BGN_STATE	**Die Thermal Foldback State End Event** 0: No rising edge on thermal foldback status is detected. 1: A rising edge on thermal foldback status is detected. **Note:** Write a 1 to THERMFB_BGN_CLR to reset.
	3	THERMWRN_END_STATE	**Thermal Warning Status End Event** 0: No falling edge on THERMWRN_STATUS is detected. 1: A falling edge on THERMWRN_STATUS is detected. **Note:** Write a 1 to THERMWRN_END_CLR to reset.
	2	THERMWRN_BGN_STATE	**Thermal Warning Status Begin Event** 0: No rising edge on THERMWRN_ STATUS is detected. 1: A rising edge on THERMWRN_STATUS is detected. **Note:** Write a 1 to THERMWRN_BGN_CLR to reset.
	1	THERMSHDN_END_STATE	**Thermal Shutdown End Event** 0: No falling edge on THERMSHDN_STATUS is detected. 1: A falling edge on THERMSHDN_STATUS is detected. **Note:** Write a 1 to THERMSHDN_END_CLR to reset.
	0	THERMSHDN_BGN_STATE	**Thermal Shutdown Begin Event** 0: No rising edge on THERMSHDN_STATUS is detected. 1: A rising edge on THERMSHDN_STATUS is detected. **Note:** Write a 1 to THERMSHDN_BGN_CLR to reset.

Table 3. Interrupt Registers (continued)

Interrupt State 1			
ADDRESS	**BIT**	**NAME**	**DESCRIPTION**
0x04	7	0	Unused: Read back is 0.
	6	ICCOVC_STATE	**ICC Overcurrent Event** 0: No rising edge on ICCOVC_STATUS is detected. 1: A rising edge on ICCOVC_STATUS is detected. **Note:** Write a 1 to ICCOVC_CLR to reset.
	5	LMTRACT_STATE	**Limiter Active Event** 0: No rising edge on LMTRACT_STATUS is detected. 1: A rising edge on LMTRACT_STATUS is detected. **Note:** Write a 1 to LMTRACT_CLR to reset.
	4	INVALSLOT_STATE	**Invalid Slot Event** 0: No rising edge on INVALSLOT_STATUS is detected. 1: A rising edge on INVALSLOT_STATUS is detected. **Note:** Write a 1 to INVALSLOT_CLR to reset.
	3	DHTACT_STATE	**DHT Active Event** 0: No rising edge on DHTACT_STATUS is detected. 1: A rising edge on DHTACT_STATUS is detected. **Note:** Write a 1 to DHTACT_STATUS to reset.
	2	SPKCURNT_STATE	**Speaker Overcurrent Event** 0: No rising edge on SPKCURNT_STATUS is detected. 1: A rising edge on SPKCURNT_STATUS is detected. **Note:** Write a 1 to SPKCURNT_CLR to reset.
	1	PVDDOVFL_STATE	**PVDD ADC Overflow Event** 0: No rising edge on PVDDOVFL_STATUS is detected. 1: A rising edge on PVDDOVFL_STATUS is detected. **Note:** Write a 1 to PVDDOVFL_CLR to reset.
	0	PVDDUVLO_STATE	**PVDD Supply Voltage Undervoltage Lockout Event** 0: No rising edge on PVDDUVLO_STATUS is detected. 1: A rising edge on PVDDUVLO_STATUS is detected. **Note:** Write a 1 to PVDDOVFL_CLR to reset.

Table 3. Interrupt Registers (continued)

Interrupt Flag 0			
ADDRESS	**BIT**	**NAME**	**DESCRIPTION**
0x05	7	0	Unused: Read back is 0.
	6	0	Unused: Read back is 0.
	5	THERMFB_END_FLAG	**Die Thermal Foldback End Flag** 0: No thermal foldback end interrupt is generated. 1: Thermal foldback end interrupt is generated.
	4	THERMFB_BGN_FLAG	**Die Thermal Foldback Begin Flag** 0: No thermal foldback begin interrupt is generated. 1: Thermal foldback begin interrupt is generated.
	3	THERMWRN_END_FLAG	**Thermal Warning End Flag** 0: No thermal warning end is interrupt generated. 1: Thermal warning end interrupt is generated.
	2	THERMWRN_BGN_FLAG	**Thermal Warning Begin Flag** 0: No thermal warning begin interrupt is generated. 1: Thermal warning begin interrupt is generated.
	1	THERMSHDN_END_FLAG	**Thermal Shutdown End Flag** 0: No thermal shutdown end interrupt is generated. 1: Thermal shutdown end interrupt is generated.
	0	THERMSHDN_BGN_FLAG	**Thermal Shutdown Begin Flag** 0: No thermal shutdown begin interrupt is generated. 1: Thermal shutdown begin interrupt is generated.

Table 3. Interrupt Registers (continued)

Interrupt Flag 1			
ADDRESS	**BIT**	**NAME**	**DESCRIPTION**
0x06	7	0	Unused: Read back 0.
	6	ICCOVC_FLAG	**ICC Overcurrent Flag** 0: No ICC overcurrent interrupt is generated. 1: ICC overcurrent interrupt is generated.
	5	LMTRACT_FLAG	**Limiter Active Flag** 0: No limiter active interrupt is generated. 1: Limiter active interrupt is generated.
	4	INVALSLOT_FLAG	**Invalid Slot Flag** 0: No invalid slot interrupt is generated. 1: Invalid slot interrupt is generated.
	3	DHTACT_FLAG	**DHT Active Flag** 0: No Dynamic Headroom Tracking active slot interrupt is generated. 1: Dynamic Headroom Tracking active slot interrupt is generated.
	2	SPKCURNT_FLAG	**Speaker Overcurrent Flag** 0: No speaker overcurrent interrupt is generated. 1: Speaker overcurrent interrupt is generated.
	1	PVDDOVFL_FLAG	**PVDD ADC Overflow Flag** 0: No PVDD ADC overflow interrupt is generated. 1: PVDD ADC overflow interrupt is generated.
	0	PVDDUVLO_FLAG	**PVDD Supply Voltage Undervoltage Lockout Flag** 0: No PVDD UVLO Interrupt is generated. 1: PVDD UVLO Interrupt is generated.

Table 3. Interrupt Registers (continued)

Interrupt Enable 0			
ADDRESS	**BIT**	**NAME**	**DESCRIPTION**
0x07	7	0	Unused: Read back is 0.
	6	0	Unused: Read back is 0.
	5	THERMFB_END_EN	**Die Thermal Foldback End Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when THERMFB_END_FLAG transitions from 0 to 1.
	4	THERMFB_BGN_EN	**Die Thermal Foldback Begin Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when THERMFB_END_FLAG transitions from 0 to 1.
	3	THERMWRN_END_ EN	**Thermal Warning End Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when THERMWRN_END_ FLAG transitions from 0 to 1.
	2	THERMWRN_BGN_ EN	**Thermal Warning Begin Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when THERMWRN_BGN_ FLAG transitions from 0 to 1.
	1	THERMSHDN_END_ EN	**Thermal Shutdown End Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when THERMSHDN_END_ FLAG transitions from 0 to 1.
	0	THERMSHDN_BGN_ EN	**Thermal Shutdown Begin Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when THERMSHDN_BGN_ FLAG transitions from 0 to 1.

Table 3. Interrupt Registers (continued)

Interrupt Enable 1			
ADDRESS	**BIT**	**NAME**	**DESCRIPTION**
0x08	7	0	Unused: Read back is 0.
	6	ICCOVC_EN	**ICC Overcurrent Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when ICCOVC_FLAG transitions from 0 to 1.
	5	LMTRACT_EN	**Limiter Active Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when LMTRACT_FLAG transitions from 0 to 1.
	4	INVALSLOT_EN	**Invalid Slot Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt enabled. $\overline{IRQ}$ is pulled low when INVALSLOT_FLAG transitions from 0 to 1.
	3	DHTACT_EN	**DHT Active Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when DHTACT_FLAG transitions from 0 to 1.
	2	SPKCURNT_EN	**Speaker Overcurrent Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when SPKCURNT_FLAG transitions from 0 to 1.
	1	PVDDOVFL_EN	**PVDD ADC Overflow Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when PVDDOVFL_FLAG transitions from 0 to 1.
	0	PVDDUVLO_EN	**PVDD Supply Voltage Undervoltage Lockout Interrupt Enable** 0: Interrupt is disabled (default). 1: Interrupt is enabled. $\overline{IRQ}$ is pulled low when PVDDUVLO_FLAG transitions from 0 to 1.

Table 3. Interrupt Registers (continued)

Interrupt Clear 0			
ADDRESS	**BIT**	**NAME**	**DESCRIPTION**
0x09	7	0	Unused: Read back is 0.
	6	0	Unused: Read back is 0.
	5	THERMFB_END_CLR	**Die Thermal Foldback End Interrupt Clear** 0: No effect. 1: Clears the THERMFB_END_STATE and THERMFB_END_FLAG.
	4	THERMFB_BGN_CLR	**Die Thermal Foldback Begin Interrupt Clear** 0: No effect. 1: Clears the THERMFB_BGN_STATE and THERMFB_BGN_FLAG.
	3	THERMWRN_END_CLR	**Thermal Warning End Interrupt Clear** 0: No effect. 1: Clears the THERMWRN_END_STATE and THERMWRN_END_FLAG.
	2	THERMWRN_BGN_CLR	**Thermal Warning Begin Interrupt Clear** 0: No effect. 1: Clears the THERMWRN_BGN_STATE and THERMWRN_BGN_FLAG.
	1	THERMSHDN_END_CLR	**Thermal Shutdown End Interrupt Clear** 0: No effect. 1: Clears the THERMSHDN_END_STATE and THERMSHDN_END_FLAG.
	0	THERMSHDN_BGN_CLR	**Thermal Shutdown Begin Interrupt Clear** 0: No effect. 1: Clears the THERMSHDN_BGN_STATE and THERMSHDN_BGN_FLAG.

Table 3. Interrupt Registers (continued)

Interrupt Clear 1			
ADDRESS	**BIT**	**NAME**	**DESCRIPTION**
0x0A	7	0	Unused: Read back 0.
	6	ICCOVC_CLR	**ICC Overcurrent Clear** 0: No effect. 1: Clears the ICCOVC_STATE and ICCOVC_FLAG.
	5	LMTRACT_CLR	**Limiter Active Interrupt Clear** 0: No effect. 1: Clears the LMTRACT_STATE and LMTRACT_FLAG.
	4	INVALSLOT_CLR	**Invalid Slot Interrupt Clear** 0: No effect. 1: Clears the INVALSLOT_STATE and INVALSLOT_FLAG.
	3	DHTACT_CLR	**DHT Active Interrupt Clear** 0: No effect. 1: Clears the DHTACT_STATE and DHTACT_FLAG.
	2	SPKCURNT_CLR	**Speaker Overcurrent Interrupt Clear** 0: No effect. 1: Clears the SPKCURNT_STATE and SPKCURNT_FLAG.
	1	PVDDOVFL_CLR	**PVDD ADC Overflow Interrupt Clear** 0: No effect. 1: Clears the PVDDOVFL_STATE and PVDDOVFL_FLAG.
	0	PVDDUVLO_CLR	**PVDD Supply Voltage Undervoltage Lockout Interrupt Clear** 0: No effect. 1: Clears the PVDDUVLO_STATE and PVDDUVLO_FLAG.

Digital Audio Interface

The digital audio interface (DAI) is highly flexible, supporting common sample rates (Table 4) with 16/24/32-bit depth for I²S/Left-Justified data as well as up to 16 slots in a time division multiplexed (TDM) format.

Operating in slave mode only, the MAX98371 eliminates the need for the external MCLK signal that is typically used in I²S applications by generating MCLK internally. This reduces EMI and improves the RF immunity of the IC. Table 5 lists the supported BCLK frequencies when operating in this mode.

Table 4. Supported Sample Rates

ADDRESS	BIT	NAME	DESCRIPTION
0x11	3	SPK_SR[3:0]	**Speaker Path Sample Rate Select** 0000–0101: Reserved 0110: 32kHz 0111: 44.1kHz 1000: 48kHz 1001: Reserved 1010: 88.2kHz 1011: 96kHz 1100–1111: Reserved
	2		
	1		
	0		

Table 5. Supported BCLK Rates in Slave Mode

ADDRESS	BIT	NAME	DESCRIPTION
0x10	3	BSEL[3:0]	**Selects the Number of BCLKs/LRCLK** 0000: Not supported 0001: Not supported 0010: 32 BCLKs 0011: 48 BCLKs 0100: 64 BCLKs 0101: 96 BCLKs 0110: 128 BCLKs 0111: 192 BCLKs 1000: 256 BCLKs 1001: 384 BCLKs 1010: 512 BCLKs 1011–1111: Not supported
	2		
	1		
	0		

Interface Format

The MAX98371 supports standard I²S, left-justified, and TDM data formats. I²S and Left-Justified formats support two audio channels of 16, 24 or 32-bit depth. TDM supports up to 16 audio channels of 16-, 24-, or 32-bit depth. The IC supports slave operation only, and the LRCLK and BCLK pins operate as inputs.

I²S (Figure 5) and Left-Justified (Figure 6) modes configure the LRCLK signal to transition before each channel. With the default I²S settings LRCLK low indicates left channel while LRCLK high indicates the right channel. The MSB of the audio word is latched on the second active BCLK edge after an LRCLK transition. In Left-Justified mode, the MSB of the audio word is latched on the first active BCLK edge after an LRCLK transition.

TDM mode (Figure 7) uses a frame sync pulse instead of a 50% duty cycle frame clock. The frame sync pulse (applied to the LRCLK pin) is equal to one BCLK period as a minimum, although the interface operates with longer periods; the rising edge of LRCLK is used to indicate the start of a new frame. The falling edge can occur at any time as long as it does not violate the setup time requirements of the LRCLK rising edge. In TDM, latch the MSB of the first audio word on the first or second active BCLK edge after an LRCLK rising edge.

Configuring the DAI Format

Specify the format by configuring the LRCLK invert, BCLK active edge, data delay, and TDM mode configuration bits (Table 6).

Table 6. Configuration for Digital Audio Interface Format

ADDRESS	BIT	NAME	DESCRIPTION
0x14	7	CHANSZ[1:0]	**Configures Channel Word Length** 00: 8 bits 10: 24 bits 01: 16 bits 11: 32 bits
	6		
	5	FORMAT[2:0]	**PCM Format Select** 000: I²S mode 001: Left-Justified 010: Right-Justified 011: TDM Mode 1 100: TDM Mode 2 101–111: Reserved
	4		
	3		
	2	BCLEDGE	**Active BCLK Edge Select** 0: Data captured and valid on rising edge of BCLK 1: Data captured and valid on the falling edge of BCLK
	1	CHANSEL	**Non-TDM LRCLK Starting Edge** 0: Falling LRCLK indicates the start of a stereo pair. Channel 0 when LRCLK is low, Channel 1 when LRCLK is high. 1: Rising LRCLK indicates the start of a stereo pair. Channel 0 when LRCLK is high, Channel 1 when LRCLK is low.
	0	0	0

Configuring the Digital Audio Input

The DAI may be configured to accept a mono PCM input, placed from anywhere from slots 1 to 16 of digital audio in TDM mode. In I²S and Left-Justified modes, two channels are available.

Route mono data directly to the speaker amplifier. If the input is stereo, input the right channel to the device and mix with the left channel if desired. Sum left and right channels with the amplitude divided by 2 to reduce the DAC input and avoid saturation. Stereo summing and L or R choices are limited to 2 adjacent slots on the TDM bus.

Table 7. Configuration for Digital Audio Interface Format

ADDRESS	BIT	NAME	DESCRIPTION
0x15	7	RX_CH7_EN	**Receive Channel Enable** 0: Receive channel 7 is disabled. 1: Receive channel 7 is enabled.
	6	RX_CH6_EN	**Receive Channel Enable** 0: Receive channel 6 is disabled. 1: Receive channel 6 is enabled.
	5	RX_CH5_EN	**Receive Channel Enable** 0: Receive channel 5 is disabled. 1: Receive channel 5 is enabled.
	4	RX_CH4_EN	**Receive Channel Enable** 0: Receive channel 4 is disabled. 1: Receive channel 4 is enabled.
	3	RX_CH3_EN	**Receive Channel Enable** 0: Receive channel 3 is disabled. 1: Receive channel 3 is enabled.
	2	RX_CH2_EN	**Receive Channel Enable** 0: Receive channel 2 is disabled. 1: Receive channel 2 is enabled.
	1	RX_CH1_EN	**Receive Channel Enable** 0: Receive channel 1 is disabled. 1: Receive channel 1 is enabled.
	0	RX_CH0_EN	**Receive Channel Enable** 0: Receive channel 0 is disabled. 1: Receive channel 0 is enabled.

Table 7. Configuration for Digital Audio Interface Format (continued)

ADDRESS	BIT	NAME	DESCRIPTION
0x16	7	RX_CH15_EN	**Receive Channel Enable** 0: Receive channel 15 is disabled. 1: Receive channel 15 is enabled.
	6	RX_CH14_EN	**Receive Channel Enable** 0: Receive channel 14 is disabled. 1: Receive channel 14 is enabled.
	5	RX_CH13_EN	**Receive Channel Enable** 0: Receive channel 13 is disabled. 1: Receive channel 13 is enabled.
	4	RX_CH12_EN	**Receive Channel Enable** 0: Receive channel 12 is disabled. 1: Receive channel 12 is enabled.
	3	RX_CH11_EN	**Receive Channel Enable** 0: Receive channel 11 is disabled. 1: Receive channel 11 is enabled.
	2	RX_CH10_EN	**Receive Channel Enable** 0: Receive channel 10 is disabled. 1: Receive channel 10 is enabled.
	1	RX_CH9_EN	**Receive Channel Enable** 0: Receive channel 9 is disabled. 1: Receive channel 9 is enabled.
	0	RX_CH8_EN	**Receive Channel Enable** 0: Receive channel 8 is disabled. 1: Receive channel 8 is enabled.

Table 8. TDM Channel Selection for Mono Replay

ADDRESS	BIT	NAME	DESCRIPTION
0x18	7	DMONOMIX_CH1_SOURCE[3:0]	**Digital Monomix Source Selection** 0000: Channel 1 gets PCM RX channel 0. 0001: Channel 1 gets PCM RX channel 1. 0010: Channel 1 gets PCM RX channel 2. 0011: Channel 1 gets PCM RX channel 3. … 1111: Channel 1 gets PCM RX channel 15.
	6		
	5		
	4		
	3	DMONOMIX_CH0_SOURCE[3:0]	**Digital Monomix Source Selection** 0000: Channel 0 gets PCM RX channel 0. 0001: Channel 0 gets PCM RX channel 1. 0010: Channel 0 gets PCM RX channel 2. 0011: Channel 0 gets PCM RX channel 3. … 1111: Channel 0 gets PCM RX channel 15.
	2		
	1		
	0		
0x19	1	DMONOMIX_CFG[1:0]	**Monomix Configuration** 00: Output of Monomix is channel 0. 01: Output of Monomix is channel 1. 10: Output of Monomix is (channel 0 + channel 1)/2. 11: Reserved
	0		

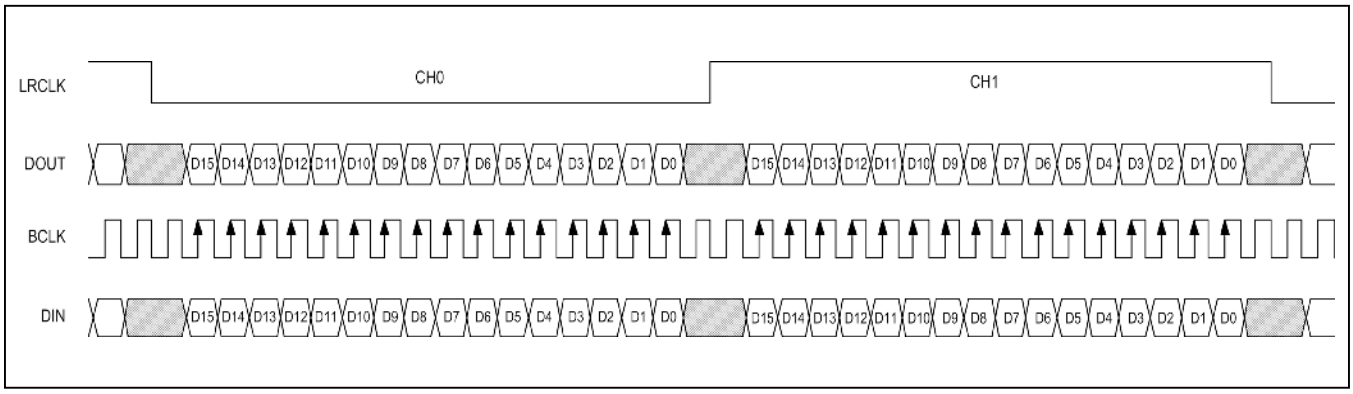


Figure 5. I²S Digital Audio Format Examples

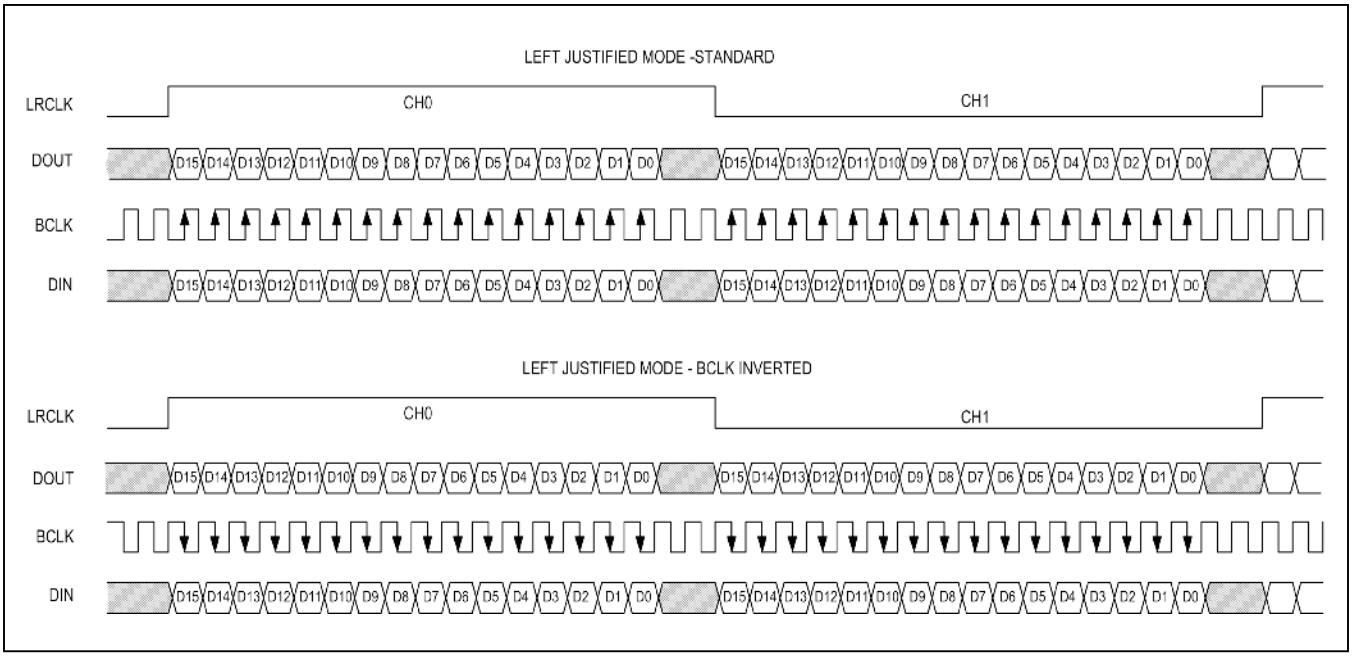


Figure 6. Left-Justified Digital Audio Format Examples

Figure 7. TDM Digital Audio Format Examples

Digital Passband Filtering

The MAX98371 features an optional highpass filter with selectable corner frequency (50Hz, 100Hz, 200Hz, 400Hz, and 800Hz), or a DC blocking filter with a cutoff frequency of 2Hz (80dB attenuation). The MAX98371 supports 5 sample rates: 32kHz, 44.1kHz, 48kHz, 88.2kHz or 96KHz. For 32kHz, 44.1kHz and 48kHz, a linear phase, half-band filter effectively defines the response. For 96kHz operation, a different filter characteristic is employed with a smooth roll off above 20kHz. Set the digital highpass filter corner frequency though the DACHPF bits in control register 0x1C (Table 9). Create user-programmed filtering through the biquad filter coefficients by setting the DACHPF[2:0] bits to 111. See the Biquad Filter section.

The MAX98371 also features a configurable PVDD ADC filter. This cutoff frequency of this filter can be adjusted by setting the PVDD_ADC_BW bits in register 0x1C. These filtered PVDD ADC measurements can be fed to the DHT or limiter. Filtered or unfiltered PVDD ADC readings can be sent to the DHT and limiter. To send filtered data to the limiter or DHT, set the PVDD_FILT_TO_LMTR or PVDD_FILT_TO_DHT bits, respectively. See Table 9.

Table 9. Digital Highpass Filter

ADDRESS	BIT	NAME	DESCRIPTION
0x1C	7	PVDD_FILT_TO_LMTR	0: Unfiltered PVDD ADC measurements are sent to the limiter. 1: Lowpass filtered PVDD ADC measurements are sent to limiter.
	6	PVDD_FILT_TO_DHT	0: Unfiltered PVDD ADC measurements are sent to DHT. 1: Lowpass filtered PVDD ADC measurements are sent to DHT.
	5	PVDD_ADC_BW[1:0]	**PVDD ADC Lowpass Filter Selection** 00: Pass through, filter off 01: 2Hz cutoff 10: 20Hz cutoff 11: 200Hz cutoff
	4		
	3	0	0
	2	DACHPF[2:0]	**Digital Highpass Filter** 000: Pass through, filter off 001: DC blocker is enabled. 010: 50Hz HPF is enabled. 011: 100Hz HPF is enabled. 100: 200Hz HPF is enabled. 101: 400Hz HPF is enabled. 110: 800Hz HPF is enabled. 111: User programmable using DAC_BQ_B[0–2] and DAC_BQ_A[1–2] registers
	1		
	0		

Biquad Filter

The digital biquad filter has five user-programmable coefficients (B0, B1, B2, A1, and A2), and each individual coefficient is 3 bytes (24 bits) long (A0 is fixed at 1). They occupy 15 consecutive registers (Table 10) and each set of three registers (per coefficient) must be programmed consecutively for the settings to take effect. The coefficients are stored using a two's complement format where the first 4 bits are the integer portion and the last 20 bits are the decimal portion that results in an approximate +8 to -8 range for each coefficient.

The digital biquad coefficients are uninitialized at power-up, and if the filter is going to be used, the coefficients must be programmed before the device and biquad filter are enabled. The transfer function is:

$$H(z) = \frac{B_0 + B_1 * Z^{-1} + B_2 * Z^{-2}}{1 + A_1 * Z^{-1} + A_2 * Z^{-2}}$$

Signal Path Delay

Delay through the signal path is minimized by use of efficient signal processing and hardware DSP. Delay is affected by the configuration of various blocks and filters in the signal path. Typical delay, listed in number of audio samples, is shown in Table 11.

Table 10. Biquad Filter Coefficient Registers

REG	REG NAME	R/W	BIT NAME	VALUE
0x1D	Biquad Coefficient B0	R/W	B0[23:16]	0x00
0x1E		R/W	B0[15:8]	0x00
0x1F		R/W	B0[7:0]	0x00
0x20	Biquad Coefficient B1	R/W	B1[23:16]	0x00
0x21		R/W	B1[15:8]	0x00
0x22		R/W	B1[7:0]	0x00
0x23	Biquad Coefficient B2	R/W	B2[23:16]	0x00
0x24		R/W	B2[15:8]	0x00
0x25		R/W	B2[7:0]	0x00
0x26	Biquad Coefficient A1	R/W	A1[23:16]	0x00
0x27		R/W	A1[15:8]	0x00
0x28		R/W	A1[7:0]	0x00
0x29	Biquad Coefficient A2	R/W	A2[23:16]	0x00
0x2A		R/W	A2[15:8]	0x00
0x2B		R/W	A2[7:0]	0x00

Table 11. Signal Path Delay

SAMPLE RATE	DELAY (SAMPLES)
32k	19
44.1k	19
48k	18
88.2k	15
96k	14

PVDD ADC

The PVDD ADC has an effective 8kHz sample rate, 8-bit resolution and full scale input of 18V. The bandwidth of the output is user programmable to reject both high frequency and audio band noise from the supply, and to tradeoff reaction time to follow the supply accurately. The PVDD_ADC values are used to by the DHT and Limiter circuits. These values can be read back over I^2C through the PVDD_ADC Register located at 0x34. See Table 12.

The PVDD ADC readback is real time and is dependant on the "PVDD_ADC_BW" register setting in register 0x1C.

Digital Volume Control

A user-controlled digital volume control with an attenuation range of 0dB to -63dB in 0.5dB steps, as well as a mute setting is available. Volume ramping is available and configurable with through the DVOL_RAMP_BYP bit in the digital volume control register. See Table 13.

Table 12. PVDD Measurement ADC

ADDRESS	BIT	NAME	DESCRIPTION
0x34	7	PVDD_ADC[7:0]	0: 5.35V 1: 5.40V 2: 5.45V 3: 5.50V … 253: 18.05V 254: 18.10V 255: 18.15V
	6		
	5		
	4		
	3		
	2		
	1		
	0		

Table 13. Digital Volume Ramping and Digital Volume

ADDRESS	BIT	NAME	DESCRIPTION
0x2D	7	DVOL_RAMP_BYP	**Digital Volume Ramp Bypass** 0: Ramping is enabled at startup, shutdown and all volume changes. 1: All volume ramping is disabled.
	6	DVOL[6:0]	**Digital Volume Control** 0: 0dB 1: -0.5dB 2: -1.0dB 3: -1.5dB … 125: -62.5dB 126: -63.0dB 127: Digital mute
	5		
	4		
	3		
	2		
	1		
	0		

Output Voltage Scaling

The MAX98371 operates over a large supply voltage range. As a result, the part must be configured to scale the output signals across possible PVDD supply range. SPK_GAIN_MAX applies gain after the DAC to achieve this voltage scaling.

Digital gain can be applied before the DAC by using the DPGA_CLIP register. In conjunction with the SPK_GAIN_MAX setting, the overall full-scale behavior of the device is set.

The DPGA and SPK_GAIN_MAX register settings are shown in Table 14.

Gain through the signal path is referenced to the full-scale output of the DAC, which is 2.1dBV. The MAX98371 output level can be calculated based on the digital input signal level and selected amplifier gain.

Output signal level (dBV) = input signal level (dBFS) + 2.1dBV + SPK_GAIN_MAX (dB)

where 0dBFS is referenced to 0dBV.

Table 14. Digital Gain Settings and Output Voltage Scaling

ADDRESS	BIT	NAME	DESCRIPTION
0x2E	7	DPGA_CLIP[3:0]	**Digital Gain Settings (dB)** 0000: 0 0110: 3.0 0001: 0.5 0111: 3.5 0010: 1.0 1000: 4.0 0011: 1.5 1001: 5.0 0100: 2.0 1010: 6.0 0101: 2.5 1011–1111: 0
	6		
	5		
	4		
	3	SPK_GAIN_MAX[3:0]	**Speaker No-Load Output Voltage Maximum** Sets the output voltage level (V_P) of 0dBFS. 0000: 5.37 (9.5dB) Guaranteed no clipping 0001: 6.03 (10.5dB) Best near 5.5V (min) operating 0010: 6.77 (11.5dB) 0011: 7.59 (12.5dB) 0100: 8.52 (13.5dB) 2-cell Li-ion operation 0101: 9.56 (14.5dB) 0110: 10.72 (15.5dB) 0111: 12.03 (16.5dB) 12V nominal 1000: 13.5 (17.5dB) 3-cell Li-ion operation 1001: 15.15 (18.5dB) 1010: 16.99 (19.5dB) Optimum for 16.5V PVDD operation 1011: 19.07 (20.5dB) 1100–1111: Reserved
	2		
	1		
	0		

Dynamic Headroom Tracking

The MAX98371 features Dynamic Headroom Tracking (DHT) to preserve consistant dynamic range in the presence of a varying supply. DHT maintains consistent volume and listening levels up to a predefined point, below full scale. DHT maintains the headroom of the amplifier at signal peaks that occur above this level (referred to as the rotation point or RP) up to full scale to ensure consistent, smooth compression of these signals in the presence of supply variations.

A key element in tracking available headroom is the PVDD ADC. The output of the ADC feeds the DHT circuitry with the necessary inputs to calculate the amount of compression (if any) applied to signal peaks. Filtering can be applied to the PVDD ADC readings used by the DHT by using the PVDD_FILT_TO_DHT bit (Table 9).

The Dynamic Headroom Tracking function relies heavily on two parameters to be effective. The first is the SPK_GAIN_MAX setting explained in the *Output Voltage Scaling* section. This sets the maximum no-load peak output voltage (V_{MPO}) that the class D amplifier reproduces when fed with a full-scale (0dBFS) signal. The second parameter is the Rotation point (RP). The rotation point sets the level in dBFS above which compression is applied to the output signal, if the PVDD voltage level drops below V_{MPO}.

DHT uses a parameter called SPK_GAIN_MIN to control the maximum compresion ratio. This parameter can enable the addition of a second inflection point on the Transfer fucntion.

The behavior of DHT has 3 modes, depending on the measured value of V_{PVDD} by the PVDD ADC:

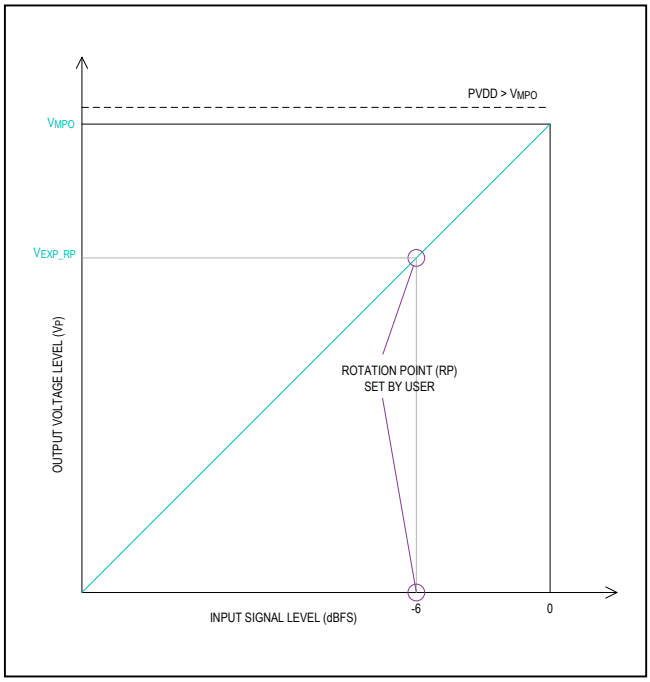


Figure 8. Example of Dynamic Headroom Tracking in Mode 1 Operation

MODE 1: PVDD voltage is greater than maximum peak output voltage. If V_{PVDD} is greater than V_{MPO} then there is no action taken by the DHT block. There is sufficient headroom for the amplifier to linearly represent any signal up to and including 0dBFS; the signal transfer function is unaffected.

MODE 2: V_{PVDD} is less than V_{MPO}, and greater than the output voltage as set by the Rotation Point register setting (V_{EXP_RP}). For example, if the RP is set for -6dBFS, then the peak voltage on the output (V_{EXP_RP}) would be $V_{MPO}/2$). If this is the case, the transfer function for signals below the RP is reproduced exactly as in Mode 1. Any signals between RP and 0dBFS are now subject to an audio compression function, acting in the DSP block of the MAX98371. This acts with appropriate attenuation for peaks over the RP in magnitude with programmable attack and release times (see DHT Ballistics). Figure 9 and 10 show the effect on the transfer function.

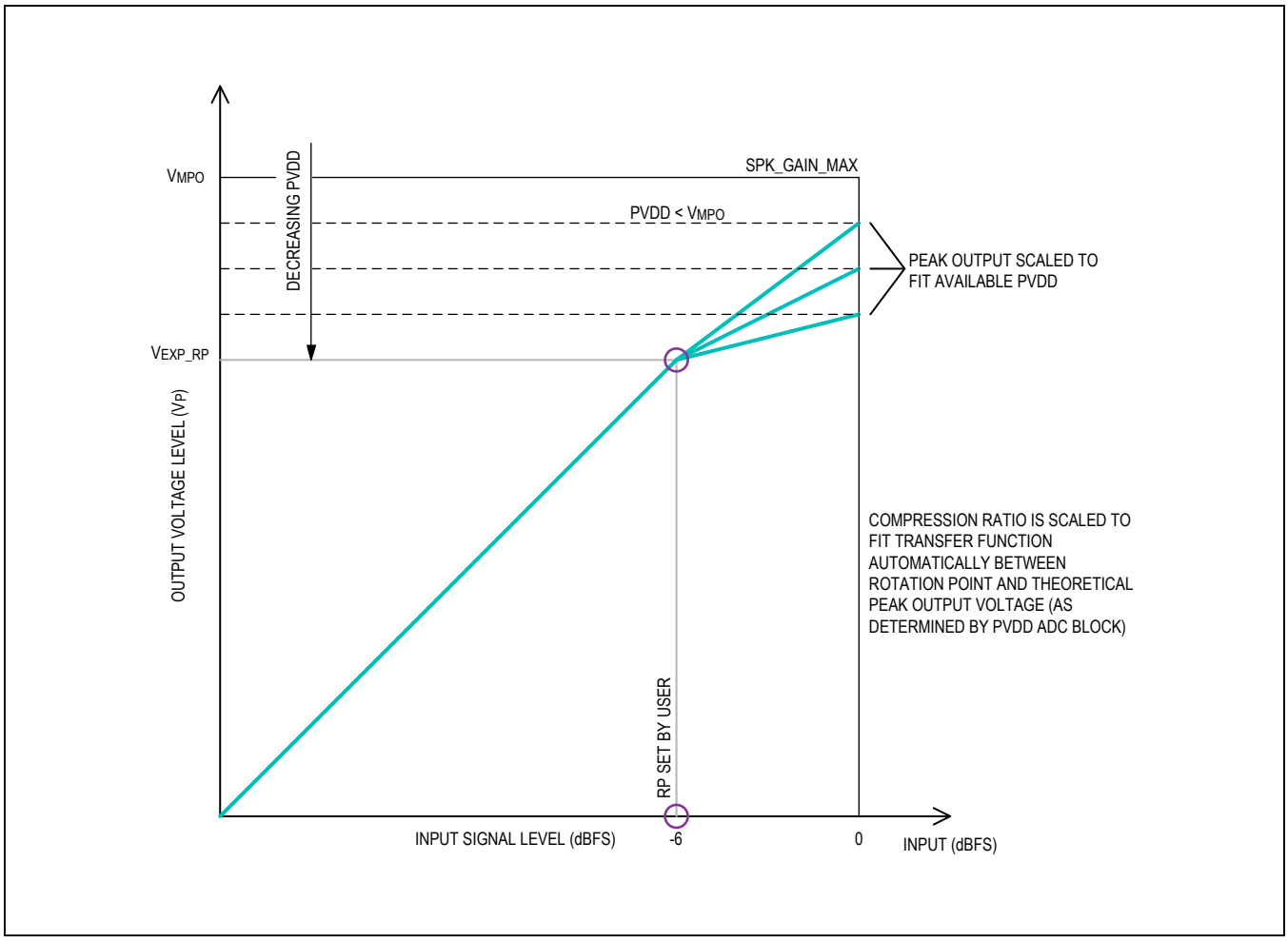


Figure 9. Example of Dynamic Headroom Tracking in Mode 2 Operation with a High RP

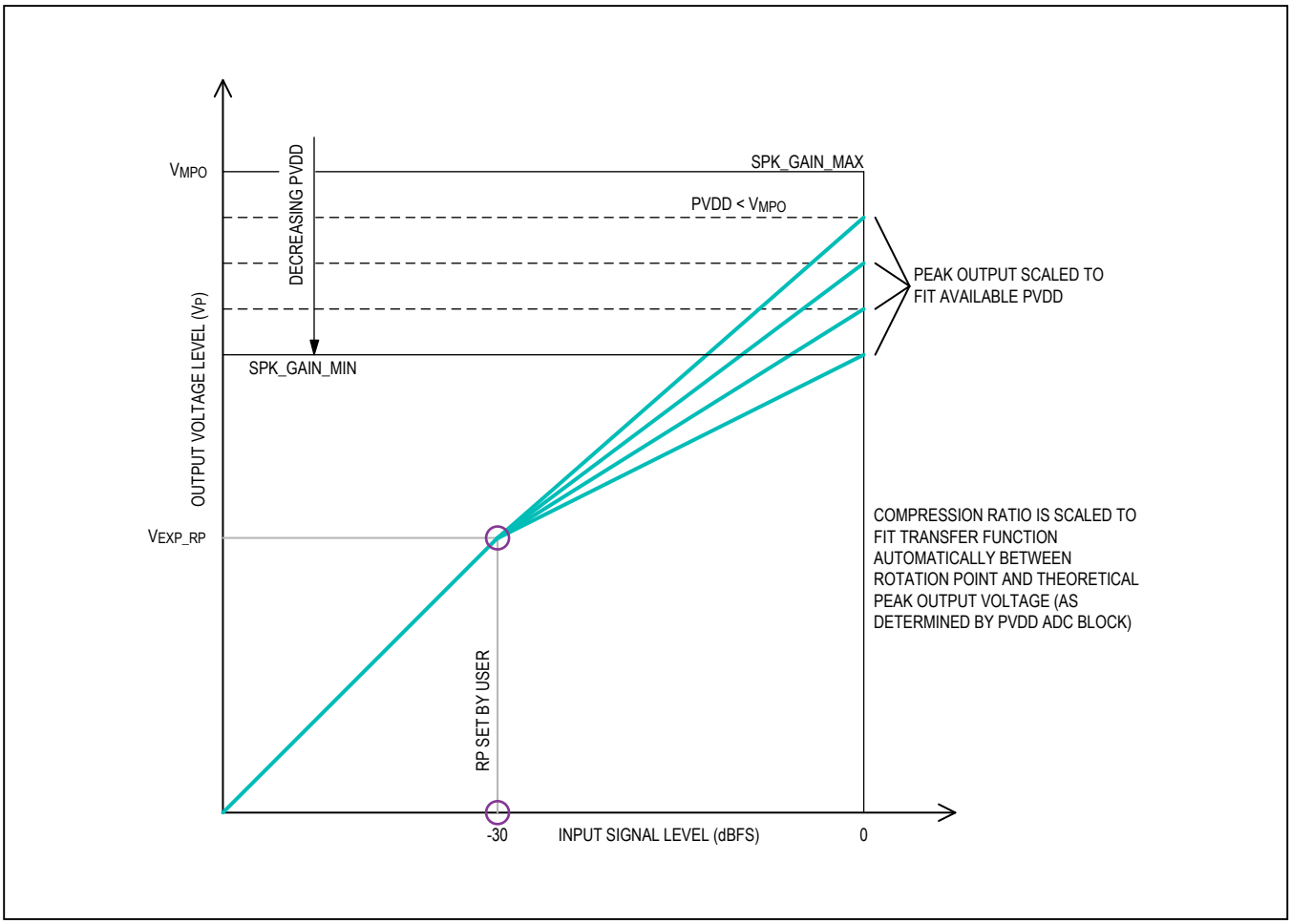


Figure 10. Example of Dynamic Headroom Tracking in Mode 2 Operation with a Low RP

The compression ratios in Mode 2 are effectively defined by the combination of: PVDD, RP, SPK_GAIN_MAX, and SPK_GAIN_MIN settings. The ballistics of the compressor (in both Mode 2 and Mode 3) are set by the parameters in Table 16 and 17.

Table 15. Speaker Gain Minimum Voltage

ADDRESS	BIT	NAME	DESCRIPTION
0x31	7 6 5 4	SPK_GAIN_MIN[3:0]	**Speaker Gain Min (V_P):** 0000: 5.37 (9.5dB) 0001: 6.03 (10.5dB) 0010: 6.77 (11.5dB) 0011: 7.59 (12.5dB) 0100: 8.52 (13.5dB) 0101: 9.56 (14.5dB) 0110: 10.72 (15.5dB) 0111: 12.03 (16.5dB) 1000: 13.5 (17.5dB) 1001: 15.15 (18.5dB) 1010: 16.99 (19.5dB) 1011: 18.0 (20.0dB) 1100–1111: Reserved
	3 2 1 0	DHT_VROT_PNT[3:0]	**DHT Rotation Point (dBFS)** 0000: -0.5 0001: -1 0010: -2 0011: -3 0100: -4 0101: -5 0110: -6 0111: -8 1000: -10 1001: -12 1010: -15 1011: -18 1100: -20 1101: -22 1110: -25 1111: -30

MODE 3a: PVDD voltage is less than the rotation points maximum output voltage, V_{EXP_RP}. When the rotation point is set to a high value (for example -6dBFS) this mode applies. If V_{PVDD} is less than V_{EXP_RP}, then hard limiting is applied to peaks and the effective RP is now set by the need to fit peak signals into the available PVDD range. The MAX98371 automatically determines a new RP based on the PVDD ADC. Normally, RP is set so that this mode is never used, and the V_{EXP_RP} as set by the RP and SPK_GAIN_MAX combination should reflect the lowest PVDD value expected. In this Mode the

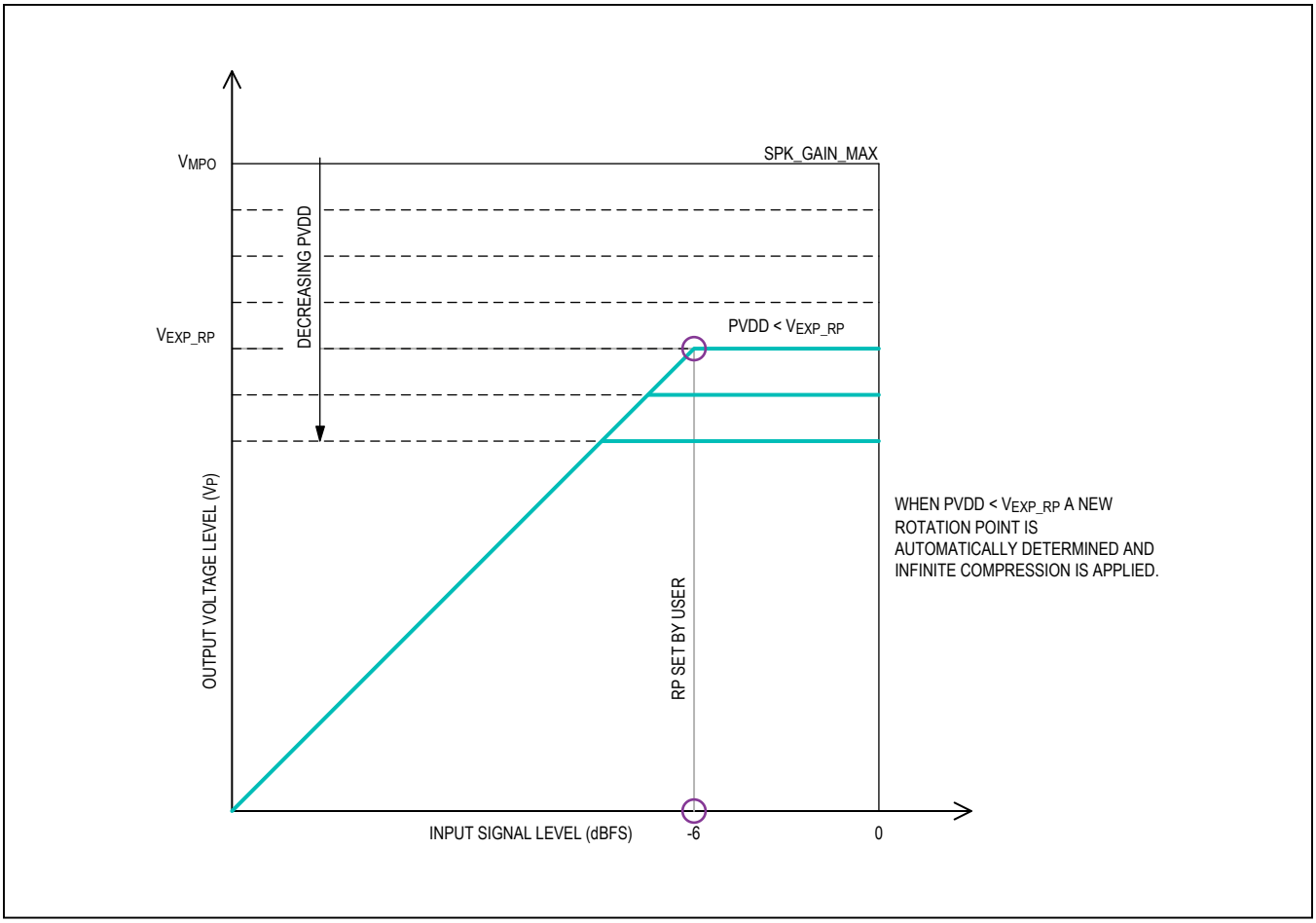


Figure 11. Example of Dynamic Headroom Tracking in Mode 3a Operation

SPK_GAIN_MIN parameter is set to be well below the V_{EXP_RP}.

MODE 3b: PVDD voltage is less than the speaker gain minimum output voltage. When the Rotation Point is set to a low value (for example -30dBFS) this mode applies. If V_{PVDD} is less than SPK_GAIN_MIN, the DHT cannot compress the signal any further. So the compression ratio stays fixed, and as PVDD decreases below SPK_GAIN_MIN, the output signal starts to clip. This clipping can be eliminated if the limiter is enabled in addition to the DHT.

Figures 10 and 12 show an additional parameter, SPK_GAIN_MIN, on the transfer function plots. This parameter is useful when a lower RP is selected. SPK_GAIN_MIN provides a means to create a maximum compression ratio. When the input signal reaches the maximum output voltage that PVDD can provide, the output signal starts to

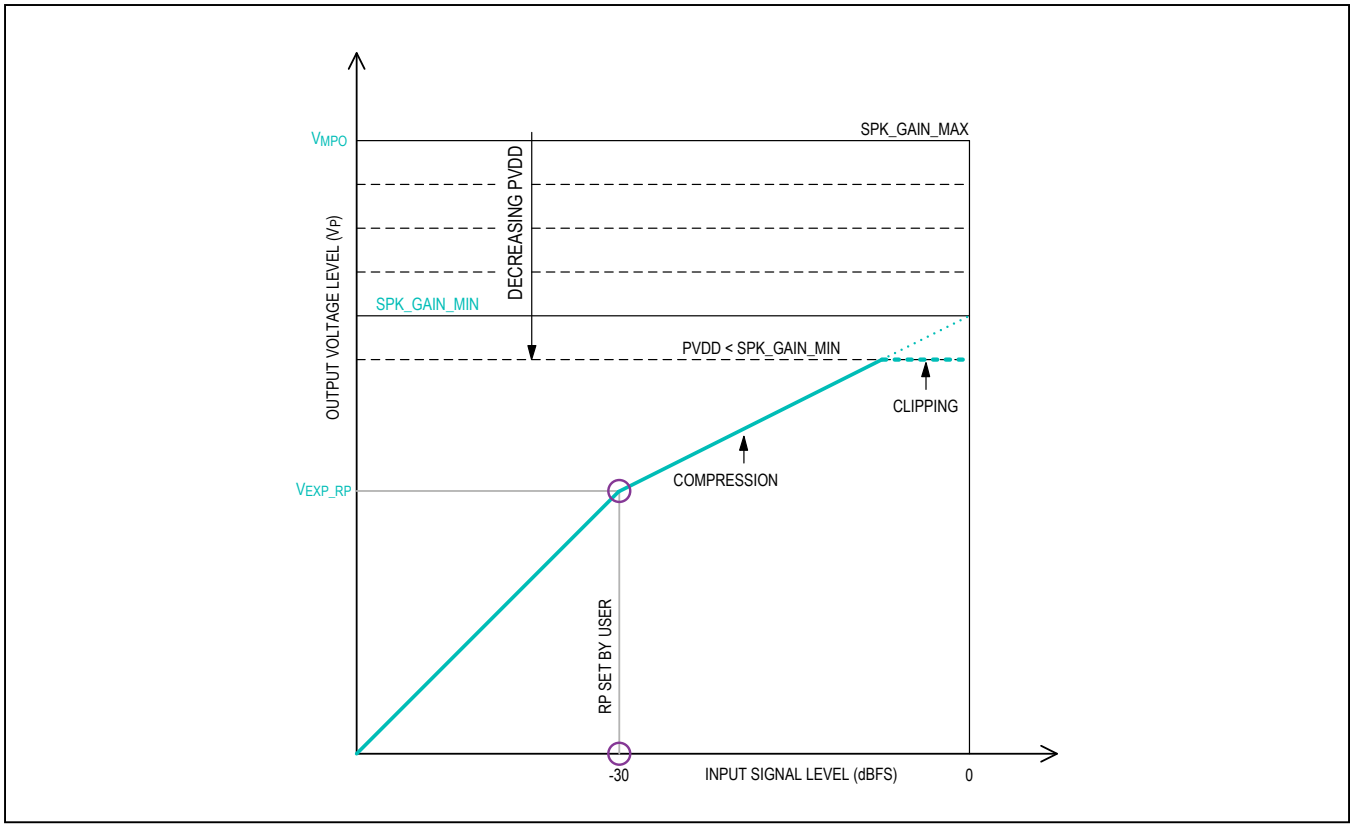


Figure 12. Example of Dynamic Headroom Tracking in Mode 3b Operation

clip (Figure 12). This behavior may not be desirable, but the clipping can be eliminated by enabling the limiter. See Figure 13.

The transfer function shown in Figure 13 is typically preferable to the transfer function shown in Figure 12. When DHT and the limiter are used together, it allows for creation of a second inflection point on the transfer

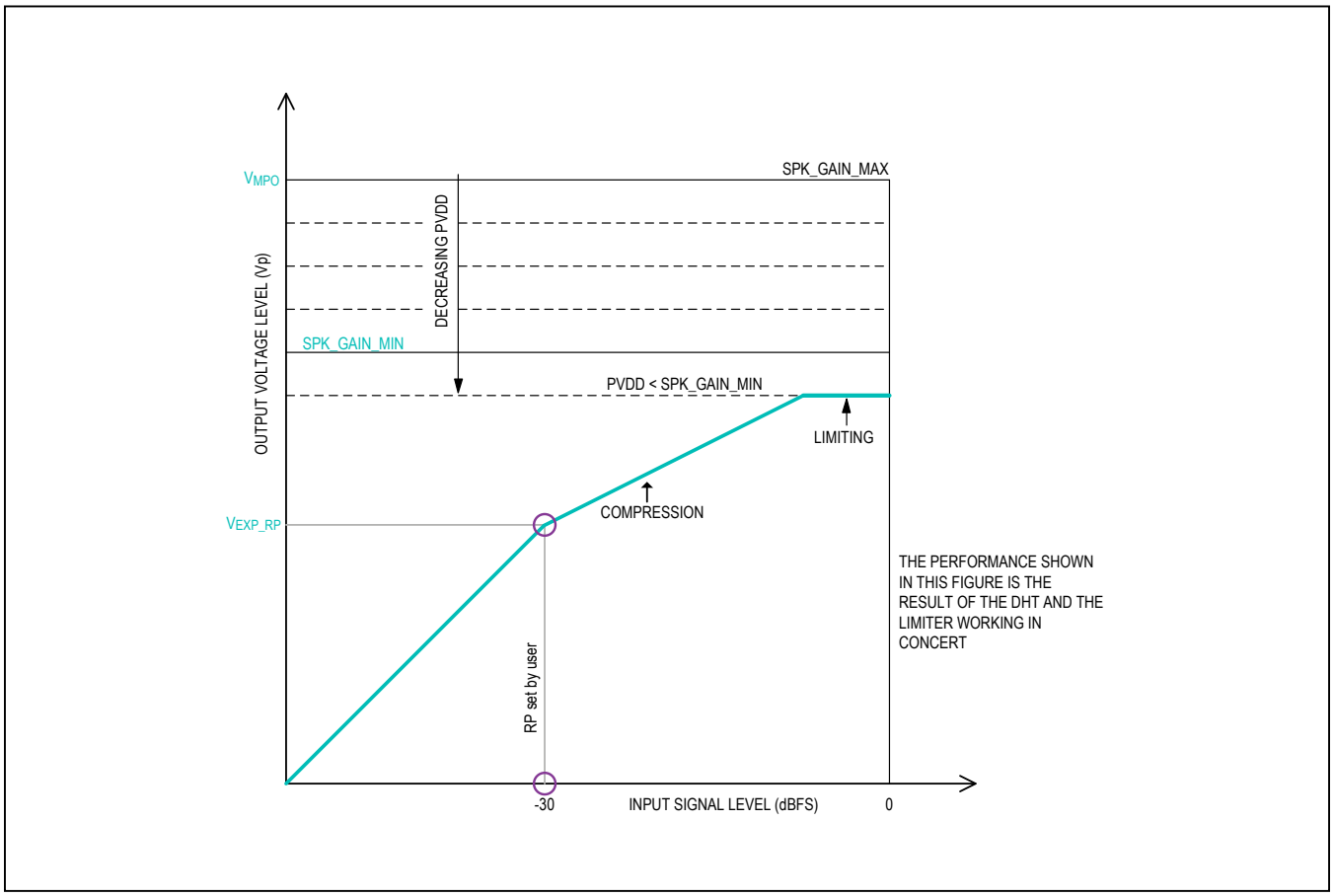


Figure 13. Example of Dynamic Headroom Tracking in Mode 3b with Limiter.

function. This second inflection point reduces the transition from compression to limiting and minimizes the audible impact of signal manipulation by the DHT.

DHT Ballistics

When an input signal exceeds the rotation point, DHT will apply attenuation to the signal over some amount of time (this is configurable by via DHT_ATK_RATE register 0x32). The instant that the large signal is input to the MAX98371 the output will try to reproduce that signal without any attenuation from the DHT. Over time the DHT will apply compression to ensure that the signal can fit within the available PVDD voltage. If a large enough input signal is applied there can be hard clipping on the output for a short time (see Figure 14). However, after the full attack time has completed there should be no clipping. Hard clipping can also be prevented by using the Limiter (see Limiter section).

If you observe the output waveform, you will notice that the amount of attenuation applied increases up to when Vin(dBFS) = PVDD (dBFS). Once Vin(dBFS) is greater than PVDD(dBFS) the amount of attenuation observed in the output waveform appears to decrease. This is a result of the output clipping against the PVDD voltage level. The DHT still takes the same amount of time to apply the compression as though it had the headroom to reproduce the signal.

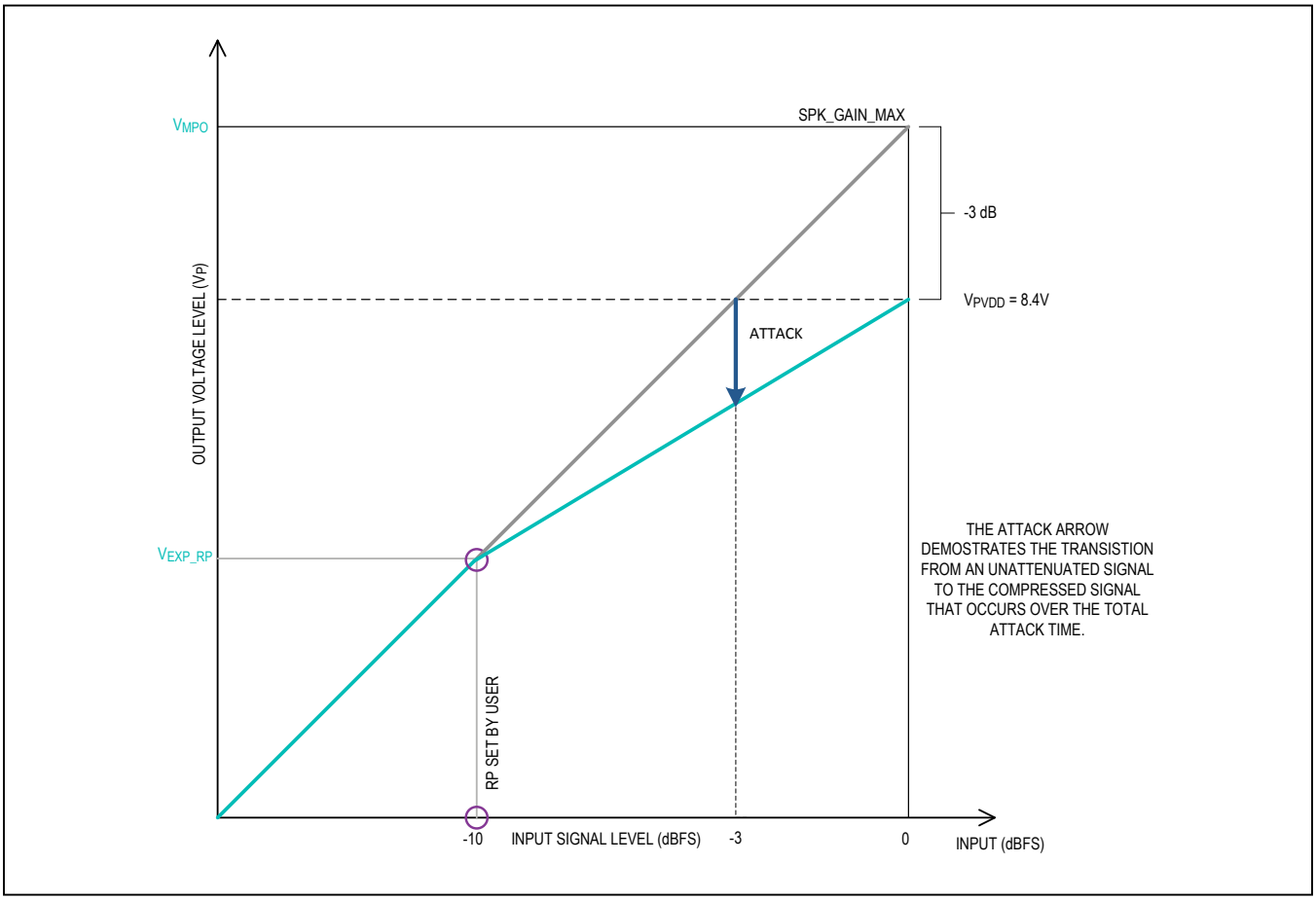


Figure 14. Dynamic Headroom Tracking Attack functionality

The amount of compression applied by DHT depends on a few parameters: SPK_GAIN_MAX, PVDD, Input Signal Amplitude and the Rotation point.

To establish where PVDD is relative to Speaker gain max use the equation 1 below.

$$\text{PVDD(dBFS)} \quad 20\log\left(\frac{\text{PVDD(V)}}{\text{MPO}}\right)$$

Where PVDD(V) is the voltage readback from the PVDD ADC, and VMPO is the maximum peak output voltage (V_{MPO}) see Table 14. For example, if PVDD = 12V and V_{MPO} = 12V then PVDD(dBFS) = 0dBFS. It should be noted that 0dBFS is the maximum value for PVDD(dBFS). If solving Eq 1 returns a value greater than 0 then 0dBFS should be used for further calculations. This is important as DHT only ever applies attenuation and never positive gain.

If PVDD = 8.4V and SPK_GAIN_MAX = 12V then solving Eq 1 gives -3.098dBFS. This is PVDD's level relative to SPK_GAIN_MAX in dB. To find the expected compressed output voltage use equation 2 below.

$$\text{ATTENUATION(dB)} = \text{PVDD(dBFS)} + \text{Input(dBFS)} \times \left(\frac{\text{-PVDD(dBFS)}}{V_{RP}\text{(dBFS)}}\right)$$

When PVDD(dBFS) = 0 we can see that the PVDD and the fraction term drop out which gives Attenuation equals zero. This makes sense because when PVDD(dBFS)= 0 there is sufficient headroom to playback any signal input into the MAX98371 and no compression will be applied.

A non-trivial case might be If PVDD = 8.4V, V_{MPO} = 12V, Rotation Point = -10dBFS and the input signal level is -5dBFS. Next, we solve equation 2 with these values.

$$= \text{PVDD(dBFS)} + \text{Input(dBFS)} \times \left(\frac{\text{-PVDD(dBFS)}}{V_{RP}\text{(dBFS)}}\right)$$

$$= \text{-3.098dBFS} + \text{-5dBFS} \times \left(\frac{\text{3.098dBFS}}{\text{-10dBFS}}\right)$$

$$= \text{-1.54dBFS}$$

For this example the total amount of compression applied by DHT 1.54dB. DHT Attack Rate and DHT Attack Step can be configured to apply the 1.54dB of attenuation of over a programmable amount of time.

As a rule of thumb, attack times (product of attack rate, attack step, and number of steps) faster than 600µs are not achievable. This is independent of sample rate. Input data is rectified, filtered and converted to the log domain. The DSP compares the input data with filtered data from the PVDD ADC then compression is applied within the DSP. The compressed data must be converted back to linear scale and then output. The large number of complex computations required in the DSP requires a fixed 600µs to complete the compression algorithm. As a result, attack times faster than 600µs are not possible. (see Table 16)

Continuing the same example when the Input signal size decreases below the rotation point DHT will release the 1.54dB of attenuation it applied to the signal. The release time for DHT is configurable via Register 0x33. (see Table 17)

Table 16. Dynamic Headroom Tracking Attack Settings

ADDRESS	BIT	NAME	DESCRIPTION
0x32	4	DHT_ATK_STEP[1:0]	**DHT Attack Step Size** 00: 0.25dB 01: 0.5 dB 10: 1.0dB 11: 2.0dB (default)
	3		
	2	DHT_ATK_RATE[2:0]	**DHT Compressor Attack Rate** All attack times in µs/step 000: 17.5 (default) 001: 35 010: 70 011: 140 100: 280 101: 560 110: 1120 111: 2240
	1		
	0		

Table 17. Dynamic Headroom Tracking Release Settings

ADDRESS	BIT	NAME	DESCRIPTION
0x33	4	DHT_REL_STEP[1:0]	**DHT Release Step Size** 00: 0.25dB 01: 0.5dB 10: 1.0dB 11: 2.0dB (default)
	3		
	2	DHT_REL_RATE[2:0]	**DHT Compressor Release Rate** All release times in ms/step 000: 45 (default) 001: 225 010: 450 011: 1150 100: 2250 101: 3100 110: 4500 111: 6750
	1		
	0		

Table 18. Dynamic Gain Enables

ADDRESS	BIT	NAME	DESCRIPTION
0x4B	2	PVADC_EN	0: PVDD ADC is disabled. 1: PVDD ADC is enabled.
	1	LMTR_EN	0: Limiter is disabled. 1: Limiter is enabled.
	0	DHT_EN	0: Dynamic headroom tracking is disabled. 1: Dynamic headroom tracking is enabled.

Table 19. Limiter Threshold Select

ADDRESS	BIT	NAME	DESCRIPTION
0x58	1	LMTR_TH_SEL[1:0]	**Limiter Threshold Select** 00: User-programmable threshold (contents of register 0x59). 01: Threshold is set by SPK_GAIN_MAX. 10–11: Threshold is set by PVDD level.
	0		

Table 20. Manual Limiter Threshold Settings

ADDRESS	BIT	NAME	DESCRIPTION
0x59	4	LMTR_THC[4:0]	**Manual Limiter Threshold Setting (Input Referred)** 00000: 0dBFS 00001: -1dBFS 00010: -2dBFS 00011: -3dBFS … 11101: -29dBFS 11110: -30dBFS 11111: -31dBFS
	3		
	2		
	1		
	0		

Limiter

The MAX98371 features a programmable limiter that is used to compress large near full-scale signals. The input signal level where the attenuation is applied varies based on how the Limiter Threshold Select register is set.

When LMTR_TH_SEL is set to 00, the limiter threshold is user configurable via register LMTR_THC (see Table 20).

When LMTR_TH_SEL is set to 01, the threshold is determined by SPK_GAIN_MAX. Table 21 provides the threshold values.

When LMTR_TH_SEL is set to 10 or 11, the part looks at the PVDD ADC and the SPK_GAIN_MAX setting and determines the maximum output swing that the part can deliver without clipping. Input signals that require more voltage than is available on PVDD are limited to prevent clipping. Filtering can be applied to the PVDD ADC readings used by the limiter with the PVDD_FILT_TO_LMTR bit (Table 9).

The limiter attack and release rates are measured in absolute time and are independent of sample rate. The limiter has its own set of configurable ballistics (Table 22).

Thermal ADC

The MAX98371 features a die temperature monitoring ADC. This 6-bit ADC with a 100kHz sample rate reports the die temperature from 100°C to 163°C. THRM_MIN_TEMP sets the temperature at which the thermal foldback circuit initially activates. The measurements from the thermal ADC can be filtered before they are used by the thermal foldback circuit, or the values can pass directly without being filtered. THRM_FILT_SEL controls the filter selection.

Table 21. Limiter Threshold

SPK_GAIN_MAX SETTING	LMTR_THRESHOLD (dB)
0x0B	0
0x0A	-1
0x09	-2
0x08	-3
…	…
0x01	-10
0x00	-11

Thermal Protection

The MAX98371 continuously monitors die temperature to ensure that the temperature does not exceed the maximum of +150°C (typ). The device can warn the host if die temperature is approaching the limit and shuts down if the limit is exceeded. As the overtemperature limit varies from part to part, the thermal warning thresholds are defined as percentages of the overtemperature limit. Once the device shuts down, it resets all register values except those related to thermal warning and overtemperature interrupt handling. The interrupt registers are maintained to ensure that host is alerted of the overtemperature event. Other registers can become corrupted by the over-temperature event and are reset to prevent unwanted behavior. Once the die temperature drops below +140°C (typ), the device alerts the host through an interrupt, indicating that it is safe to reprogram the device and resume audio playback.

Table 22. Limiter Attack and Release Settings

ADDRESS	BIT	NAME	DESCRIPTION
0x55	5	LMTR_REL_RATE[2:0]	**Limiter Release Time** Total time required for limiter to fully release 000: 15ms 001: 40ms 010: 70ms 011: 160ms 100: 300ms 101: 450ms 110: 600ms 111: 850ms
	4		
	3		
	2	LMTR_ATK_RATE[2:0]	**Limiter Attack Time** Total time required for limiter to fully attack 000 - 100: 160µs 101: 320µs 110: 640µs 111: 1280µs
	1		
	0		

Table 23. Thermal ADC Measurements

ADDRESS	BIT	NAME	DESCRIPTION
0x37	5	THRM_ADC_MEAS[7:0]	0: 100°C 1: 101°C … 62: 162°C 63: 163°C
	4		
	3		
	2		
	1		
	0		
0x38	5	THRM_MIN_TEMP[6:0]	0: 100°C 1: 101°C … 20: 120°C (default) … 39: 139°C 40-63: 140°C
	4		
	3		
	2		
	1		
	0		
0x39	2	THRM_FILT_SEL[2:0]	000: THRM ADC LPF filter on f_C = 0.55kHz 001: THRM ADC LPF filter on f_C = 2.15kHz 010: THRM ADC LPF filter on f_C = 4.55kHz 011: Bypass filter (default) 100: THRM ADC peak detect filter on f_C = 0.55kHz 101: THRM ADC peak detect filter on f_C = 2.15kHz 110: THRM ADC peak detect filter on f_C = 4.55kHz 111: Bypass filter
	1		
	0		

Thermal Foldback

To allow a smoother audio response to high temperature events the MAX97805B features a thermal foldback loop. As the die temperature rises above a threshold of set by THRM_MIN_TEMP register (+120°C by default), the audio path is subjected to increasing attenuation, up to a maximum of -12dB.See Table 23.

The thermal foldback feature can be turned on through the THRM_FB_EN bit, default is off (Table 25). The release rate of the attenuation and the slope of the effect can be set by the user (Table 24), the attack time is fixed at 10µs/dB.

THRM_HOLD controls how long the temperature must stay on one side of the hysteresis threshold. THRM_REL controls the release rate of the attenuation applied by the thermal foldback circuit. THRM_SLOPE controls the amount of attenuation per °C. See Table 24.

Regardless of whether the thermal foldback feature is enabled, the thermal warning bit in the interrupt registers assert and generate an interrupt through the Interrupt Mask register when the +125°C (typ) temperature threshold is crossed.

DOUT Operation and Data format

The MAX98371 features a bidirectional DOUT pin to provide feedback data to the applications processor and other MAX98371s. The data output from DOUT shares the status of amplifier DHT and thermal foldback adjustments. The data format used to frame the data carried on DOUT is the same as the data format of the input data on the DIN pin. The DOUT pin only drives out during the slot assigned to the amplifier by TX_CH#_EN bit. At all other times, the pin is an input (to allow other devices to drive the DOUT signal).

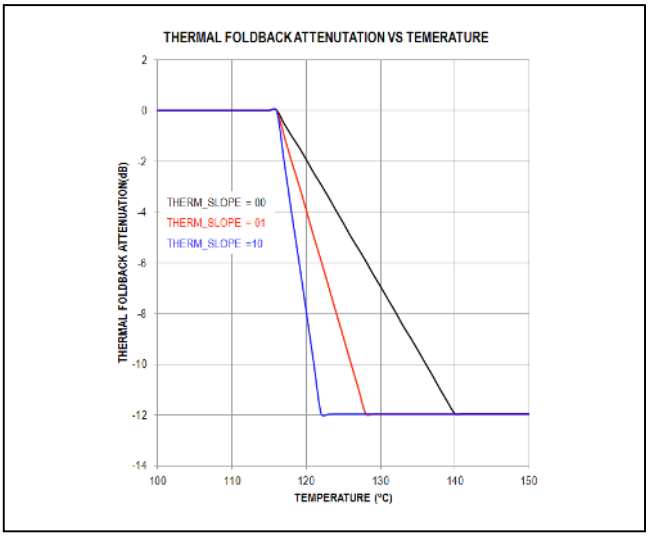


Figure 15. Thermal Foldback performance

Table 24. Thermal Foldback Settings

ADDRESS	BIT	NAME	DESCRIPTION
0x36	7	THRM_HOLD[1:0]	**Thermal Foldback Hold Settings** 00: 0ms 01: 20ms 10: 40ms 11: 80ms (default)
	6		
	5	0	-
	4	0	-
	3	THRM_REL[1:0]	**Thermal Foldback Release Times** 00: 3ms/dB 01: 10ms/dB 10: 100ms/dB 11: 300ms/dB
	2		
	1	THRM_SLOPE[1:0]	**Thermal Foldback Slope Settings** 00: 0.5dB/°C 01: 1.0dB/°C 10: 2.0dB/°C 11: Reserved
	0		

Table 25. Thermal Foldback Enable

ADDRESS	BIT	NAME	DESCRIPTION
0x4C	0	THRM_FB_EN	**Thermal Foldback Enable** 0: Thermal foldback disabled 1: Thermal foldback enabled

The data output on the DOUT pin is structured as shown in Figure 16.

Where DHT_INFO[7:0] contains the DHT attenuation (in dB) and THERM_INFO [5:0] contains the attenuation thermal foldback attenuation broadcast out to other amplifiers on the same bus. It is decoded as shown in Figure 16.

The THRM_LINK_EN and DHT_LINK_EN are intended to be used as the global enables of receive data function of the ICC. It should also be noted that for the ICC to function properly ICC_OC_ENA bit in register 0x5C must be set to 1 so that the overcurrent protection on DOUT is enabled.

Table 26. DHT INFO

VALUE	DECODE (dB)
0	-95.625
1	-95.25
2	-94.875
…	0.375 (steps)
253	-0.750
254	-0.375
255	0

Table 27. THERM INFO

VALUE	DECODE (°C)
0	No thermal adjustment needed
1	+1
2	+2
…	1 (steps)
61	+61
62	+62
63	+63

Note: XX are padding bits and zeros that make up the remaining bits in the rest of the frame.

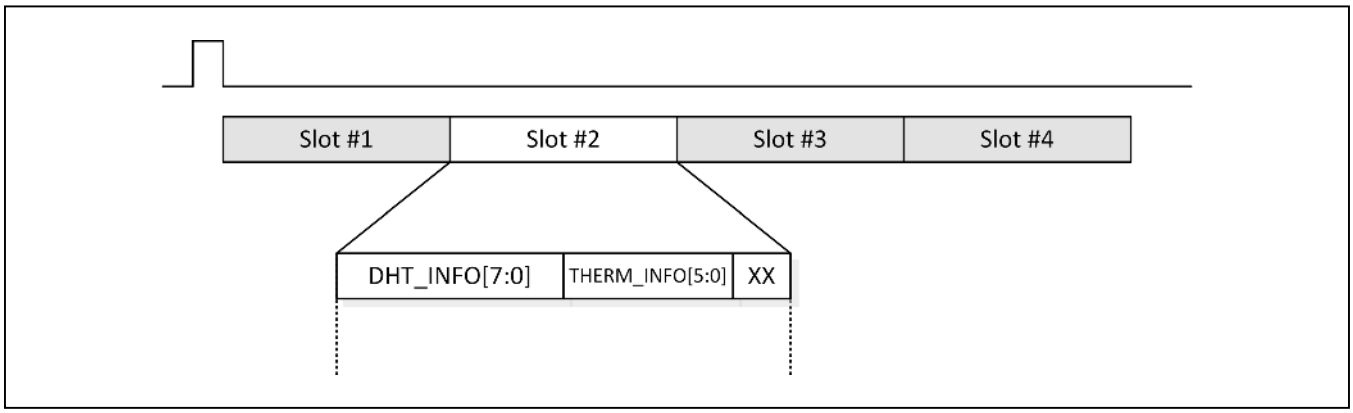


Figure 16. DOUT data structure

Table 28. Thermal and DHT Link Enables

ADDRESS	BIT	NAME	DESCRIPTION
0x4E	1	THRM_LINK_EN	0: Disable THRM link. 1: Enable THRM link.
	0	DHT_LINK_EN	0: Disable DHT link. 1: Enable DHT link.

Interchip Communication

The MAX98371 features an interchip communication (ICC) bus that facilitates synchronized gain adjustments between groups of MAX98371 amplifiers.

Multiamplifier Grouping

By setting registers 0x3A through register 0x3F, it is possible to group MAX98371 amplifiers so that any gain adjustments due to DHT and/or thermal foldback are synchronized.

Each amplifier is configured by a register setting to monitor DOUT during certain slots. The slots selected define to which group each amplifier belongs. Therefore, each amplifier in a group must have the same settings for RX enables. Each individual amplifier must also have only one TX_CH# enable set as well as the corresponding RX_CH# enable.

For example, if we have four amplifiers and we want two groups, then one configuration may be that amplifiers 1 and 3 would belong to one group and amplifiers 2 and 4 belong to another. We can assign amplifier 1 to broadcast on Slot 0 through the TX_CH0_EN bit enable and amplifier 3 to broadcast on Slot 2 through the TX_CH2_EN bit. We would then configure both amplifiers to enable RX enable to listen to both slots 0 and 2, so both amplifiers would have RX_DHT_CH0_EN and RX_DHT_CH2_EN enabled. While this configuration groups the amplifier in the same DHT group, there is another set of grouping registers for thermal foldback. These registers can be configured identically or differently to accommodate the desired behavior. To configure the second group, set amplifier 2 to broadcast on slot 1 through TX_CH1_EN and set amplifier 4 to broadcast on slot 3 through TX_CH3_EN. Then configure both amplifiers to enable RX enable to listen to both slots 1 and 3, so both amps would have RX_DHT_CH1_EN and RX_DHT_CH3_EN enabled.

By definition, the minimum size of a group is two amplifiers, so the maximum number of groups that is supported is eight. A group can contain as many as 16 amplifiers, but then only one group is supported.

It is a requirement of the host processor to ensure that the RX register bits are set to the same values across all amplifiers intended to be used in a group. Devices in the same DHT group must also be configured with the same DHT parameters (SPK_GAIN_MAX, RP, and Ballistics) to achieve a balanced response across the group. The same is true of the THERM group.

Table 29. InterChip Communication Configuration

ADDRESS	BIT	NAME	DESCRIPTION
0x5C	6	ICC_OC_ENA	0: Disable overcurrent protection on DOUT. 1: Enable overcurrent protection on DOUT.
	5	ICC_DOUTEN_EXTFF	0: Disable faster drive enable of the DOUT. 1: Enable faster drive enable of the DOUT for the ICC with BCLK rate greater than 12.288MHz.
	4	ICC_DOUT_EXTFF	0: Disable faster drive of the DOUT. 1: Enable faster drive of the DOUT for the ICC with BCLK rate greater than 12.288MHz.
	3	ICC_PAD_CTRL[3:0]	**DOUT Drive Strength Control** 0000: 1 (default) 0001 and 0010: 7/8 0011 and 0100: 3/4 0101 and 0110: 5/8 0111 and 1000: 1/2 1001 and 1010: 3/8 1011 and 1100: 1/4 1101: 1/8 1110: 1/8 with Miller slew rate reduction (Improves EMI) 1111: off
	2		
	1		
	0		

Double Data Drive

If the shared DOUT trace has a high capacitance that needs to be driven at high speed then the double-data drive feature can be used. This gives a longer drive time for each device.

When the BCLK is less than or equal to 25MHz, DOUT can be clocked with standard clocking: data changes on the falling edge and is valid on the rising edge of each BCLK (Table 30).

When the BCLK is greater than 25MHz, DOUT should be clocked using a double-data drive method: data changes on the falling edge and is valid on the second rising edge.

In this way, the DOUT data transfer rate is effectively half of the BCLK speed. This is accomplished by setting DRIVE_MODE = 1.

This has implications for the supported slot lengths. When double-data drive is enabled, only 32-bit slot lengths are permitted.

Additional MAX98371 devices correctly interpret the double-data drive format (if enabled). Any other attached hardware, such as an applications processor, which is expecting standard timing, needs to ensure that it omits away the information captured on the nonvalid rising edge each time and reconstruct the samples accordingly.

Table 30. DOUT Double Data Drive Mode

ADDRESS	BIT	NAME	DESCRIPTION
0x40	3	DRIVE_MODE	0: Single data drive (default) 1: Double data drive

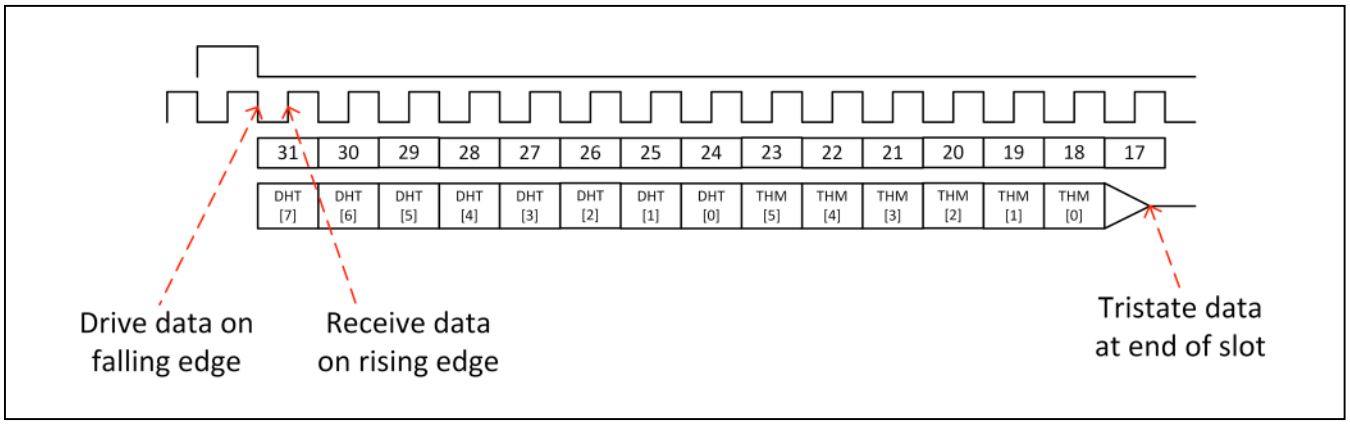


Figure 17. Single Data Drive

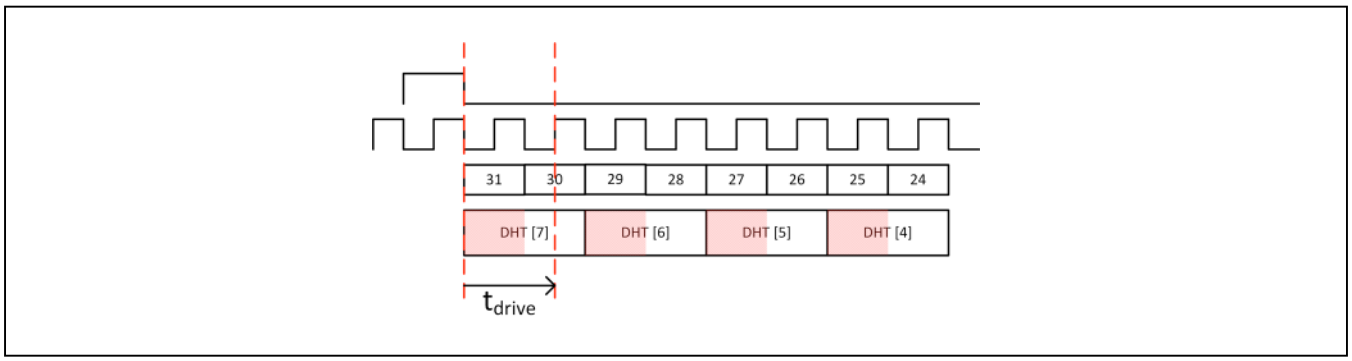


Figure 18. Double Data Drive illustration

Table 31. DOUT DHT Receive Channel Configuration

ADDRESS	BIT	NAME	DESCRIPTION
0x3A	7	RXDHT_CH7_EN	0: DHT receive channel 7 is disabled. 1: DHT receive channel 7 is enabled.
	6	RXDHT_CH6_EN	0: DHT receive channel 6 is disabled. 1: DHT receive channel 6 is enabled.
	5	RXDHT_CH5_EN	0: DHT receive channel 5 is disabled. 1: DHT receive channel 5 is enabled.
	4	RXDHT_CH4_EN	0: DHT receive channel 4 is disabled. 1: DHT receive channel 4 is enabled.
	3	RXDHT_CH3_EN	0: DHT receive channel 3 is disabled. 1: DHT receive channel 3 is enabled.
	2	RXDHT_CH2_EN	0: DHT receive channel 2 is disabled. 1: DHT receive channel 2 is enabled.
	1	RXDHT_CH1_EN	0: DHT receive channel 1 is disabled. 1: DHT receive channel 1 is enabled.
	0	RXDHT_CH0_EN	0: DHT receive channel 0 is disabled. 1: DHT receive channel 0 is enabled.
0x3B	7	RXDHT_CH15_EN	0: DHT receive channel 15 is disabled. 1: DHT receive channel 15 is enabled.
	6	RXDHT_CH14_EN	0: DHT receive channel 14 is disabled. 1: DHT receive channel 14 is enabled.
	5	RXDHT_CH13_EN	0: DHT receive channel 13 is disabled. 1: DHT receive channel 13 is enabled.
	4	RXDHT_CH12_EN	0: DHT receive channel 12 is disabled. 1: DHT receive channel 12 is enabled.
	3	RXDHT_CH11_EN	0: DHT receive channel 11 is disabled. 1: DHT receive channel 11 is enabled.
	2	RXDHT_CH10_EN	0: DHT receive channel 10 is disabled. 1: DHT receive channel 10 is enabled.
	1	RXDHT_CH9_EN	0: DHT receive channel 9 is disabled. 1: DHT receive channel 9 is enabled.
	0	RXDHT_CH8_EN	0: DHT receive channel 8 is disabled. 1: DHT receive channel 8 is enabled.

Table 32. DOUT Thermal Foldback Receive Channel Configuration

ADDRESS	BIT	NAME	DESCRIPTION
0x3C	7	RXTHM_CH7_EN	0: THRM FB receive channel 7 is disabled. 1: THRM FB receive channel 7 is enabled.
	6	RXTHM_CH6_EN	0: THRM FB receive channel 6 is disabled. 1: THRM FB receive channel 6 is enabled.
	5	RXTHM_CH5_EN	0: THRM FB receive channel 5 is disabled. 1: THRM FB receive channel 5 is enabled.
	4	RXTHM_CH4_EN	0: THRM FB receive channel 4 is disabled. 1: THRM FB receive channel 4 is enabled.
	3	RXTHM_CH3_EN	0: THRM FB receive channel 3 is disabled. 1: THRM FB receive channel 3 is enabled.
	2	RXTHM_CH2_EN	0: THRM FB receive channel 2 is disabled. 1: THRM FB receive channel 2 is enabled.
	1	RXTHM_CH1_EN	0: THRM FB receive channel 1 is disabled. 1: THRM FB receive channel 1 is enabled.
	0	RXTHM_CH0_EN	0: THRM FB receive channel 0 is disabled. 1: THRM FB receive channel 0 is enabled.
0x3D	7	RXTHM_CH15_EN	0: THRM FB receive channel 15 is disabled. 1: THRM FB receive channel 15 is enabled.
	6	RXTHM_CH14_EN	0: THRM FB receive channel 14 is disabled. 1: THRM FB receive channel 14 is enabled.
	5	RXTHM_CH13_EN	0: THRM FB receive channel 13 is disabled. 1: THRM FB receive channel 13 is enabled.
	4	RXTHM_CH12_EN	0: THRM FB receive channel 12 is disabled. 1: THRM FB receive channel 12 is enabled.
	3	RXTHM_CH11_EN	0: THRM FB receive channel 11 is disabled. 1: THRM FB receive channel 11 is enabled.
	2	RXTHM_CH10_EN	0: THRM FB receive channel 10 is disabled. 1: THRM FB receive channel 10 is enabled.
	1	RXTHM_CH9_EN	0: THRM FB receive channel 9 is disabled. 1: THRM FB receive channel 9 is enabled.
	0	RXTHM_CH8_EN	0: THRM FB receive channel 8 is disabled. 1: THRM FB receive channel 8 is enabled.

Table 33. DOUT Thermal Foldback Receive Channel Configuration

ADDRESS	BIT	NAME	DESCRIPTION
0x3E	7	TX_CH7_EN	0: Transmit channel 7 is disabled. 1: Transmit channel 7 is enabled.
	6	TX_CH6_EN	0: Transmit channel 6 is disabled. 1: Transmit channel 6 is enabled.
	5	TX_CH5_EN	0: Transmit channel 5 is disabled. 1: Transmit channel 5 is enabled.
	4	TX_CH4_EN	0: Transmit channel 4 is disabled. 1: Transmit channel 4 is enabled.
	3	TX_CH3_EN	0: Transmit channel 3 is disabled. 1: Transmit channel 3 is enabled.
	2	TX_CH2_EN	0: Transmit channel 2 is disabled. 1: Transmit channel 2 is enabled.
	1	TX_CH1_EN	0: Transmit channel 1 is disabled. 1: Transmit channel 1 is enabled.
	0	TX_CH0_EN	0: Transmit channel 0 is disabled. 1: Transmit channel 0 is enabled.
0x3F	7	TX_CH15_EN	0: Transmit channel 15 is disabled. 1: Transmit channel 15 is enabled.
	6	TX_CH14_EN	0: Transmit channel 14 is disabled. 1: Transmit channel 14 is enabled.
	5	TX_CH13_EN	0: Transmit channel 13 is disabled. 1: Transmit channel 13 is enabled.
	4	TX_CH12_EN	0: Transmit channel 12 is disabled. 1: Transmit channel 12 is enabled.
	3	TX_CH11_EN	0: Transmit channel 11 is disabled. 1: Transmit channel 11 is enabled.
	2	TX_CH10_EN	0: Transmit channel 10 is disabled. 1: Transmit channel 10 is enabled.
	1	TX_CH9_EN	0: Transmit channel 9 is disabled. 1: Transmit channel 9 is enabled.
	0	TX_CH8_EN	0: Transmit channel 8 is disabled. 1: Transmit channel 8 is enabled.

Table 34. Extra BCLK Cycle Configuration

ADDRESS	BIT	NAME	DESCRIPTION
0x41	1	TX_EXTRA_HIZ	0: Extra BCLK cycles are driven to zero. 1: Extra BCLK cycles are driven to high impedance.

Table 35. Manual HIZ Mode Configuration

ADDRESS	BIT	NAME	DESCRIPTION
0x42	7	TX_CH7_HIZ	0: Transmit Channel 7 outputs data/zeros. 1: Transmit Channel 7 outputs high impedance.
	6	TX_CH6_HIZ	0: Transmit Channel 6 outputs data/zeros. 1: Transmit Channel 6 outputs high impedance.
	5	TX_CH5_HIZ	0: Transmit Channel 5 outputs data/zeros. 1: Transmit Channel 5 outputs high impedance.
	4	TX_CH4_HIZ	0: Transmit Channel 4 outputs data/zeros. 1: Transmit Channel 4 is enabled.
	3	TX_CH3_HIZ	0: Transmit Channel 3 outputs data/zeros. 1: Transmit Channel 3 outputs high impedance.
	2	TX_CH2_HIZ	0: Transmit Channel 2 outputs data/zeros. 1: Transmit Channel 2 outputs high impedance.
	1	TX_CH1_HIZ	0: Transmit Channel 1 outputs data/zeros. 1: Transmit Channel 1 outputs high impedance.
	0	TX_CH0_HIZ	0: Transmit Channel 0 outputs data/zeros. 1: Transmit Channel 0 outputs high impedance.
0x43	7	TX_CH15_HIZ	0: Transmit Channel 15 outputs data/zeros. 1: Transmit Channel 15 outputs high impedance.
	6	TX_CH14_HIZ	0: Transmit Channel 14 outputs data/zeros. 1: Transmit Channel 14 outputs high impedance.
	5	TX_CH13_HIZ	0: Transmit Channel 13 outputs data/zeros. 1: Transmit Channel 13 outputs high impedance.
	4	TX_CH12_HIZ	0: Transmit Channel 12 outputs data/zeros. 1: Transmit Channel 12 outputs high impedance.
	3	TX_CH11_HIZ	0: Transmit Channel 11 outputs data/zeros. 1: Transmit Channel 11 outputs high impedance.
	2	TX_CH10_HIZ	0: Transmit Channel 10 outputs data/zeros. 1: Transmit Channel 10 outputs high impedance.
	1	TX_CH9_HIZ	0: Transmit Channel 9 outputs data/zeros. 1: Transmit Channel 9 outputs high impedance.
	0	TX_CH8_HIZ	0: Transmit Channel 8 outputs data/zeros. 1: Transmit Channel 8 outputs high impedance.

Table 36. Speaker Configuration

ADDRESS	BIT	NAME	DESCRIPTION
0x4A	7	SPK_SWCLK	**Class D output Switching Frequency Select** 0: Speaker switching frequency is set to 472kHz. 1: Speaker switching frequency is set to 330kHz.
	6	—	—
	5	—	—
	4	—	—
	3	SPK_EDGE[1:0]	**Programmable Speaker Edge Rate Control** 00: Nominal edge rate 01: +15% faster edge rate 10: -40% slower edge rate 11: -20% slower edge eate
	2		
	1	—	—
	0	SPK_EN	**Speaker amplifier Enable** 0: Speaker amplifier is disabled (default). 1: Enable

Class D Output Stage

The MAX98371 Class D output stage with Active Emissions Limiting (AEL) provides optimum suppression and control of output switching harmonics that most directly contribute to EMI and radiated emissions. Programmable speaker edge rate control is available to help tweak EMI performance. As the edge rate increases the efficiency goes up slightly, and as the edge rate slows the efficiency goes down. Set the speaker edge rate with bits SPK_EDGE bits in register 0x4A.

The default Class D output switching frequency is 472kHz for the best THD performance. To trade off THD performance for higher efficiency the output switching frequency can be set to 330kHz by setting SPK_SWCLK to 1.

To achieve the lower power consumption the output switching of the Class D amplifier the part can be disabled through the SPK_EN bit. See Table 36 for speaker configuration.

Ultra-Low EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters, or shielding, to meet electromagnetic-interference (EMI) regulation standards. The active emissions limiting edge-rate control circuitry reduce EMI emissions so that with 18in of speaker cable the MAX98371 passes the EN55022B standard without the need for external filtering components.

V_{DVDD} and V_{PVDD} UVLO

The MAX98371 monitors both DVDD and PVDD for low voltage conditions that would prevent the speaker amplifier from operating normally. If the voltage on DVDD drops below the DVDD-UVLO threshold ($V_{DVDD-UVLO}$), the device is placed in hardware shutdown. All the I^2C internal registers reset to their default values. The device can be commanded to leave this state through the I^2C command if the voltage on DVDD later exceeds the $V_{DVDD-UVLO}$ threshold.

If the voltage PVDD drops below the PVDD-UVLO threshold, the audio output is muted to prevent the PVDD supply from being used by the amplifier. If the voltage on PVDD later exceeds the $V_{PVDD-UVLO}$ threshold, the device can be commanded to unmute through the I^2C command.

Click-and-Pop Suppression

The MAX98371 speaker amplifier features Maxim's comprehensive click-and-pop suppression. During power-up and power-down, the click-and-pop suppression circuitry reduces any audible transient sources internal to the device.

At startup, the PGA gain is automatically ramped from mute to the desired setting at a rate of 200µs/dB. Similarly, the gain is ramped down to mute at shutdown at the same rate. For faster startup and shutdown, disable gain ramping.

During normal operation, any requested gain changes are ramped from the old value to the new value at a value determined by the ballistics within the volume control block.

Amplifier Current Limit

The MAX98371 features current limit protection that protects the device against shorts. If the output current of the speaker amplifier exceeds the current limit (6A typ) the IC disables the outputs for approximately 100µs. After 100ms, the outputs are reenabled. If the fault condition still exists, the IC continues to disable and re-enable the outputs until the fault condition is removed. Set OVC_SEL low to disable this behavior (see Table 37). The current limit protects against both high current and short-circuit events.

Thermal Shutdown Recovery

When the temperate of the die exceeds +150°C, the part enters thermal shutdown. However, the MAX98371 features a configurable thermal shutdown autorecovery mode. When the die temperate has decreased by 30°C from the thermal shutdown event, the MAX98371 attempts to resume the previous operating state. Set TSHDN_AUTO_RESTART high to enable auto recovery mode. (See Table 37)

Output Sensing When Using Ferrites

The MAX98371 features two remote sensing pins OUTN_SNS and OUTP_SNS. Remotely sensing the voltage at the load provides a THD+N advantage over sensing at the DUT output when ferrite beads are used. (see Figure 20) The remote sense lines connect the output signal at the load to the inverting terminal of the internal error amplifier of the Class D. (see Figure 19) Ferrites are highly nonlinear so sensing at the load versus at the output pins ensures that any signal degradation caused by the filtering components is appropriately compensated.

However, in many applications, there may not be a need to filter the output with a Ferrite bead.

Clocking Architecture

The MAX98371 includes a flexible clocking architecture and operation with no MCLK input.

A configurable internal clock monitor circuit monitors the internal clock source (BCLK) and automatically places the device in software shutdown if the clock source is removed. Set CMON_ENA high to enable the clock monitor. This prevents unwanted signals from being applied to the speaker during a fault condition. When CMON_AUOT_RESTART is high the device will automatically return to normal operatrion when the clock source is subsequently reapplied. (See Table 37)

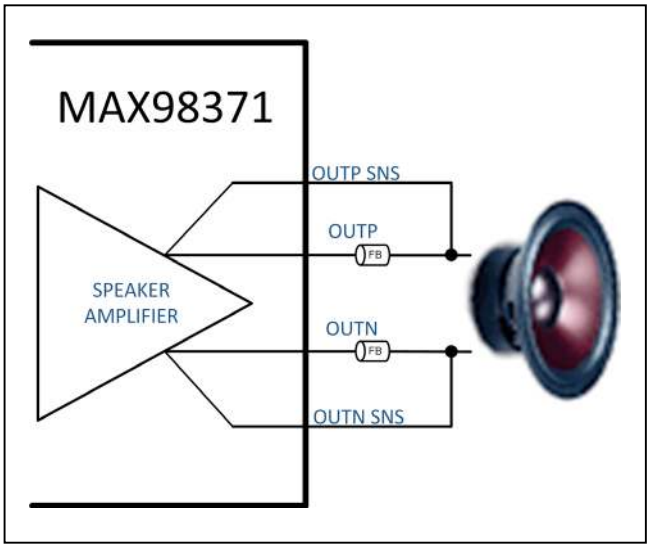


Figure 19. Typical Application Circuit with Ferrites Beads Used

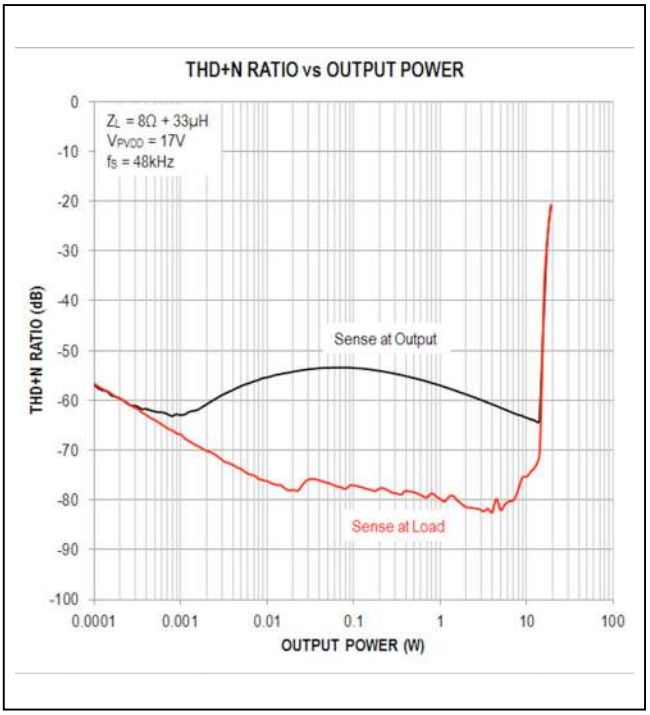


Figure 20 .THD Performance Improvement Enabled by Remote Sensing

Reset

The MAX98371 features an active-low hardware reset. When the voltage-on reset is pulled low, the part enters global shutdown. To reenable the part the reset pin must be pulled high and a global enable I²C command must be issued.

Hardware Reset

When the reset pin is pulled low, the device is in its lowest power-down state and communication over I²C is not possible. After exiting reset mode, all registers are set to their default POR values.

Also, if DVDD is removed while PVDD is still applied, the device goes into a hardware shutdown mode and communication through I²C is not possible.

Software Reset

Write 1 to bit 0 of register 0x51 to trigger a software reset. Software reset is used to return most registers to their default (POR) states. Biquad equalizer coefficients are not reset.

The software reset register is a write only register. As a result, a read of this register always returns 0x00. Writing logic-high to RST triggers a software register reset, while writing a logic-low to RST has no effect.

Also if PVDD is removed while DVDD is still applied the device goes into software shutdown mode where all blocks are disabled except I²C control block.

Table 37. Clock Monitor Configuration

ADDRESS	BIT	NAME	DESCRIPTION
0x4D	3	CMON_AUTO_RESTART	0: Device does not restart after a clock monitor event. 1: Device restarts automatically when BCLK is restarted.
	2	CMON_ENA	0: Clock monitor is disabled (default). 1: Clock monitor is enabled.
	1	OVC_SEL	0: Current limit recovery is in manual mode. 1: Current limit recovery is in auto recover mode.
	0	TSDHN_AUTO_RESTART	0: Thermal-protection recovery is in manual mode. 1: Thermal-protection recovery is in auto recover mode.

Table 38. Reset Register

ADDRESS	BIT	NAME	DESCRIPTION
0x51	0	RST	**Reset** 0: No action is taken. 1: Reset. All registers return to their POR (default) values.

Table 39. Global Enable Register

ADDRESS	BIT	NAME	DESCRIPTION
0x50	0	EN	**Global Enable:** 0: Disabled 1: Enabled

I²C Serial Interface

The MAX98371 features an I²C 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the IC and the master at clock rates up to 400kHz. Figure 21 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the IC by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the IC is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the IC transmits the proper slave address followed by a series of nine SCL pulses. The IC transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the IC from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 21). A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early Stop Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the IC the seven most significant bits are programmable through the ADDR1 and ADDR0 bumps. Setting the read/write bit to 1 configures the IC for read mode. Setting the read/write bit to 0 configures the IC for write mode. The slave address is the first byte of information sent to the IC after the START condition.

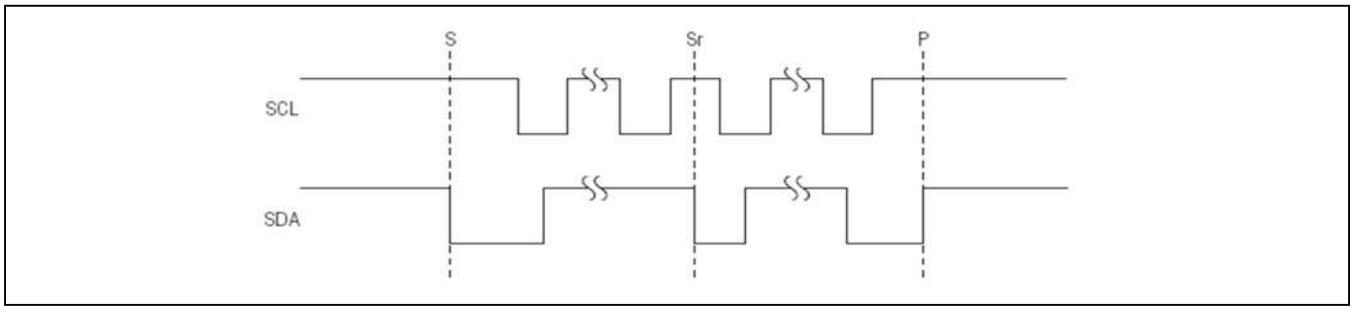


Figure 21. START, STOP, and REPEATED START Conditions

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the IC uses to handshake receipt each byte of data when in write mode (Figure 22). The IC pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master reattempts communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the IC is in read mode.

An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the IC, followed by a STOP condition.

Write Data Format

A write to the IC includes transmission of a START condition, the slave address with the R/W bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 23 illustrates the proper frame format for writing one byte of data to the IC. Figure 24 illustrates the frame format for writing n-bytes of data to the IC.

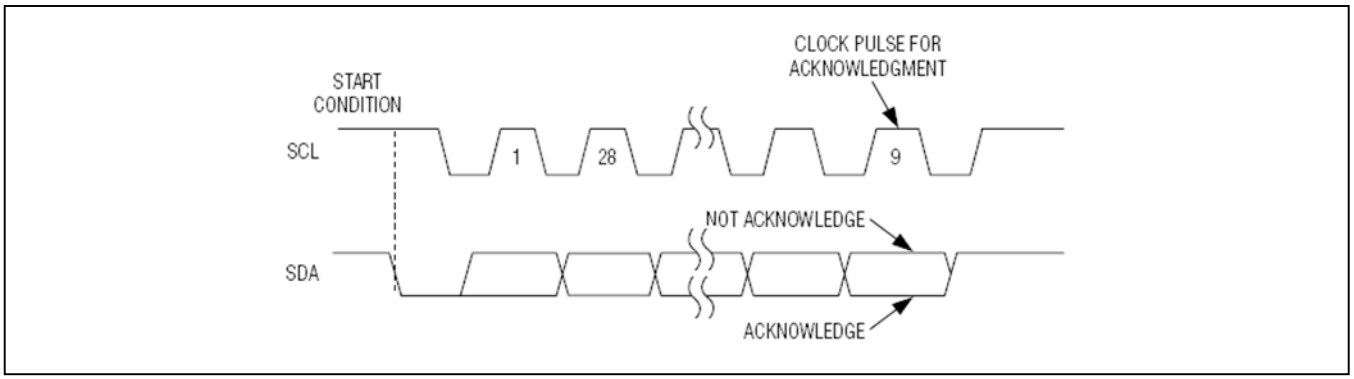


Figure 22. Acknowledge

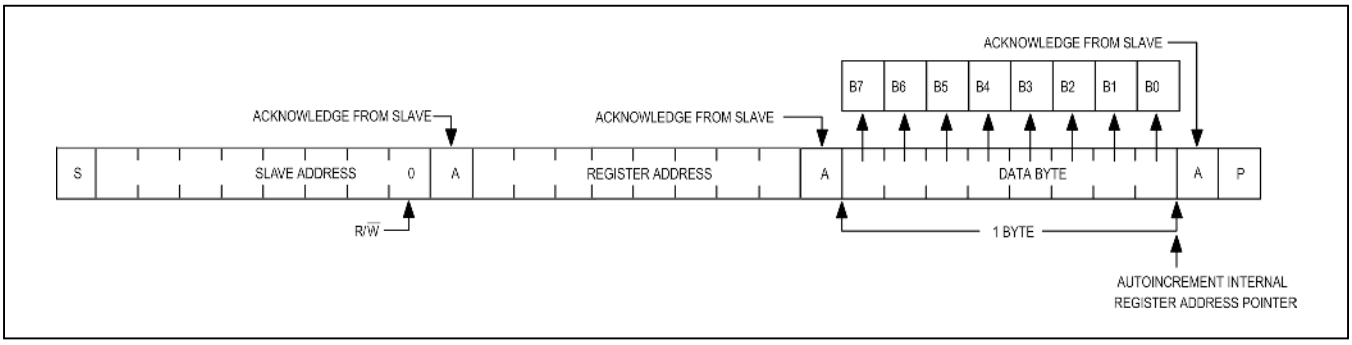


Figure 23. Writing One Byte of Data to the MAX98371

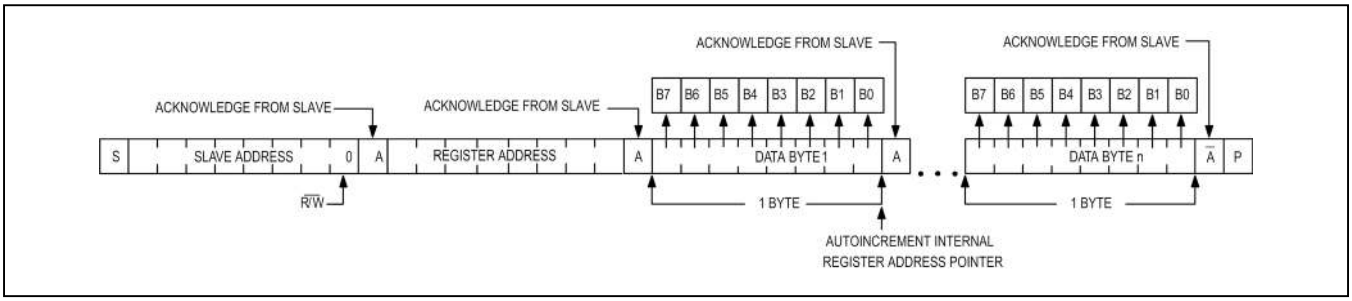


Figure 24. n-Bytes of Data to the MAX98371

The slave address with the R/W bit set to 0 indicates that the master intends to write data to the IC. The IC acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the IC's internal register address pointer. The pointer tells the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data.

The third byte sent to the IC contains the data that is written to the chosen register. An acknowledge pulse from the IC signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition.

Read Data Format

Send the slave address with the R/W bit set to 1 to initiate a read operation. The IC acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the IC is the content of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the IC's slave address with the R/W bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/W bit set to 1. The IC then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 25 illustrates the frame format for reading one byte from the IC. Figure 26 illustrates the frame format for reading multiple bytes from the IC.

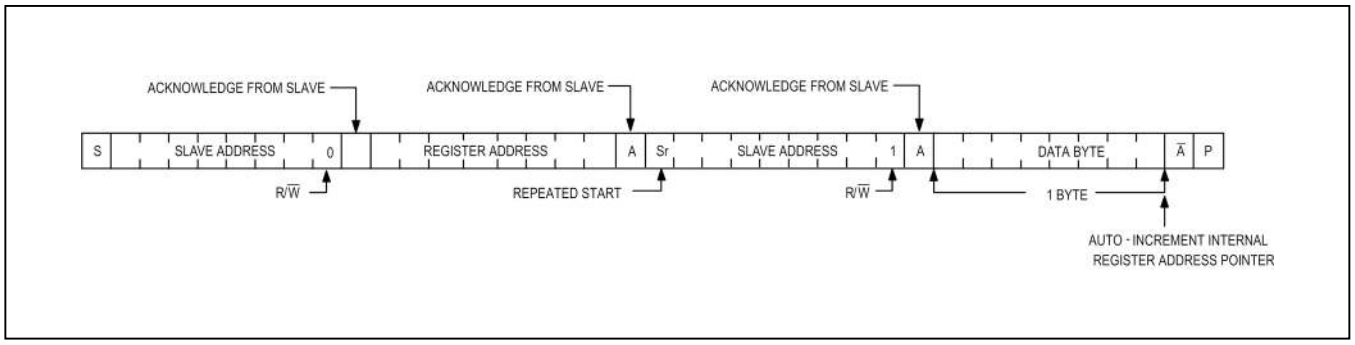


Figure 25. Reading One Byte of Data from the MAX98371

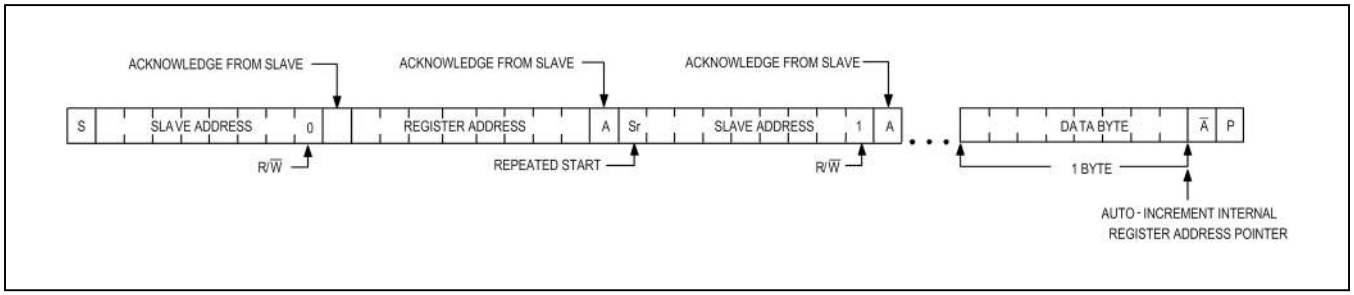


Figure 26. Reading n-Bytes of Data from the MAX98371

I²C Slave Addresses

The MAX98371 is configured using the I²C control bus. The addresses effectively allow unique audio endpoint destinations in systems that use multiples of the device. The IC uses hardware select slave addresses determined by the configuration of ADDR0, ADDR1 as shown in Table 40. See the I²C Serial Interface section for a complete interface description.

Applications Information

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Use at least 4 PCB layers, and add thermal vias to the ground/power plane close to the MAX98371 to ensure good thermal performance and high-end output power. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal. Ground the power signals and the analog signals of the IC separately at the system ground plane, to prevent switching interference from corrupting sensitive analog signals.

Place the recommended supply decoupling capacitors as close as possible to the IC. The PVDD to PGND connection must be kept short and should have minimum trace length and loop area to ensure optimumal performance.

Use wide, low-resistance output, supply and ground traces. As load impedance decreases, the current drawn from the device outputs increase. At higher current, the resistance of the output traces decreases the power delivered to the load. For example, if 2W is delivered from the speaker output to a 4Ω load through a 100mΩ trace, 49mW is consumed in the trace. If power is delivered through a 10mΩ trace, only 5mW is consumed in the trace. Wide output, supply, and ground traces also improve the power dissipation of the device.

The MAX98371 is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on the top and bottom PCB planes.

It is generally advisable to follow the layout of the MAX98371 evaluation kit as closely as is practical in the application.

Thermal and performance measurements shown in this Datasheet were measured with a 6 layer board with 2 signal layers and 4 ground layers. As a result our EVKit performance is likely better than what can be achieved with a JEDEC standard Board.

Table 40. ADDR I²C Address Select

ADDR1	ADDR0	I²C WRITE ADDRESS SELECT
ADDR1 connected to DVDD	ADDR0 connected to DGND	0x62
ADDR1 connected to DGND	ADDR0 connected to DGND	0x64
ADDR1 connected to SDA	ADDR0 connected to DGND	0x66
ADDR1 connected to SCL	ADDR0 connected to DGND	0x68
ADDR1 connected to DVDD	ADDR0 connected to SDA	0x6A
ADDR1 connected to DGND	ADDR0 connected to SDA	0x6C
ADDR1 connected to SDA	ADDR0 connected to SDA	0x6E
ADDR1 connected to SCL	ADDR0 connected to SDA	0x70
ADDR1 connected to DVDD	ADDR0 connected to DVDD	0x72
ADDR1 connected to DGND	ADDR0 connected to DVDD	0x74
ADDR1 connected to SDA	ADDR0 connected to DVDD	0x76
ADDR1 connected to SCL	ADDR0 connected to DVDD	0x78
ADDR1 connected to DVDD	ADDR0 connected to SCL	0x7A
ADDR1 connected to DGND	ADDR0 connected to SCL	0x7C
ADDR1 connected to SDA	ADDR0 connected to SCL	0x7E
ADDR1 connected to SCL	ADDR0 connected to SCL	0x80

Table 41. Recommended External Components

BUMP	VALUE (µF)	SIZE	VOLTAGE RATING (V)	DIELECTRIC
PVDD	10	0603	50	X5R
PVDD	10	0603	50	X5R
PVDD	0.1	0402	25	X5R
PVDD	0.1	0402	25	X5R
PVDD	220	—	35	Alum-Elec
V_{REFC}	1	0201	6.3	X5R
DVDD	1	0201	6.3	X5R
$\overline{IRQ}$	10	0201	—	—

WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications.* See Figure 27 for the recommended PCB footprint of the MAX98371.

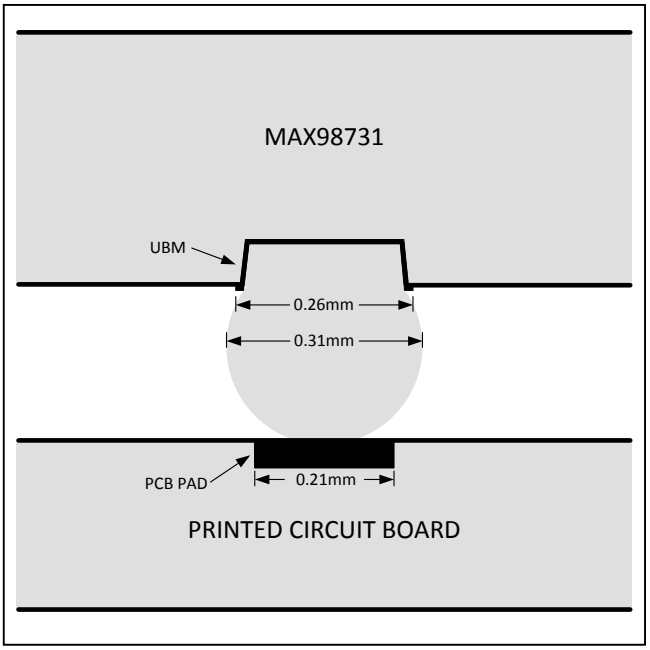
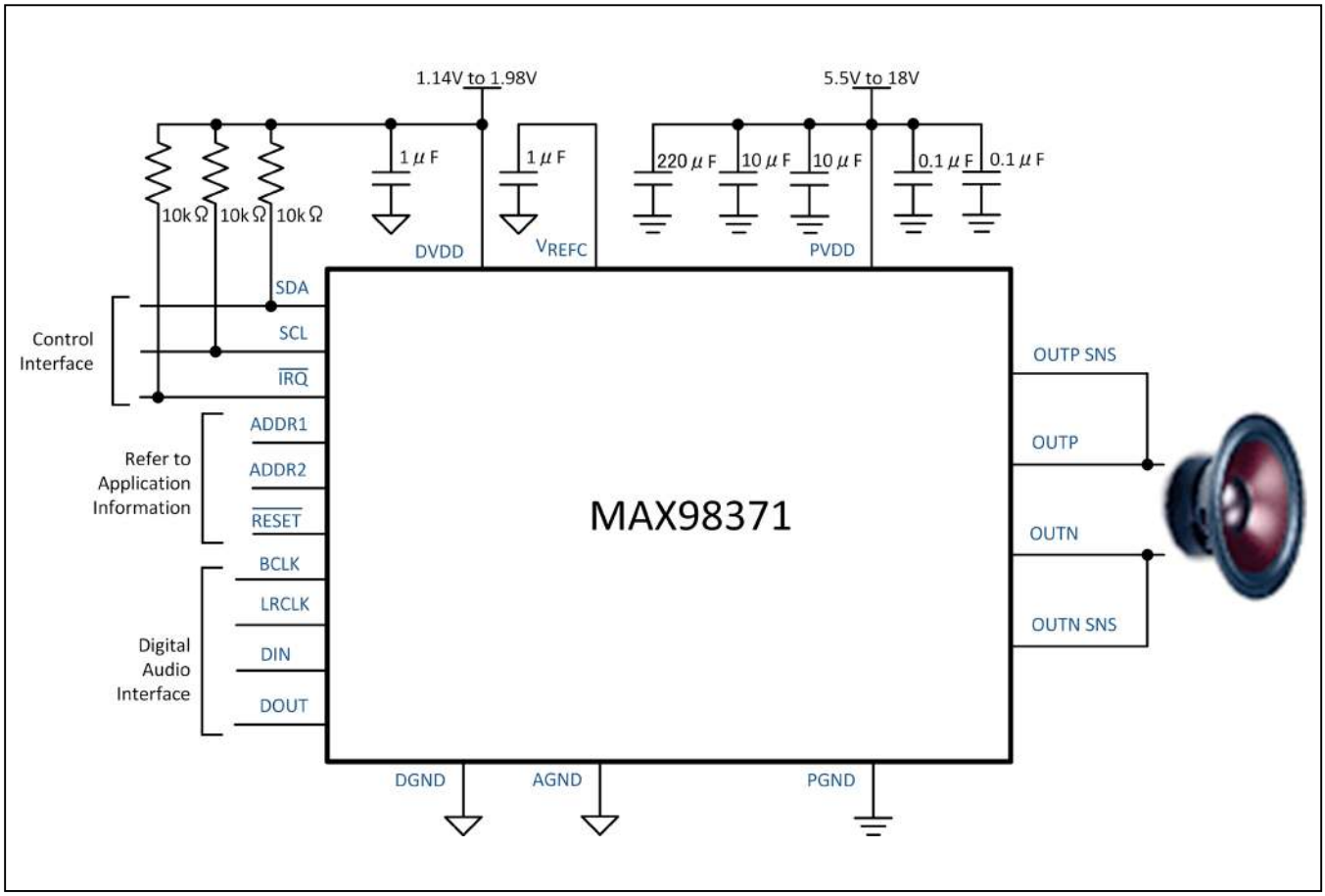


Figure 27. MAX98371+ WLP Ball Dimensions

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX98371EWV+T	-40°C to +85°C	30 WLP
MAX98371EWV+	-40°C to +85°C	30 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = *Tape and reel.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
30-WLP	W302E2+1	**21-0016**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/15	Initial release	—