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Kind regards,

Team Nexperia



# PIMN31

# 500 mA, 50 V NPN/NPN double resistor-equipped transistor; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$

Rev. 01 — 19 June 2007

**Product data sheet** 

# 1. Product profile

### 1.1 General description

500 mA, 50 V NPN/NPN double Resistor-Equipped Transistor (RET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

#### 1.2 Features

- 500 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

## 1.3 Applications

- Digital application in automotive and industrial segments
- Switching loads

#### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per transis	stor					
$V_{CEO}$	collector-emitter voltage	open base	-	-	50	V
I <sub>O</sub>	output current		-	-	500	mA
R1	bias resistor 1 (input)		0.7	1	1.3	$k\Omega$
R2/R1	bias resistor ratio		9	10	11	



## 500 mA, 50 V NPN/NPN double RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$

# 2. Pinning information

Table 2. Pinning

Table 2.	Filling		
Pin	Description	Simplified outline	Symbol
1	GND (emitter) TR1		
2	input (base) TR1	6   5   4	6 5 4
3	output (collector) TR2		
4	GND (emitter) TR2		R1 R2
5	input (base) TR2		TR1
6	output (collector) TR1		R2 R1 R1 1 2 3 svm063

# 3. Ordering information

Table 3. Ordering information

Type number	Package	Package			
	Name	Description	Version		
PIMN31	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457		

# 4. Marking

Table 4. Marking codes

Type number	Marking code
PIMN31	4E

# 5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transist	or				
$V_{CBO}$	collector-base voltage	open emitter	-	50	V
$V_{CEO}$	collector-emitter voltage	open base	-	50	V
$V_{EBO}$	emitter-base voltage	open collector	-	5	V
$V_{I}$	input voltage				
	positive		-	+12	V
	negative		-	-5	V
I <sub>O</sub>	output current		-	500	mA
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25  ^{\circ}C$	<u>[1]</u> -	290	mW

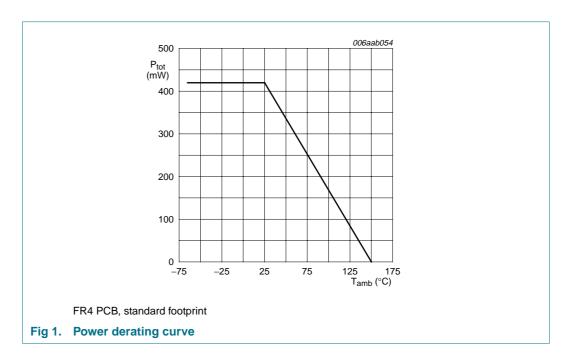
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#### 500 mA, 50 V NPN/NPN double RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$

**Table 5.** Limiting values ...continued In accordance with the Absolute Maximum Rating System (IEC 60134).

			<u> </u>		
Symbol	Parameter	Conditions	Min	Max	Unit
Per device					
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25  ^{\circ}C$	<u>[1]</u> _	420	mW
T <sub>j</sub>	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-65	+150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

<sup>[1]</sup> Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



## 6. Thermal characteristics

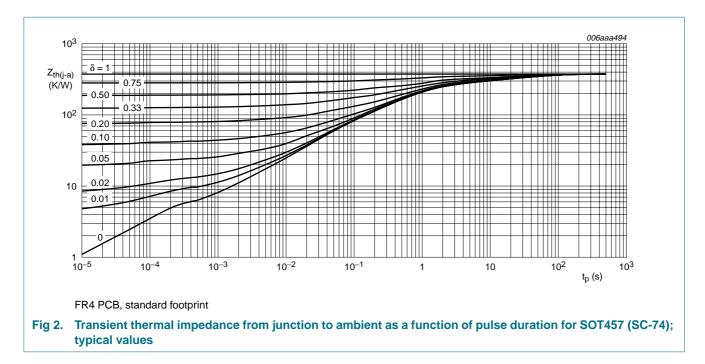
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per transis	stor					
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	<u>[1]</u> -	-	431	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	105	K/W
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] -	-	298	K/W

<sup>[1]</sup> Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

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500 mA, 50 V NPN/NPN double RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 



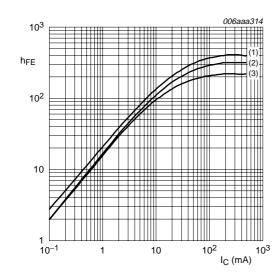
## 7. Characteristics

Table 7. Characteristics

 $T_{amb} = 25 \,^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per transi	stor					
I <sub>CBO</sub>	collector-base cut-off current	$V_{CB} = 50 \text{ V}; I_E = 0 \text{ A}$	-	-	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	$V_{CE} = 50 \text{ V}; I_{B} = 0 \text{ A}$	-	-	0.5	μΑ
I <sub>EBO</sub>	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_{C} = 0 \text{ A}$	-	-	0.72	mA
h <sub>FE</sub>	DC current gain	$V_{CE} = 5 \text{ V}; I_{C} = 50 \text{ mA}$	70	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_C = 50 \text{ mA}; I_B = 2.5 \text{ mA}$	-	-	0.3	V
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5 \text{ V}; I_{C} = 100 \mu\text{A}$	0.3	0.6	1	V
V <sub>I(on)</sub>	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_{C} = 20 \text{ mA}$	0.4	0.8	1.4	V
R1	bias resistor 1 (input)		0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		9	10	11	
C <sub>c</sub>	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz	-	7	-	pF

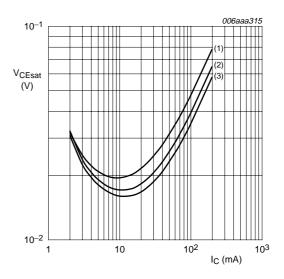
### 500 mA, 50 V NPN/NPN double RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$



$$V_{CE} = 5 V$$

- (1)  $T_{amb} = 100 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = -40 \, ^{\circ}C$

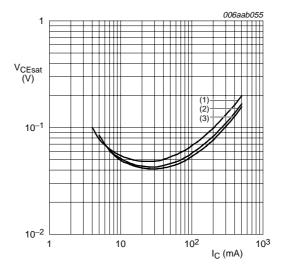
Fig 3. DC current gain as a function of collector current; typical values



$$I_{\rm C}/I_{\rm B} = 20$$

- (1)  $T_{amb} = 100 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = -40 \, ^{\circ}C$

Fig 4. Collector-emitter saturation voltage as a function of collector current; typical values

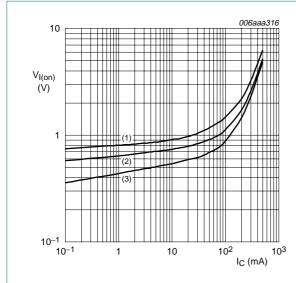


$$I_{\rm C}/I_{\rm B} = 50$$

- (1) T<sub>amb</sub> = 100 °C
- (2)  $T_{amb} = 25 \,^{\circ}C$
- (3)  $T_{amb} = -40 \, ^{\circ}C$

Fig 5. Collector-emitter saturation voltage as a function of collector current; typical values

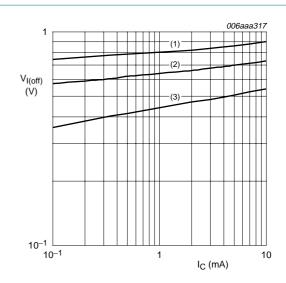
#### 500 mA, 50 V NPN/NPN double RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$



$$V_{CE} = 0.3 \text{ V}$$

- (1)  $T_{amb} = -40 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = 100 \, ^{\circ}C$

Fig 6. On-state input voltage as a function of collector current; typical values



$$V_{CE} = 5 V$$

- (1)  $T_{amb} = -40 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = 100 \, ^{\circ}C$

Fig 7. Off-state input voltage as a function of collector current; typical values

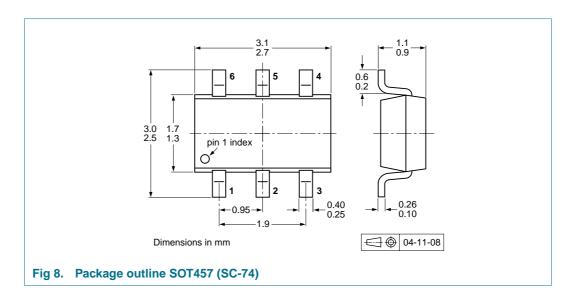
# 8. Test information

### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 (Stress qualification for discrete semiconductors) and is suitable for use in automotive critical applications.

500 mA, 50 V NPN/NPN double RET; R1 = 1 kΩ, R2 = 10 kΩ

# 9. Package outline



# 10. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description		Packing quantity	
				3000	10000
PIMN31	SOT457	4 mm pitch, 8 mm tape and reel; T1	[2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2	[3]	-125	-165

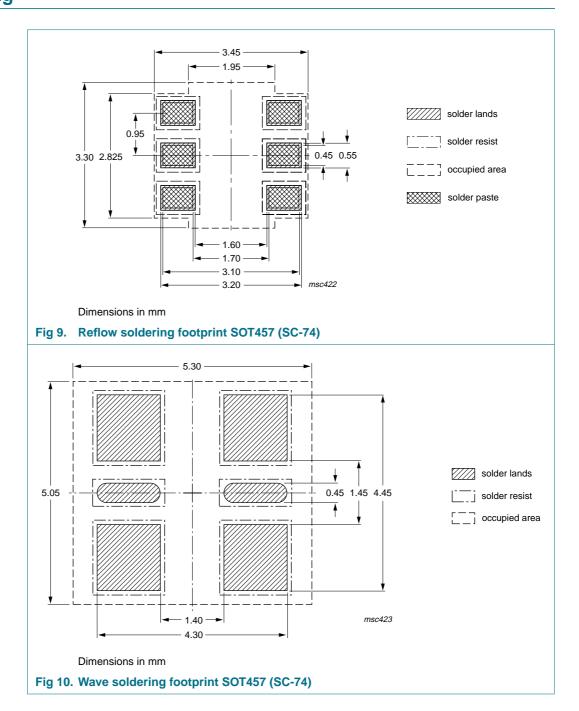
<sup>[1]</sup> For further information and the availability of packing methods, see Section 14.

[2] T1: normal taping

[3] T2: reverse taping

## 500 mA, 50 V NPN/NPN double RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$

# 11. Soldering



500 mA, 50 V NPN/NPN double RET; R1 = 1 kΩ, R2 = 10 kΩ

# 12. Revision history

## Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PIMN31_1	20070619	Product data sheet	-	-

500 mA, 50 V NPN/NPN double RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$ 

## 13. Legal information

#### 13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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## 500 mA, 50 V NPN/NPN double RET; R1 = 1 k $\Omega$ , R2 = 10 k $\Omega$

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