32-Bit

Microcontroller

TC35x

32-Bit Single-Chip Microcontroller
AB-Step

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.1, 2021-03

Microcontrollers

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
V 0.4, 2018-03	
	Version 0.4 is the first version of this document
V 0.6, 2018-05	
	The history is documented in the last chapter
V 0.61, 2018-11	
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V 0.7, 2019-03	
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	The history is documented in the last chapter

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Last Trademarks Update 2011-11-11

Table of Contents

1 Summary of Features

The TC35x product family has the following features:

- High Performance Microcontroller with three CPU cores
- Three 32-bit super-scalar TriCore CPUs (TC1.6.2P), each having the following features:
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - up to 300 MHz operation at full temperature range
  - up to 240 Kbyte Data Scratch-Pad RAM (DSPR)
  - up to 64 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - up to 64 Kbyte Data RAM (DLMU)
  - 32 Kbyte Instruction Cache (ICACHE)
  - 16 Kbyte Data Cache (DCACHE)
- Lockstepped shadow cores for two TC1.6.2P
- Multiple on-chip memories
  - All embedded NVM and SRAM are ECC protected
  - up to 4 Mbyte Program Flash Memory (PFLASH)
  - up to 128 Kbyte Data Flash Memory (DFLASH 0) usable for EEPROM emulation
  - 512 Kbyte Memory (LMU)
  - BootROM (BROM)
- 64-Channel DMA Controller with safe data transfer
- Sophisticated interrupt system (ECC protected)
- High performance on-chip bus structure
  - 64-bit Cross Bar Interconnect (SRI) giving fast parallel access between bus masters, CPUs and memories
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - SRI to SPB bus bridges (SFI Bridge)
- Optional Hardware Security Module (HSM) on some variants
- Safety Management Unit (SMU) handling safety monitor alarms
- Memory Test Unit with ECC, Memory Initialization and MBIST functions (MTU)
- Hardware I/O Monitor (IOM) for checking of digital I/O
- Versatile On-chip Peripheral Units
  - 4 Asynchronous/Synchronous Serial Channels (ASCLIN) with hardware LIN support (V1.3, V2.0, V2.1 and J2602) up to 50 MBaud
  - 4 Queued SPI Interface Channels (QSPI) with master and slave capability up to 50 Mbit/s
  - 2 MCMCAN Modules with 4 CAN nodes for high efficiency data handling via FIFO buffering
  - 1 FlexRay^{TM} module with 2 channels (E-Ray) supporting V2.1
  - One Capture / Compare 6 module (Two kernels CCU60 and CCU61)
  - One General Purpose 12 Timer Unit (GPT120)
  - 1 Inter-Integrated Circuit Bus Interface (I2C) conforming to V2.1

  - 1 IEEE802.3 Ethernet MAC with RMII and MII interfaces (ETH)
- Versatile Successive Approximation ADC (VADC)
  - Cluster of 2 independent ADC kernels
  - Input voltage range from 0 V to 5.5V (ADC supply)
- Digital programmable I/O ports
- On-chip debug support for OCDS Level 1 (CPUs, DMA, On Chip Buses)
- Multi-core debugging, real time tracing, and calibration
- Four/five wire JTAG (IEEE 1149.1) or DAP (Device Access Port) interface
- Power Management System and on-chip regulators
- Clock Generation Unit with System PLL and Peripheral PLL
- Embedded Voltage Regulator
- Qualified for automotive application according to AEC-Q100 (only applicable after delivery release of the corresponding sales codes)
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL D (only applicable for sales codes listed within a released Safety Package Release Note from IFX)

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

Table 1-1 Platform Feature Overview

Feature		TC35x
CPUs	Type	TC1.6.2
	Cores / Checker Cores	3 / 2
	Max. Freq.	300 MHz
Cache per CPU	Program	32 KB
	Data	16 KB
SRAM per CPU	PSPR	64 KB
	DSPR	240 KB for CPU0,1/ 96 KB else
	DLMU	64 KB
SRAM global	LMU	512 KB
	DAM	- KB
Extension Memory	TCM	2 MB
	XCM	- MB
	XTM	16 KB
Program Flash	Size	4 MB
	Banks	2 x 2 MB
Data Flash	Size (single-ended)	128 KB (DF0) + 128 KB (DF1)
DMA	Channels	64
CONVCTRL	Modules	1
EVADC	Primary Groups/Channels	2 / 16
	Secondary Groups/Channels	- / -
	Fast Compare Channels	-
EDSADC	Channels	-

Table 1-1 Platform Feature Overview (cont'd)

Feature		TC35x
GTM	Clusters	-
	TIM (8 ch)	-
	TOM (16 ch)	-
	ATOM (8 ch)	-
	MCS (8 ch)	-
	CMU / ICM	-
	PSM	-
	TBU channels	-
	SPE	-
	CMP / MON	-
	BRC / DPLL	-
	CDTM modules	-
	DTM modules	-
Timer	GPT12	1
	CCU6	1
STM	Modules	3
FlexRay	Modules	1
	Channels	2
CAN	Modules	2
	Nodes	2 x 4
	of which support TT-CAN	-
QSPI	Modules	4
	HSIC Channels	2
ASCLIN	Modules	4
I2C	Interfaces	1
SENT	Channels	-
PSI5	Modules	-
PSI5-S	Modules	-
HSSL	Channels	-
MSC	Channels	-
EBU	External Bus	-
SDMMC	eMMC/SD Interface	-
Ethernet (10/100Mbit/1Gbit)	Modules	1
ASIL	Level	up to ASIL D
FCE	Modules	1
Safety Support	SMU	yes
	IOM	yes

Table 1-1 Platform Feature Overview (cont'd)

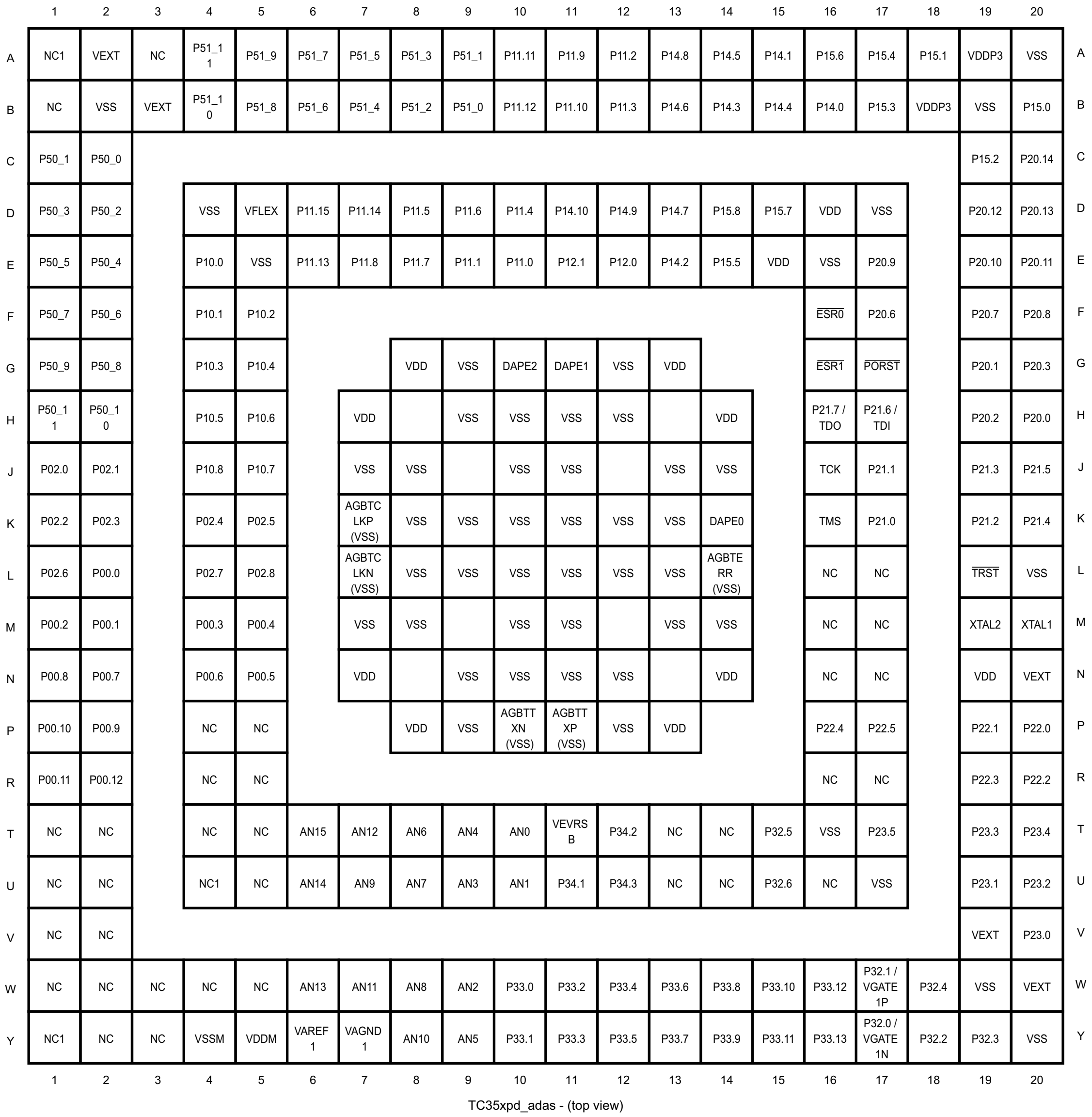
Feature		**TC35x**
SPU	Modules	2
RIF	Modules	2
HSDPM	Modules	1
Security	HSM+	1
Debug	OCDS	yes
	MCDS	-
	miniMCDS	-
	miniMCDS TRAM	- KB
	MCDS light	yes
	AGBT 1)	yes
Low Power Features	Standby RAM	2
	SCR	yes
Packages	Type	LFBGA-292 / LFBGA-180
I/O	Type	5 V CMOS / 3.3 V CMOS / LVDS
$T_{ambient}$	Range	−40 … +125°C

1) The Aurora Gigabit Trace Module (AGBT) is a trace interface intended for development use only (not to be used in series production). It is only available on the specific emulation devices with feature package E, T, and on ADAS devices with feature package A, H of the TC39x, TC37xEXT, TC35x, TC33xEXT. AGBT I/O functions are only available for packages with 292 or more pins. For details on AGBT parameters see the "TC3xx Emulation Devices" Data Sheet.

2 TC35x Pin Definition and Functions:

The following figures are showing the TC35x Logic Symbols for the package variants:

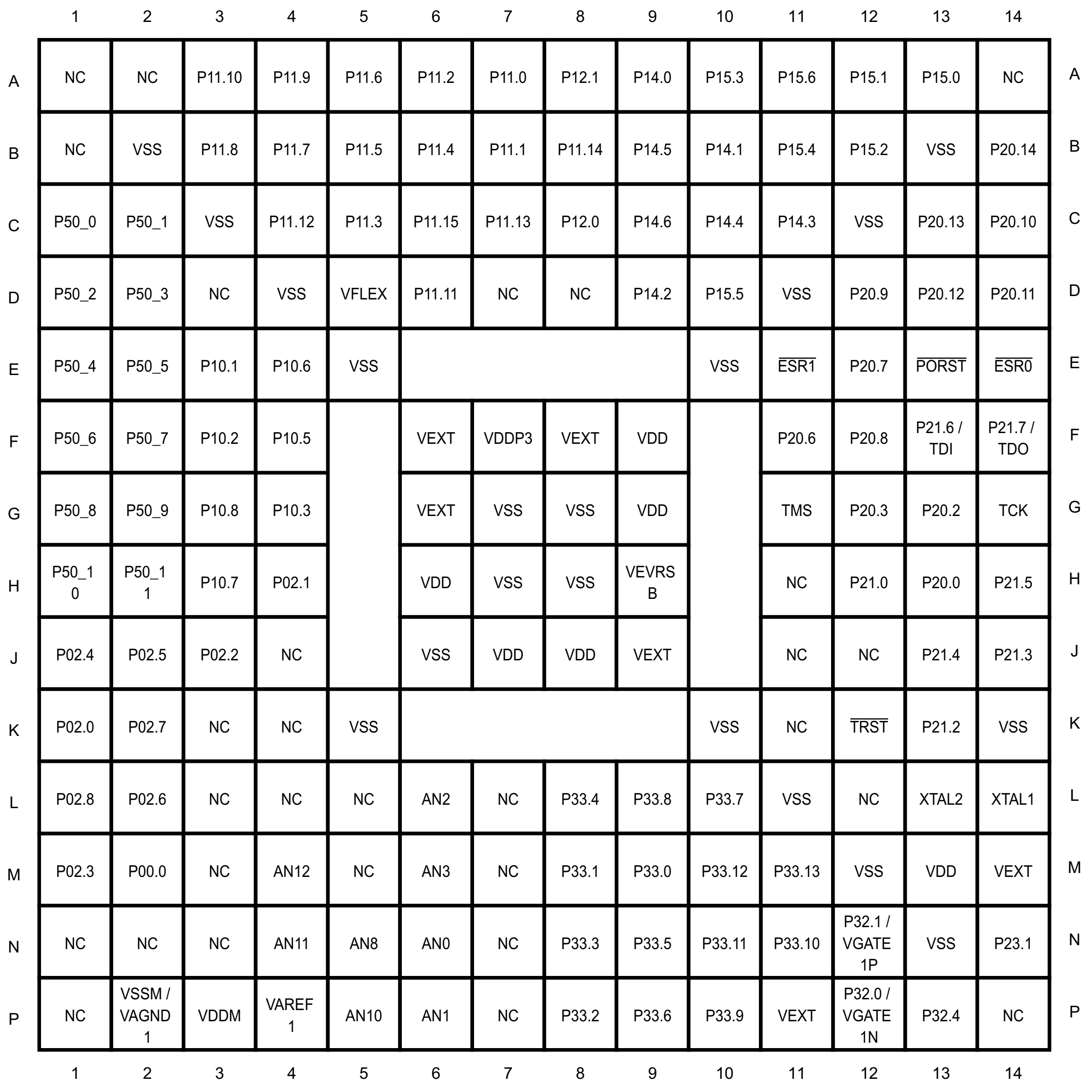
- LFBGA-292 (**Figure 2-1**)
- LFBGA-180 (**Figure 2-2**)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	NC1	VEXT	NC	P51_11	P51_9	P51_7	P51_5	P51_3	P51_1	P11.11	P11.9	P11.2	P14.8	P14.5	P14.1	P15.6	P15.4	P15.1	VDDP3	VSS	A
B	NC	VSS	VEXT	P51_10	P51_8	P51_6	P51_4	P51_2	P51_0	P11.12	P11.10	P11.3	P14.6	P14.3	P14.4	P14.0	P15.3	VDDP3	VSS	P15.0	B
C	P50_1	P50_0																	P15.2	P20.14	C
D	P50_3	P50_2		VSS	VFLEX	P11.15	P11.14	P11.5	P11.6	P11.4	P14.10	P14.9	P14.7	P15.8	P15.7	VDD	VSS		P20.12	P20.13	D
E	P50_5	P50_4		P10.0	VSS	P11.13	P11.8	P11.7	P11.1	P11.0	P12.1	P12.0	P14.2	P15.5	VDD	VSS	P20.9		P20.10	P20.11	E
F	P50_7	P50_6		P10.1	P10.2											$\overline{\text{ESR0}}$	P20.6		P20.7	P20.8	F
G	P50_9	P50_8		P10.3	P10.4			VDD	VSS	DAPE2	DAPE1	VSS	VDD			$\overline{\text{ESR1}}$	$\overline{\text{PORST}}$		P20.1	P20.3	G
H	P50_11	P50_10		P10.5	P10.6		VDD		VSS	VSS	VSS	VSS		VDD		P21.7 / TDO	P21.6 / TDI		P20.2	P20.0	H
J	P02.0	P02.1		P10.8	P10.7		VSS	VSS		VSS	VSS		VSS	VSS		TCK	P21.1		P21.3	P21.5	J
K	P02.2	P02.3		P02.4	P02.5		AGBTCLKP (VSS)	VSS	VSS	VSS	VSS	VSS	VSS	DAPE0		TMS	P21.0		P21.2	P21.4	K
L	P02.6	P00.0		P02.7	P02.8		AGBTCLKN (VSS)	VSS	VSS	VSS	VSS	VSS	VSS	AGBTERR (VSS)		NC	NC		$\overline{\text{TRST}}$	VSS	L
M	P00.2	P00.1		P00.3	P00.4		VSS	VSS		VSS	VSS		VSS	VSS		NC	NC		XTAL2	XTAL1	M
N	P00.8	P00.7		P00.6	P00.5		VDD		VSS	VSS	VSS	VSS		VDD		NC	NC		VDD	VEXT	N
P	P00.10	P00.9		NC	NC			VDD	VSS	AGBTTXN (VSS)	AGBTTXP (VSS)	VSS	VDD			P22.4	P22.5		P22.1	P22.0	P
R	P00.11	P00.12		NC	NC											NC	NC		P22.3	P22.2	R
T	NC	NC		NC	NC	AN15	AN12	AN6	AN4	AN0	VEVRSB	P34.2	NC	NC	P32.5	VSS	P23.5		P23.3	P23.4	T
U	NC	NC		NC1	NC	AN14	AN9	AN7	AN3	AN1	P34.1	P34.3	NC	NC	P32.6	NC	VSS		P23.1	P23.2	U
V	NC	NC																	VEXT	P23.0	V
W	NC	NC	NC	NC	NC	AN13	AN11	AN8	AN2	P33.0	P33.2	P33.4	P33.6	P33.8	P33.10	P33.12	P32.1 / VGATE1P	P32.4	VSS	VEXT	W
Y	NC1	NC	NC	VSSM	VDDM	VAREF1	VAGND1	AN10	AN5	P33.1	P33.3	P33.5	P33.7	P33.9	P33.11	P33.13	P32.0 / VGATE1N	P32.2	P32.3	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

TC35xpd_adas - (top view)

Figure 2-1 TC35x Logic Symbol for the package variant LFBGA-292



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	P11.10	P11.9	P11.6	P11.2	P11.0	P12.1	P14.0	P15.3	P15.6	P15.1	P15.0	NC	A
B	NC	VSS	P11.8	P11.7	P11.5	P11.4	P11.1	P11.14	P14.5	P14.1	P15.4	P15.2	VSS	P20.14	B
C	P50_0	P50_1	VSS	P11.12	P11.3	P11.15	P11.13	P12.0	P14.6	P14.4	P14.3	VSS	P20.13	P20.10	C
D	P50_2	P50_3	NC	VSS	VFLEX	P11.11	NC	NC	P14.2	P15.5	VSS	P20.9	P20.12	P20.11	D
E	P50_4	P50_5	P10.1	P10.6	VSS					VSS	$\overline{\text{ESR1}}$	P20.7	$\overline{\text{PORST}}$	$\overline{\text{ESR0}}$	E
F	P50_6	P50_7	P10.2	P10.5		VEXT	VDDP3	VEXT	VDD		P20.6	P20.8	P21.6 / TDI	P21.7 / TDO	F
G	P50_8	P50_9	P10.8	P10.3		VEXT	VSS	VSS	VDD		TMS	P20.3	P20.2	TCK	G
H	P50_10	P50_11	P10.7	P02.1		VDD	VSS	VSS	VEVRSB		NC	P21.0	P20.0	P21.5	H
J	P02.4	P02.5	P02.2	NC		VSS	VDD	VDD	VEXT		NC	NC	P21.4	P21.3	J
K	P02.0	P02.7	NC	NC	VSS					VSS	NC	$\overline{\text{TRST}}$	P21.2	VSS	K
L	P02.8	P02.6	NC	NC	NC	AN2	NC	P33.4	P33.8	P33.7	VSS	NC	XTAL2	XTAL1	L
M	P02.3	P00.0	NC	AN12	NC	AN3	NC	P33.1	P33.0	P33.12	P33.13	VSS	VDD	VEXT	M
N	NC	NC	NC	AN11	AN8	AN0	NC	P33.3	P33.5	P33.11	P33.10	P32.1 / VGATE1P	VSS	P23.1	N
P	NC	VSSM / VAGND1	VDDM	VAREF1	AN10	AN1	NC	P33.2	P33.6	P33.9	VEXT	P32.0 / VGATE1N	P32.4	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

TC35xpd_adas - (top view)

Figure 2-2 TC35x Logic Symbol for the package variant LFBGA-180

2.1 LFBGA-292 Package Variant Pin Configuration of TC35x

Table 2-1 Port 00 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
L2	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**
M2	P00.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CCU60_CC60INB			**T12 capture input 60**
	ASCLIN3_ARXE			**Receive input**
	CAN10_RXDA			**CAN receive input node 0**
	CCU61_CC60INA			**T12 capture input 60**
	P00.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M1	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	P00.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
M4	P00.3	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	CCU60_CC61INB			**T12 capture input 61**
	CAN03_RXDA			**CAN receive input node 3**
	CCU61_CC61INA			**T12 capture input 61**
	P00.3	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M5	P00.4	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	SCU_E_REQ2_2			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P00.4	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	CAN11_TXD	O3		**CAN transmit output node 1**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
N5	P00.5	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	CCU60_CC62INB			**T12 capture input 62**
	CCU61_CC62INA			**T12 capture input 62**
	CAN11_RXDB			**CAN receive input node 1**
	P00.5	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI3_SLSO3	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**
N4	P00.6	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	P00.6	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**

Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N2	P00.7	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	CCU61_CC60INC			**T12 capture input 60**
	GPT120_T2INA			**Trigger/gate input of timer T2**
	CCU61_CCPOS0A			**Hall capture input 0**
	CCU60_T12HRB			**External timer start 12**
	P00.7	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**
N1	P00.8	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	CCU61_CC61INC			**T12 capture input 61**
	GPT120_T2EUDA			**Count direction control input of timer T2**
	CCU61_CCPOS1A			**Hall capture input 1**
	CCU60_T13HRB			**External timer start 13**
	P00.8	O0		**General-purpose output**
	—	O1		**Reserved**
	QSPI3_SLSO6	O2		**Master slave select output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P2	P00.9	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	CCU61_CC62INC			**T12 capture input 62**
	CCU61_CCPOS2A			**Hall capture input 2**
	GPT120_T4EUDA			**Count direction control input of timer T4**
	CCU60_T13HRC			**External timer start 13**
	CCU60_T12HRC			**External timer start 12**
	P00.9	O0		**General-purpose output**
	—	O1		**Reserved**
	QSPI3_SLSO7	O2		**Master slave select output**
	ASCLIN3_ARTS	O3		**Ready to send output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**
P1	P00.10	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	P00.10	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
R1	P00.11	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	CCU60_CTRAPA			**Trap input capture**
	CCU61_T12HRE			**External timer start 12**
	P00.11	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R2	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	ASCLIN3_ACTSA			**Clear to send input**
	P00.12	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**

Table 2-2 Port 02 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
J1	P02.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CCU61_CC60INB			**T12 capture input 60**
	ASCLIN2_ARXG			**Receive input**
	CCU60_CC60INA			**T12 capture input 60**
	SCU_E_REQ3_2			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P02.0	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO1	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

Table 2-2 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J2	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P02.1	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI3_SLSO2	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
K1	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	P02.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

Table 2-2 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	P02.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	ERAY0_RXDB2			**Receive Channel B2**
	CAN02_RXDB			**CAN receive input node 2**
	ASCLIN1_ARXG			**Receive input**
	P02.3	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI3_SLSO4	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**
K4	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CCU61_CC62INB			**T12 capture input 62**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	P02.4	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	—	O4		**Reserved**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

Table 2-2 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K5	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	I2C0_SCLA			**Serial Clock Input 0**
	QSPI3_MRSTA			**Master SPI data input**
	P02.5	O0		**General-purpose output**
	—	O1		**Reserved**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
L1	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CCU60_CC60INC			**T12 capture input 60**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	RIF0_RAMP1B			**External RAMP B input**
	P02.6	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI3_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

Table 2-2 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L4	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CCU60_CC61INC			**T12 capture input 61**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	CCU60_CCPOS1A			**Hall capture input 1**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
L5	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CCU60_CC62INC			**T12 capture input 62**
	CCU60_CCPOS2A			**Hall capture input 2**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CCU61_T13HRC			**External timer start 13**
	P02.8	O0		**General-purpose output**
	—	O1		**Reserved**
	QSPI3_SLSO5	O2		**Master slave select output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

Table 2-3 Port 10 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
E4	P10.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GPT120_T6EUDB			**Count direction control input of core timer T6**
	GETH_RXERC			**Receive Error MII**
	P10.0	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI1_SLSO10	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
F4	P10.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GPT120_T5EUDB			**Count direction control input of timer T5**
	QSPI1_MRSTA			**Master SPI data input**
	P10.1	O0		**General-purpose output**
	—	O1		**Reserved**
	QSPI1_MTSR	O2		**Master SPI data output**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-3 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F5	P10.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CAN02_RXDE			**CAN receive input node 2**
	QSPI1_SCLKA			**Slave SPI clock inputs**
	GPT120_T6INB			**Trigger/gate input of core timer T6**
	SCU_E_REQ2_0			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P10.2	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
G4	P10.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI1_MTSRA			**Slave SPI data input**
	SCU_E_REQ3_0			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T5INB			**Trigger/gate input of timer T5**
	P10.3	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**

Table 2-3 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G5	P10.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI1_MTSRC			**Slave SPI data input**
	CCU60_CCPOS0C			**Hall capture input 0**
	GPT120_T3INB			**Trigger/gate input of core timer T3**
	P10.4	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI1_SLSO8	O3		**Master slave select output**
	QSPI1_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
H4	P10.5	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	PMS_HWCFG4IN			**HWCFG4 pin input**
	P10.5	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO8	O3		**Master slave select output**
	QSPI1_SLSO9	O4		**Master slave select output**
	GPT120_T6OUT	O5		**External output for overflow/underflow detection of core timer T6**
	ASCLIN2_ASLSO	O6		**Slave select signal output**
	—	O7		**Reserved**

Table 2-3 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H5	P10.6	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	ASCLIN2_ARXD			**Receive input**
	QSPI3_MTSRB			**Slave SPI data input**
	PMS_HWCFG5IN			**HWCFG5 pin input**
	P10.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_MTSR	O3		**Master SPI data output**
	GPT120_T3OUT	O4		**External output for overflow/underflow detection of core timer T3**
	—	O5		**Reserved**
	QSPI1_MRST	O6		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O7		**Reserved**
J5	P10.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GPT120_T3EUDB			**Count direction control input of core timer T3**
	ASCLIN2_ACTSA			**Clear to send input**
	QSPI3_MRSTB			**Master SPI data input**
	SCU_E_REQ0_2			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS1C			**Hall capture input 1**
	P10.7	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CAN12_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**

Table 2-3 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J4	P10.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CAN12_RXDB			**CAN receive input node 2**
	GPT120_T4INB			**Trigger/gate input of timer T4**
	QSPI3_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ1_2			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS2C			**Hall capture input 2**
	RIF1_RAMP1B			**External RAMP B input**
	P10.8	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI3_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-4 Port 11 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
E10	P11.0	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	ASCLIN3_ARXB			**Receive input**
	P11.0	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN11_TXD	O5		**CAN transmit output node 1**
	GETH_TXD3	O6		**Transmit Data**
	—	O7		**Reserved**

Table 2-4 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E9	P11.1	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	P11.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	GETH_TXD2	O6		**Transmit Data**
	—	O7		**Reserved**
A12	P11.2	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	P11.2	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**Master slave select output**
	QSPI1_SLSO5	O4		**Master slave select output**
	—	O5		**Reserved**
	GETH_TXD1	O6		**Transmit Data**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
B12	P11.3	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	QSPI1_MRSTB			**Master SPI data input**
	P11.3	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	ERAY0_TXDA	O4		**Transmit Channel A**
	—	O5		**Reserved**
	GETH_TXD0	O6		**Transmit Data**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

Table 2-4 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D10	P11.4	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GETH_RXCLKB			**Receive Clock MII**
	P11.4	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN13_TXD	O5		**CAN transmit output node 3**
	GETH_TXER	O6		**Transmit Error MII**
	GETH_TXCLK	O7		**Transmit Clock Output for RGMII**
D8	P11.5	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GETH_TXCLKA			**Transmit Clock Input for MII**
	GETH_GREFCLK			**Gigabit Reference Clock input for RGMII (125 MHz high precission)**
	P11.5	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
D9	P11.6	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	QSPI1_SCLKB			**Slave SPI clock inputs**
	P11.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ERAY0_TXENB	O2		**Transmit Enable Channel B**
	QSPI1_SCLK	O3		**Master SPI clock output**
	ERAY0_TXENA	O4		**Transmit Enable Channel A**
	—	O5		**Reserved**
	GETH_TXEN	O6		**Transmit Enable MII and RMII**
	GETH_TCTL			**Transmit Control for RGMII**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

Table 2-4 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E8	P11.7	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GETH_RXD3A			**Receive Data 3 MII and RGMII (RGMII can use RXD3A only)**
	CAN11_RXDD			**CAN receive input node 1**
	P11.7	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
E7	P11.8	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GETH_RXD2A			**Receive Data 2 MII and RGMII (RGMII can use RXD2A only)**
	CAN12_RXDD			**CAN receive input node 2**
	P11.8	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-4 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A11	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	QSPI1_MTSRB			**Slave SPI data input**
	ERAY0_RXDA1			**Receive Channel A1**
	GETH_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P11.9	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
B11	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	CAN03_RXDD			**CAN receive input node 3**
	ERAY0_RXDB1			**Receive Channel B1**
	ASCLIN1_ARXE			**Receive input**
	SCU_E_REQ6_3			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GETH_RXD0A			**Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)**
	QSPI1_SLSIA			**Slave select input**
	P11.10	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SLSO3	O3		**Master slave select output**
	QSPI1_SLSO3	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

Table 2-4 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A10	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GETH_CRSDVA			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVA			**Receive Data Valid MII**
	GETH_CRSB			**Carrier Sense MII**
	GETH_RCTLA			**Receive Control for RGMII**
	P11.11	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SLSO4	O3		**Master slave select output**
	QSPI1_SLSO4	O4		**Master slave select output**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
B10	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GETH_REFCLKA			**Reference Clock input for RMII (50 MHz)**
	GETH_TXCLKB			**Transmit Clock Input for MII**
	GETH_RXCLKA			**Receive Clock MII**
	P11.12	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	—	O3		**Reserved**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

Table 2-4 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E6	P11.13	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GETH_RXERA			**Receive Error MII**
	CAN13_RXDD			**CAN receive input node 3**
	P11.13	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
D7	P11.14	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GETH_CRSDVB			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVB			**Receive Data Valid MII**
	GETH_CRSA			**Carrier Sense MII**
	P11.14	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
D6	P11.15	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GETH_COLA			**Collision MII**
	P11.15	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-5 Port 12 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
E12	P12.0	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	CAN00_RXDC			**CAN receive input node 0**
	GETH_RXCLKC			**Receive Clock MII**
	P12.0	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_MDC	O6		**MDIO clock**
	—	O7		**Reserved**
E11	P12.1	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GETH_MDIOC			**MDIO Input**
	P12.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

Table 2-6 Port 14 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B16	P14.0	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	P14.0	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	ERAY0_TXDA	O3		**Transmit Channel A**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
A15	P14.1	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	ERAY0_RXDA3			**Receive Channel A3**
	ASCLIN0_ARXA			**Receive input**
	ERAY0_RXDB3			**Receive Channel B3**
	CAN01_RXDB			**CAN receive input node 1**
	SCU_E_REQ3_1			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	PMS_PINAWKP			**PINA (P14.1) pin input**
	P14.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

Table 2-6 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E13	P14.2	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	PMS_HWCFG2IN			**HWCFG2 pin input**
	P14.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO1	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN2_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
B14	P14.3	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	PMS_HWCFG3IN			**HWCFG3 pin input**
	ASCLIN2_ARXA			**Receive input**
	SCU_E_REQ1_0			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P14.3	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO3	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	ASCLIN3_ASLSO	O5		**Slave select signal output**
	—	O6		**Reserved**
	—	O7		**Reserved**
B15	P14.4	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	PMS_HWCFG6IN			**HWCFG6 pin input**
	P14.4	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**

Table 2-6 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A14	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	P14.5	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	—	O7		**Reserved**
B13	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P14.6	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	—	O7		**Reserved**
D13	P14.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	ERAY0_RXDB0			**Receive Channel B0**
	CAN10_RXDB			**CAN receive input node 0**
	CAN13_RXDA			**CAN receive input node 3**
	P14.7	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN0_ARTS	O2		**Ready to send output**
	QSPI2_SLSO4	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-6 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A13	P14.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	ERAY0_RXDA0			**Receive Channel A0**
	CAN02_RXDD			**CAN receive input node 2**
	ASCLIN1_ARXD			**Receive input**
	P14.8	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
D12	P14.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	ASCLIN0_ACTSA			**Clear to send input**
	P14.9	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	CAN10_TXD	O4		**CAN transmit output node 0**
	ERAY0_TXENB	O5		**Transmit Enable Channel B**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	—	O7		**Reserved**
D11	P14.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P14.10	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	ASCLIN1_ATX	O4		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	—	O7		**Reserved**

Table 2-7 Port 15 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B20	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	P15.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
A18	P15.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7_2			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

Table 2-7 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C19	P15.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI2_SLSIA			**Slave select input**
	QSPI2_MRSTE			**Master SPI data input**
	QSPI2_HSICINA			**Highspeed capture channel**
	P15.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SLSO0	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
B17	P15.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CAN01_RXDA			**CAN receive input node 1**
	ASCLIN0_ARXB			**Receive input**
	QSPI2_SCLKA			**Slave SPI clock inputs**
	QSPI2_HSICINB			**Highspeed capture channel**
	P15.3	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-7 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A17	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.4	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**
E14	P15.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	ASCLIN1_ARXB			**Receive input**
	I2C0_SDAC			**Serial Data Input 2**
	QSPI2_MTSRA			**Slave SPI data input**
	SCU_E_REQ4_3			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.5	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SDA	O6		**Serial Data Output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

Table 2-7 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A16	P15.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI2_MTSRB			**Slave SPI data input**
	P15.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	QSPI2_SCLK	O5		**Master SPI clock output**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**
D15	P15.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	ASCLIN3_ARXA			**Receive input**
	QSPI2_MRSTB			**Master SPI data input**
	P15.7	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

Table 2-7 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D14	P15.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI2_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ5_0			**ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.8	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

Table 2-8 Port 20 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
H20	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**

Table 2-8 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G19	P20.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CBS_TGI1			**Trigger input**
	P20.1	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO1	O		**Trigger output**
H19	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**
G20	P20.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	ASCLIN3_ARXC			**Receive input**
	GPT120_T6INA			**Trigger/gate input of core timer T6**
	P20.3	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI0_SLSO9	O3		**Master slave select output**
	QSPI2_SLSO9	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-8 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F17	P20.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CAN12_RXDA			**CAN receive input node 2**
	P20.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI0_SLSO8	O3		**Master slave select output**
	QSPI2_SLSO8	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
F19	P20.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CAN00_RXDB			**CAN receive input node 0**
	ASCLIN1_ACTSA			**Clear to send input**
	P20.7	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
F20	P20.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P20.8	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ASLSO	O2		**Slave select signal output**
	QSPI0_SLSO0	O3		**Master slave select output**
	QSPI1_SLSO0	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

Table 2-8 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E17	P20.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CAN03_RXDE			**CAN receive input node 3**
	ASCLIN1_ARXC			**Receive input**
	QSPI0_SLSIB			**Slave select input**
	SCU_E_REQ7_0			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P20.9	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**Master slave select output**
	QSPI1_SLSO1	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
E19	P20.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P20.10	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO6	O3		**Master slave select output**
	QSPI2_SLSO7	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

Table 2-8 Port 20 Functions (cont'd)

Ball	**Symbol**	**Ctrl.**	**Buffer Type**	**Function**
E20	P20.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI0_SCLKA			**Slave SPI clock inputs**
	P20.11	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
D19	P20.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI0_MRSTA			**Master SPI data input**
	IOM_PIN_13			**GPIO pad input to FPC**
	P20.12	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

Table 2-8 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D20	P20.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI0_SLSIA			**Slave select input**
	IOM_PIN_14			**GPIO pad input to FPC**
	P20.13	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**Master slave select output**
	QSPI1_SLSO2	O4		**Master slave select output**
	QSPI0_SCLK	O5		**Master SPI clock output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
C20	P20.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI0_MTSRA			**Slave SPI data input**
	IOM_PIN_15			**GPIO pad input to FPC**
	P20.14	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-9 Port 21 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
K17	P21.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	DMU_FDEST			**Enter destructive debug mode**
	P21.0	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM1	O		**Pin Output Value**
J17	P21.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P21.1	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM2	O		**Pin Output Value**
K19	P21.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	SCU_EMGSTOP_PORT_B			**Emergency stop Port Pin B input request**
	P21.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	GETH_MDC	O5		**MDIO clock**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-9 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J19	P21.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GETH_MDIOD			**MDIO Input**
	P21.3	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**
K20	P21.4	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	P21.4	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
J20	P21.5	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	P21.5	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-9 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H17	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**
	DAPE1	I/O		**DAPE: DAPE1 Data I/O**
H16	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	**General-purpose input**
	GPT120_T5INA			**Trigger/gate input of timer T5**
	CBS_TGI3			**Trigger input**
	GETH_RXERB			**Receive Error MII**
	P21.7	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**External output for overflow/underflow detection of core timer T6**
	CBS_TGO3	O		**Trigger output**
	DAP2	I/O		**DAP: DAP2 Data I/O**
	DAPE2	I/O		**DAPE: DAPE2 Data I/O**
	TDO	O		**JTAG Module Data Output**

Table 2-10 Port 22 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
P20	P22.0	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	P22.0	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
P19	P22.1	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	P22.1	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
R20	P22.2	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	P22.2	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
R19	P22.3	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	P22.3	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	HSPDM_MUTE	O7		**Mute output from the micro controller which could be used to control an external Transmitter**

Table 2-10 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P16	P22.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P22.4	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_SLSO12	O4		**Master slave select output**
	—	O5		**Reserved**
	CAN13_TXD	O6		**CAN transmit output node 3**
	HSPDM_BS0_OUT	O7		**Bit stream 0 output to the pad**
P17	P22.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI0_MTSRC			**Slave SPI data input**
	CAN13_RXDC			**CAN receive input node 3**
	P22.5	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	HSPDM_BS1_OUT	O7		**Bit stream 1 output to the pad**

Table 2-11 Port 23 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
V20	P23.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CAN10_RXDC			**CAN receive input node 0**
	P23.0	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-11 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U19	P23.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P23.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ARTS	O2		**Ready to send output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	CCU_EXTCLK0	O6		**External Clock 0**
	—	O7		**Reserved**
U20	P23.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	P23.2	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
T19	P23.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CAN12_RXDC			**CAN receive input node 2**
	P23.3	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
T20	P23.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P23.4	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-11 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T17	P23.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P23.5	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-12 Port 32 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
Y17	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	P32.0	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
W17	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	P32.1	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-12 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y18	P32.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CAN03_RXDB			**CAN receive input node 3**
	ASCLIN3_ARXD			**Receive input**
	P32.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	PMS_DCDCSYNCO	O6		**DC-DC synchronization output**
	—	O7		**Reserved**
Y19	P32.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	P32.3	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN3_ASCLK	O4		**Shift clock output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-12 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W18	P32.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	ASCLIN1_ACTSB			**Clear to send input**
	P32.4	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	PMS_DCDCSYNCO	O		**DC-DC synchronization output**
T15	P32.5	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	P32.5	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**

Table 2-12 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U15	P32.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CAN02_RXDC			**CAN receive input node 2**
	CBS_TGI4			**Trigger input**
	ASCLIN2_ARXF			**Receive input**
	P32.6	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI2_SLSO12	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO4	O		**Trigger output**

Table 2-13 Port 33 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
W10	P33.0	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	IOM_PIN_0			**GPIO pad input to FPC**
	P33.0	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
Y10	P33.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	IOM_PIN_1			**GPIO pad input to FPC**
	P33.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W11	P33.2	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	IOM_PIN_2			**GPIO pad input to FPC**
	P33.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	QSPI2_SLSO10	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**
Y11	P33.3	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	IOM_PIN_3			**GPIO pad input to FPC**
	P33.3	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**
W12	P33.4	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	CCU61_CTRAPC			**Trap input capture**
	IOM_PIN_4			**GPIO pad input to FPC**
	P33.4	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI2_SLSO12	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	—	O6		**Reserved**
	CAN13_TXD	O7		**CAN transmit output node 3**

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y12	P33.5	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GPT120_T4EUDB			**Count direction control input of timer T4**
	ASCLIN2_ACTSB			**Clear to send input**
	CCU61_CCPOS2C			**Hall capture input 2**
	CAN13_RXDB			**CAN receive input node 3**
	IOM_PIN_5			**GPIO pad input to FPC**
	P33.5	O0		**General-purpose output**
	—	O1		**Reserved**
	QSPI0_SLSO7	O2		**Master slave select output**
	QSPI1_SLSO7	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	—	O6		**Reserved**
	—	O7		**Reserved**
W13	P33.6	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GPT120_T2EUDB			**Count direction control input of timer T2**
	CCU61_CCPOS1C			**Hall capture input 1**
	IOM_PIN_6			**GPIO pad input to FPC**
	P33.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI2_SLSO11	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y13	P33.7	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	CAN00_RXDE			**CAN receive input node 0**
	GPT120_T2INB			**Trigger/gate input of timer T2**
	CCU61_CCPOS0C			**Hall capture input 0**
	SCU_E_REQ4_0			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	IOM_PIN_7			**GPIO pad input to FPC**
	P33.7	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
W14	P33.8	I	FAST / HighZ / VEVRSB	**General-purpose input**
	ASCLIN2_ARXE			**Receive input**
	SCU_EMGSTOP_PORT_A			**Emergency stop Port Pin A input request**
	IOM_PIN_8			**GPIO pad input to FPC**
	P33.8	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SMU_FSP0	O		**FSP[1..0] Output Signals - Generated by SMU_core**

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y14	P33.9	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	QSPI3_HSICINA			**Highspeed capture channel**
	IOM_PIN_9			**GPIO pad input to FPC**
	P33.9	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN2_ASCLK	O4		**Shift clock output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ATX	O6		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**
W15	P33.10	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	QSPI3_HSICINB			**Highspeed capture channel**
	CAN01_RXDD			**CAN receive input node 1**
	ASCLIN0_ARXD			**Receive input**
	IOM_PIN_10			**GPIO pad input to FPC**
	P33.10	O0		**General-purpose output**
	—	O1		**Reserved**
	QSPI1_SLSO6	O2		**Master slave select output**
	—	O3		**Reserved**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
	SMU_FSP1	O		**FSP[1..0] Output Signals - Generated by SMU_core**

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y15	P33.11	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	IOM_PIN_11			**GPIO pad input to FPC**
	P33.11	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
W16	P33.12	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	CAN00_RXDD			**CAN receive input node 0**
	PMS_PINBWKP			**PINB (P33.12) pin input**
	IOM_PIN_12			**GPIO pad input to FPC**
	P33.12	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN1_ASCLK	O4		**Shift clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y16	P33.13	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	ASCLIN1_ARXF			**Receive input**
	P33.13	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	—	O3		**Reserved**
	QSPI2_SLSO6	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

Table 2-14 Port 34 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
U11	P34.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	P34.1	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	CAN00_TXD	O4		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

Table 2-14 Port 34 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T12	P34.2	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	CAN00_RXDG			**CAN receive input node 0**
	P34.2	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**
U12	P34.3	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	P34.3	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI2_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

Table 2-15 Port 50 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
C2	P50.0	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D1N			**LVDS RX Input (inverted Data Bits of Channel #0)**
C1	P50.1	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D1P			**LVDS RX Input (Data Bits of Channel #0)**
D2	P50.2	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D2N			**LVDS RX Input (inverted Data Bits of Channel #1)**

Table 2-15 Port 50 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D1	P50.3	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D2P			**LVDS RX Input (Data Bits of Channel #1)**
E2	P50.4	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_CLKN			**LVDS RX Input (inverted Serial Clock)**
E1	P50.5	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_CLKP			**LVDS RX Input (Serial Clock)**
F2	P50.6	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_FRP			**LVDS RX Input (FrameClock)**
F1	P50.7	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_FRN			**LVDS RX Input (inverted FrameClock)**
G2	P50.8	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D3P			**LVDS RX Input (Data Bits of Channel #2)**
G1	P50.9	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D3N			**LVDS RX Input (inverted Data Bits of Channel #2)**
H2	P50.10	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D4P			**LVDS RX Input (Data Bits of Channel #3)**
H1	P50.11	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D4N			**LVDS RX Input (inverted Data Bits of Channel #3)**

Table 2-16 Port 51 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B9	P51.0	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_D1N			**LVDS RX Input (inverted Data Bits of Channel #0)**

Table 2-16 Port 51 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A9	P51.1	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_D1P			**LVDS RX Input (Data Bits of Channel #0)**
B8	P51.2	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_D2N			**LVDS RX Input (inverted Data Bits of Channel #1)**
A8	P51.3	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_D2P			**LVDS RX Input (Data Bits of Channel #1)**
B7	P51.4	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_CLKN			**LVDS RX Input (inverted Serial Clock)**
A7	P51.5	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_CLKP			**LVDS RX Input (Serial Clock)**
B6	P51.6	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_FRP			**LVDS RX Input (FrameClock)**
A6	P51.7	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_FRN			**LVDS RX Input (inverted FrameClock)**
B5	P51.8	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_D3P			**LVDS RX Input (Data Bits of Channel #2)**
A5	P51.9	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_D3N			**LVDS RX Input (inverted Data Bits of Channel #2)**
B4	P51.10	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_D4P			**LVDS RX Input (Data Bits of Channel #3)**
A4	P51.11	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF1_D4N			**LVDS RX Input (inverted Data Bits of Channel #3)**

Table 2-17 Analog Inputs

Ball	Symbol	Ctrl.	Buffer Type	Function
T10	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
U10	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
W9	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
U9	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
T9	AN4	I	D / HighZ / VDDM	**Analog Input 4**
	EVADC_G0CH4			**Analog input channel 4, group 0**
Y9	AN5	I	D / HighZ / VDDM	**Analog Input 5**
	EVADC_G0CH5			**Analog input channel 5, group 0**
T8	AN6	I	D / HighZ / VDDM	**Analog Input 6**
	EVADC_G0CH6			**Analog input channel 6, group 0**
U8	AN7	I	D / HighZ / VDDM	**Analog Input 7**
	EVADC_G0CH7			**Analog input channel 7, group 0**
W8	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G1CH0			**Analog input channel 0, group 1**
U7	AN9	I	D / HighZ / VDDM	**Analog Input 9**
	EVADC_G1CH1			**Analog input channel 1, group 1**
Y8	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G1CH2			**Analog input channel 2, group 1**
W7	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
T7	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**
W6	AN13	I	D / HighZ / VDDM	**Analog Input 13**
	EVADC_G1CH5			**Analog input channel 5, group 1**
U6	AN14	I	D / HighZ / VDDM	**Analog Input 14**
	EVADC_G1CH6			**Analog input channel 6, group 1**
T6	AN15	I	D / HighZ / VDDM	**Analog Input 15**
	EVADC_G1CH7			**Analog input channel 7, group 1**

Note: Port Pins P32.0 and P32.1 are bidirectional pads and are having the following two functionalities implemented:

1. *In case the pins are used as standard GPIOs the functions defined in the pin configuration tables of P32.0 and P32.1 are available.*
2. *In case the pins are used as pre-drivers for external MOSFETs (internal DCDC usecase) P32.0 and P32.1 act as analog IOs named VGATE1N and VGATE1P.*

Table 2-18 System I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
L7	AGBTCLKN (VSS)	I	AGBT_CLK / VEXT	**Input PAD (negative pole) for the external 100 MHz differential clock.** AGBT Input
K7	AGBTCLKP (VSS)	I	AGBT_CLK / VEXT	**Input PAD (positive pole) for the external 100 MHz differential clock.** AGBT Input
P10	AGBTTXN (VSS)	O	AGBT_TX / VEXT	**Off-chip driver output PAD of the 2.5Gbps transmitter, negative pole** AGBT Output
P11	AGBTTXP (VSS)	O	AGBT_TX / VEXT	**Off-chip driver output PAD of the 2.5Gbps transmitter, positive pole** AGBT Output
L14	AGBTERR (VSS)	I	FAST / PD / VEXT	**Input PAD for CRC error from FPGA.** AGBT Input
W17	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
Y17	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
M20	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
M19	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
K14	DAPE0	I	FAST / PD2 / VEXT	**DAPE: DAPE0 Clock Input** DAPE: DAPE0 clock input
L19	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input**
	DAPE0	I		**DAPE: DAPE0 Clock Input**
K16	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input**
	DAP1	I/O		**DAP: DAP1 Data I/O**

Table 2-18 System I/O (cont’d)

Ball	Symbol	Ctrl.	Buffer Type	Function
J16	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input**
	DAP0	I		**DAP: DAP0 Clock Input**
G11	DAPE1	I/O	FAST / PD2 / VEXT	**DAPE: DAPE1 Data I/O** DAPE: DAPE1 Data I/O
G10	DAPE2	I/O	FAST / PD2 / VEXT	**DAPE: DAPE2 Data I/O** DAPE: DAPE2 Data I/O
F16	$\overline{\text{ESR0}}$	I	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**
G17	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.
G16	$\overline{\text{ESR1}}$	I	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**

Table 2-19 Supply

Ball	Symbol	Ctrl.	Buffer Type	Function
P8, P13, N7, N14, E15, H14, D16, G13, G8, H7	VDD	I	—	**Digital Core Power Supply (1.25V)**
A2, B3, V19, W20	VEXT	I	—	**External Power Supply (5V / 3.3V)**
D5	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**
Y5	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**

Table 2-19 Supply (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B18, A19	VDDP3	I	—	**Flash Power Supply (3.3V)**
B2, D4, E5, T16, U17, W19, Y20, E16, D17, B19, A20	VSS	I	—	**Digital Ground**
Y4	VSSM	I	—	**Analog Ground for VDDM**
P9, P12, N9, N10, N11, N12, M7, M8, M10, M11, M13, M14, L8, L9, L10, L11, L12, L13, K8, K9, K10, K11, K12, K13, J7, J8, J10, J11, J13, J14, H9, H10, H11, H12, G9, G12	VSS	I	—	**Digital Ground**
L20	VSS	I	—	**Oscillator Ground, VSS(OSC)**
Y6	VAREF1	I	—	**Positive Analog Reference Voltage 1**
Y7	VAGND1	I	—	**Negative Analog Reference Voltage 1**
A3, B1, L16, L17, M16, M17, N16, N17, P4, P5, R4, R5, R16, R17, T1, T2, T4, T5, T13, T14, U1, U2, U5, U13, U14, U16, V1, V2, W1, W2, W3, W4, W5, Y2, Y3	NC	I	—	**Not connected. These pins are reserved for future extensions and shall not be connected externally**
A1, Y1, U4	NC1	I	—	**Not connected. These pins are not connected on package level and will not be used for future extensions**
T11	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**

Table 2-19 Supply (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N19	VDD	I	—	**Digital Power Supply for Oscillator (1.25V), VDD(OSC)**
N20	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)**

2.2 LFBGA-180 Package Variant Pin Configuration of TC35x

Table 2-20 Port 00 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
M2	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

Table 2-21 Port 02 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
K1	P02.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	CCU61_CC60INB			T12 capture input 60
	ASCLIN2_ARXG			Receive input
	CCU60_CC60INA			T12 capture input 60
	SCU_E_REQ3_2			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.0	O0		General-purpose output
	—	O1		Reserved
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO1	O3		Master slave select output
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	ERAY0_TXDA	O6		Transmit Channel A
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1
H4	P02.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2_1			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.1	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	QSPI3_SLSO2	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1

Table 2-21 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J3	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	P02.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
M1	P02.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	ERAY0_RXDB2			**Receive Channel B2**
	CAN02_RXDB			**CAN receive input node 2**
	ASCLIN1_ARXG			**Receive input**
	P02.3	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI3_SLSO4	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

Table 2-21 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J1	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CCU61_CC62INB			**T12 capture input 62**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	P02.4	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	—	O4		**Reserved**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**
J2	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	I2C0_SCLA			**Serial Clock Input 0**
	QSPI3_MRSTA			**Master SPI data input**
	P02.5	O0		**General-purpose output**
	—	O1		**Reserved**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

Table 2-21 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L2	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CCU60_CC60INC			**T12 capture input 60**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	RIF0_RAMP1B			**External RAMP B input**
	P02.6	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI3_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**
K2	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CCU60_CC61INC			**T12 capture input 61**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	CCU60_CCPOS1A			**Hall capture input 1**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

Table 2-21 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L1	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CCU60_CC62INC			**T12 capture input 62**
	CCU60_CCPOS2A			**Hall capture input 2**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CCU61_T13HRC			**External timer start 13**
	P02.8	O0		**General-purpose output**
	—	O1		**Reserved**
	QSPI3_SLSO5	O2		**Master slave select output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

Table 2-22 Port 10 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
E3	P10.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GPT120_T5EUDB			**Count direction control input of timer T5**
	QSPI1_MRSTA			**Master SPI data input**
	P10.1	O0		**General-purpose output**
	—	O1		**Reserved**
	QSPI1_MTSR	O2		**Master SPI data output**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-22 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F3	P10.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CAN02_RXDE			**CAN receive input node 2**
	QSPI1_SCLKA			**Slave SPI clock inputs**
	GPT120_T6INB			**Trigger/gate input of core timer T6**
	SCU_E_REQ2_0			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P10.2	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
G4	P10.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI1_MTSRA			**Slave SPI data input**
	SCU_E_REQ3_0			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T5INB			**Trigger/gate input of timer T5**
	P10.3	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**

Table 2-22 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F4	P10.5	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	PMS_HWCFG4IN			**HWCFG4 pin input**
	P10.5	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO8	O3		**Master slave select output**
	QSPI1_SLSO9	O4		**Master slave select output**
	GPT120_T6OUT	O5		**External output for overflow/underflow detection of core timer T6**
	ASCLIN2_ASLSO	O6		**Slave select signal output**
	—	O7		**Reserved**
E4	P10.6	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	ASCLIN2_ARXD			**Receive input**
	QSPI3_MTSRB			**Slave SPI data input**
	PMS_HWCFG5IN			**HWCFG5 pin input**
	P10.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_MTSR	O3		**Master SPI data output**
	GPT120_T3OUT	O4		**External output for overflow/underflow detection of core timer T3**
	—	O5		**Reserved**
	QSPI1_MRST	O6		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O7		**Reserved**

Table 2-22 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H3	P10.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GPT120_T3EUDB			**Count direction control input of core timer T3**
	ASCLIN2_ACTSA			**Clear to send input**
	QSPI3_MRSTB			**Master SPI data input**
	SCU_E_REQ0_2			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS1C			**Hall capture input 1**
	P10.7	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CAN12_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**
G3	P10.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CAN12_RXDB			**CAN receive input node 2**
	GPT120_T4INB			**Trigger/gate input of timer T4**
	QSPI3_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ1_2			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS2C			**Hall capture input 2**
	RIF1_RAMP1B			**External RAMP B input**
	P10.8	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI3_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-23 Port 11 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A7	P11.0	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	ASCLIN3_ARXB			**Receive input**
	P11.0	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN11_TXD	O5		**CAN transmit output node 1**
	GETH_TXD3	O6		**Transmit Data**
	—	O7		**Reserved**
B7	P11.1	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	P11.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	GETH_TXD2	O6		**Transmit Data**
	—	O7		**Reserved**
A6	P11.2	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	P11.2	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**Master slave select output**
	QSPI1_SLSO5	O4		**Master slave select output**
	—	O5		**Reserved**
	GETH_TXD1	O6		**Transmit Data**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

Table 2-23 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C5	P11.3	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	QSPI1_MRSTB			**Master SPI data input**
	P11.3	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	ERAY0_TXDA	O4		**Transmit Channel A**
	—	O5		**Reserved**
	GETH_TXD0	O6		**Transmit Data**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
B6	P11.4	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GETH_RXCLKB			**Receive Clock MII**
	P11.4	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN13_TXD	O5		**CAN transmit output node 3**
	GETH_TXER	O6		**Transmit Error MII**
	GETH_TXCLK	O7		**Transmit Clock Output for RGMII**
B5	P11.5	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GETH_TXCLKA			**Transmit Clock Input for MII**
	GETH_GREFCLK			**Gigabit Reference Clock input for RGMII (125 MHz high precission)**
	P11.5	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-23 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A5	P11.6	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	QSPI1_SCLKB			**Slave SPI clock inputs**
	P11.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ERAY0_TXENB	O2		**Transmit Enable Channel B**
	QSPI1_SCLK	O3		**Master SPI clock output**
	ERAY0_TXENA	O4		**Transmit Enable Channel A**
	—	O5		**Reserved**
	GETH_TXEN	O6		**Transmit Enable MII and RMII**
	GETH_TCTL			**Transmit Control for RGMII**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**
B4	P11.7	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GETH_RXD3A			**Receive Data 3 MII and RGMII (RGMII can use RXD3A only)**
	CAN11_RXDD			**CAN receive input node 1**
	P11.7	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
B3	P11.8	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GETH_RXD2A			**Receive Data 2 MII and RGMII (RGMII can use RXD2A only)**
	CAN12_RXDD			**CAN receive input node 2**
	P11.8	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-23 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A4	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	QSPI1_MTSRB			**Slave SPI data input**
	ERAY0_RXDA1			**Receive Channel A1**
	GETH_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P11.9	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
A3	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	CAN03_RXDD			**CAN receive input node 3**
	ERAY0_RXDB1			**Receive Channel B1**
	ASCLIN1_ARXE			**Receive input**
	SCU_E_REQ6_3			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GETH_RXD0A			**Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)**
	QSPI1_SLSIA			**Slave select input**
	P11.10	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SLSO3	O3		**Master slave select output**
	QSPI1_SLSO3	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

Table 2-23 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D6	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GETH_CRSDVA			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVA			**Receive Data Valid MII**
	GETH_CRSB			**Carrier Sense MII**
	GETH_RCTLA			**Receive Control for RGMII**
	P11.11	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SLSO4	O3		**Master slave select output**
	QSPI1_SLSO4	O4		**Master slave select output**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
C4	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GETH_REFCLKA			**Reference Clock input for RMII (50 MHz)**
	GETH_TXCLKB			**Transmit Clock Input for MII**
	GETH_RXCLKA			**Receive Clock MII**
	P11.12	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	—	O3		**Reserved**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

Table 2-23 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C7	P11.13	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GETH_RXERA			**Receive Error MII**
	CAN13_RXDD			**CAN receive input node 3**
	P11.13	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
B8	P11.14	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GETH_CRSDVB			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVB			**Receive Data Valid MII**
	GETH_CRSA			**Carrier Sense MII**
	P11.14	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
C6	P11.15	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GETH_COLA			**Collision MII**
	P11.15	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-24 Port 12 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
C8	P12.0	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	CAN00_RXDC			**CAN receive input node 0**
	GETH_RXCLKC			**Receive Clock MII**
	P12.0	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_MDC	O6		**MDIO clock**
	—	O7		**Reserved**
A8	P12.1	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GETH_MDIOC			**MDIO Input**
	P12.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

Table 2-25 Port 14 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A9	P14.0	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	P14.0	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	ERAY0_TXDA	O3		**Transmit Channel A**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
B10	P14.1	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	ERAY0_RXDA3			**Receive Channel A3**
	ASCLIN0_ARXA			**Receive input**
	ERAY0_RXDB3			**Receive Channel B3**
	CAN01_RXDB			**CAN receive input node 1**
	SCU_E_REQ3_1			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	PMS_PINAWKP			**PINA (P14.1) pin input**
	P14.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

Table 2-25 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D9	P14.2	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	PMS_HWCFG2IN			**HWCFG2 pin input**
	P14.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO1	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN2_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
C11	P14.3	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	PMS_HWCFG3IN			**HWCFG3 pin input**
	ASCLIN2_ARXA			**Receive input**
	SCU_E_REQ1_0			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P14.3	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO3	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	ASCLIN3_ASLSO	O5		**Slave select signal output**
	—	O6		**Reserved**
	—	O7		**Reserved**
C10	P14.4	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	PMS_HWCFG6IN			**HWCFG6 pin input**
	P14.4	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**

Table 2-25 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B9	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	P14.5	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	—	O7		**Reserved**
C9	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P14.6	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	—	O7		**Reserved**

Table 2-26 Port 15 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A13	P15.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P15.0	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO13	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**

Table 2-26 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A12	P15.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CAN02_RXDA			**CAN receive input node 2**
	ASCLIN1_ARXA			**Receive input**
	QSPI2_SLSIB			**Slave select input**
	SCU_E_REQ7_2			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
B12	P15.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI2_SLSIA			**Slave select input**
	QSPI2_MRSTE			**Master SPI data input**
	QSPI2_HSICINA			**Highspeed capture channel**
	P15.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SLSO0	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**

Table 2-26 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A10	P15.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CAN01_RXDA			**CAN receive input node 1**
	ASCLIN0_ARXB			**Receive input**
	QSPI2_SCLKA			**Slave SPI clock inputs**
	QSPI2_HSICINB			**Highspeed capture channel**
	P15.3	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
B11	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.4	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

Table 2-26 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D10	P15.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	ASCLIN1_ARXB			**Receive input**
	I2C0_SDAC			**Serial Data Input 2**
	QSPI2_MTSRA			**Slave SPI data input**
	SCU_E_REQ4_3			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.5	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SDA	O6		**Serial Data Output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
A11	P15.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI2_MTSRB			**Slave SPI data input**
	P15.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	QSPI2_SCLK	O5		**Master SPI clock output**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

Table 2-27 Port 20 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
H13	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
G13	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**
G12	P20.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	ASCLIN3_ARXC			**Receive input**
	GPT120_T6INA			**Trigger/gate input of core timer T6**
	P20.3	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI0_SLSO9	O3		**Master slave select output**
	QSPI2_SLSO9	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-27 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F11	P20.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	CAN12_RXDA			**CAN receive input node 2**
	P20.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI0_SLSO8	O3		**Master slave select output**
	QSPI2_SLSO8	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
E12	P20.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CAN00_RXDB			**CAN receive input node 0**
	ASCLIN1_ACTSA			**Clear to send input**
	P20.7	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
F12	P20.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P20.8	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ASLSO	O2		**Slave select signal output**
	QSPI0_SLSO0	O3		**Master slave select output**
	QSPI1_SLSO0	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

Table 2-27 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D12	P20.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	CAN03_RXDE			**CAN receive input node 3**
	ASCLIN1_ARXC			**Receive input**
	QSPI0_SLSIB			**Slave select input**
	SCU_E_REQ7_0			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P20.9	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**Master slave select output**
	QSPI1_SLSO1	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
C14	P20.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P20.10	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO6	O3		**Master slave select output**
	QSPI2_SLSO7	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

Table 2-27 Port 20 Functions (cont'd)

Ball	**Symbol**	**Ctrl.**	**Buffer Type**	**Function**
D14	P20.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI0_SCLKA			**Slave SPI clock inputs**
	P20.11	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
D13	P20.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI0_MRSTA			**Master SPI data input**
	IOM_PIN_13			**GPIO pad input to FPC**
	P20.12	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

Table 2-27 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C13	P20.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI0_SLSIA			**Slave select input**
	IOM_PIN_14			**GPIO pad input to FPC**
	P20.13	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**Master slave select output**
	QSPI1_SLSO2	O4		**Master slave select output**
	QSPI0_SCLK	O5		**Master SPI clock output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
B14	P20.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	QSPI0_MTSRA			**Slave SPI data input**
	IOM_PIN_15			**GPIO pad input to FPC**
	P20.14	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-28 Port 21 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
H12	P21.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	DMU_FDEST			**Enter destructive debug mode**
	P21.0	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM1	O		**Pin Output Value**
K13	P21.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	SCU_EMGSTOP_PORT_B			**Emergency stop Port Pin B input request**
	P21.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	GETH_MDC	O5		**MDIO clock**
	—	O6		**Reserved**
	—	O7		**Reserved**
J14	P21.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GETH_MDIOD			**MDIO Input**
	P21.3	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

Table 2-28 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J13	P21.4	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	P21.4	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
H14	P21.5	I	FAST / PU1 / VEXT / ES6	**General-purpose input**
	P21.5	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
F13	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**
	DAPE1	I/O		**DAPE: DAPE1 Data I/O**

Table 2-28 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F14	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	**General-purpose input**
	GPT120_T5INA			**Trigger/gate input of timer T5**
	CBS_TGI3			**Trigger input**
	GETH_RXERB			**Receive Error MII**
	P21.7	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**External output for overflow/underflow detection of core timer T6**
	CBS_TGO3	O		**Trigger output**
	DAP2	I/O		**DAP: DAP2 Data I/O**
	DAPE2	I/O		**DAPE: DAPE2 Data I/O**
	TDO	O		**JTAG Module Data Output**

Table 2-29 Port 23 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
N14	P23.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	P23.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ARTS	O2		**Ready to send output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	CCU_EXTCLK0	O6		**External Clock 0**
	—	O7		**Reserved**

Table 2-30 Port 32 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
P12	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	P32.0	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
N12	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	P32.1	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
P13	P32.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	ASCLIN1_ACTSB			**Clear to send input**
	P32.4	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	PMS_DCDCSYNCO	O		**DC-DC synchronization output**

Table 2-31 Port 33 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
M9	P33.0	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	IOM_PIN_0			**GPIO pad input to FPC**
	P33.0	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
M8	P33.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	IOM_PIN_1			**GPIO pad input to FPC**
	P33.1	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**
P8	P33.2	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	IOM_PIN_2			**GPIO pad input to FPC**
	P33.2	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	QSPI2_SLSO10	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-31 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N8	P33.3	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	IOM_PIN_3			**GPIO pad input to FPC**
	P33.3	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**
L8	P33.4	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	CCU61_CTRAPC			**Trap input capture**
	IOM_PIN_4			**GPIO pad input to FPC**
	P33.4	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI2_SLSO12	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	—	O6		**Reserved**
	CAN13_TXD	O7		**CAN transmit output node 3**
N9	P33.5	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GPT120_T4EUDB			**Count direction control input of timer T4**
	ASCLIN2_ACTSB			**Clear to send input**
	CCU61_CCPOS2C			**Hall capture input 2**
	CAN13_RXDB			**CAN receive input node 3**
	IOM_PIN_5			**GPIO pad input to FPC**
	P33.5	O0		**General-purpose output**
	—	O1		**Reserved**
	QSPI0_SLSO7	O2		**Master slave select output**
	QSPI1_SLSO7	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-31 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P9	P33.6	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GPT120_T2EUDB			**Count direction control input of timer T2**
	CCU61_CCPOS1C			**Hall capture input 1**
	IOM_PIN_6			**GPIO pad input to FPC**
	P33.6	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI2_SLSO11	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	—	O6		**Reserved**
	—	O7		**Reserved**
L10	P33.7	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	CAN00_RXDE			**CAN receive input node 0**
	GPT120_T2INB			**Trigger/gate input of timer T2**
	CCU61_CCPOS0C			**Hall capture input 0**
	SCU_E_REQ4_0			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	IOM_PIN_7			**GPIO pad input to FPC**
	P33.7	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-31 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L9	P33.8	I	FAST / HighZ / VEVRSB	**General-purpose input**
	ASCLIN2_ARXE			**Receive input**
	SCU_EMGSTOP_PORT_A			**Emergency stop Port Pin A input request**
	IOM_PIN_8			**GPIO pad input to FPC**
	P33.8	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SMU_FSP0	O		**FSP[1..0] Output Signals - Generated by SMU_core**

Table 2-31 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P10	P33.9	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	QSPI3_HSICINA			**Highspeed capture channel**
	IOM_PIN_9			**GPIO pad input to FPC**
	P33.9	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN2_ASCLK	O4		**Shift clock output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ATX	O6		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**
N11	P33.10	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	QSPI3_HSICINB			**Highspeed capture channel**
	CAN01_RXDD			**CAN receive input node 1**
	ASCLIN0_ARXD			**Receive input**
	IOM_PIN_10			**GPIO pad input to FPC**
	P33.10	O0		**General-purpose output**
	—	O1		**Reserved**
	QSPI1_SLSO6	O2		**Master slave select output**
	—	O3		**Reserved**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
	SMU_FSP1	O		**FSP[1..0] Output Signals - Generated by SMU_core**

Table 2-31 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N10	P33.11	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	IOM_PIN_11			**GPIO pad input to FPC**
	P33.11	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
M10	P33.12	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	CAN00_RXDD			**CAN receive input node 0**
	PMS_PINBWKP			**PINB (P33.12) pin input**
	IOM_PIN_12			**GPIO pad input to FPC**
	P33.12	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN1_ASCLK	O4		**Shift clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

Table 2-31 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M11	P33.13	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	ASCLIN1_ARXF			**Receive input**
	P33.13	O0		**General-purpose output**
	—	O1		**Reserved**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	—	O3		**Reserved**
	QSPI2_SLSO6	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

Table 2-32 Port 50 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
C1	P50.0	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D1N			**LVDS RX Input (inverted Data Bits of Channel #0)**
C2	P50.1	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D1P			**LVDS RX Input (Data Bits of Channel #0)**
D1	P50.2	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D2N			**LVDS RX Input (inverted Data Bits of Channel #1)**
D2	P50.3	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D2P			**LVDS RX Input (Data Bits of Channel #1)**
E1	P50.4	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_CLKN			**LVDS RX Input (inverted Serial Clock)**

Table 2-32 Port 50 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E2	P50.5	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_CLKP			**LVDS RX Input (Serial Clock)**
F1	P50.6	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_FRP			**LVDS RX Input (FrameClock)**
F2	P50.7	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_FRN			**LVDS RX Input (inverted FrameClock)**
G1	P50.8	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D3P			**LVDS RX Input (Data Bits of Channel #2)**
G2	P50.9	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D3N			**LVDS RX Input (inverted Data Bits of Channel #2)**
H1	P50.10	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D4P			**LVDS RX Input (Data Bits of Channel #3)**
H2	P50.11	I	LVDS_RX / HighZ / VEXT / ES	—
	RIF0_D4N			**LVDS RX Input (inverted Data Bits of Channel #3)**

Table 2-33 Analog Inputs

Ball	Symbol	Ctrl.	Buffer Type	Function
N6	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
P6	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
L6	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
M6	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
N5	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G1CH0			**Analog input channel 0, group 1**

Table 2-33 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P5	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G1CH2			**Analog input channel 2, group 1**
N4	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
M4	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**

Note: Port Pins P32.0 and P32.1 are bidirectional pads and are having the following two functionalities implemented:

3. *In case the pins are used as standard GPIOs the functions defined in the pin configuration tables of P32.0 and P32.1 are available.*
4. *In case the pins are used as pre-drivers for external MOSFETs (internal DCDC usecase) P32.0 and P32.1 act as analog IOs named VGATE1N and VGATE1P.*

Table 2-34 System I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
N12	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
P12	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
L14	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
L13	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
K12	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input**
	DAPE0	I		**DAPE: DAPE0 Clock Input**
G11	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input**
	DAP1	I/O		**DAP: DAP1 Data I/O**
G14	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input**
	DAP0	I		**DAP: DAP0 Clock Input**

Table 2-34 System I/O (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E14	$\overline{\text{ESR0}}$	I	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**
E13	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.
E11	$\overline{\text{ESR1}}$	I	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**

Table 2-35 Supply

Ball	Symbol	Ctrl.	Buffer Type	Function
F9, G9, H6, J7, J8	VDD	I	—	**Digital Core Power Supply (1.25V)**
F6, F8, G6, J9, P11	VEXT	I	—	**External Power Supply (5V / 3.3V)**
D5	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**
P3	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
F7	VDDP3	I	—	**Flash Power Supply (3.3V)**
B2, C3, D4, E5, K10, L11, M12, N13	VSS	I	—	**Digital Ground**
B13, C12, D11, E10, G7, G8, H7, H8, J6, K5	VSS	I	—	**Digital Ground**
K14	VSS	I	—	**Oscillator Ground, VSS(OSC)**
P4	VAREF1	I	—	**Positive Analog Reference Voltage 1**

Table 2-35 Supply (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A1, A2, A14, B1, D3, D7, D8, H11, J4, J11, J12, K3, K4, K11, L3, L4, L5, L7, L12, M3, M5, M7, N1, N2, N3, N7, P1, P7, P14	NC	I	—	**Not connected. These pins are reserved for future extensions and shall not be connected externally**
H9	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**
M13	VDD	I	—	**Digital Power Supply for Oscillator (1.25V), VDD(OSC)**
M14	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)**
P2	VSSM/VAGND1	I	—	**Analog Ground for VDDM / Negative Analog Reference Voltage 1**

2.3 Sequence of Pads in Pad Frame

Table 2-36 Pad List

Number	Pad Name	Pad Type	X	Y	Comment
1	VEXT	Vx	249800	175644	Supply Voltage
2	VSS	Vx	350698	175644	Supply Voltage
3	P14.0	FAST / PU1 / VEXT / ES2	451598	175644	General-purpose I/O
4	VSS	Vx	552496	175644	Supply Voltage
5	VDDP3	Vx	624082	322614	Supply Voltage
6	VDD	Vx	695668	175644	Supply Voltage
7	P14.4	SLOW / PU2 / VEXT / ES	767254	322614	General-purpose I/O
8	P15.7	FAST / PU1 / VEXT / ES	822254	175644	General-purpose I/O
9	P14.1	FAST / PU1 / VEXT / ES2	877252	322614	General-purpose I/O
10	VDD	Vx	948838	175644	Supply Voltage
11	P14.3	SLOW / PU2 / VEXT / ES	1020424	322614	General-purpose I/O
12	VSS	Vx	1092010	175644	Supply Voltage
13	P14.5	FAST / PU2 / VEXT / ES	1163596	322614	General-purpose I/O
14	P15.8	FAST / PU1 / VEXT / ES	1218596	175644	General-purpose I/O
15	VEXT	Vx	1273594	322614	Supply Voltage
16	VSS	Vx	1328594	175644	Supply Voltage
17	P14.8	SLOW / PU1 / VEXT / ES	1383592	322614	General-purpose I/O
18	VDD	Vx	1455178	175644	Supply Voltage
19	P14.6	FAST / PU1 / VEXT / ES	1526764	322614	General-purpose I/O
20	VSS	Vx	1598350	175644	Supply Voltage
21	VDD	Vx	1692346	175644	Supply Voltage
22	VDD	Vx	1786342	175644	Supply Voltage
23	VSS	Vx	1880338	175644	Supply Voltage
24	VSS	Vx	1974334	175644	Supply Voltage
25	VDDP3	Vx	2068330	175644	Supply Voltage
26	VDDP3	Vx	2123330	322614	Supply Voltage
27	VDDP3	Vx	2178328	175644	Supply Voltage
28	VEXT	Vx	2402914	322614	Supply Voltage
29	VSS	Vx	2457914	175644	Supply Voltage

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
30	P14.7	SLOW / PU1 / VEXT / ES	2512912	322614	General-purpose I/O
31	P14.2	SLOW / PU2 / VEXT / ES	2567912	175644	General-purpose I/O
32	VDD	Vx	2622910	322614	Supply Voltage
33	VSS	Vx	2677910	175644	Supply Voltage
34	VSS	Vx	2771906	175644	Supply Voltage
35	VDD	Vx	2865902	175644	Supply Voltage
36	VDD	Vx	2959898	175644	Supply Voltage
37	P14.9	FAST / PU1 / VEXT / ES	3031484	322614	General-purpose I/O
38	VSS	Vx	3103070	175644	Supply Voltage
39	P14.10	FAST / PU1 / VEXT / ES	3174656	322614	General-purpose I/O
40	VSS	Vx	3246242	175644	Supply Voltage
41	VDD	Vx	3340238	175644	Supply Voltage
42	VDD	Vx	3434234	175644	Supply Voltage
43	VDD	Vx	3533036	175644	Supply Voltage
44	P12.0	SLOW / PU1 / VFLEX / ES	3602434	322614	General-purpose I/O
45	VSS	Vx	3671834	175644	Supply Voltage
46	P12.1	SLOW / PU1 / VFLEX / ES	3745606	322614	General-purpose I/O
47	P11.14	SLOW / PU1 / VFLEX / ES	3800606	175644	General-purpose I/O
48	P11.13	SLOW / PU1 / VFLEX / ES	3855604	322614	General-purpose I/O
49	VDD	Vx	3927190	175644	Supply Voltage
50	P11.15	SLOW / PU1 / VFLEX / ES	3998776	322614	General-purpose I/O
51	VSS	Vx	4070362	175644	Supply Voltage
52	P11.0	RFAST / PU1 / VFLEX / ES	4210497	322614	General-purpose I/O
53	VFLEX	Vx	4257495	175644	Supply Voltage
54	P11.1	RFAST / PU1 / VFLEX / ES	4332699	322614	General-purpose I/O
55	VSS	Vx	4379697	175644	Supply Voltage
56	P11.2	RFAST / PU1 / VFLEX / ES	4454901	322614	General-purpose I/O
57	VDD	Vx	4501899	175644	Supply Voltage

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
58	P11.4	RFAST / PU1 / VFLEX / ES	4617603	322614	General-purpose I/O
59	VSS	Vx	4705101	175644	Supply Voltage
60	P11.3	RFAST / PU1 / VFLEX / ES	4780305	322614	General-purpose I/O
61	VFLEX	Vx	4827303	175644	Supply Voltage
62	P11.6	RFAST / PU1 / VFLEX / ES	4902507	322614	General-purpose I/O
63	VSS	Vx	4949505	175644	Supply Voltage
64	P11.5	SLOW / RGMII_Input / PU1 / VFLEX / ES	4996503	322614	General-purpose I/O
65	P11.7	SLOW / RGMII_Input / PU1 / VFLEX / ES	5048883	175644	General-purpose I/O
66	P11.9	FAST / RGMII_Input / PU1 / VFLEX / ES	5099481	322614	General-purpose I/O
67	VFLEX	Vx	5150079	175644	Supply Voltage
68	P11.8	SLOW / RGMII_Input / PU1 / VFLEX / ES	5197077	322614	General-purpose I/O
69	P11.10	FAST / RGMII_Input / PU1 / VFLEX / ES	5247675	175644	General-purpose I/O
70	P11.11	FAST / RGMII_Input / PU1 / VFLEX / ES	5298273	322614	General-purpose I/O
71	VSS	Vx	5348871	175644	Supply Voltage
72	P11.12	FAST / RGMII_Input / PU1 / VFLEX / ES	5395869	322614	General-purpose I/O
73	VSS	Vx	5473683	175644	Supply Voltage
74	VEXT	Vx	5520681	322614	Supply Voltage
75	P51.0	LVDS_RX / HighZ / VEXT / ES	5584680	175644	General-purpose I/O

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
76	P51.1	LVDS_RX / HighZ / VEXT / ES	5665680	175644	General-purpose I/O
77	P51.2	LVDS_RX / HighZ / VEXT / ES	5746680	175644	General-purpose I/O
78	P51.3	LVDS_RX / HighZ / VEXT / ES	5827680	175644	General-purpose I/O
79	P51.4	LVDS_RX / HighZ / VEXT / ES	5908680	175644	General-purpose I/O
80	P51.5	LVDS_RX / HighZ / VEXT / ES	5989680	175644	General-purpose I/O
81	P51.6	LVDS_RX / HighZ / VEXT / ES	6106680	175644	General-purpose I/O
82	P51.7	LVDS_RX / HighZ / VEXT / ES	6187680	175644	General-purpose I/O
83	P51.8	LVDS_RX / HighZ / VEXT / ES	6268680	175644	General-purpose I/O
84	P51.9	LVDS_RX / HighZ / VEXT / ES	6349680	175644	General-purpose I/O
85	P51.10	LVDS_RX / HighZ / VEXT / ES	6430680	175644	General-purpose I/O
86	P51.11	LVDS_RX / HighZ / VEXT / ES	6511680	175644	General-purpose I/O
87	VEXT	Vx	6647796	249800	Supply Voltage
88	VSS	Vx	6647796	350698	Supply Voltage
89	VSS	Vx	6647796	451598	Supply Voltage
90	VDD	Vx	6647796	552496	Supply Voltage
91	P50.0	LVDS_RX / HighZ / VEXT / ES	6647796	666396	General-purpose I/O
92	P50.1	LVDS_RX / HighZ / VEXT / ES	6647796	747396	General-purpose I/O

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
93	P50.2	LVDS_RX / HighZ / VEXT / ES	6647796	828396	General-purpose I/O
94	P50.3	LVDS_RX / HighZ / VEXT / ES	6647796	909396	General-purpose I/O
95	P50.4	LVDS_RX / HighZ / VEXT / ES	6647796	990396	General-purpose I/O
96	P50.5	LVDS_RX / HighZ / VEXT / ES	6647796	1071396	General-purpose I/O
97	P50.6	LVDS_RX / HighZ / VEXT / ES	6647796	1188396	General-purpose I/O
98	P50.7	LVDS_RX / HighZ / VEXT / ES	6647796	1269396	General-purpose I/O
99	P50.8	LVDS_RX / HighZ / VEXT / ES	6647796	1350396	General-purpose I/O
100	P50.9	LVDS_RX / HighZ / VEXT / ES	6647796	1431396	General-purpose I/O
101	P50.10	LVDS_RX / HighZ / VEXT / ES	6647796	1512396	General-purpose I/O
102	P50.11	LVDS_RX / HighZ / VEXT / ES	6647796	1593396	General-purpose I/O
103	VEXT	Vx	6500826	1701284	Supply Voltage
104	VSS	Vx	6647796	1756282	Supply Voltage
105	P10.1	FAST / PU1 / VEXT / ES	6500826	1811282	General-purpose I/O
106	P10.6	SLOW / PU2 / VEXT / ES	6647796	1866280	General-purpose I/O
107	P10.0	SLOW / PU1 / VEXT / ES	6500826	1921280	General-purpose I/O
108	VSS	Vx	6647796	1992866	Supply Voltage
109	P10.2	FAST / PU1 / VEXT / ES	6500826	2064452	General-purpose I/O
110	VDD	Vx	6647796	2136038	Supply Voltage
111	P10.3	FAST / PU1 / VEXT / ES	6500826	2207624	General-purpose I/O

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
112	P10.4	FAST / PU1 / VEXT / ES	6647796	2262622	General-purpose I/O
113	P10.7	SLOW / PU1 / VEXT / ES	6500826	2317622	General-purpose I/O
114	P10.8	SLOW / PU1 / VEXT / ES	6647796	2372620	General-purpose I/O
115	P10.5	SLOW / PU2 / VEXT / ES	6500826	2427620	General-purpose I/O
116	P02.4	FAST / PU1 / VEXT / ES	6647796	2482618	General-purpose I/O
117	P02.0	FAST / PU1 / VEXT / ES	6500826	2537618	General-purpose I/O
118	P02.5	FAST / PU1 / VEXT / ES	6647796	2592616	General-purpose I/O
119	P02.1	SLOW / PU1 / VEXT / ES	6500826	2647616	General-purpose I/O
120	P02.2	FAST / PU1 / VEXT / ES	6647796	2702614	General-purpose I/O
121	P02.3	SLOW / PU1 / VEXT / ES	6500826	2757614	General-purpose I/O
122	P02.8	SLOW / PU1 / VEXT / ES	6647796	2812612	General-purpose I/O
123	P00.0	FAST / PU1 / VEXT / ES	6500826	2867612	General-purpose I/O
124	P02.7	FAST / PU1 / VEXT / ES	6647796	2922610	General-purpose I/O
125	VEXT	Vx	6500826	2986610	Supply Voltage
126	VSS	Vx	6647796	3041608	Supply Voltage
127	P02.6	FAST / PU1 / VEXT / ES	6500826	3096608	General-purpose I/O
128	P00.4	SLOW / PU1 / VEXT / ES1	6647796	3151606	General-purpose I/O
129	P00.1	SLOW / PU1 / VEXT / ES	6500826	3206606	General-purpose I/O
130	P00.5	SLOW / PU1 / VEXT / ES1	6647796	3261604	General-purpose I/O
131	P00.2	SLOW / PU1 / VEXT / ES1	6500826	3316604	General-purpose I/O
132	VSS	Vx	6647796	3388190	Supply Voltage
133	P00.3	SLOW / PU1 / VEXT / ES1	6500826	3459776	General-purpose I/O
134	VDD	Vx	6647796	3531362	Supply Voltage

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
135	P00.7	SLOW / PU1 / VEXT / ES1	6500826	3602948	General-purpose I/O
136	P00.6	SLOW / PU1 / VEXT / ES1	6647796	3657946	General-purpose I/O
137	P00.8	SLOW / PU1 / VEXT / ES1	6500826	3712946	General-purpose I/O
138	P00.9	SLOW / PU1 / VEXT / ES1	6647796	3767944	General-purpose I/O
139	P00.10	SLOW / PU1 / VEXT / ES1	6500826	3822944	General-purpose I/O
140	P00.12	SLOW / PU1 / VEXT / ES1	6647796	3894530	General-purpose I/O
141	P00.11	SLOW / PU1 / VEXT / ES1	6500826	3966116	General-purpose I/O
142	VSS	Vx	6647796	4021114	Supply Voltage
143	VEXT	Vx	6500826	4076114	Supply Voltage
144	AGBTCLKN (VSS)	LVDS_RX / VEXT	6647841	4228182	Input PAD (negative pole) for the external 100 MHz differential clock. AGBT Input
145	AGBTCLKP (VSS)	LVDS_RX / VEXT	6647841	4309272	Input PAD (positive pole) for the external 100 MHz differential clock. AGBT Input
146	VEXT	Vx	6647841	4390182	Supply Voltage
147	VSS	Vx	6647841	4471182	Supply Voltage
148	AGBTTXN (VSS)	LVDS_TX / VEXT	6647841	4579114	Off-chip driver output PAD of the 2.5Gbps transmitter, negative pole AGBT Output
149	AGBTTXP (VSS)	LVDS_TX / VEXT	6647841	4660204	Off-chip driver output PAD of the 2.5Gbps transmitter, positive pole AGBT Output
150	AGBTERR (VSS)	FAST / PD / VEXT	6647702	4850402	Input PAD for CRC error from FPGA. AGBT Input
151	VEXT	Vx	6500826	4975011	Supply Voltage
152	VSS	Vx	6647796	5030010	Supply Voltage
153	VDD	Vx	6500826	5085009	Supply Voltage
154	VSS	Vx	6647796	5156595	Supply Voltage
155	AN15	D / HighZ / VDDM	6500826	5261846	Analog Input 15

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
156	AN14	D / HighZ / VDDM	6647796	5316844	Analog Input 14
157	AN13	D / HighZ / VDDM	6500826	5371844	Analog Input 13
158	AN12	D / HighZ / VDDM	6647796	5426842	Analog Input 12
159	VDDM	Vx	6500826	5481842	Supply Voltage
160	VSSM	Vx	6647796	5536840	Supply Voltage
161	VAREF0	Vx	6500826	5591840	Supply Voltage
162	VAGND0	Vx	6647796	5646838	Supply Voltage
163	AN11	D / HighZ / VDDM	6500826	5701838	Analog Input 11
164	AN10	D / HighZ / VDDM	6647796	5756836	Analog Input 10
165	AN9	D / HighZ / VDDM	6647796	5857736	Analog Input 9
166	AN8	D / HighZ / VDDM	6647796	5958634	Analog Input 8
167	AN7	D / HighZ / VDDM	6647796	6059534	Analog Input 7
168	AN6	D / HighZ / VDDM	6541780	6125796	Analog Input 6
169	AN5	D / HighZ / VDDM	6440882	6125796	Analog Input 5
170	AN4	D / HighZ / VDDM	6385882	5978826	Analog Input 4
171	AN3	D / HighZ / VDDM	6330884	6125796	Analog Input 3
172	AN2	D / HighZ / VDDM	6275884	5978826	Analog Input 2
173	AN1	D / HighZ / VDDM	6220886	6125796	Analog Input 1
174	AN0	D / HighZ / VDDM	6165886	5978826	Analog Input 0
175	VSS	Vx	5988244	6125796	Supply Voltage
176	VEXT	Vx	5916658	5978826	Supply Voltage
177	VDD	Vx	5845072	6125796	Supply Voltage
178	VDD	Vx	5751076	6125796	Supply Voltage
179	VSS	Vx	5657080	6125796	Supply Voltage
180	VDD	Vx	5563084	6125796	Supply Voltage
181	VDD	Vx	5469088	6125796	Supply Voltage

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
182	VSS	Vx	5375092	6125796	Supply Voltage
183	RESERVED	Vx	5187100	6125796	Must be bonded to VSS
184	VEVRSB	Vx	4988210	5978826	Supply Voltage
185	VSS	Vx	4911880	6125796	Supply Voltage
186	VDD	Vx	4826552	5978826	Supply Voltage
187	VSS	Vx	4771552	6125796	Supply Voltage
188	P33.1	SLOW / PU1 / VEVRSB / ES5	4677556	5978826	General-purpose I/O
189	P33.0	SLOW / PU1 / VEVRSB / ES5	4601228	6125796	General-purpose I/O
190	P33.3	SLOW / PU1 / VEVRSB / ES5	4524898	5978826	General-purpose I/O
191	P33.2	SLOW / PU1 / VEVRSB / ES5	4448570	6125796	General-purpose I/O
192	VDD	Vx	4372240	5978826	Supply Voltage
193	VSS	Vx	4317242	6125796	Supply Voltage
194	P33.5	SLOW / PU1 / VEVRSB / ES5	4223246	5978826	General-purpose I/O
195	P33.4	SLOW / PU1 / VEVRSB / ES5	4146916	6125796	General-purpose I/O
196	P33.7	SLOW / PU1 / VEVRSB / ES5	4070588	5978826	General-purpose I/O
197	P33.6	SLOW / PU1 / VEVRSB / ES5	3994258	6125796	General-purpose I/O
198	VDD	Vx	3917930	5978826	Supply Voltage
199	VSS	Vx	3862930	6125796	Supply Voltage
200	P33.9	SLOW / PU1 / VEVRSB / ES5	3768934	5978826	General-purpose I/O
201	P33.8	FAST / HighZ / VEVRSB	3692606	6125796	General-purpose I/O
202	P33.10	FAST / PU1 / VEVRSB / ES5	3616276	5978826	General-purpose I/O
203	VSS	Vx	3539948	6125796	Supply Voltage

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
204	P33.11	FAST / PU1 / VEVRSB / ES5	3463618	5978826	General-purpose I/O
205	VEVRSB	Vx	3387290	6125796	Supply Voltage
206	VDD	Vx	3310960	5978826	Supply Voltage
207	VSS	Vx	3255962	6125796	Supply Voltage
208	P33.13	FAST / PU1 / VEVRSB / ES5	3161966	5978826	General-purpose I/O
209	P34.1	SLOW / PU1 / VEVRSB / ES5	3085636	6125796	General-purpose I/O
210	P33.12	FAST / PU1 / VEVRSB / ES5	3009308	5978826	General-purpose I/O
211	P34.3	SLOW / PU1 / VEVRSB / ES	2932978	6125796	General-purpose I/O
212	VDD	—	2868592	5978826	Supply Voltage
213	VSS	—	2813594	6125796	Supply Voltage
214	VEVRSB	Vx	2610302	6125796	Supply Voltage
215	VEVRSB	Vx	2516306	6125796	Supply Voltage
216	P34.2	SLOW / PU1 / VEVRSB / ES	2422310	6125796	General-purpose I/O
217	VSS	Vx	2328314	6125796	Supply Voltage
218	VEXT	Vx	2198102	6125796	Supply Voltage
219	P32.1	SLOW / PU1 / VEXT / ES	2104106	6125796	General-purpose I/O
220	VGATE1P	Vx	2010110	6125796	DCDC P ch. MOSFET gate driver output
221	VSS	Vx	1916114	6125796	Supply Voltage
222	VGATE1N	Vx	1822118	6125796	DCDC N ch. MOSFET gate driver output
223	P32.0	SLOW / PU1 / VEXT / ES	1728122	6125796	General-purpose I/O
224	VSS	Vx	1625126	6125796	Supply Voltage
225	VDD	Vx	1531130	6125796	Supply Voltage
226	P32.2	SLOW / PU1 / VEXT / ES	1437134	5978826	General-purpose I/O
227	P32.5	SLOW / PU1 / VEXT / ES	1360804	6125796	General-purpose I/O
228	P32.4	FAST / PU1 / VEXT / ES	1302476	5978826	General-purpose I/O

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
229	VDD	Vx	1230890	6125796	Supply Voltage
230	VSS	Vx	1136894	6125796	Supply Voltage
231	VDD	Vx	1081894	5978826	Supply Voltage
232	VSS	Vx	1010308	6125796	Supply Voltage
233	P32.3	SLOW / PU1 / VEXT / ES	938722	5978826	General-purpose I/O
234	VSS	Vx	867136	6125796	Supply Voltage
235	VDD	Vx	773140	6125796	Supply Voltage
236	VEXT	Vx	701554	5978826	Supply Voltage
237	VDD	Vx	629968	6125796	Supply Voltage
238	P32.6	SLOW / PU1 / VEXT / ES	558382	5978826	General-purpose I/O
239	VSS	Vx	457484	6125796	Supply Voltage
240	VDD	Vx	356584	6125796	Supply Voltage
241	VSS	Vx	255686	6125796	Supply Voltage
242	P23.5	FAST / PU1 / VEXT / ES	175644	6046240	General-purpose I/O
243	P23.1	FAST / PU1 / VEXT / ES	175644	5945342	General-purpose I/O
244	P23.0	SLOW / PU1 / VEXT / ES	322614	5844442	General-purpose I/O
245	P23.4	FAST / PU1 / VEXT / ES	175644	5788894	General-purpose I/O
246	P23.2	SLOW / PU1 / VEXT / ES	322614	5733346	General-purpose I/O
247	VDD	Vx	175644	5661760	Supply Voltage
248	P23.3	SLOW / PU1 / VEXT / ES	322614	5590174	General-purpose I/O
249	VSS	Vx	175644	5518588	Supply Voltage
250	VEXT	Vx	322614	5447002	Supply Voltage
251	VSS	Vx	175644	5392004	Supply Voltage
252	P22.2	FAST / PU1 / VEXT / ES6	322614	5335906	General-purpose I/O
253	VDD	Vx	175644	5264320	Supply Voltage
254	VSS	Vx	175644	5170324	Supply Voltage
255	P22.3	FAST / PU1 / VEXT / ES6	322614	5098738	General-purpose I/O
256	P22.0	FAST / PU1 / VEXT / ES6	175644	5043190	General-purpose I/O
257	P22.1	FAST / PU1 / VEXT / ES6	322614	4987642	General-purpose I/O

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
258	VDD	Vx	348147	4837707	Supply Voltage
259	VSS	Vx	179145	4790709	Supply Voltage
260	XTAL1	XTAL / VEXT	179145	4631058	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
261	XTAL2	XTAL / VEXT	179145	4537062	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
262	VSS	—	179145	4377411	Supply Voltage
263	VEXT	Vx	348147	4330413	Supply Voltage
264	VDD	Vx	175644	4156510	Supply Voltage
265	P22.4	FAST / PU1 / VEXT / ES	322614	4084924	General-purpose I/O
266	VSS	Vx	175644	4013338	Supply Voltage
267	P22.5	FAST / PU1 / VEXT / ES	322614	3941752	General-purpose I/O
268	VSS	Vx	175644	3883982	Supply Voltage
269	VEXT	Vx	322614	3828982	Supply Voltage
270	VDD	Vx	175644	3754624	Supply Voltage
271	DAPE0	FAST / PD2 / VEXT	322614	3683038	DAPE: DAPE0 Clock Input DAPE: DAPE0 clock input
272	VSS	Vx	175644	3611452	Supply Voltage
273	$\overline{\text{TRST}}$	FAST / PU2 / VEXT	322614	3539866	JTAG Module Reset/Enable Input
274	VDD	Vx	175644	3468280	Supply Voltage
275	P21.4	FAST / PU1 / VEXT / ES6	322614	3396694	General-purpose I/O
276	VSS	Vx	175644	3325108	Supply Voltage
277	P21.2	FAST / PU1 / VEXT / ES	322614	3253522	General-purpose I/O
278	VSS	Vx	175644	3181936	Supply Voltage
279	VEXT	Vx	322614	3126938	Supply Voltage
280	P21.0	FAST / PU1 / VEXT / ES	175644	3066394	General-purpose I/O
281	P21.3	FAST / PU1 / VEXT / ES	322614	3008624	General-purpose I/O
282	TMS	FAST / PD2 / VEXT	175644	2950852	JTAG Module State Machine Control Input
283	P21.5	FAST / PU1 / VEXT / ES6	322614	2893082	General-purpose I/O

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
284	P21.1	FAST / PU1 / VEXT / ES	175644	2835310	General-purpose I/O
285	P20.0	FAST / PU1 / VEXT / ES	322614	2777540	General-purpose I/O
286	TCK	FAST / PD2 / VEXT	175644	2719768	JTAG Module Clock Input
287	P20.2	S / PU / VEXT	322614	2661998	General-purpose I/O This pin is latched at power on reset release to enter test mode.
288	VDD	Vx	175644	2590412	Supply Voltage
289	VDD	Vx	175644	2496416	Supply Voltage
290	P20.3	SLOW / PU1 / VEXT / ES	322614	2424830	General-purpose I/O
291	VSS	Vx	175644	2353244	Supply Voltage
292	DAPE1	FAST / PD2 / VEXT	322614	2281658	DAPE: DAPE1 Data I/O DAPE: DAPE1 Data I/O
293	P21.6/TDI	FAST / PD / PU2 / VEXT / ES3	175644	2223886	General-purpose I/O PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
294	DAPE2	FAST / PD2 / VEXT	322614	2166116	DAPE: DAPE2 Data I/O DAPE: DAPE2 Data I/O
295	VSS	Vx	175644	2108344	Supply Voltage
296	VEXT	Vx	322614	2053346	Supply Voltage
297	P21.7/TDO	FAST / PU2 / VEXT / ES4	175644	1992802	General-purpose I/O
298	P20.8	FAST / PU1 / VEXT / ES	322614	1935032	General-purpose I/O
299	VDD	Vx	175644	1860674	Supply Voltage
300	P20.1	SLOW / PU1 / VEXT / ES	322614	1789088	General-purpose I/O
301	VSS	Vx	175644	1717502	Supply Voltage
302	P20.11	FAST / PU1 / VEXT / ES	322614	1645916	General-purpose I/O

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
303	$\overline{\text{ESR0}}$	FAST / OD / VEXT	175644	1579144	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
304	$\overline{\text{PORST}}$	PORST / PD / VEXT	322614	1521374	PORST pin Power On Reset Input. Additional strong PD in case of power fail.
305	P20.6	SLOW / PU1 / VEXT / ES	175644	1463602	General-purpose I/O
306	P20.7	FAST / PU1 / VEXT / ES	322614	1405832	General-purpose I/O
307	P15.5	FAST / PU1 / VEXT / ES	175644	1348060	General-purpose I/O
308	P20.10	FAST / PU1 / VEXT / ES	322614	1290290	General-purpose I/O
309	VSS	Vx	175644	1232518	Supply Voltage
310	P20.13	FAST / PU1 / VEXT / ES	322614	1174748	General-purpose I/O
311	VEXT	Vx	175644	1116976	Supply Voltage
312	P20.12	FAST / PU1 / VEXT / ES	322614	1059206	General-purpose I/O
313	VDD	Vx	175644	987620	Supply Voltage
314	P20.14	FAST / PU1 / VEXT / ES	322614	916034	General-purpose I/O
315	VSS	Vx	175644	844448	Supply Voltage
316	P15.0	FAST / PU1 / VEXT / ES	322614	772862	General-purpose I/O

Table 2-36 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
317	P20.9	FAST / PU1 / VEXT / ES	175644	715090	General-purpose I/O
318	P15.2	FAST / PU1 / VEXT / ES	322614	657320	General-purpose I/O
319	P15.3	FAST / PU1 / VEXT / ES	175644	599548	General-purpose I/O
320	$\overline{\text{ESR1}}$	FAST / PU1 / VEXT	322614	541778	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
321	P15.1	FAST / PU1 / VEXT / ES	175644	484006	General-purpose I/O
322	P15.6	FAST / PU1 / VEXT / ES	175644	383108	General-purpose I/O
323	P15.4	FAST / PU1 / VEXT / ES	175644	282208	General-purpose I/O

Whenever in table of section 3 'Electrical Specification' the term 'neighbor pads' is used, the detailed definition is provided by **Figure 2-36**. This statement is also valid for next/nearest neighbor pads.

In order to find out who is affecting operation on a target pad (interfering) a number of active close-neighbor pads (ACNP) has to be defined.

Finding close-neighbor pads.

The Pad Ring has four edges: bottom, left, top, right. Each edge is limited, i.e. it has two ends.

Each pad has two direct (first) neighbors unless it is located at the end of the edge. In that case it only has one neighbor. Similarly, each pad has two indirect (second) neighbors unless it or its first neighbor is located at the end of the edge. These first and second neighbors we will collectively call Close-Neighbor pads. Therefore each pad has 2 to 4 close-neighbor pads.

Finding close-neighbors can be done with the following sequence:

1.) Choose a target pad and lookup its "X" and "Y" coordinates in the table **Figure 2-36**.

2.) Find first and second neighbors by calculating "X" and "Y" distance from the selected pad. **Figure 2-36** is sorted by "Y" coordinate, which might help locate the 4 close-neighbor candidates (if the pad is near the edge, it might end up with less than 4 close-neighbors).

Defining active pads:

Pad is active if it is currently in use and if it doesn't have "Vxx" in the name.

Figuring out number of active close-neighbor pads follow next rules:

- If the first neighbor is active, then we count it and also check if second neighbor (on the same side of selected pad) is active.

- If the first neighbor is not active, then we do not check the second on the same side.

2.4 Legend

The data in this chapter 2 match with the file TC35xpd_IO_Spirit_v1.0.0.1.22.xml.

Column “Ctrl.”:

I = Input (for GPIO port lines with IOCR bit field Selection PCx = $0XXX_B$)

O = Output (for GPIO port lines the ´O´ represents in most cases the port HWOUT function)

O0 = Output with IOCR bit field selection PCx = $1X000_B$

O1 = Output with IOCR bit field selection PCx = $1X001_B$ (ALT1)

O2 = Output with IOCR bit field selection PCx = $1X010_B$ (ALT2)

O3 = Output with IOCR bit field selection PCx = $1X011_B$ (ALT3)

O4 = Output with IOCR bit field selection PCx = $1X100_B$ (ALT4)

O5 = Output with IOCR bit field selection PCx = $1X101_B$ (ALT5)

O6 = Output with IOCR bit field selection PCx = $1X110_B$ (ALT6)

O7 = Output with IOCR bit field selection PCx = $1X111_B$ (ALT7)

Column “Buffer Type”:

FAST = Pad class FAST (5V/3.3V)

RFAST = Pad class RFAST (5V/3.3V)

SLOW = Pad class SLOW (5V/3.3V)

LVDS_TX = Pad class LVDS Transmit

LVDS_RX = Pad class LVDS Receive

D = Pad class D (Analog Input)

Porst = Porst input Pad

XTAL1 = XTAL1 input Pad

XTAL2 = XTAL2 input Pad

PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)

PU1 = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)[1)]

PU2 = with pull-up device connected during startup and reset, HighZ in Standby mode

PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)

PD1 = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)[1)]

PD2 = with pull-down device connected during startup and reset, HighZ in Standby mode

OD = open drain during reset ($\overline{\text{PORST}}$ = 0)

ES = Supports Emergency Stop

ES1 = ES. ES can be overruled by , control via P00_PCSR

ES2 = ES. ES can be overruled by DXCPL - DAP over CAN physical layer, No overruling for DXCM - Debug over CAN message

ES3 = ES. ES can be overruled by JTAG mode if this pin is used as TDI

ES4 = ES. ES can be overruled by JTAG or Three Pin DAP mode

ES5 = ES. ES can be overruled by the Standby Controller - SCR - if implemented. Overruling can be disabled via the control register P33_PCSR and P34_PCSR

[1)] The default state of GPIOs (Px.y) during and after PORST active is controllled via HWCFG6 (P14.4). Pls. see also chapter PMS, HWCFG[6].

3 Electrical Specification

3.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC35x and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC35x and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must be provided by the microcontroller system in which the TC35x designed in.

3.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the Operational Conditions of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3-1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature	T_{ST} SR	-65	-	150	°C	upto 65h @ T_J = 150°C
Voltage at V_{DD} power supply pins with respect to V_{SS} 1) 2)	V_{DD} SR	-	-	1.65	V	upto 2.8h
		-	-	1.45	V	upto 72h
Voltage at V_{DDP3} power supply pins with respect to V_{SS}	V_{DDP3} SR	-	-	4.43	V	
Voltage at V_{DDM}, V_{EXT}, V_{FLEX} and V_{EVRSB} power supply pins with respect to V_{SS}	V_{DDM} SR	-	-	6.75	V	upto 2.8h
		-	-	5.6	V	upto 72h
Voltage on all analog and class S input pins with respect to V_{SS} 3)	V_{IN} SR	-0.7	-	6.75	V	
Voltage on all other input pins with respect to V_{SS} 3)	V_{IN} SR	-0.7	-	6.75	V	
Input current on any pin during overload condition 4) 5)	I_{IN} SR	-10	-	10	mA	
Absolute maximum sum of all input circuit currents during overload condition. 4)	ΣI_{IN} SR	-100	-	100	mA	

1) Valid for cumulated for up to 2.8h and pulse forms followed a power supply switch on phase, where the rise and fall times are related to the system capacities and coils.

2) Due to EVRC output voltage oscillation during switch off phase V_{DD} can drop down to -0.72V. For V_{DD} an input level down to -0.72V during switch off phase will not cause any damage or reliability problem.

3) Voltages below V_{INmin} have no Impact to the device reliability as Long as the times and currents defined in section Pin Reliability in Overload for the affected pad(s) are not violated.

4) This parameter is an Absolute Maximum Rating. Exposure to Absolute Maximum Ratings for extended periods of time may damage the device.

5) The specified min. and max. values represent the current limits, which have to be maintained, in case of a short circuit condition on the output of any Fast, RFast, Slow and Class S pad, not being used during operation.
This covers also output currents due to switching in operation for C_L=200pF.

3.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

The following table defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- allowed time interval (defined in Note column) for overload condition is not exceeded. If no time limit is defined the allowed time includes both ‘Operation Lifetime hours’ and ‘Inactive Lifetime hours’. The number of hours in **Table 3-58** and **Table 3-59** are examples only and the applicable numbers are defined by the customer profiles accepted by Infineon.
- **Operating Conditions** are met for
  - pad supply levels
  - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Table 3-2 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	I_{IN}	-5	-	5	mA	except LVDS pins
		-15 [1]	-	15 [1]	mA	except LVDS pins; limited to max. 20 pulses with 1ms pulse length
Input current on LVDS pin during overload condition	I_{INLVDS}	-3	-	3	mA	
Input current on analog input pin during overload condition	I_{INANA}	-3	-	3	mA	
		-5	-	5	mA	limited to 60h over lifetime
Absolute sum of all analog input currents for analog inputs during overload condition	I_{INSA}	-20	-	20	mA	
Absolute maximum sum of all input circuit currents during overload condition (digital and analog combined)	ΣI_{INS}	-100	-	100	mA	
Signal voltage over/undershoot at GPIOs	V_{OUS}	V_{SS} - 2	-	$V_{\mathrm{EXT/FLEX}}$ + 2	V	limited to 60h over lifetime; Valid for non LVDS and analoge pads
Sum of all inactive device pin currents	I_{IDS}	-100	-	100	mA	
Static pin output current	I_{OUT} CC	-	-	2.5	mA	100% duty cycle; output driver = medium
		-	-	5	mA	100% duty cycle; output driver = strong

Table 3-2 Overload Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for digital inputs, negative	K_{OVDN} CC	-	-	$3*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor fast pads; -5mA < I_{IN} < 0mA
		-	-	$2*10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads VGASTE1N and VGATE1P; -5mA < I_{IN} < 0mA
		-	-	$1*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads; -5mA < I_{IN} < 0mA
		-	-	0.8		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
Overload coupling factor for digital inputs, positive	K_{OVDP} CC	-	-	$1.5*10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pads
		-	-	1		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
Overload coupling factor for analog inputs, negative [2)]	K_{OVAN} CC	-	-	$1*10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; -5mA < I_{IN} < 0mA
		-	-	$1*10^{-5}$		else; -5mA < I_{IN} < 0mA
Overload coupling factor for analog inputs, positive [2)]	K_{OVAP} CC	-	-	$2*10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; 0mA < I_{IN} < 5mA
		-	-	$2*10^{-5}$		else; 0mA < I_{IN} < 5mA

1) Reduced VADC / DSADC result accuracy and / or GPIO input levels (V_{IL} and V_{IH}) can differ from specified parameters.

2) Overload coupling on analog inputs is caused by parasitic effects between pads, input multiplexers and surrounding structures.
The given parameters have been verified for all permutations of channels. Also watch multiple connections of a pin to several channels.

3.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC35x. All parameters specified in the following tables refer to these operating conditions, unless otherwise noticed.

Digital supply voltages applied to the TC35x must be static regulated voltages.

All parameters specified in the following tables refer to these operating conditions (see table below), unless otherwise noticed in the Note / Test Condition column.

Table 3-3 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SRI frequency	f_{SRI} SR	-	-	300	MHz	
CPU Frequency (All CPUs)	f_{CPUx} SR	-	-	300	MHz	
PLL0 output frequency	f_{PLL0} SR	20	-	300	MHz	
SPB frequency	f_{SPB} SR	-	-	100	MHz	
FSI2 frequency	f_{FSI2} SR	-	-	300	MHz	
FSI frequency	f_{FSI} SR	20	-	100	MHz	
STM frequency	f_{STM} SR	-	-	100	MHz	
ERAY frequency	f_{ERAY} SR	-	80	-	MHz	
BBB frequency	f_{BBB} SR	-	-	150	MHz	
VADC frequency	f_{ADC} SR	-	-	160	MHz	
ASCLIN Operating Frequency	$f_{ASCLINx}$ SR	-	-	200	MHz	
CAN frequency	f_{CAN} SR	-	-	80	MHz	
I2C frequency	f_{I2C} SR	-	-	100	MHz	
PLL1 output frequency from PER PLL	f_{PLL1} SR	20	-	320	MHz	
PLL2 output frequency from PER PLL	f_{PLL2} SR	20	-	200	MHz	
QSPI Frequency	f_{QSPI} SR	-	-	200	MHz	
ADAS clock frequency	f_{ADAS} CC	200	-	300	MHz	
MCANH frequency	f_{MCANH} CC	-	-	100	MHz	
GETH frequency	f_{GETH} CC	100	-	150	MHz	
Ambient Temperature	T_A SR	-40	-	125	°C	valid for all SAK products
Junction Temperature	T_J SR	-40	-	150	°C	valid for all SAK products
Core Supply Voltage	V_{DD} SR	1.125 1)	1.25	1.375 2)	V	
ADC analog supply voltage	V_{DDM} SR	2.97	5.0	5.5 3)	V	

Table 3-3 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital external supply voltage for pads and EVR	V_{EXT} SR	4.5	5.0	5.5 [3]	V	Nominal 5V Pad / Port Pin supply range. 5V pad parameters are valid.
		2.97	3.3	3.63	V	Nominal 3.3V Pad / Port Pin supply range with VDDP3 supplied externally and EVR33 inactive. 3.3V pad parameters are valid.
		3.6	-	4.5	V	Flash configured in cranking mode; Flash read operation with reduced performance. EVR33 active in low voltage mode. 3.3V pad parameters are valid.
		2.97	-	3.6	V	Incase EVR33 is active, Flash configured in sleep mode and execution switched to RAM. 3.3V pad parameters are valid.
Digital supply voltage for Flex port	V_{FLEX} SR	2.97	-	4.0	V	3.3V pad parameters are valid
		4.5	5.0	5.5 [3]	V	5V pad parameters are valid
Digital supply voltage for Flash	V_{DDP3} SR	2.97	3.3	3.63 [4]	V	
		2.6	-	3.63	V	Flash configured in cranking mode; Flash read operation with reduced performance.
Digital ground voltage	V_{SS} SR	0	-	-	V	
Analog ground voltage for V_{DDM}	V_{SSM} CC	-0.1	0	0.1	V	
Digital external supply voltage for EVR and during Standby mode	V_{EVRSB} SR	2.97 [5]	-	5.5	V	
Voltage to ensure defined pad states	V_{DDPPA} CC	1.3 [6]	-	-	V	

1) For V_{DD} 1.08V ≤ V_{DD} < 1.125V operation is still possible but with relaxed parameters.

2) Voltage overshoot to 1.69V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.

3) Voltage overshoot to 6.5V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
4) Voltage overshoot to 4.29V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
5) V_{EVRSB} supply voltage can drop down upto 2.6V during Standby mode. It is required to have a capictor of 100nF on V_{EVRSB} supply pin.
6) HWCFG[6] pin is latched and pull-up or tristate is activated at Port pins when VEXT has reached this level.

Limitation of Supply Voltage over Time

The maximum operation voltage for $V_{\mathrm{EXT/FLEX/DDM}}$ supply rails is limited over the complete lifetime.

The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-4 Example Voltage Profile

$V_{\mathrm{EXT/FLEX/DDM}}$=	**Duration [h]**
5.4 V < $V_{\mathrm{EXT/FLEX/DDM}}$ ≤ 5.5 V	≤ 5% of lifetime
5.15 V < $V_{\mathrm{EXT/FLEX/DDM}}$ ≤ 5.4 V	≤ 15% of lifetime
4.85 V < $V_{\mathrm{EXT/FLEX/DDM}}$ ≤ 5.15 V	≤ 60% of lifetime
4.6 V < $V_{\mathrm{EXT/FLEX/DDM}}$ ≤ 4.85 V	≤ 15% of lifetime
4.5 V < $V_{\mathrm{EXT/FLEX/DDM}}$ ≤ 4.6 V	≤ 5% of lifetime

The maximum operation voltage for V_{DD} supply rails is limited over the complete lifetime.

The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-5 Example Voltage Profile

V_{DD}=	**Duration [h]**
1.325 V < V_{DD} ≤ 1.375 V	≤ 5% of lifetime
1.275 V < V_{DD} ≤ 1.325 V	≤ 15% of lifetime
1.225 V < V_{DD} ≤ 1.275 V	≤ 60% of lifetime
1.175 V < V_{DD} ≤ 1.225 V	≤ 15% of lifetime
1.125 V < V_{DD} ≤ 1.175V	≤ 5% of lifetime

3.5 5 V / 3.3 V switchable Pads

Pad classes slow GPIO and fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degrade in TTL operation.

Table 3-6 $\overline{\text{PORST}}$ Pad

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\overline{\text{PORST}}$ pad Output current	I_{PORST} CC	13	-	-	mA	V_{EXT} = 2.97V; V_{PORST} = 0.9V
Spike filter always blocked pulse duration	t_{SF1} CC	-	-	80	ns	
Spike filter pass-through blocked pulse duration	t_{SF2} CC	260	-	-	ns	without additional PORST Digtial Filter active (PORSTDF = 0).
Input hysteresis [1]	HYS CC	0.055 * V_{EXT}	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
Pull-down current [2]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; TTL (degraded, used for CIF)
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-450	-	450	nA	TJ≤150°C ; (0.1 * V_{EXT}) < V_{IN} < (0.9 * V_{EXT})
		-500	-	500	nA	TJ≤150°C ;else
		-900	-	900	nA	TJ≤170°C ; (0.1 * V_{EXT}) < V_{IN} < (0.9 * V_{EXT})
		-950	-	950	nA	TJ≤170°C ; else
Input high voltage level	V_{IH} SR	1.4	-	-	V	TTL (degraded, used for CIF); V_{EXT} = 2.97V
		2.0	-	-	V	TTL; V_{EXT} = 4.5V
Input low voltage level	V_{IL} SR	-	-	0.5	V	TTL (degraded, used for CIF); V_{EXT} = 2.97V
		-	-	0.8	V	TTL; V_{EXT} = 4.5V
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

2) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-7 Fast 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH / OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH / OL}$ = 8mA
Rise / Fall time [1] [2]	t_{RF} CC	1.6	-	3.2	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX/EVRSB}$ to 0.8 * $V_{EXT/FLEX/EVRSB}$
		4+0.55*C_L	4+0.75*C_L	12+1.0*C_L	ns	driver = medium; C_L≤200pF
		1.0+0.18*C_L	2.5+0.27*C_L	5.0+0.35*C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.5+0.08*C_L	0.5+0.11*C_L	1.0+0.17*C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3]	HYS CC	0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Pull-down current [5]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL

Table 3-7 Fast 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-1100	-	1100	nA	$T_J \leq 150°C$; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-2500	-	2500	nA	$T_J \leq 150°C$; (0.1 * $V_{EXT/FLEX}$) < V_{IN} < (0.9 * $V_{EXT/FLEX}$) ; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \leq 150°C$; LVDS_RX / Fast pad type ; else
		-3200	-	3200	nA	$T_J \leq 150°C$; LVDS_TX / Fast pad type ; else
		-1500	-	1500	nA	$T_J \leq 150°C$; else
		-2000	-	2000	nA	$T_J \leq 170°C$; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-4000	-	4000	nA	$T_J \leq 170°C$; (0.1 * $V_{EXT/FLEX}$) < V_{IN} < (0.9 * $V_{EXT/FLEX}$) ; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \leq 170°C$; LVDS_RX / Fast pad type ; else
		-5100	-	5100	nA	$T_J \leq 170°C$; LVDS_TX / Fast pad type ; else
		-2500	-	2500	nA	$T_J \leq 170°C$; else
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.

2) Rise / fall times are defined 10% - 90% of pad supply voltage.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.

5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-8 Fast 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH / OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH / OL}$ = 8mA
Rise / Fall time [1] [2]	t_{RF} CC	1.6	-	4.5	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX/EVRSB}$ to 0.8 * $V_{EXT/FLEX/EVRSB}$
		-	-	5	ns	C_L = 25pF; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		2+0.57*C_L	5.5+0.75*C_L	10+1.25*C_L	ns	driver = medium; C_L≤200pF
		1.5+0.18*C_L	1.5+0.28*C_L	8+0.4*C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.75+0.08*C_L	0.75+0.11*C_L	2.5+0.21*C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3]	HYS CC	0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

Table 3-8 Fast 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current [4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL and TTL (degraded, used for CIF)
Pull-down current [5]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-1100	-	1100	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-2500	-	2500	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX}) < V_{IN} < (0.9 * V_{EXT/FLEX})$; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \leq 150°C$; LVDS_RX / Fast pad type ; else
		-3200	-	3200	nA	$T_J \leq 150°C$; LVDS_TX / Fast pad type ; else
		-1500	-	1500	nA	$T_J \leq 150°C$; else
		-2000	-	2000	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-4000	-	4000	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX}) < V_{IN} < (0.9 * V_{EXT/FLEX})$; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \leq 170°C$; LVDS_RX / Fast pad type ; else
		-5100	-	5100	nA	$T_J \leq 170°C$; LVDS_TX / Fast pad type ; else
		-2500	-	2500	nA	$T_J \leq 170°C$; else

Table 3-8 Fast 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	V_{ILH} SR	1.0	-	1.9	V	RGMII; no hysteresis available
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.

2) Rise / fall times are defined 10% - 90% of pad supply voltage.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.

5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-9 Slow 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH / OL}$ = 2mA
Rise / Fall time 1) 2)	t_{RF} CC	4+0.55*C_L	4+0.75*C_L	12+1*C_L	ns	driver = medium edge = medium ; C_L≤200pF
		1.5+0.25*C_L	2.5+0.40*C_L	7+0.55*C_L	ns	driver = medium edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	

Table 3-9 Slow 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis [3]	HYS CC	0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|30|	-	-	µA	V_{IH};AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
		-	-	|130|	µA	V_{IL}; AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
Pull-down current [5]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL
Input leakage current	I_{OZ} CC	-300	-	300	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-400	-	400	nA	$T_J \leq 150°C$; else
		-600	-	600	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-750	-	750	nA	$T_J \leq 170°C$; else
		-18000	-	18000	nA	P32.0 and P32.1;$T_J \leq 150°C$
		-38000	-	38000	nA	P32.0 and P32.1;$T_J \leq 170°C$
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL

Table 3-9 Slow 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
2) Rise / fall times are defined 10% - 90% of pad supply voltage.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-10 Slow 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH / OL}$ = 2mA
Rise / Fall time [1] [2]	t_{RF} CC	$2+0.57*C_L$	$5.5+0.75*C_L$	$10+1.25*C_L$	ns	driver = medium edge = medium ; C_L≤200pF
		$2+0.30*C_L$	$3.5+0.50*C_L$	$5+0.70*C_L$	ns	driver = medium edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3]	HYS CC	0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

Table 3-10 Slow 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current [4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C
		|11|	-	-	µA	V_{IH}; TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
		-	-	|80|	µA	V_{IL}; AL and TTL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C
Pull-down current [5]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-300	-	300	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-400	-	400	nA	$T_J \leq 150°C$; else
		-600	-	600	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-750	-	750	nA	$T_J \leq 170°C$; else
		-18000	-	18000	nA	P32.0 and P32.1;$T_J \leq 150°C$
		-38000	-	38000	nA	P32.0 and P32.1;$T_J \leq 170°C$
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

Table 3-10 Slow 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	V_{ILH} SR	1.0	-	1.9	V	RGMII; no hysteresis available
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.

2) Rise / fall times are defined 10% - 90% of pad supply voltage.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.

5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-11 RFast 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH / OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH / OL}$ = 8mA
Rise / Fall time 1) 2)	t_{RF} CC	1.6	-	3.2	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * V_{FLEX} to 0.8 * V_{FLEX}
		4+0.55*C_L	4+0.75*C_L	12+1.0*C_L	ns	driver = medium; C_L≤200pF
		1.0+0.18*C_L	2.5+0.27*C_L	5.0+0.35*C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.5+0.08*C_L	0.5+0.11*C_L	1.0+0.17*C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-0.5	-	0.5	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	

Table 3-11 RFast 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis [3]	HYS CC	0.09 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|30|	-	-	μA	V_{IH}; AL or TTL
		-	-	|130|	μA	V_{IL}; AL or TTL
Pull-down current [5]	I_{PDL} CC	-	-	|130|	μA	V_{IH}; AL or TTL
		|30|	-	-	μA	V_{IL}; AL
		|28|	-	-	μA	V_{IL}; TTL
Input leakage current	I_{OZ} CC	-1700	-	1700	nA	$T_{\mathrm{J}} \leq 150°\mathrm{C}$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-2100	-	2100	nA	$T_{\mathrm{J}} \leq 150°\mathrm{C}$; else
		-3000	-	3000	nA	$T_{\mathrm{J}} \leq 170°\mathrm{C}$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-4000	-	4000	nA	$T_{\mathrm{J}} \leq 170°\mathrm{C}$; else
Input high voltage level	V_{IH} SR	0.7 * V_{FLEX}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * V_{FLEX}	V	AL
		-	-	0.8	V	TTL
Pin capacitance	C_{IO} CC	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_{L} needs to be entered in pF to obtain results in ns.

2) Rise / fall times are defined 10% - 90% of pad supply voltage.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.

5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-12 RFast 3.3V pad

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	8	20	30	Ohm	Driver = RGMII; $I_{OH / OL}$ = 8mA
		125	225	320	Ohm	medium driver; $I_{OH / OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH / OL}$ = 8mA
Input Duty Cycle	f_D SR	47.5	50	52.5		
Rise / Fall time 1) 2)	t_{RF} CC	1.6	-	4.5	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * V_{FLEX} to 0.8 * V_{FLEX}
		-	-	5	ns	C_L = 25pF; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		-	-	1	ns	Driver = RGMII; from 20%V to 80%V; C_L=15pF
		2+0.57*C_L	5.5+0.75*C_L	10+1.25*C_L	ns	driver = medium; C_L≤200pF
		1.5+0.18*C_L	1.5+0.28*C_L	8+0.4*C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.75+0.08*C_L	0.75+0.11*C_L	2.5+0.21*C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-0.4	-	0.4	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	

Table 3-12 RFast 3.3V pad (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis [3]	HYS CC	0.055 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * V_{FLEX}	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|17|	-	-	μA	V_{IH}; AL and TTL (degraded, used for CIF)
		|11|	-	-	μA	V_{IH}; TTL
		-	-	|80|	μA	V_{IL}; AL and TTL and TTL (degraded, used for CIF)
Pull-down current [5]	I_{PDL} CC	-	-	|105|	μA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	μA	V_{IH}; TTL
		|19|	-	-	μA	V_{IL}; AL and TTL
		|15|	-	-	μA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-1700	-	1700	nA	$T_J \leq 150°C$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-2100	-	2100	nA	$T_J \leq 150°C$; else
		-3000	-	3000	nA	$T_J \leq 170°C$; (0.1 * V_{FLEX}) < V_{IN} < (0.9 * V_{FLEX})
		-4000	-	4000	nA	$T_J \leq 170°C$; else
Input high voltage level	V_{IH} SR	0.7 * V_{FLEX}	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

Table 3-12 RFast 3.3V pad (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * V_{FLEX}	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Pin capacitance	C_{IO} CC	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.

2) Rise / fall times are defined 10% - 90% of pad supply voltage.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.

5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-13 Class D

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq 150°C$; else
		-300 (1)	-	300 (1)	nA	$T_J \leq 150°C$; PDD option available
		-300	-	300	nA	$T_J \leq 170°C$; else
		-600 (2)	-	600 (2)	nA	$T_J \leq 170°C$; PDD option available
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added

1) For AN11, 100 nA need to be added.

2) For AN11, 200 nA need to be added .

Table 3-14 ADC Reference Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current for V_{AREF}	I_{OZ2} CC	-1	-	1	µA	$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; used for EVADC
		-2	-	2	µA	$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; used for EVADC
		-3.5	-	3.5	µA	$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EVADC
		-7	-	7	µA	$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EVADC

Table 3-15 Driver Mode Selection for Slow Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	X	0	Speed grade 1	medium sharp edge (sm)
X	X	1	Speed grade 2	medium medium edge (m)

Table 3-16 Driver Mode Selection for Fast Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	Reserved, do not use this combination

Table 3-17 Driver Mode Selection for RFast Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	RGMII function is active

3.6 High performance LVDS Pads

This LVDS pad type is used for the high speed chip to chip communication interface of the new TC35x. It consists of a LVDS pad and a fast pad.

C_L = 2.5 pF for all LVDS parameters.

Table 3-18 LVDS - IEEE standard LVDS general purpose link (GPL)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range	V_I SR	0	-	1600	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ±10%
		0	-	2400	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ±20%
Input differential threshold	V_{idth} SR	-100	-	100	mV	Driver ground potential difference < 925 mV
Receiver differential input impedance	R_{in} CC	80	-	120	Ohm	$V_I \leq 2400$ mV
Duty cycle	t_{duty} CC	45	-	55	%	

Note: Driver ground potential difference is defined as driver-receiver potential difference, that can result in a voltage shift when comparing driver output voltage level and receiver input voltage level of a transmitted signal.

*Note: R_T in table 'LVDS - IEEE standard LVDS general purpose Link (GPL)' is as termination resistor of the receiver according to figure 3-5 in IEEE Std 1596.3-1996 and is represented in **Figure 3-1** either by R_{in} or by R_T=100Ohm but not both. If R_T is mentioned in column Note / Test Condition always the internal resistor R_{in} in **Figure 3-1** is the selected one.*

default after start-up = CMOS function

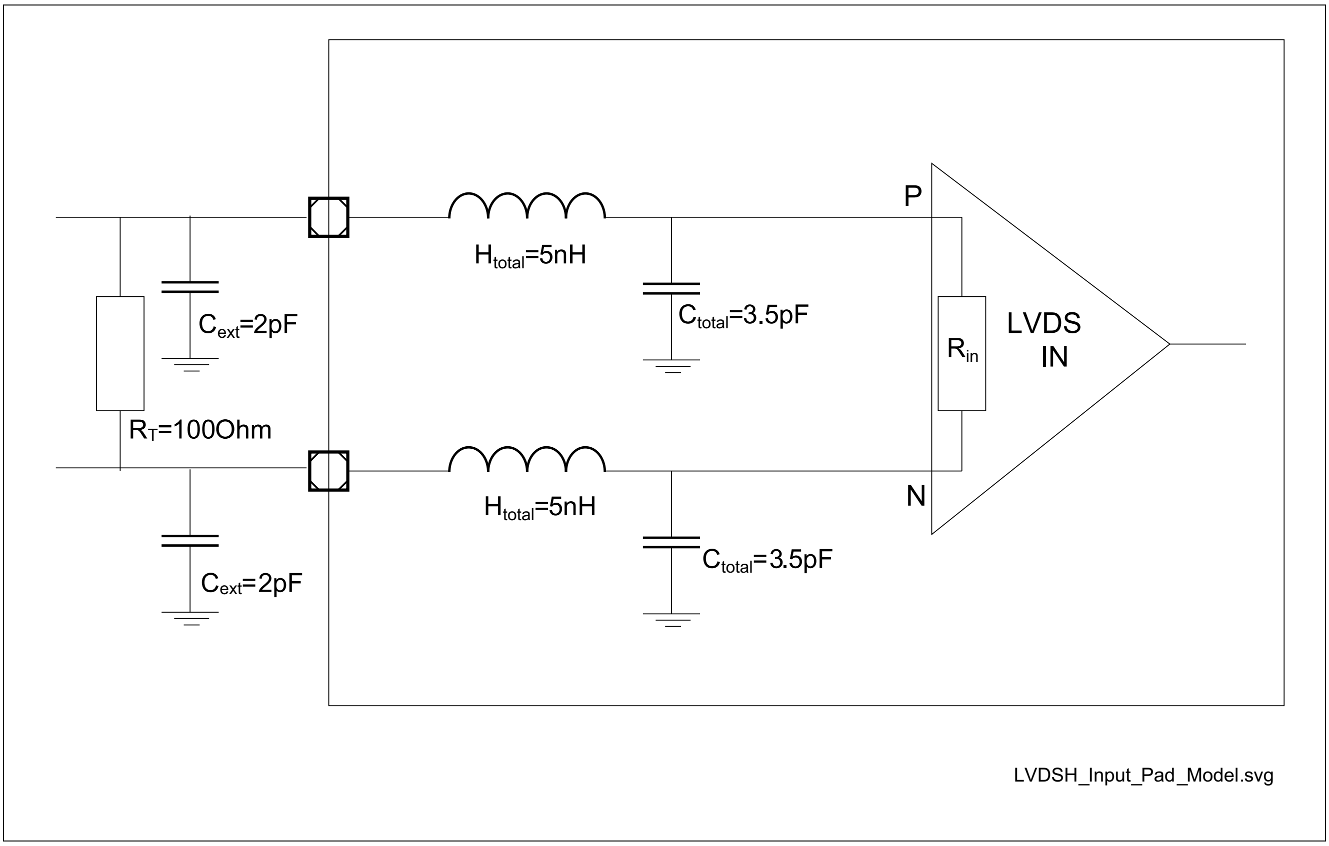


Figure 3-1 LVDS pad Input model

3.7 VADC Parameters

The accuracy of the converter results depends on the reference voltage range. The parameters in the table below are valid for a reference voltage range of (V_{AREF} - V_{AGND}) >= 4.5 V. If the reference voltage range is below 4.5 V by a factor of k (e.g. 3.3 V), the accuracy parameters increase by a factor of 1.1/k (e.g. 1.1 × 4.5 / 3.3 = 1.5).

Noise on supply voltage V_{DDM} influences the conversion. The accuracy (error) parameters are defined for a supply voltage ripple of below 20 mVpp up to 10 MHz (below 5 mVpp above 10 MHz).

Digital functions overlapping analog inputs influence accuracy.

The total unadjusted error (TUE) is defined without noise. The overall deviation depends on TUE and EN_{RMS} (depending on the noise distribution). Example: For a noise distribution of 4 sigma and EN_{RMS} = 1.0 the additional peak-peak noise error is ±(4 × 1.0) = 8 LSB_{12}.

Fast compare operations are executed with 10-bit values.

The noise reduction feature improves the result by adding additional conversion steps. The conversion times, therefore, increase accordingly (4 × t_{ADCI} + 3 × t_{ADC} for each of 1, 3, or 7 steps).

Table 3-19 VADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EVADC IVR output voltage	V_{DDK} CC	1.13	-	1.33	V	Measured at low temperature.
Deviation of IVR output voltage V_{DDK}	dV_{DDK} CC	-2	-	2	%	Based on device-specific value
Analog reference voltage [1]	V_{AREF} SR	4.5	5.0	V_{DDM} + 0.05	V	4.5 V ≤ V_{DDM} ≤ 5.5 V
		2.97	3.3	V_{DDM} + 0.05	V	2.97 V ≤ V_{DDM} < 4.5 V
Analog reference ground	V_{AGND} SR	V_{SSM}	V_{SSM}	V_{SSM}	V	V_{SSM} and V_{AGND} are connected together
Analog input voltage range	V_{AIN} SR	V_{AGND}	-	V_{AREF}	V	V_{AIN} is limited by the respective pad supply voltage; see pin configuration (buffer type)
Converter reference clock	f_{ADCI} SR	16	40	53.33	MHz	4.5 V ≤ V_{DDM} ≤ 5.5 V
		16	20	26.67	MHz	2.97 V ≤ V_{DDM} < 4.5 V
Total Unadjusted Error [2] [3]	TUE CC	-4	-	4	LSB	12-bit resolution for primary/secondary groups, 10-bit resolution for fast compare channels
INL Error [2]	EA_{INL} CC	-3	-	3	LSB	
DNL error [2][4]	EA_{DNL} CC	-1	-	3	LSB	
Gain Error [2]	EA_{GAIN} CC	-3.5	-	3.5	LSB	
Offset Error [2][3]	EA_{OFF} CC	-4	-	4	LSB	

Table 3-19 VADC 5V (cont'd)

Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**
		Min.	**Typ.**	**Max.**		
RMS Noise [2)5) 6)]	EN_{RMS} CC	-	0.5	0.8	LSB	Noise reduction level 3
		-	0.5	1.0	LSB	Standard conversion
Reference input charge consumption per conversion (from V_{AREF}) [7) 8) 9)]	Q_{CONV} CC	-	-	20	pC	V_{AIN} = 0 V (worst case), precharging disabled
		-	-	10	pC	V_{AIN} = 0 V (worst case), precharging enabled, $V_{\mathrm{DDM}} - 5\% < V_{\mathrm{AREF}} < V_{\mathrm{DDM}} + 50$ mV
Switched capacitance of an analog input	C_{AINS} CC	-	2.5	3.4	pF	Input buffer disabled
Analog input charge consumption [10)]	Q_{AINS} CC	-	-	4.4	pC	Primary groups; $V_{\mathrm{AIN}} = V_{\mathrm{AREF}}$; V_{DDM} = 5.0 V; input buffer enabled; $T_{\mathrm{J}} \leq 150°\mathrm{C}$
		-	-	4.8	pC	Primary groups; $V_{\mathrm{AIN}} = V_{\mathrm{AREF}}$; V_{DDM} = 5.0 V; input buffer enabled; $T_{\mathrm{J}} > 150°\mathrm{C}$
Sampling time	t_{S} SR	300	-	-	ns	Primary group, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer disabled
		500	-	-	ns	Primary group, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer enabled
		600	-	-	ns	Primary group, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer disabled
		800	-	-	ns	Primary group, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer enabled
Sampling time for calibration	t_{SCAL} SR	50	-	-	ns	4.5 V ≤ V_{DDM} ≤ 5.5 V
		300	-	-	ns	2.97 V ≤ V_{DDM} < 4.5 V
Input buffer switch-on time	t_{BUF} CC	-	0.4	1	µs	
Wakeup time	t_{WU} CC	-	0.1	0.2	µs	Fast standby mode
		-	1.6	3	µs	Slow standby mode
Broken wire detection delay against V_{AREF}	t_{BWR} CC	-	100	-	cycles	Result above 80% of full scale range, analog input buffer disabled
Broken wire detection delay against V_{AGND}	t_{BWG} CC	-	100	-	cycles	Result below 10% of full scale range, analog input buffer disabled

Table 3-19 VADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Converter diagnostics unit resistance [11]	R_{CSD} CC	45	-	75	kOhm	
Converter diagnostics voltage accuracy	dV_{CSD} CC	-10	-	10	%	Percentage refers to V_{DDM}
Resistance of the multiplexer diagnostics pull-up device	R_{MDU} CC	30	-	42	kOhm	$0\ \mathrm{V} \leq V_{\mathrm{IN}} \leq 0.9^* V_{\mathrm{DDM}}$, Automotive Levels
		56	-	78	kOhm	$0\ \mathrm{V} \leq V_{\mathrm{IN}} \leq 0.9^* V_{\mathrm{DDM}}$, TTL Levels
Resistance of the multiplexer diagnostics pull-down device	R_{MDD} CC	43	-	58	kOhm	$0.1^*V_{\mathrm{DDM}} \leq V_{\mathrm{IN}} \leq V_{\mathrm{DDM}}$, Automotive level
		18	-	25	kOhm	$0.1^*V_{\mathrm{DDM}} \leq V_{\mathrm{IN}} \leq V_{\mathrm{DDM}}$, TTL level
Resistance of the pull-down test device	R_{PDD} CC	-	-	0.3	kOhm	Measured at pad input voltage $V_{\mathrm{IN}} = V_{\mathrm{DDM}} / 2$.

1) These limits apply to the standard reference input as well as to the alternate reference input.

2) Parameter depends on reference voltage range and supply ripple, see introduction.
Resulting worst case combined error is arithmetic combination of TUE and EN_{RMS}.
Tests are done with postcalibration disabled, after completing the startup calibration.

3) Analog inputs mapped to pads of the type SLOW influence accuracy. The values for this parameter increase by 3 LSB_{12}.

4) Monotonic characteristic, no missing codes when calibrated.

5) Parameter $\mathrm{EN}_{\mathrm{RMS}}$ refers to a 1 sigma distribution.

6) Analog inputs mapped to pads of the type SLOW the RMS noise (EN_{RMS}) can be up to 2 LSB_{12} (soft switching for DC/DC enabled).

7) For reduced reference voltages VAREF < 3.375V, the consumed charge QCONV is reduced by the factor of k2 = VAREF [V] / 3.375. For reduced reference voltages 4.5V < VAREF ≤ 3.375V, QCONV is not reduced.

8) Maximum charge increases by 15 pC when BWD (Broken Wire Detection) is active.

9) Fast compare channels only consume 1/3 of the charge for a primary/secondary group.

10) For analog inputs with overlaid digital GPIOs or with PDD function this value increases by 1 pC.

11) Use a sample time of at least 1.1 µs to enable proper settling of the test voltage.

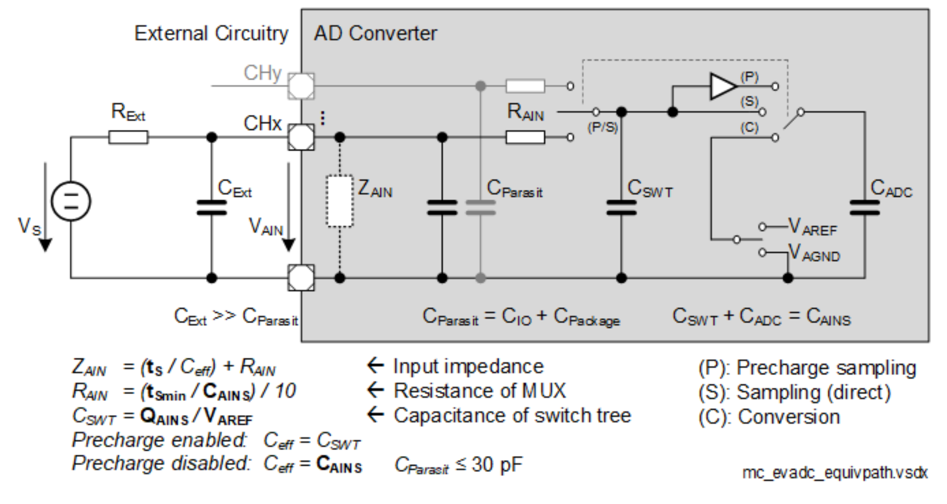


Figure 3-2 Equivalent Circuitry for Analog Inputs

3.8 MHz Oscillator

OSC_XTAL is used as accurate and exact clock source. OSC_XTAL supports 16 MHz to 40 MHz crystals external outside of the device. Support of ceramic resonators is also provided.

Table 3-20 OSC_XTAL

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-70	-	70	µA	V_{IN}>0V ; V_{IN}<V_{EXT}
Oscillator frequency	f_{OSC} SR	4	-	40	MHz	Direct Input Mode selected, if shaper is not bypassed
		16	-	40	MHz	External Crystal Mode selected
Oscillator start-up time	t_{OSCS} CC	-	-	3 (1)	ms	20MHz ≤ f_{OSC} and 8pF load capacitance
Input voltage at XTAL1 (2)	V_{IX} SR	-0.7	-	V_{EXT} + 0.5	V	If shaper is not bypassed
Input amplitude (peak to peak) at XTAL1	V_{PPX} SR	0.3*V_{EXT}	-	V_{EXT} + 1.0	V	If shaper is not bypassed; f_{OSC} > 25MHz
		0.35*V_{EXT}	-	V_{EXT} + 1.0	V	If shaper is not bypassed; f_{OSC} ≤ 25MHz
Internal load capacitor	C_{L0} CC	1.30	1.40	1.55	pF	enabled via bit OSCCON.CAP0EN
Internal load capacitor	C_{L1} CC	3.05	3.35	3.70	pF	enabled via bit OSCCON.CAP1EN
Internal load capacitor	C_{L2} CC	7.85	8.70	9.55	pF	enabled via bit OSCCON.CAP2EN
Internal load capacitor	C_{L3} CC	12.05	13.35	14.65	pF	enabled via bit OSCCON.CAP3EN
Internal load stray capacitor between XTAL1 and XTAL2	C_{XINTS} CC	1.15	1.20	1.25	pF	
Internal load stray capacitor between XTAL1 and ground	C_{XTAL1} CC	-	2.5	4	pF	
Duty cycle at XTAL1 (3)	DC_{X1} SR	35	-	65	%	V_{XTAL1} = 0.5*V_{PPX}
Absolute RMS jitter at XTAL1 (3)	J_{ABSX1} SR	-	-	28	ps	10 KHz to f_{OSC}/2
Slew rate at XTAL1 (3)	SR_{XTAL1} SR	0.3	-	-	V/ns	Maximum 30% difference between rising and falling slew rate

1) This value depends on the frequency of the used external crystal. For faster crystal frequencies this value decrease.

2) For Supply (V_{EXT} < 5.3V V_{IX}) min could be down to -0.9V. For XTAL1 an input level down to -0.9V will not cause a damage or a reliability problem operating with an external crystal.

3) Square wave input signal for XTAL1.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

3.9 Back-up Clock

The back-up clock provides an alternative clock source.

Table 3-21 Back-up Clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Back-up clock accuracy before trimming	f_{BACKUT} CC	70	100	130	MHz	$V_{\mathrm{EXT}} \geq 2.97\mathrm{V}$
Back-up clock accuracy after trimming [1]	f_{BACKT} CC	98	100	102	MHz	$V_{\mathrm{EXT}} \geq 2.97\mathrm{V}$
Standby clock	f_{SB} CC	25	70	110	kHz	$V_{\mathrm{EXT}} \geq 2.97\mathrm{V}$

1) A short term trimming providing the accuracy required by LIN communication is possible by periodic trimming every 2 ms for temperature and voltage drifts up to temperatures of 125 celcius

3.10 Temperature Sensor

Table 3-22 DTS PMS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion [1]	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Calibration reference accuracy	T_{CALACC} CC	-1	-	1	°C	calibration points @ T_J=-40°C and T_J=127°C
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) After warm reset t_M is not restarted and is measured from last conversion.

Table 3-23 DTS Core

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion [1]	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Temperature difference between on chip temperature sensors	ΔT CC	-3	-	3	°C	
Calibration reference accuracy	T_{CALACC} CC	-2	-	2	°C	calibration points @ T_J=-40°C and T_J=127°C
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) After warm reset t_M is not restarted and is measured from last conversion.

3.11 Power Supply Current

The total power supply current defined below consists of leakage and switching component.

Application relevant values are typically lower than those given in the following table and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

The operating conditions for the parameters in the following table are:

The ADAS realistic (real) power pattern defines the following conditions:

- T_J = 150 °C
- $f_{SRI} = f_{CPUx}$ = 300 MHz
- f_{GTM} = 100 MHz
- f_{SPU} = 300 MHz; (FFT length =512, complex windowing)
- $f_{SPB} = f_{STM} = f_{BAUD1} = f_{BAUD2} = f_{ASCLINx}$ = 100 MHz
- V_{DD} = 1.275 V
- $V_{DDP3/EXT/FLEX/EVRSB}$ = 3.366 V
- V_{DDM} = 5.1 V
- CPU0/CPU1 (IPC=1.2) and CPU2 (IPC=0.6) cores are active including CPU0 lockstep core; CPU1 is active without lockstep core
- the following modules are inactive: HSM, GETH, I2C, FCE, and MTU

The ADAS maximum (max) power pattern defines the following conditions:

- T_J = 150 °C
- $f_{SRI} = f_{CPUx}$ = 300 MHz
- f_{GTM} = 100 MHz
- f_{SPU} = 300 MHz; (FFT length =2048, complex windowing)
- $f_{SPB} = f_{STM} = f_{BAUD1} = f_{BAUD2} = f_{ASCLINx}$ = 100 MHz
- V_{DD} = 1.375 V
- $V_{DDP3/EXT/FLEX/EVRSB}$ = 3.63 V
- V_{DDM} = 5.5 V
- CPU0/CPU1 (IPC=1.2) and CPU2 (IPC=0.6) cores are active including CPU0/CPU1 lockstep cores
- the following modules are inactive: GETH, I2C, FCE, and MTU

Table 3-24 Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\sum$ Sum of I_{DD} core and peripheral supply currents (incl. $I_{DDPORST}$+ $\sum I_{DDCx0}$+ $\sum I_{DDCxx}$+ I_{DDGTM}+I_{DDSB})	I_{DDRAIL} CC	-	-	1500	mA	ADAS max power pattern
		-	-	1275	mA	ADAS real power pattern
I_{DD} core current during active power-on reset (PORST pin held low). Leakage current of core domain. [1]	$I_{DDPORST}$ CC	-	-	210	mA	V_{DD} = 1.275V; T_J=125°C
		-	-	360	mA	V_{DD} = 1.275V; T_J=150°C

Table 3-24 Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of I_{DDP3} 3.3 V supply currents	$I_{DDP3RAIL}$ CC	-	-	45	mA	max power pattern incl. Flash read current and Dflash programming current.
		-	-	36 [2]	mA	real power pattern incl. Flash read current and Dflash programming current.
∑ Sum of external I_{EXT} supply currents (incl. $I_{EXTFLEX}+I_{EVRSB}+I_{EXTLVDS}$)	$I_{EXTRAIL}$ CC	-	-	44	mA	max power pattern
		-	-	39	mA	real power pattern
I_{EXT} and I_{FLEX} supply current	$I_{EXTFLEX}$ CC	-	-	27 [3]	mA	real power pattern with port activity absent; PORST output inactive.
I_{EVRSB} supply current [1]	I_{EVRSB} CC	-	-	8.5	mA	real power pattern; PMS/EVR module current considered without SCR and Standby RAM during RUN mode.
∑ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC}+I_{DDMEDSADC}$)	I_{DDM} CC	-	-	6	mA	real power pattern; sum of currents of EVADC modules
∑ Sum of all currents (incl. $I_{EXTRAIL}+I_{DDMRAIL}+I_{DDx3RAIL}+I_{DD}$)	I_{DDTOT} CC	-	-	1356	mA	real power pattern; T_J=150°C
∑ Sum of all currents with DC-DC EVRC regulator active [4]	$I_{DDTOTDC3}$ CC	-	-	750	mA	real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 3.3V; T_J=150°C
∑ Sum of all currents (SLEEP mode) [1]	I_{SLEEP} CC	-	-	25	mA	All CPUs in idle, All peripherals in sleep, $f_{SRI/SPB}$ = 1 MHz via LPDIV divider; T_J = 25°C
∑ Sum of all currents (STANDBY mode) drawn at V_{EVRSB} supply pin [5]	$I_{STANDBY}$ CC	-	-	130 [6]	µA	32 kB Standby RAM block active. SCR inactive. Power to remaining domains switched off. T_J = 25°C; V_{EVRSB} = 5V
Maximum power dissipation [7]	PD SR	-	-	2360	mW	max power pattern
		-	-	1900	mW	real power pattern

1) Limits are defined for real power pattern (V_{DD}=1.275V). For max power pattern limit has to be multiplied by the factor 1.22.

2) Realistic Pflash read pattern with 50% Pflash bandwidth utlilization and a code mix of 50% 0s and 50% 1s. A common decoupling capacitor of atleast 100nF for (V_{DDP3}) is used. Continuous Dflash programming in burst mode with 3.3 V supply and realistic Pflash read access in parallel. Erase currents of the corresponding flash modules are less than the respective programming currents at V_{DDP3} pin. Programming and erasing flash may generate transient current spikes of up to 45 mA / 20 ns
which are handled by the decoupling and buffer capacitors. This parameter is relevant for external power supply dimensioning and not for thermal considerations.

3) The current consumption includes only minimal port activity.

4) The total current drawn from external regulator is estimated with 72% EVRC SMPS regulator efficiency. IDDTOTDCx is calculated from IDDTOT using the scaled core current [(IDD x VDD)/(VinxEfficiency)] and constitutes all other rail currents and IDDM.

5) The same current limits apply also for the other power pattern.

6) ∑ Sum of all currents during RUN mode at VEVRSB supply pin is less than (IEVRSB + 4 mA Standby RAM current + ISCRSB if SCR active). ∑ It is recommended to have atleast 100 nF decoupling capacitor at this pin. 32kB of Standby SRAM contributes less than 10uA to ISTANDBY current.

7) The values are only valid if all supplies are applied from external and do not contain the power losses of EVR33 and EVRC.

Table 3-25 Module Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DDP3} supply current for programming of a Pflash or Dflash bank 1)	$I_{DDP3PROG}$ CC	-	-	25	mA	Pflash 3.3V programming current adder when using external 3.3V supply.
		-	-	9 2)	mA	Pflash 3.3V programming current adder when using external 5V supply.
I_{EXT} supply current added by LVDS pads in LVDS mode 1)	$I_{EXTLVDS}$ CC	-	-	9	mA	real power pattern; 6 pairs of LVDS pins active with receive function (RIF Interface)
∑ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC}+I_{DDMEDSADC}$)	I_{DDM} CC	-	-	6	mA	real power pattern; current for EVADC modules; 2 EVADC modules active.
		-	-	6 3)	mA	max power pattern; current for EVADC modules; all EVADC modules active.
I_{DDP3} supply current for erasing of a Pflash or Dflash bank	$I_{DDP3ERASE}$ CC	-	-	25	mA	Pflash 3.3V erasing current adder when using external 3.3V supply.

Table 3-25 Module Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at V_{EVRSB} supply pin	I_{SCRSB} CC	-	-	7	mA	SCR power pattern incl. PMS current consumption with fback clock active; f_{SYS_SCR} = 20MHz; T_J=150°C
		-	0.150	-	mA	SCR power pattern incl. PMS current consumption with fback inactive; fSYS_SCR = 70kHz; T_J=25°C
SCR 8-bit Standby Controller CPU in IDLE mode [4]	$I_{SCRIDLE}$ CC	-	-	3.5	mA	real power pattern. CPU set into idle mode.

[1] The same current limits apply also for the other power pattern.

[2] During Pflash programming at 5V, additional 2 mA is drawn at VEXT supply rail.

[3] A single VADC unit consumes 1.3 mA.

[4] Limits are defined for real power pattern (V_{DD}=1.275V). For max power pattern limit has to be multiplied by the factor 1.22.

Table 3-26 Module Core Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DD} core current of CPUx main core with CPUx lockstep core inactive	I_{DDCx0} CC	-	-	70	mA	max power pattern; IPC=1.2
		-	-	45	mA	real power pattern; IPC=0.6
I_{DD} core current of CPUx main core with CPUx lockstep core active	I_{DDCxx} CC	-	-	I_{DDCx0} + 50	mA	max power pattern; IPC=1.2
		-	-	I_{DDCx0} + 40	mA	real power pattern; IPC=0.6
I_{DD} core current added by HSM	I_{DDHSM} CC	-	-	20 [1]	mA	max power pattern; HSM running at 100MHz.
I_{DD} core current added by SPU	I_{DDSPU1} CC	-	-	360 [2]	mA	CTRL.DIV = 00; SPU @ 300 MHz; FFT length 2048; DATSRC=EMEM; complex windowing

Table 3-26 Module Core Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DD} core current added by SPU	I_{DDSPU2} CC	-	-	310 2)	mA	CTRL.DIV = 00; SPU @ 300 MHz; FFT length 512; DATSRC=EMEM; complex windowing
I_{DD} core dynamic current load jump during IDDSPU1 pattern.	$I_{DDSPULJ1}$ CC	-	-	390 3)	mA	CTRL.DIV = 00; SPU @ 300 MHz; FFT length 2048; DATSRC=EMEM; complex windowing
I_{DD} core dynamic current load jump during IDDSPU2 pattern.	$I_{DDSPULJ2}$ CC	-	-	310 3)	mA	CTRL.DIV = 00; SPU @ 300 MHz; FFT length 512; DATSRC=EMEM; complex windowing
I_{DD} core dynamic current added by LBIST	$I_{DDLBIST}$ CC	-	-	200 4)	mA	LBIST Configuration A; 1.2V ≤ V_{DD}
I_{DD} core dynamic current added by MBIST	$I_{DDMBIST}$ CC	-	-	200	mA	Non Destructive Test (4N) on all RAMs sequentially; fMBIST = 300MHz; tMBIST < 6ms.

1) The current consumption includes basic HSM activity incl. AES module.

2) The current is estimated as the sum of the SPU base load current at clock activation and average current caused by SPU dynamic activity as defined in the conditions. Secondary Voltage Monitor over-voltage threshold shall be set to VDD + 10% and under-voltage threshold shall be set to VDD - 9% respectively.
During the SPU operational phase for $I_{DDSPU1/2}$ usecase, the externally supplied V_{DD} voltage has to be equal or greater than 1.225V (V_{DD} nominal - 2%) for static accuracy part and the overall static and dynamic at the V_{DD} supply pin shall be limited to (V_{DD} nominal -8%).

3) The dynamic current load jump during SPU activity as defined by the conditions observed at the VDD pin beyond a settling time duration of 20 us.

4) LBIST is executed either during start-up phase or can be triggered by application software. Secondary voltage monitors are inactive during the LBIST execution time (t_{LBIST}).
During the start-up phase externally supplied V_{DD} voltage has to be equal or greater than 1.2V (V_{DD} nominal - 4%) for static accuracy.
If V_{DD} is supplied internally by EVRC, EVRC takes care not to violate the V_{DD} 1.2V static under voltage limit.

3.11.1 Calculating the 1.25 V Current Consumption

The current consumption of the 1.25 V rail is composed of two parts:

- Static current consumption
- Dynamic current consumption

The static current consumption is related to the device temperature T_J and the dynamic current consumption depends on the configured clocking frequencies and the software application executed. These two parts need to be added in order to get the rail current consumption.

$$I_0 = 4,8379\left[\frac{mA}{C}\right] \quad e^{0,02224 \quad T_J[C]} \tag{3.1}$$

$$I_0 = 14,2656\left[\frac{mA}{C}\right] \quad e^{0,02121 \quad T_J[C]} \tag{3.2}$$

Equation (3.1) defines the typical static current consumption and **Equation (3.2)** defines the maximum static current consumption. Both functions are valid for V_{DD} = 1.275 V.

3.12 Power Supply Infrastructure and Supply Start-up

3.12.1 Supply Ramp-up and Ramp-down Behavior

Start-up slew rates for supply rails shall comply to SR (see **Table 3-30** Supply Ramp).

3.12.1.1 Single Supply mode (a)

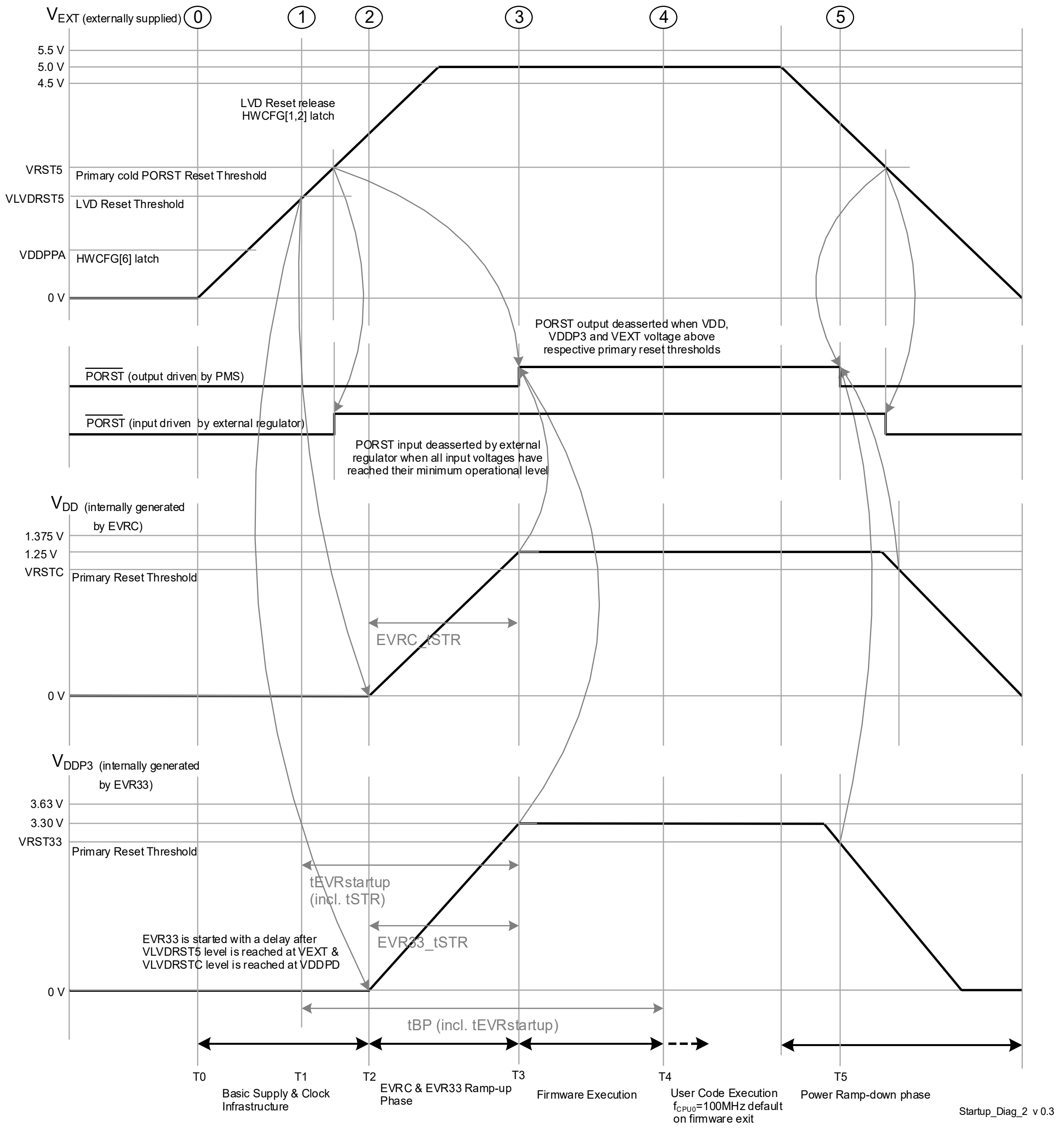


Figure 3-3 Single Supply mode (a) - V_{EXT} (5 V) single supply

V_{EXT} = 5 V single supply mode. V_{DD} and V_{DDP3} are generated internally by the EVRC and EVR33 internal regulators.

- The rate at which current is drawn from the external regulator (dIEXT /dt) is limited during the basic infrastructure and EVRx regulator start-up phase (T0 up to T2) to a maximum of 100 mA with 100 us settling time. Start-up slew rates for supply rails shall comply to parameter SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.
- Furthermore it is also ensured that the current drawn from the regulator (dIDD/dt) is limited during the Firmware start-up phase (T3 up to T4) to a maximum of 100 mA with 100 us settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (V_{DD}, V_{DDP3} or V_{EXT}) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of up to 150 mA (dIDD) is expected.
- The power sequence as shown in **Figure 3-3** is enumerated below
  - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started.The supply mode is evaluated based on the HWCFG[1:2,4,5,6] and TESTMODE pins. These events are initiated after LVD reset release at T1 after V_{EXT} ad VEVRSB supply rails have reached VLVDRST5 level and internal pre-regulator VDDPD voltage has reached VLVDRSTC level.
  - T2 refers to the point in time where consequently a soft start of EVRC and EVR33 regulators are initiated. PORST (input) does not have any affect on EVR33 or EVRC output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the tSTR time to avoid overshoots.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVRC and EVR33 regulators have ramped up. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as tEVRstartup.
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP.
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (V_{DD}, V_{DDP3} or V_{EXT}) drop below their respective primary under-voltage reset thresholds.

3.12.1.2 Single Supply mode (e)

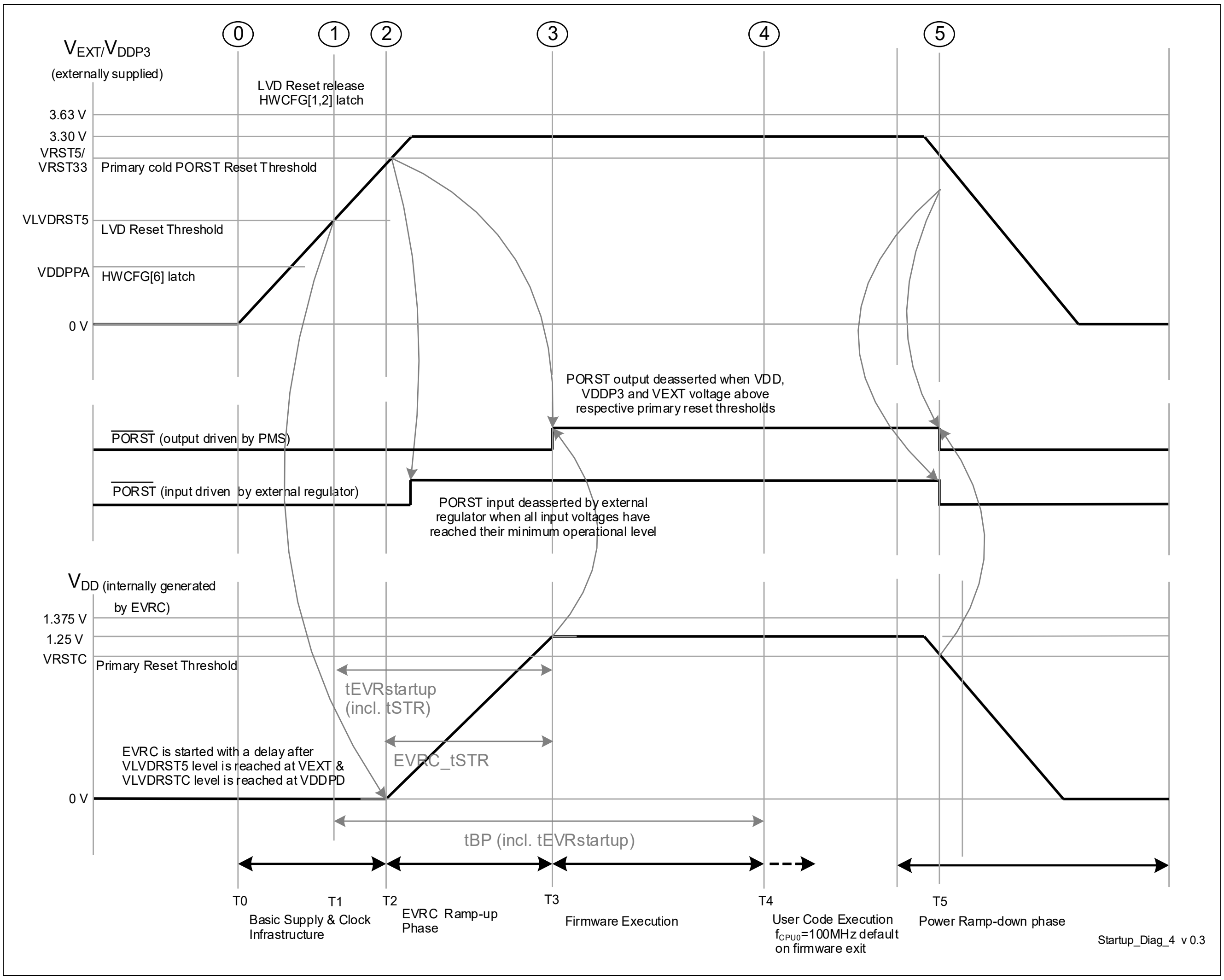


Figure 3-4 Single Supply mode (e) - (V_{EXT} & V_{DDP3}) 3.3 V single supply

V_{EXT} = V_{DDP3} = 3.3 V single supply mode. V_{DD} is generated internally by the EVRC regulator.

- The rate at which current is drawn from the external regulator (dIEXT /dt) is limited in the Start-up phase to a maximum of 100 mA with 100 us settling time. Start-up slew rates for supply rails shall comply to SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (V_{DD}, V_{DDP3} or V_{EXT}) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of up to 150 mA (dIDD) is expected.

- The power sequence as shown in **Figure 3-4** is enumerated below
  - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started.The supply mode is evaluated based on the HWCFG[1:2,4,5,6] and TESTMODE pins. These events are initiated after LVD reset release at T1 after V_{EXT} ad VEVRSB supply rails have reached VLVDRST5 level and internal pre-regulator VDDPD voltage has reached VLVDRSTC level.
  - T2 refers to the point in time where consequently a soft start of EVRC regulator is initiated. PORST (input) does not have any affect on EVRC output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the tSTR time to avoid overshoots.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVRC regulator has ramped up. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as tEVRstartup.
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP.
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (V_{DD}, V_{DDP3} or V_{EXT}) drop below their respective primary under-voltage reset thresholds.

3.12.1.3 External Supply mode (d)

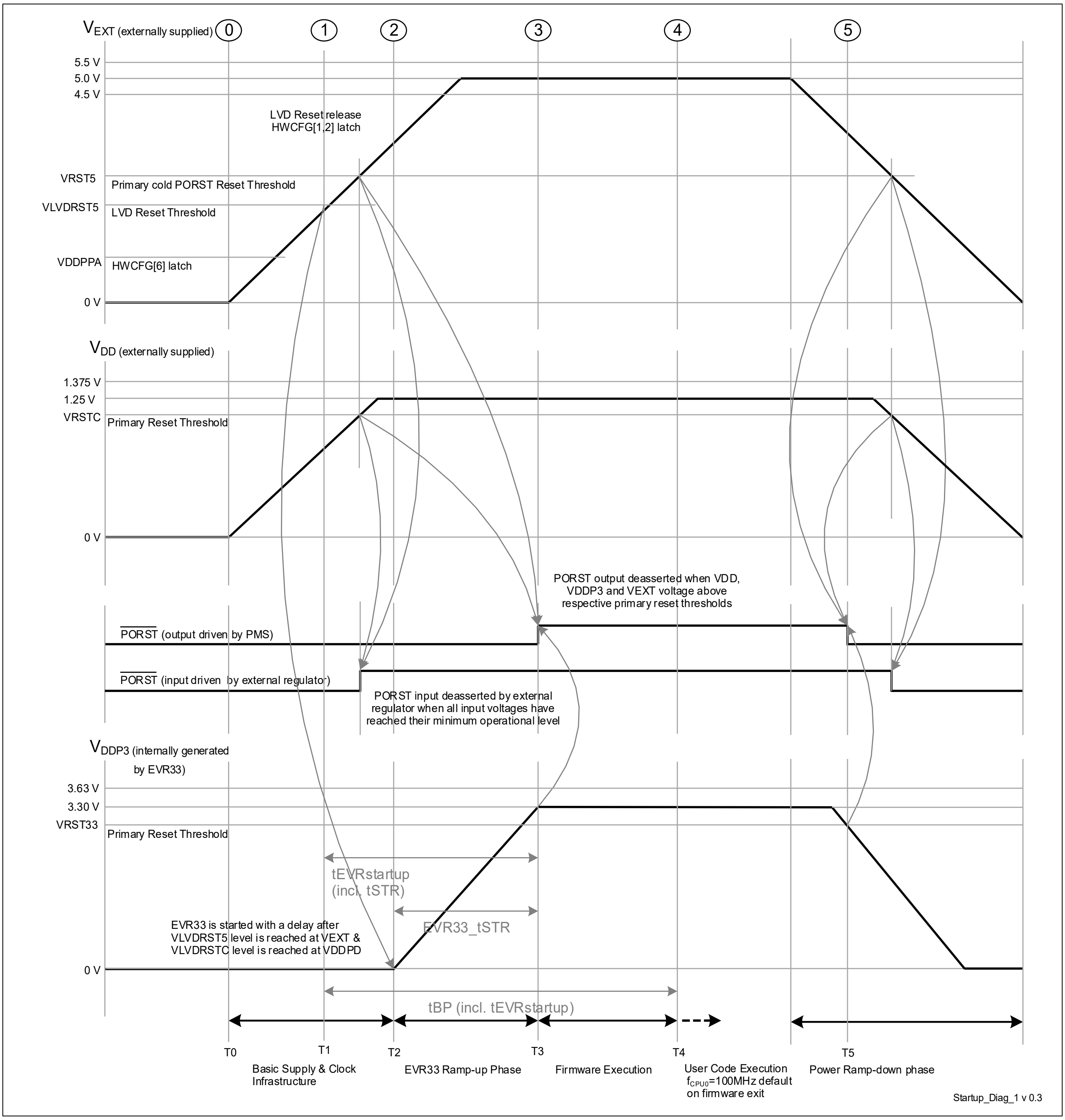


Figure 3-5 External Supply mode (d) - V_{EXT} and V_{DD} externally supplied

V_{EXT} = 5 V and V_{DD} supplies are externally supplied. 3.3V is generated internally by the EVR33 regulator.

- External supplies V_{EXT} and V_{DD} may ramp-up or ramp-down independent of each other with regards to start, rise and fall time(s). Start-up slew rates for supply rails shall comply to SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification. It is expected that during start-up, V_{EXT} ramps up before V_{DD} rail. Incase V_{DD} voltage rail is ramped up before V_{EXT}; V_{DD} supply overshoots during start-up shall be limited within the operational voltage range.

- The rate at which current is drawn from the external regulator (dIEXT /dt or dIDD /dt) is limited in the Start-up phase to a maximum of 100 mA with 100 us settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until all the external supplies are above their primary reset thresholds.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (V_{DD}, V_{DDP3} or V_{EXT}) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of up to 150 mA (dIDD) is expected.
- The power sequence as shown in **Figure 3-5** is enumerated below
  - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started. The supply mode is evaluated based on the HWCFG[1:2,4,5,6] and TESTMODE pins. These events are initiated after LVD reset release at T1 after V_{EXT} ad VEVRSB supply rails have reached VLVDRST5 level and internal pre-regulator VDDPD voltage has reached VLVDRSTC level.
  - T2 refers to the point in time where consequently a soft start of EVR33 regulator is initiated. PORST (input) does not have any affect on EVR33 output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the tSTR time to avoid overshoots.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVR33 regulators has ramped up. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as tEVRstartup.
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP.
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (V_{DD}, V_{DDP3} or V_{EXT}) drop below their respective primary under-voltage reset thresholds.

3.12.1.4 External Supply mode (h)

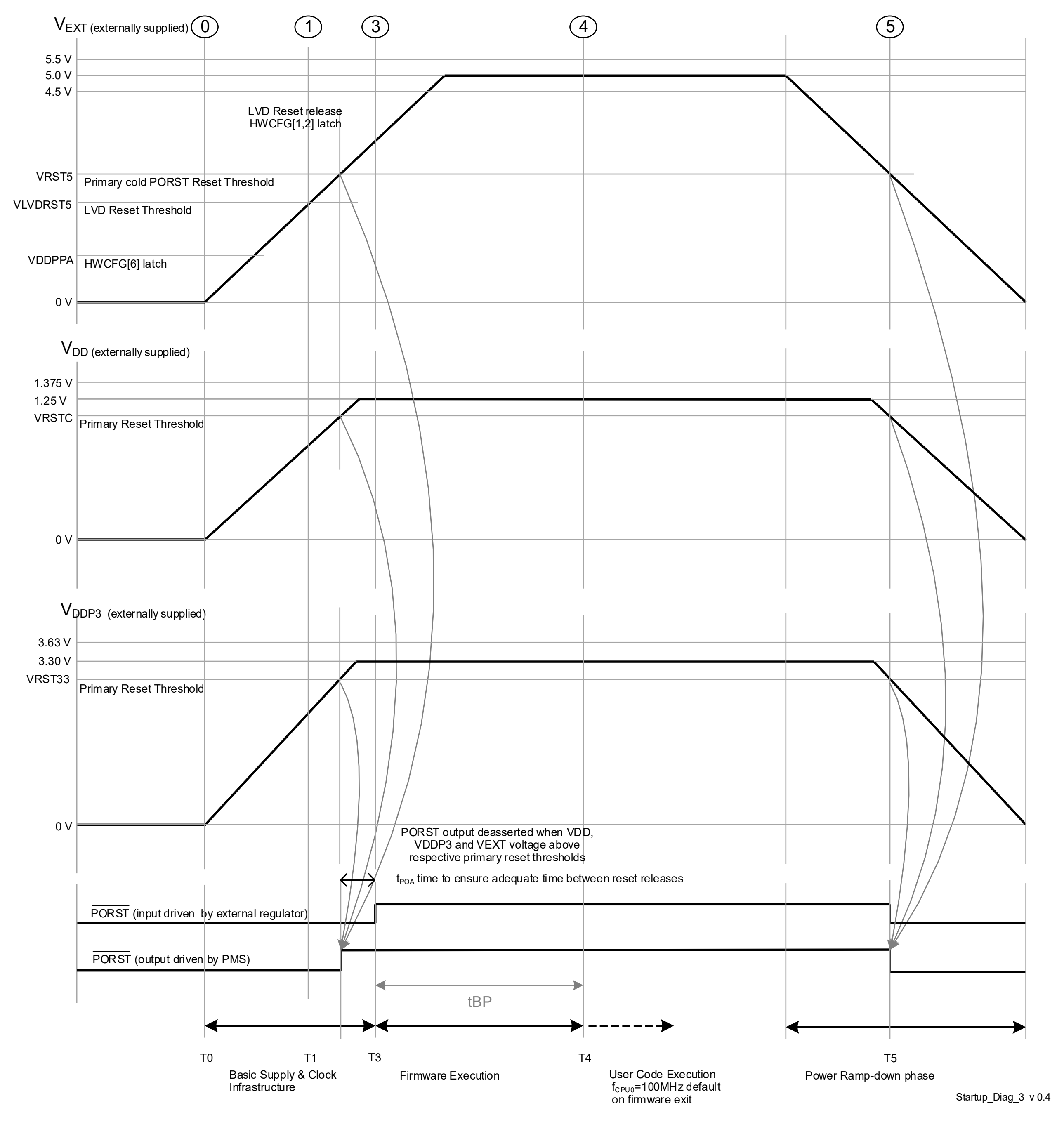


Figure 3-6 External Supply mode (h) - V_{EXT}, V_{DDP3} & V_{DD} externally supplied

All supplies, namely V_{EXT}, V_{DDP3} & V_{DD} are externally supplied.

- External supplies V_{EXT}, V_{DDP3} & V_{DD} may ramp-up or ramp-down independent of each other with regards to start, rise and fall time(s). Start-up slew rates for supply rails shall comply to SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification. It is expected that during start-up, V_{EXT} ramps up before V_{DDP3} and V_{DD} rails. Incase smaller voltage rails are ramped up before V_{EXT}; V_{DD} and V_{DDP3} supply overshoots during start-up shall be limited within the operational voltage ranges of the respective rails.

- The rate at which current is drawn from the external regulator (dIEXT /dt, dIDD /dt or dIDDP3 /dt) is limited in the Start-up phase to a maximum of 100 mA with 100 us settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until all the external supplies are above their primary reset thresholds.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (V_{DD}, V_{DDP3} or V_{EXT}) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of up to 150 mA (dIDD) is expected.
- The power sequence as shown in **Figure 3-6** is enumerated below
  - T1 up to T3 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started. The supply mode is evaluated based on the HWCFG[1:2,4,5,6] and TESTMODE pins. These events are initiated after LVD reset release at T1 after V_{EXT} ad VEVRSB supply rails have reached VLVDRST5 level and internal pre-regulator VDDPD voltage has reached VLVDRSTC level.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated.
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP.
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided supplies (V_{DD}, V_{DDP3} or V_{EXT}) drop below their respective primary under-voltage reset thresholds.

3.13 Reset Timing

Table 3-27 Reset

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time	t_B CC	-	-	400	µs	operating with max. frequencies, with valid BMI header
System Reset Boot Time	t_{BS} CC	-	-	1.1	ms	RAM initialization and HSM boot time are not included, with valid BMI header
Cold Power on Reset Boot Time 1)	t_{BP} CC	-	-	3.1	ms	$dVEXT/dT=1V/ms$. $VEXT>VLVDRST5$. Boot time after Cold PORST including EVR ramp-up and Firmware execution time; RAM initialization and HSM boot time are not included.
		-	-	1.6	ms	Firmware execution time after PORST release without EVR ramp-up; RAM initialization and HSM boot time is not included
Minimum cold PORST reset hold time in case of power fail event issued by EVR primary monitors	t_{EVRPOR} CC	10 2)	-	-	µs	
PMS Infrastructure, EVRC and EVR33 overall start-up time till cold PORST reset release	$t_{EVRstartup}$ CC	-	-	1	ms	$dV/dT=1V/ms$. EVRC and EVR33 active
Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up	t_{POA} SR	1 3)	-	-	ms	
Configurable PORST digital filter delay in addition to analog pad filter delay	$t_{PORSTDF}$ CC	600	-	1200	ns	
Warm Reset Sequencing Delay	$t_{WARMRSTSEQ}$ CC	-	-	180	µs	
HWCFG pins hold time from ESR0 rising edge	t_{HDH} CC	$16 / f_{SPB}$	-	-	ns	

Table 3-27 Reset (cont'd)

Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**
		Min.	**Typ.**	**Max.**		
HWCFG pins setup time to ESR0 rising edge	t_{HDS} CC	0	-	-	ns	
Ports inactive after ESR0 reset active	t_{PI} CC	$8000/f_{BACKT}$	-	$18000/f_{BACKT}$	s	
Ports inactive after PORST reset active	t_{PIP} CC	-	-	160	ns	
Hold time from PORST rising edge	t_{POH} SR	150	-	-	ns	
Setup time to PORST rising edge	t_{POS} SR	0	-	-	ns	
Warm PORST reset boot time	t_{BWP} CC	-	-	1.5	ms	without RAM initalization
LBIST execution time extending the boot time	t_{LBIST} CC	-	-	6	ms	LBIST Configuration A; 1.2V ≤ V_{DD}
SCR reset boot time	t_{SCR} CC	-	-	5	µs	User Mode 0
		-	-	16	µs	User Mode 1
		-	13.3	-	µs	WDT double bit ECC, soft reset
Minimum external supplies hold time after warm reset assertion	$t_{SUPHOLD}$ CC	-	-	250	µs	external supplies are V_{EVRSB}, V_{EXT}, V_{FLEX}, V_{DDM}, V_{DDP3} and V_{DD}

1) RAM initialization add 500µs in addition.

2) Cold PORST reset is driven by uC and maintained in an extended voltage range between VDDPPA limit and absolute maximum rating VEXT/VEVRSB voltage limits.

3) The reset release on supply ramp-up or supply restoration is delayed by a voltage hysteresis of 1.5% (default value) above the undervoltage reset limit implemented on VEXT, VDDP3 and VDD rails. This mechanism helps to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released.

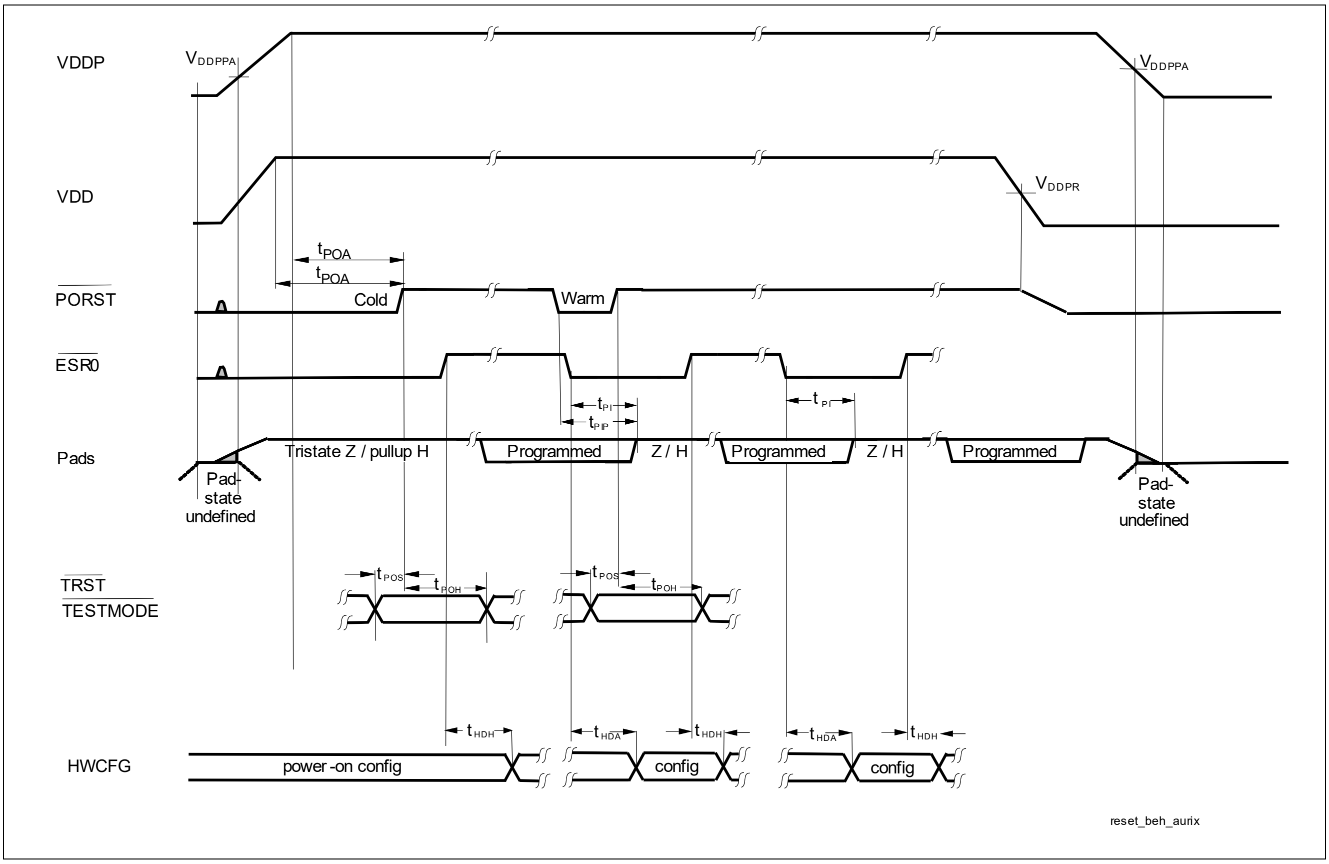


Figure 3-7 Power, Pad and Reset Timing

3.14 EVR

Table 3-28 EVR33 LDO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range	V_{IN} SR	3.60 [1]	-	5.50	V	Normal RUN mode
		2.97 [2]	-	5.50	V	Low voltage cranking mode
Output voltage operational range including load/line regulation and aging [3]	V_{OUT} CC	2.97	3.3	3.63	V	Normal RUN mode
		2.60	3.3	3.63	V	Low voltage cranking mode; I_{DDP3}=50mA
Output V_{DDx3} static voltage accuracy after trimming and aging without dynamic load/line regulation.	V_{OUTT} CC	3.225	3.3	3.375	V	Normal RUN mode
		2.78	3.3	3.375	V	Low voltage cranking mode; I_{DDP3}=50mA
Output buffer capacitance on V_{OUT}	C_{OUT} SR	1.45	2.2	3	µF	
Output buffer capacitor ESR	C_{OUTESR} SR	-	-	100 [4]	mOhm	f > 0.5MHz; f < 10MHz
Maximum output current of the regulator	I_{MAX} CC	60 [5]	-	-	mA	Normal RUN mode
Startup time	t_{STR} CC	-	500	1000	µs	Normal RUN mode
External V_{IN} supply ramp [6]	$dVin/dt$ SR	-	1	-	V/ms	
Ripple on Output Voltage	ΔV_{OUTTC} CC	-	-	33	mV	V_{EXT} ≥ 2.97V ; V_{EXT} ≤ 5.5V ; I_{OUTTC} ≥ 10mA ; I_{OUTTC} ≤ 60mA; ΔV_{OUTTC} = (peak to peak ripple / 2)
Load step response [7]	$dVout/dIout$ CC	-165	-	-	mV	Normal RUN mode; dI=10 to 60mA; dt=20ns; $Tsettle$=20us
		-	-	165	mV	Normal RUN mode; dI=60 to 10mA; dt=20ns; $Tsettle$=20us
		-180	-	-	mV	Low voltage cranking mode; dI=10 to 50 mA; dt=20ns; $Tsettle$=20us
		-	-	180	mV	Low voltage cranking mode; dI=50 to 10mA; dt=20ns; $Tsettle$=20us

Table 3-28 EVR33 LDO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line step response	$dVout/dVin$ CC	-	-	40	mV	$dVin/dT$=1V/ms; dV= 3.6 to 5V; I_{MAX}=60mA; ΔV_{OUTTC} is included
		-40	-	-	mV	$dVin/dT$=1V/ms; dV= 5 to 3.6V; I_{MAX}=60mA; ΔV_{OUTTC} is included
		-	-	280	mV	$dVin/dT$=50V/ms; dV= 3.6 to 5V; I_{MAX}=60mA
		-165	-	-	mV	$dVin/dT$=50V/ms; dV= 5 to 3.6V; I_{MAX}=60mA

1) A maximum pass device dropout voltage of 300mV is included in the minimum input voltage to ensure optimal pass device performance during normal operation.

2) VEXT Input voltage drop up to 2.97V leading to VDDP3 output voltage drop upto 2.6V can be tolerated if Flash is switched before to low performance mode.

3) No external inductive load permissible if EVR33 is used.

4) It is also recommended that the resistance of the supply trace from the pin to the EVR output capacitor is less than 100 mOhm. An additional decoupling capacitor of 100nF shall be located close to the pin before Cout.

5) IMAX is limited to 40 mA incase of Low voltage mode (cranking case) with on chip pass devices. In case EVR33 is not used, Injection current into 3.3V VDDP3 supply rail with active sink on 5V VEXT rail should be limited to 500 mA if during power sequencing 3.3V is supplied before 5V by external regulator.

6) EVR is robust against residual voltage ramp-up starting between 0 - 2.97 V. A VEXT voltage ramp range between 0.5V/min upto 120V/ms is covered in robustness validation. The generated voltage itself follows a soft ramp-up over the tSTR time to avoid overshoots.

7) Settling time is defined until output voltage is within +-1% of the mean(VOUTT) of the individual device.

Table 3-29 Supply Monitors

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Primary Undervoltage Reset threshold for V_{DDP3} before trimming 1)	V_{RST33} CC	-	-	3.00	V	by reset release before EVR trimming on supply ramp-up
Primary undervoltage reset threshold for V_{DD} before trimming	V_{RSTC} CC	-	-	1.138	V	by reset release before trimming on supply ramp-up including 2 LSB voltage Hysteresis
V_{EXT} primary undervoltage monitor accuracy after trimming 2)	$V_{EXTPRIUV}$ CC	2.86	2.92	2.97	V	V_{EXT} = Undervoltage cold PORST Primary Monitor Threshold
V_{DDP3} primary undervoltage monitor accuracy after trimming 2)	$V_{DDP3PRIUV}$ CC	2.86 3)	2.90	2.97	V	VDDP3 = Undervoltage cold PORST Primary Monitor Threshold

Table 3-29 Supply Monitors (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DD} primary undervoltage monitor accuracy after trimming [2]	$V_{DDPRIUV}$ CC	1.08 [3]	1.105	1.125	V	VDD = Undervoltage cold PORST Primary Monitor Threshold
EVR primary monitor measurement latency for a new supply value	t_{PRIUV} CC	-	-	300	ns	The supply ramp / line jump slope is limited to 50V/ms for V_{EXT}, V_{DDP3} and V_{DD} rails.
V_{EXT}, V_{DDM} & V_{EVRSB} secondary supply monitor accuracy after trimming [4] [5]	V_{EXTMON} CC	3.2	3.3	3.4	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=3.3V=90h(OV,UV).
		4.5	4.6	4.7	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=4.6V=C9h(OV)/C8h(UV).
		5.3	5.4	5.5	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5.4V=ECh(OV)/EAh(UV).
		4.9	5.0	5.1	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5V=DAh(OV)/D9h(UV).
V_{DDP3} secondary supply monitor accuracy after trimming [5]	$V_{DDP3MON}$ CC	2.97	3.035	3.1	V	EVR33xxVAL V_{DDP3} monitoring threshold=3.035V=CCh(OV)/CBh(UV).
		3.235	3.30	3.365	V	EVR33xxVAL V_{DDP3} monitoring threshold=3.3V=DDh(OV,UV).
		3.5	3.565	3.63	V	EVR33xxVAL V_{DDP3} monitoring threshold=3.565V=EFh(OV)/EEh(UV).

Table 3-29 Supply Monitors (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DD} & V_{DDPD} secondary supply monitor accuracy after trimming [5]	V_{DDMON} CC	1.125	1.15	1.175	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.15V=C8h(OV)/C7h(UV).
		1.225	1.25	1.275	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.25V=D9h(OV, UV).
		1.325	1.35	1.375	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.35V=EBh (OV)/EAh(UV).
V_{EXT} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRST5}$ CC	2.3	-	2.72	V	Power-down
		2.4	-	2.75	V	Power-up
V_{EVRSB} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRSTSB}$ CC	2.18	-	2.47	V	Power-down
		2.21	-	2.5	V	Power-up
V_{EXT} and V_{EVRSB} PBIST primary overvoltage Monitor threshold	V_{PBIST5} CC	5.63	-	-	V	
Primary undervoltage reset threshold for V_{EXT} before trimming	V_{RST5} CC	-	-	3.0	V	by last cold PORST release on supply ramp-up including voltage hysteresis.
EVR secondary monitor measurement latency for all 6 supply rails	t_{MON} CC	-	-	3.2	µs	HPOSC and SHPBG bandgap trimmed

1) The reset release on supply ramp-up is delayed by a time duration 20-40 us after reaching undervoltage reset threshold and by a voltage hysteresis of 1.5% above the undervoltage reset limit. These mechanisms serve as hysteresis to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released. The reset limit of 2,97V at pin is for the case with 3.3V generated internally from EVR33. In case the 3.3V supply is provided externally, the bondwire drop will cause a reset at a higher voltage of 3.0V at the VDDP3 pin.

2) The monitor tolerances constitute the inherent variation of the band gap and ADC over process, voltage and temperature operational ranges. The VxxPRIUV parameters are device individually tested in production with +-1% tolerance about the VxxPRIUV limits. All voltages are measured on pins.

3) VRSTxx parameters are relevant only for the first cold PORST release. Later the reset levels are trimmed by the Firmware and reflected as VxxPRIUV parameters before device is used with full performance. The cold PORST is released with a voltage hysteresis on all the primary monitors to avoid consecutive PORST toggling behavior.

4) In case the application is using 3.3V single supply (Single Supply mode (e), i.e. VEXT and VDDP3 are shorted together), it is recommended to use secondary supply monitoring on channel VDDP3, because of the better accuracy of parameter VDDP3MON.

5) To monitor voltage level not provided in conditions the values for OV and UV thresholds can be generated by a linear interpolation or extrapolation based on the given points.

Table 3-30 Supply Ramp

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External V_{EXT} & V_{EVRSB} supply ramp-up and ramp-down slope 1) 2) 3)	$dVEXT/dt$ SR	8.3E-6	1	100	V/ms	
External V_{DDP3} supply ramp-up and ramp-down slope 1)3)	$dVDDP3/dt$ SR	8.3E-6	1	100	V/ms	
External V_{DD} supply ramp-up and ramp-down slope 1)3)	$dVDD/dt$ SR	8.3E-6	1	100	V/ms	
External V_{DDM} supply ramp-up and ramp-down slope 1)3)	$dVDDM/dt$ SR	8.3E-6	1	100	V/ms	

1) The device is robust against residual voltage ramp-up starting between 0 - 2.97 V for VEXT, VEVRSB, VDDP3 and VDDM and 0-1 V for VDD. A voltage ramp range between 0.5V/min upto 120V/ms is covered in robustness validation.

2) Also valid in case EVR33 or EVRC is used. The generated voltage itself follows a soft ramp-up over the tSTR time to avoid overshoots.

3) The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.

Up to 1000000 power-cycles, matching the limits defined in the table ’Supply Ramp’, are allowed for TC35x, without any restriction to reliability.

Table 3-31 EVRC SMPS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input V_{EXT} Voltage range	V_{IN} SR	2.97	-	5.5	V	Start-up VEXT voltage > 2.6 V
SMPS regulator output voltage range including load/line regulation and aging	V_{DDDC} CC	1.125	-	1.375	V	$V_{EXT} \geq 2.97V$; $V_{EXT} \leq 5.5V$; $I_{DDDC} \geq 1mA$; $I_{DDDC} \leq 1.5A$; untrimmed
SMPS regulator static voltage output accuracy after trimming without dynamic load/line regulation.	V_{DDDCT} CC	1.225	1.25	1.275	V	$V_{EXT} \geq 2.97V$; $V_{EXT} \leq 5.5V$; $I_{DDDC} \geq 1mA$; $I_{DDDC} \leq 1.5A$
Programmable switching frequency	f_{DCDC} SR	1.6	1.82	2.0	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation.
		-	0.8	-	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation. 0.8 MHz to be set in SW.

Table 3-31 EVRC SMPS (cont'd)

Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**
		Min.	**Typ.**	**Max.**		
Startup time	t_{STRDC} CC	-	-	900	μs	SMPS Start-up Mode. It is is defined beween $V_{EXTPRIUV}$ reset threshold till PORST release, on condition that all other PORST requirements were released before. I_{START} < 700mA.
Switching frequency modulation spread	Δf_{DCSPR} CC	-	1.8%	-	MHz	
Maximum ripple at I_{MAX}	ΔV_{DDDC} CC	-	-	16	mV	$V_{EXT} \geq 2.97$V ; $V_{EXT} \leq 5.5$V ; $I_{DDDC} \geq 300$mA ; $I_{DDDC} \leq 1.5$A ; ΔV_{DDDC} = (Peak to Peak ripple / 2)
No load current consumption of SMPS regulator	I_{DCNL} CC	-	15	19	mA	$f_{DCDC}=1.82MHz$; $I_{DDDC}=I_{SLEEP}$; V_{EXT} > 2.97 V; T_J=25°C
		-	5	-	mA	LPM mode; $I_{DDDC}=I_{SLEEP}$; V_{EXT} > 2.97 V; T_J=25°C
SMPS regulator load transient response	dV_{DDDCT} / dI_{OUT} CC	-50	-	75	mV	$dI < -250mA$; $I_{DDDC}=280\text{-}1500mA$; $t_r=0.1us$; $t_f=0.1us$; $V_{DDDC}=1.25V$; $T_{settle}=100\ us$
		-50	-	87	mV	$dI < -450mA$; $I_{DDDC}=500\text{-}1500mA$; $t_r=0.1us$; $t_f=0.1us$; $V_{DDDC}=1.25V$; $T_{settle}=100\ us$
		-100	-	145	mV	$dI < -700mA$; $I_{DDDC}=750\text{-}1500mA$; $t_r=0.1us$; $t_f=0.1us$; $V_{DDDC}=1.25V$; $T_{settle}=100\ us$
		-26	-	26	mV	$dI < 100mA$; $I_{DDDC}=50\text{-}1500mA$; $t_r=0.1us$; $t_f=0.1us$; $V_{DDDC}=1.25V$; $T_{settle}=20us$;

Table 3-31 EVRC SMPS (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output current	I_{MAX} CC	100	-	-	mA	LPM mode. Typical current in LPM Mode = I_{SLEEP}
		1.5	-	-	A	limited by thermal constraints and component choice
SMPS regulator line transient response	dV_{DDDCT} / $\mathrm{d}V_{\mathrm{IN}}$ CC	-75	-	75	mV	dV/dT=120V/ms; $dV <$ 2.97 - 5.5V ; I_{DDDC}=50-1500mA;
		-12.5	-	12.5	mV	dV/dT=1V/ms; $dV <$ 2.97 - 5.5V ; I_{DDDC}=50-1500mA;
SMPS regulator efficiency	n_{DC} CC	-	80	-	%	V_{IN}=3.3V; I_{DDDC}=1500mA; f_{DCDC}=1.82MHz
		-	75	-	%	V_{IN}=5V; I_{DDDC}=1500mA; f_{DCDC}=1.82MHz
Input Synchronisation frequency	f_{DCDCSYNC} SR	1.6	1.82	2.0	MHz	

Table 3-32 EVRC SMPS External components

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External output capacitor value 1)	C_{OUT} SR	20.8	32	43.2	µF	I_{DDDC}=1.5A; f_{DDDC} = 0.8MHz
		15.4	22	29.7	µF	I_{DDDC}=1.5A; f_{DDDC} = 1.82MHz
External output capacitor ESR	$C_{\mathrm{OUT\_ESR}}$ SR	-	-	50	mOhm	f≥0.5MHz ; f≤10MHz
		-	-	100	Ohm	f=10Hz
External input capacitor value 1)	C_{IN} SR	6.5	10	13.5	µF	I_{DDDC}=1.5A
		4.42	6.8	9.18	µF	I_{DDDC}=500mA
External input capacitor ESR	$C_{\mathrm{IN\_ESR}}$ SR	-	-	50	mOhm	f≥0.5MHz ; f≤10MHz
		-	-	100	Ohm	f=100Hz
External inductor value	L_{DC} SR	3.29	4.7	6.11	µH	f_{DCDC}=0.8MHz
		2.31	3.3	4.29	µH	f_{DCDC}=1.82MHz
External inductor DCR	$L_{\mathrm{DC\_DCR}}$ SR	-	-	0.2	Ohm	
P + N-channel MOSFET logic level	V_{LL} SR	-	-	2.5	V	
P + N-channel MOSFET drain source breakdown voltage	$\lvert V_{\mathrm{BR\_DS}} \rvert$ SR	+7	-	-	V	NMOS - V_{GS} = 0.
		-	-	-7	V	PMOS - V_{GS} = 0.

Table 3-32 EVRC SMPS External components (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
P + N-channel MOSFET drain source ON-state resistance	R_{ON} SR	-	150	-	mOhm	I_{DDDC}=1.5A; $\lvert V_{\mathrm{GS}}\rvert$=2.5$V$; T_{A}=25$°C$
		-	200	-	mOhm	I_{DDDC}=500mA; $\lvert V_{\mathrm{GS}}\rvert$=2.5$V$; T_{A}=25$°C$
P + N-channel MOSFET Gate Charge	Q_{G} SR	-	-	8	nC	I_{DDDC}=1.5A; NMOS-$\lvert V_{\mathrm{GS}}\rvert$=5V; 1.5A pulsed drain current
		-8	-	-	nC	I_{DDDC}=1.5A; PMOS-$\lvert V_{\mathrm{GS}}\rvert$=5V; 1.5A pulsed drain current
		-	-	4	nC	I_{DDDC}=500mA; NMOS-$\lvert V_{\mathrm{GS}}\rvert$=5V; 0.5A pulsed drain current
		-4	-	-	nC	I_{DDDC}=500mA; PMOS-$\lvert V_{\mathrm{GS}}\rvert$=5V; 0.5A pulsed drain current
External Inductor Saturation Current Margin	ΔI_{SAT} SR	400	-	-	mA	The saturation current of the coil must be larger than I_{DDDC} + ΔI_{SAT}
P + N-channel MOSFET Gate threshold voltage	V_{GSTH} SR	-	1	-	V	NMOS
		-	-1	-	V	PMOS
N-channel MOSFET reverse diode forward voltage	V_{RDN} SR	-	0.8	-	V	

1) Capacitor min-max range represent typical +-35% tolerance including DC bias effect. The trace resistance from the capacitor to the supply or ground rail should be limited to 25 mOhm.

3.15 System Phase Locked Loop (SYS_PLL)

Table 3-33 PLL System

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DCO Input frequency range	f_{REF} CC	10	-	40	MHz	
Modulation Amplitude	MA CC	0	-	2	%	
Peak Period jitter	DP CC	-200	-	200	ps	without modulation (PLL output frequency)
Peak Accumulated Jitter	D_{PP} CC	-5	-	5	ns	without modulation
Total long term jitter	J_{TOT} CC	-	-	11.5	ns	including modulation; MA 1.25%; f_{REF} 20MHz
System frequency deviation	f_{SYSD} CC	-	-	0.01	%	with active modulation
DCO frequency range	f_{DCO} CC	400	-	800	MHz	
PLL lock-in time	t_L CC	4	-	100	µs	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

3.16 Peripheral Phase Locked Loop (PER_PLL)

Table 3-34 PLL Peripheral

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak Accumulated jitter at SYSCLK pin	D_{PP} CC	-1000	-	1000	ps	Peak only
Peak accumulated jitter	D_{PPI} CC	-700	-	700	ps	Peak only
RMS Accumulated jitter	D_{RMS} CC	-100	-	100	ps	measured over 1 µs; f_{REF} = 20 MHz and f_{DCO} = 640 MHz or f_{REF} = 25 MHz and f_{DCO} = 800 MHz
Peak Period jitter	DP CC	-200	-	200	ps	f_{DCO} = 640 MHz or f_{DCO} = 800 MHz
Absolute RMS jitter (PLL out)	J_{ABS10} CC	-125	-	125	ps	f_{REF} = 10 MHz; f_{DCO} = 640 MHz
Absolute RMS jitter (PLL out)	J_{ABS20} CC	-85	-	85	ps	f_{REF} = 20 MHz; f_{DCO} = 640 MHz
Absolute RMS jitter (PLL out)	J_{ABS25} CC	-85	-	85	ps	f_{REF} = 25 MHz; f_{DCO} = 800 MHz
DCO frequency range	f_{DCO} CC	400	-	800	MHz	
DCO input frequency range	f_{REF} CC	10	-	40	MHz	
PLL lock-in time	t_L CC	4	-	100	µs	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L *= 20 pF with the maximum driver and sharp edge.*

Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of V_{PP} *= 100 mV for noise frequencies below 300 KHz and* V_{PP} *= 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.*

3.17 AC Specifications

All AC parameters are specified for the complete operating range defined in **Chapter 3.4** unless otherwise noted in column Note / Test Condition.

Unless otherwise noted in the figures the timings are defined with the following guidelines:

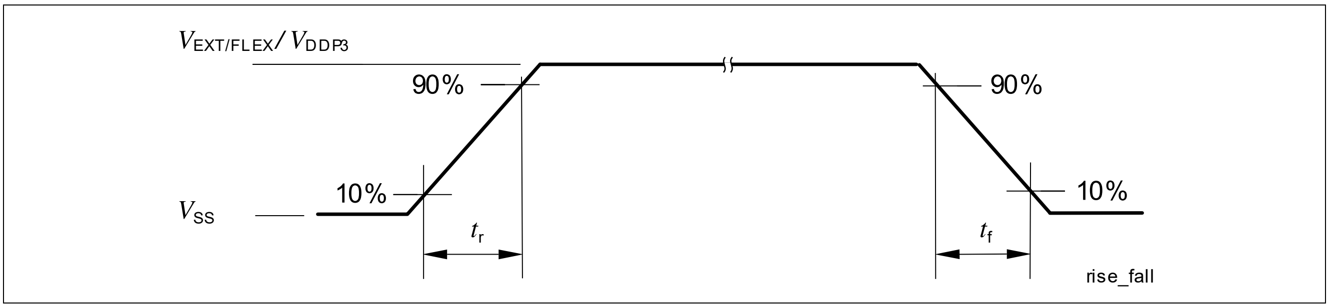


Figure 3-8 Definition of rise / fall times

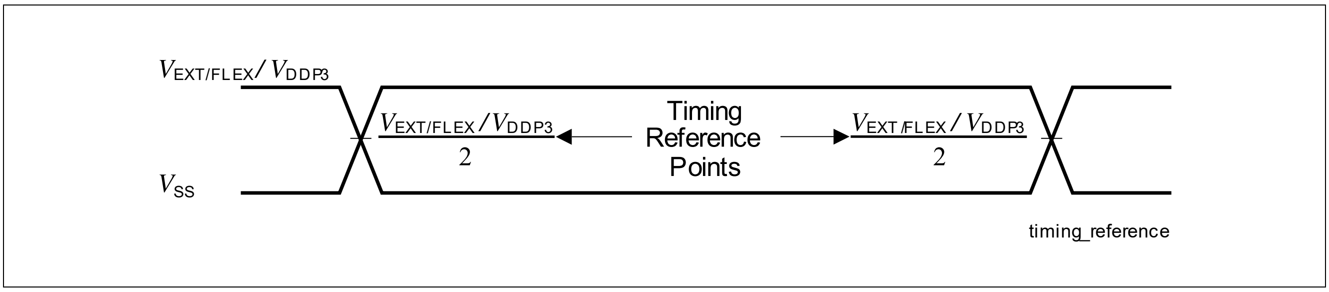


Figure 3-9 Time Reference Point Definition

3.18 JTAG Parameters

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Table 3-35 JTAG

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	-	-	ns	
TCK high time	t_2 SR	10	-	-	ns	
TCK low time	t_3 SR	10	-	-	ns	
TCK clock rise time	t_4 SR	-	-	4	ns	
TCK clock fall time	t_5 SR	-	-	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6.0	-	-	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6.0	-	-	ns	
TDO valid after TCK falling edge (propagation delay)	t_8 CC	3.0	-	-	ns	$C_L \le 20$pF
		-	-	25	ns	$C_L \le 50$pF
TDO hold after TCK falling edge	t_{18} CC	2	-	-	ns	
TDO high impedance to valid from TCK falling edge	t_9 CC	-	-	25	ns	$C_L \le 50$pF
TDO valid output to high impedance from TCK falling edge	t_{10} CC	-	-	25	ns	$C_L \le 50$pF

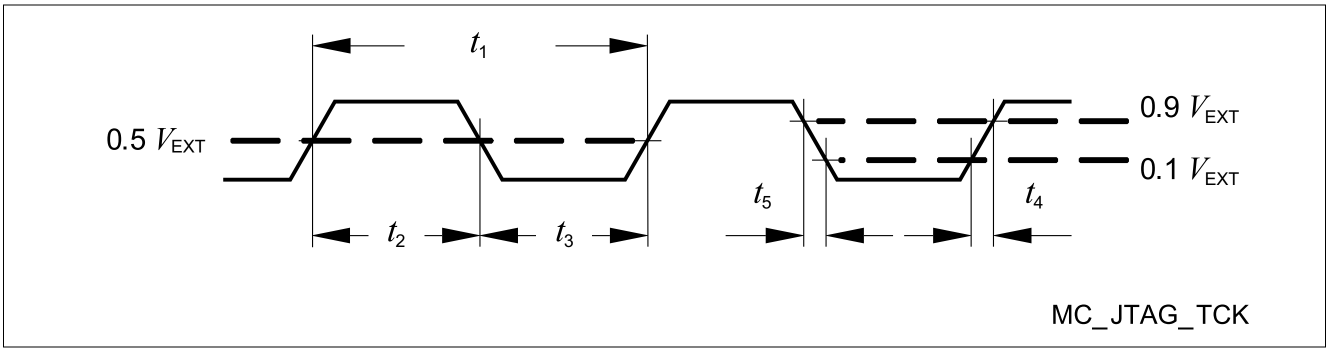


Figure 3-10 Test Clock Timing (TCK)

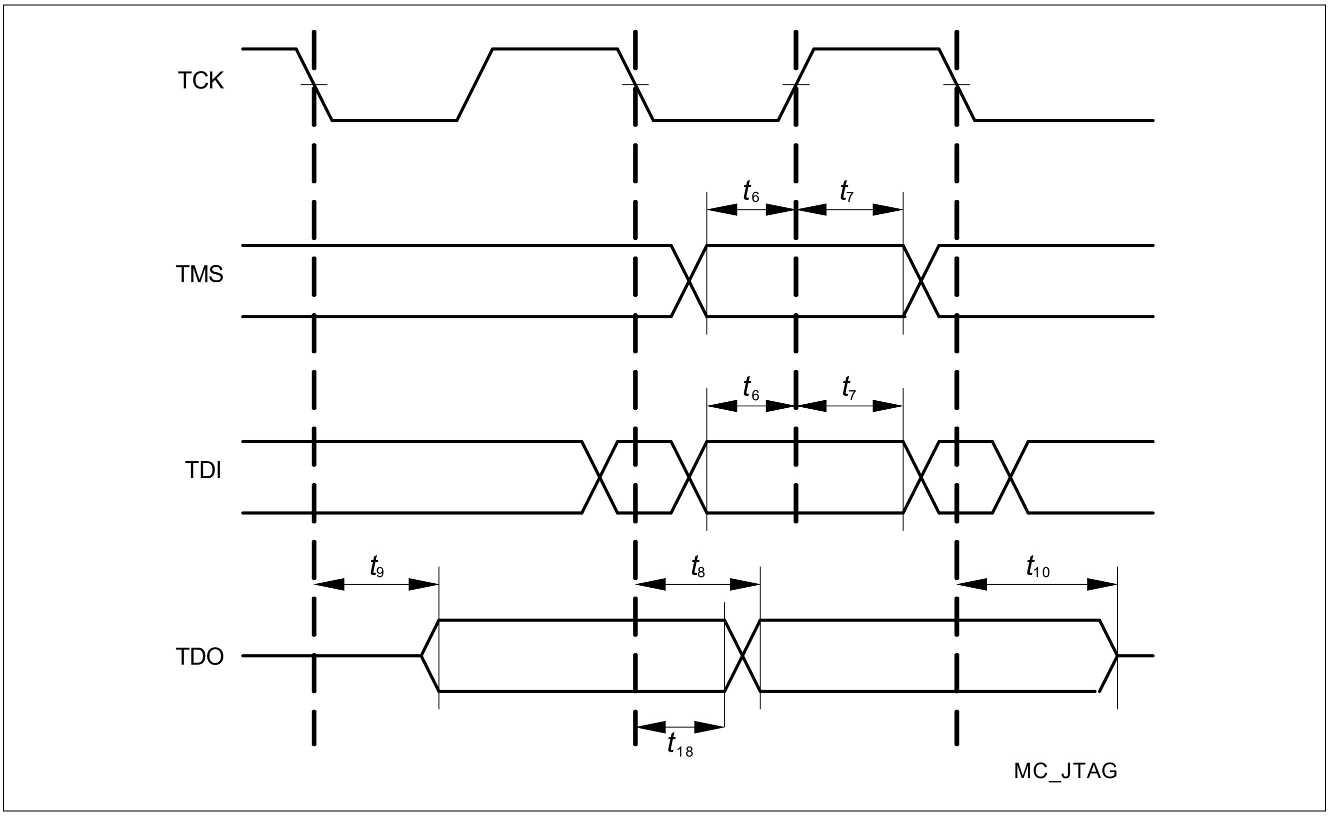


Figure 3-11 JTAG Timing

3.19 DAP Parameters

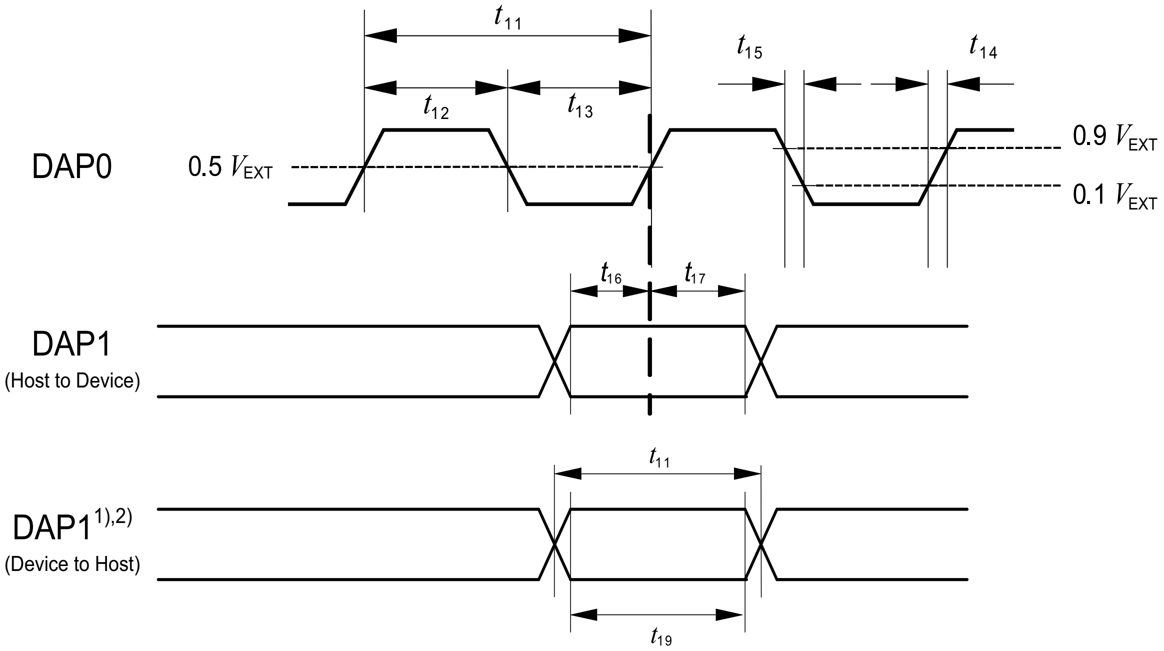
The following parameters are applicable for communication through the DAP debug interface.

Table 3-36 DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP0 clock fall time	t_{15} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	4	-	-	ns	
		5	-	-	ns	f=40MHz
DAP1 hold after DAP0 rising edge	t_{17} SR	2	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	4	-	-	ns	C_L=20pF ; f=160MHz
		8	-	-	ns	C_L=20pF ; f=80MHz
		10	-	-	ns	C_L=50pF ; f=40MHz
DAP0 high time	t_{12} SR	2	-	-	ns	
DAP0 low time	t_{13} SR	2	-	-	ns	
DAP0 clock period	t_{11} SR	6.25	-	-	ns	

Table 3-37 SCR DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	8	ns	f=20MHz
DAP0 clock fall time	t_{15} SR	-	-	8	ns	f=20MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	10	-	-	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	10	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	30	-	-	ns	C_L=20pF ; f=20MHz
DAP0 high time	t_{12} SR	15	-	-	ns	
DAP0 low time	t_{13} SR	15	-	-	ns	
DAP0 clock period	t_{11} SR	50	-	-	ns	



1) The DAP1 and DAP2 device to host timing is individual for both pins. There is no guaranteed max. signal skew.

2) No explicite setup and hold times are given for DAP1 for the direction Device to Host. Only t11 and t19 are guaranteed and the tool may set the sample point freely.

Figure 3-12 DAP Timing

Note: The DAP1 and DAP2 device to host timing is individual for both pins. There is no guaranteed max. signal skew.

3.20 ASCLIN SPI Master Timing

This section defines the timings for the ASCLIN in the TC35x.

Note: Pad asymmetry is already included in the following timings.

Table 3-38 Master Mode strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	20	-	-	ns	C_L=25pF
Deviation from ideal duty cycle	t_{500} CC	-2	-	2	ns	C_L=25pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-3.5	-	3.5	ns	C_L=25pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-3	-	3.5	ns	C_L=25pF
MRST setup to ASCLKO latching edge	t_{52} SR	25	-	-	ns	C_L=25pF
MRST hold from ASCLKO latching edge	t_{53} SR	-2	-	-	ns	C_L=25pF

Table 3-39 Master Mode strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	50	-	-	ns	C_L=50pF
Deviation from ideal duty cycle	t_{500} CC	-5	-	5	ns	C_L=50pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-7	-	7	ns	C_L=50pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-7	-	7	ns	C_L=50pF
MRST setup to ASCLKO latching edge	t_{52} SR	35	-	-	ns	C_L=50pF
MRST hold from ASCLKO latching edge	t_{53} SR	-5	-	-	ns	C_L=50pF

Table 3-40 Master Mode medium (m) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	160	-	-	ns	C_L=50pF
Deviation from ideal duty cycle	t_{500} CC	-10	-	10	ns	C_L=50pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-20	-	20	ns	C_L=50pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-20	-	20	ns	C_L=50pF

Table 3-40 Master Mode medium (m) output pads (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MRST setup to ASCLKO latching edge	t_{52} SR	80	-	-	ns	C_L=50pF
MRST hold from ASCLKO latching edge	t_{53} SR	-15	-	-	ns	C_L=50pF

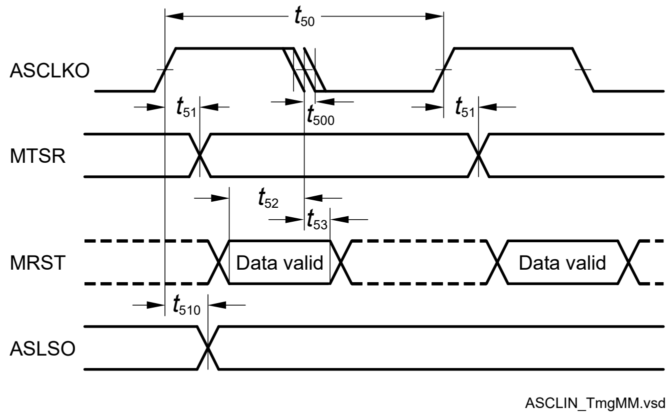


Figure 3-13 ASCLIN SPI Master Timing

3.21 QSPI Timings, Master and Slave Mode

This section defines the timings for the QSPI in the TC35x.
It is assumed that SCLKO, MTSR, and SLSO pads have the same pad settings:

Note: Pad asymmetry is already included in the following timings.

Table 3-41 Master Mode Timing, LVDS output pads for data and clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	20 [1]	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	t_{500} CC	-1 [1]	-	1 [1]	ns	CL=25pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-3 [1]	-	4 [1]	ns	CL=25pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-4 [1]	-	5.5 [1]	ns	C_L=25pF, driver strength ss
		-10 [1]	-	10 [1]	ns	C_L=25pF, driver strength sm
		-30 [1]	-	30 [1]	ns	C_L=25pF, driver strength m
MRST setup to SCLK latching edge	t_{52} SR	18 [1]	-	-	ns	CL=25pF; valid for LVDS Input pads of QSPI2 only
MRST hold from SCLK latching edge	t_{53} SR	-1 [1]	-	-	ns	CL=25pF; valid for LVDS Input pads only

1) The load (C_L=25pF) defined in the condition list is a load definition for the single end signal SLSO and does not intend to add an additional load inside the differential signal lines. For single end signals the load definition defines the max length of the signal on the PCB layout. For the LVDS pads the IEEE Std 1596.3-1996 load definitions apply.

Table 3-42 Master Mode Strong Sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	50	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	t_{500} CC	-2	-	2	ns	CL=25pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-4	-	5	ns	CL=25pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-4	-	5	ns	CL=25pF
MRST setup to SCLK latching edge	t_{52} SR	25 [1] [2]	-	-	ns	CL=25pF
MRST hold from SCLK latching edge	t_{53} SR	-2 [1][2]	-	-	ns	CL=25pF

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-43 Master Mode Strong Medium (sm) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	50	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	t_{500} CC	-5	-	5	ns	CL=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-7	-	7	ns	CL=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-7	-	7	ns	CL=50pF
MRST setup to SCLK latching edge	t_{52} SR	35 1) 2)	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	t_{53} SR	-5 1)2)	-	-	ns	CL=50pF

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-44 Master Mode Medium (m) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	160	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	t_{500} CC	-10	-	10	ns	CL=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-20	-	20	ns	CL=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-20	-	20	ns	CL=50pF
MRST setup to SCLK latching edge	t_{52} SR	80 1) 2)	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	t_{53} SR	-15 1)2)	-	-	ns	CL=50pF
		-13 1)2)	-	-	ns	CL=50pF; SCR SSC

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

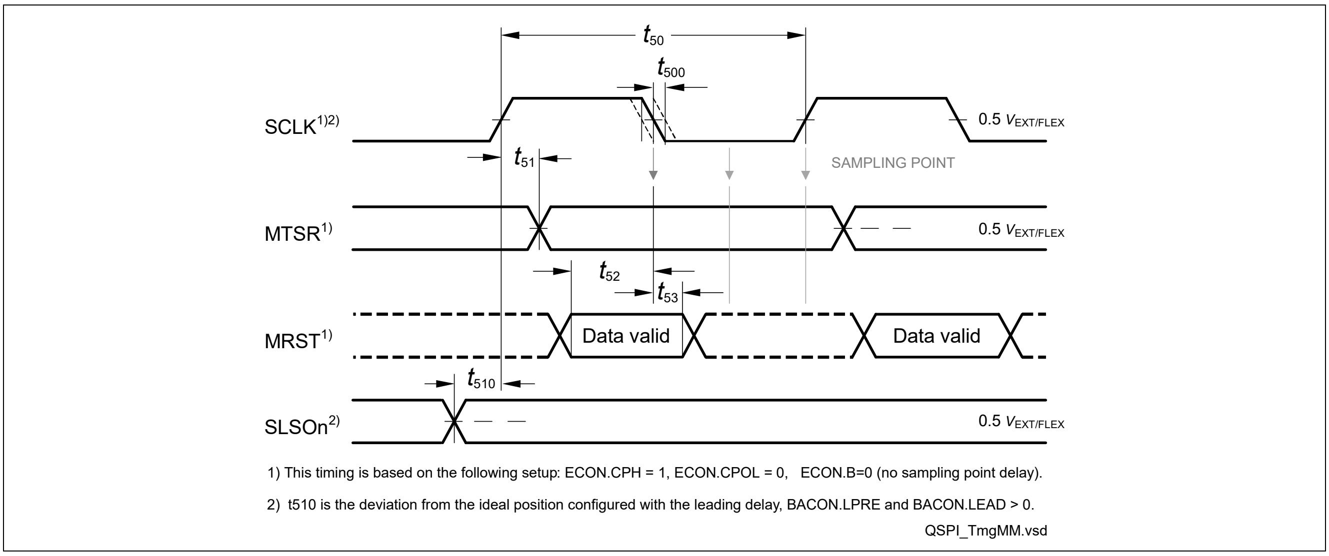
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-45 Slave mode timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period	t_{54} SR	4 x T_{MAX}	-	-	ns	
SCLK duty cycle	$t_{55/t54}$ SR	40	-	60	%	
MTSR setup to SCLK latching edge	t_{56} SR	6	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL

Table 3-45 Slave mode timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MTSR hold from SCLK latching edge	t_{57} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI setup to first SCLK shift edge	t_{58} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI hold from last SCLK latching edge	t_{59} SR	3	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MRST delay from SCLK shift edge	t_{60} CC	5	-	35	ns	driver = strong edge = medium ; C_{L}=50pF
		2	-	24	ns	driver = strong edge = sharp ; C_{L}=50pF
		15	-	80	ns	medium driver ; C_{L}=50pF
		14	-	-	ns	medium driver ; C_{L}=50pF; SCR SSC



1) This timing is based on the following setup: ECON.CPH = 1, ECON.CPOL = 0, ECON.B=0 (no sampling point delay).

2) t510 is the deviation from the ideal position configured with the leading delay, BACON.LPRE and BACON.LEAD > 0.

QSPI_TmgMM.vsd

Figure 3-14 Master Mode Timing

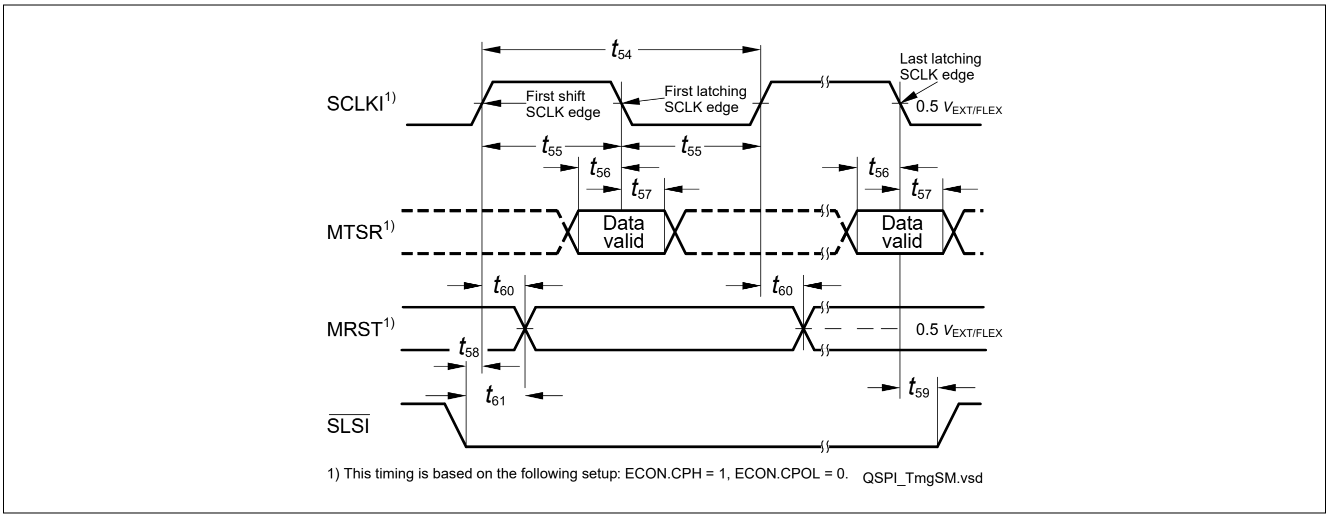


Figure 3-15 Slave Mode Timing

3.22 Ethernet Interface (ETH) Characteristics

3.22.1 ETH Measurement Reference Points

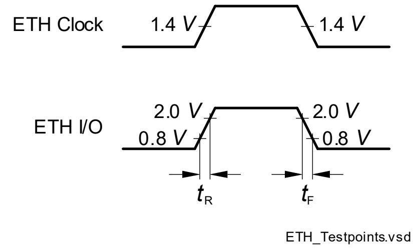


Figure 3-16 ETH Measurement Reference Points

3.22.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 3-46 ETH Management Signal Parameters valid for 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_MDC period	t_1 CC	400	-	-	ns	CL=25pF
ETH_MDC high time	t_2 CC	160	-	-	ns	CL=25pF
ETH_MDC low time	t_3 CC	160	-	-	ns	CL=25pF
ETH_MDIO setup time (output)	t_4 CC	10	-	-	ns	CL=25pF
ETH_MDIO hold time (output)	t_5 CC	10	-	-	ns	CL=25pF
ETH_MDIO data valid (input)	t_6 SR	0	-	300	ns	CL=25pF

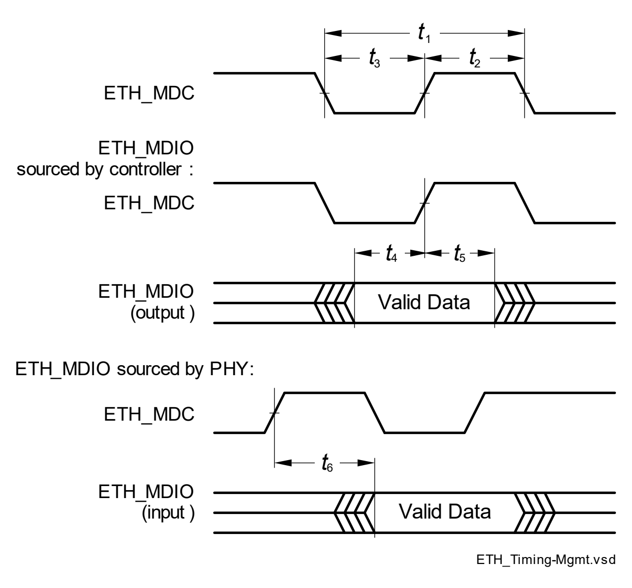


Figure 3-17 ETH Management Signal Timing

3.22.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 3-47 ETH MII Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_7 SR	-	40	-	ns	CL=25pF ; baudrate=100Mbps
		-	400	-	ns	CL=25pF ; baudrate=10Mbps
Clock high time	t_8 SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 1)	-	260 2)	ns	CL=25pF ; baudrate=10Mbps
Clock low time	t_9 SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 1)	-	260 2)	ns	CL=25pF ; baudrate=10Mbps
Input setup time	t_{10} SR	10	-	-	ns	CL=25pF
Input hold time	t_{11} SR	10	-	-	ns	CL=25pF
Output valid time	t_{12} CC	0	-	25	ns	CL=25pF

1) Defined by 35% of clock period.

2) Defined by 65% of clock period.

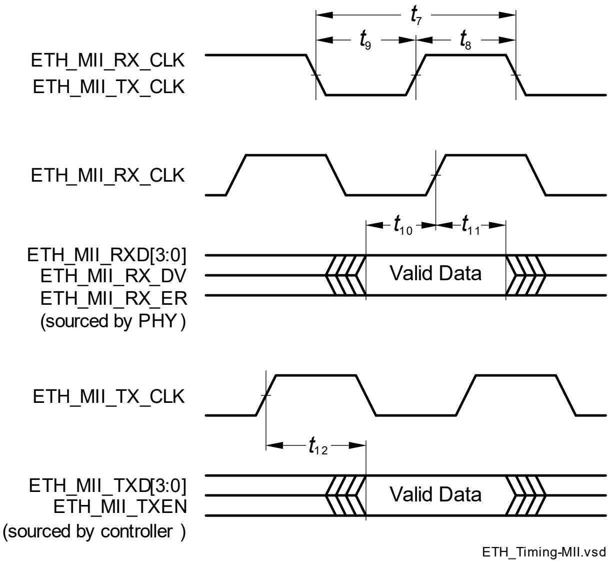


Figure 3-18 ETH MII Signal Timing

3.22.4 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 3-48 ETH RMII Signal Timing Parameters valid for 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13} SR	-	20	-	ns	50ppm ; CL=25pF
ETH_RMII_REF_CL clock high time	t_{14} SR	7 ¹⁾	-	13 ²⁾	ns	CL=25pF
ETH_RMII_REF_CL clock low time	t_{15} SR	7 ¹⁾	-	13 ²⁾	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; setup time ³⁾	t_{16} CC	4	-	-	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; hold time ³⁾	t_{17} CC	2	-	-	ns	CL=25pF

1) Defined by 35% of clock period.

2) Defined by 65% of clock period.

3) For ETHRXD and ETHCRSDV signals this parameter is a SR.

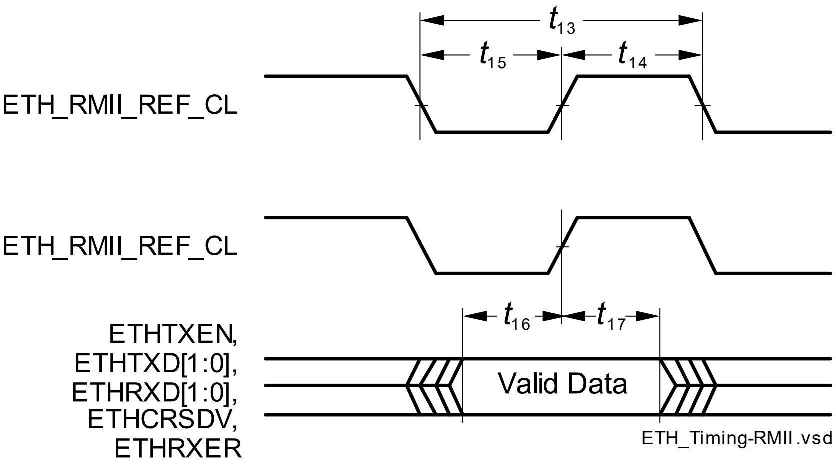


Figure 3-19 ETH RMII Signal Timing

3.22.5 ETH RGMII Parameters

In the following, the parameters of the RGMII are described.

Table 3-49 ETH RGMII Signal Timing Parameters valid for 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TX Clock period	t_{19} CC	36	40	44	ns	100Mbps
		360	400	440	ns	10Mbps
		7.2	8	8.8	ns	Gigabit
Data to Clock Output skew	t_{20} CC	-500	0	500	ps	
Data to Clock input skew (at receiver)	t_{21} SR	1	1.8	2.6	ns	SKEWCTL.RXCFG = 0; SKEWCTL.TXCFG = 0
Clock duty cycle	t_{duty} CC	40	50	60	%	10/100Mbps
		45	50	55	%	Gigabit
GREFCLK duty cycle	t_{duty_in} SR	45	-	55	%	
GREFCLK Input accuracy	ACC SR	-0.005	-	0.005	%	

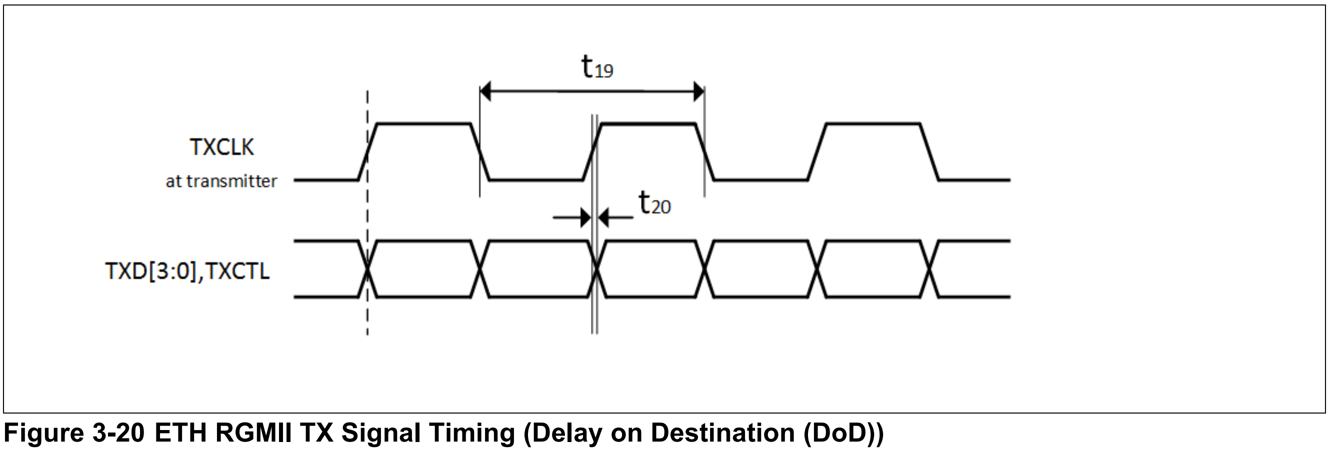


Figure 3-20 ETH RGMII TX Signal Timing (Delay on Destination (DoD))

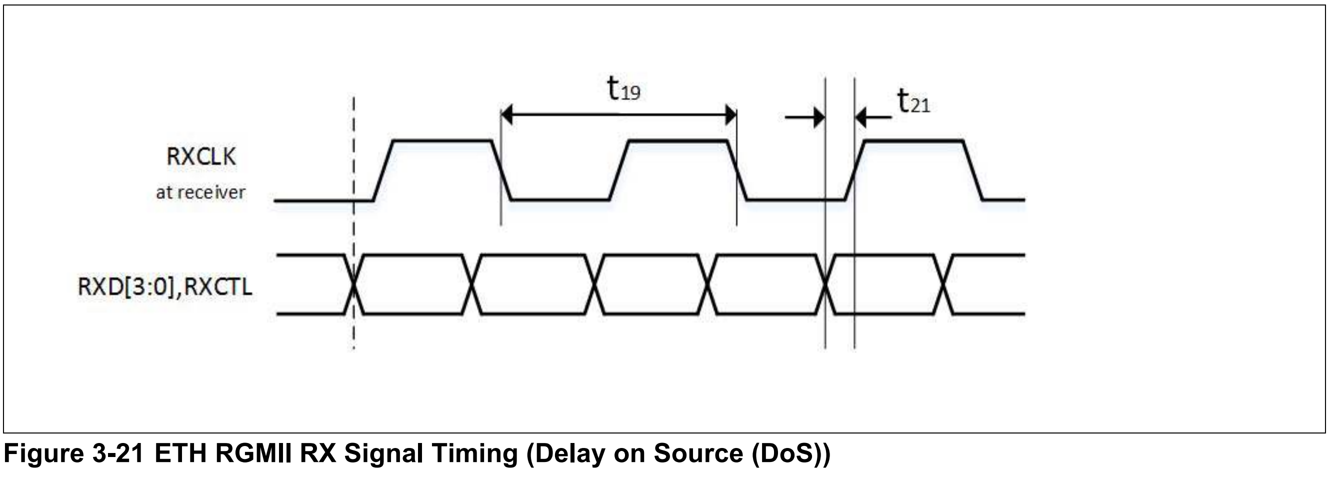


Figure 3-21 ETH RGMII RX Signal Timing (Delay on Source (DoS))

3.23 E-Ray Parameters

The timings of this section are valid for the strong driver and sharp edge settings of the output drivers with C_L = 25 pF.

Table 3-50 Transmit Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time of TxEN	$t_{\mathrm{dCCTxENRise25}}$ CC	-	-	9	ns	C_L=25pF
Fall time of TxEN	$t_{\mathrm{dCCTxENFall25}}$ CC	-	-	9	ns	C_L=25pF
Sum of rise and fall time	$t_{\mathrm{dCCTxRise25+dCCTxFall25}}$ CC	-	-	9	ns	20% - 80% ; C_L=25pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN	$t_{\mathrm{dCCTxEN01}}$ CC	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN	$t_{\mathrm{dCCTxEN10}}$ CC	-	-	25	ns	
Asymmetry of sending	$t_{\mathrm{tx\_asym}}$ CC	-2.45	-	2.45	ns	C_L=25pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD	t_{dCCTxD01} CC	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD	t_{dCCTxD10} CC	-	-	25	ns	
TxD signal sum of rise and fall time at TP1_BD	$t_{\mathrm{txd\_sum}}$ CC	-	-	9	ns	

Table 3-51 Receive Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Acceptance of asymmetry at receiving part	$t_{\mathrm{dCCTxAsymAccept25}}$ SR	-30.5	-	43.0	ns	C_L=25pF
Acceptance of asymmetry at receiving part	$t_{\mathrm{dCCTxAsymAccept15}}$ SR	-31.5	-	44.0	ns	C_L=15pF
Threshold for detecting logical high	$T_{\mathrm{uCCLogic1}}$ SR	35	-	70	%	
Threshold for detecting logical low	$T_{\mathrm{uCCLogic0}}$ SR	30	-	65	%	

Table 3-51 Receive Parameters (cont'd)

Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**
		Min.	**Typ.**	**Max.**		
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD	t_{dCCRxD01} CC	-	-	10	ns	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, falling edge of RxD	t_{dCCRxD10} CC	-	-	10	ns	

3.24 Inter-IC (I2C) Interface Timing

All I2C timing parameter are SR for Master Mode and CC for Slave Mode.

Table 3-52 I2C Standard Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	-	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	t_{10}	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	-	-	1000	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	t_3	0	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	t_4	250	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	t_5	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	t_6	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

Table 3-52 I2C Standard Mode Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Set-up time for (repeated) START condition	t_8	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	t_9	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

Table 3-53 I2C Fast Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	20+0.1*C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	t_{10}	1.3	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	20+0.1*C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	t_3	0	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	t_4	100	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	t_5	1.3	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	t_6	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

Table 3-53 I2C Fast Mode Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Hold time for the (repeated) START condition	t_7	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for (repeated) START condition	t_8	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	t_9	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

Table 3-54 I2C High Speed Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Fall time of SCL	t_{11}	10 1)	-	40 1)	ns	bus line load of 100pF
Fall time of SDA	t_{12}	10 1)	-	80 1)	ns	bus line load of 100pF
Rise time of SCL	t_{13}	10 1)	-	40 1)	ns	bus line load of 100pF
Rise time of SDA	t_{14}	10 1)	-	80 1)	ns	bus line load of 100pF
Data hold time	t_3	0 1)	-	70 1)	ns	bus line load of 100pF
Data set-up time	t_4	10 1)	-	-	ns	bus line load of 100pF
Low period of SCL clock	t_5	160 1)	-	-	ns	bus line load of 100pF
High period of SCL clock	t_6	60 1)	-	-	ns	bus line load of 100pF
Hold time for the (repeated) START condition	t_7	160 1)	-	-	ns	bus line load of 100pF
Set-up time for (repeated) START condition	t_8	160 1)	-	-	ns	bus line load of 100pF
Set-up time for STOP condition	t_9	160 1)	-	-	ns	bus line load of 100pF

1) Values are defined for C_b = 100pF, for the Timing of C_b = 400pF see the I2C Standard.

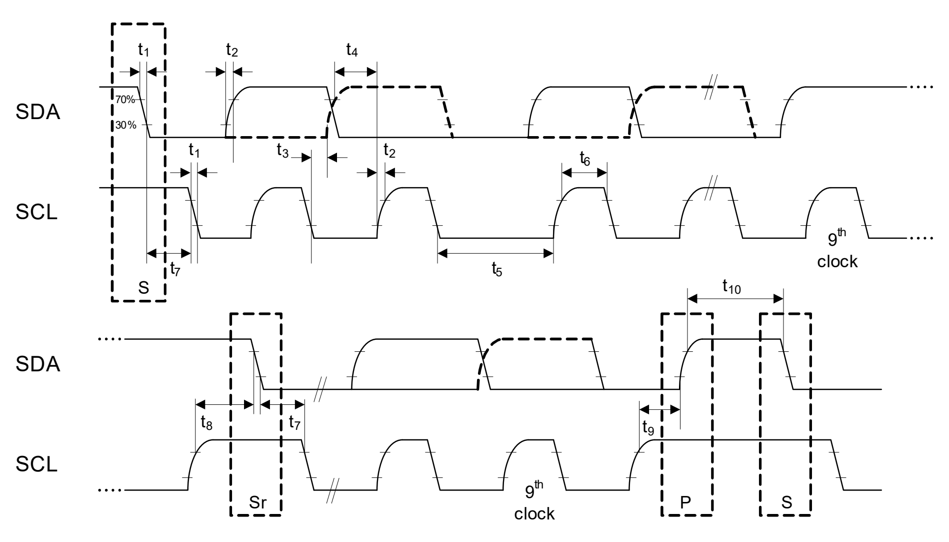


Figure 3-22 I2C Standard and Fast Mode Timing

3.25 Radar Interface Timing

Table 3-55 Skew Calibration Related

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Bit time	t_{80} CC	2.5	-	-	ns	
Set-up time	t_{82} SR	0.8	-	-	ns	
Hold time	t_{83} SR	0.8	-	-	ns	
RAMP1 set-up time relative to the FRAME rising edge	t_{88} SR	30	-	-	ns	
RAMP1 hold time relative to the FRAME rising edge	t_{89} SR	30	-	-	ns	

3.26 Flash Target Parameters

Table 3-56 Flash

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program Flash Erase Time per logical sector [1]	t_{ERP} CC	-	-	0.5	s	cycle count < 1000
Program Flash Erase Time per Multi-Sector Command [1]	t_{MERP} CC	-	-	0.5	s	For consecutive logical sectors in a physical sector with total range ≤ 512 kByte; cycle count < 1000
Program Flash program time per page in 5 V mode [1]	t_{PRP5} CC	-	-	80	µs	32 Byte
Program Flash program time per page in 3.3 V mode [1]	t_{PRP3} CC	-	-	115	µs	32 Byte
Program Flash program time per burst in 5 V mode [1]	t_{PRPB5} CC	-	-	220	µs	256 Byte
Program Flash program time per burst in 3.3 V mode [1]	t_{PRPB3} CC	-	-	530	µs	256 Byte
Program Flash program time for 1 MByte with burst programming in 3.3 V mode excluding communication [1]	$t_{\mathrm{PRPB3\_1MB}}$ CC	-	-	2.2	s	Derived value for documentation purpose
Program Flash program time for 1 MByte with burst programming in 5 V mode excluding communication [1]	$t_{\mathrm{PRPB5\_1MB}}$ CC	-	-	1	s	Derived value for documentation purpose
Program Flash program time for complete PFlash with burst programming in 5 V mode excluding communication [1]	$t_{\mathrm{PRPB5\_PF}}$ CC	-	-	4	s	Derived value for documentation purpose
Write Page Once adder [1]	t_{ADD} CC	-	-	20	µs	Adder to Program Time when using Write Page Once
Program Flash suspend to read latency [1]	t_{SPNDP} CC	-	-	120	µs	For Write Burst, Verify Erased and for multi-(logical) sector erase commands
Data Flash Erase Disturb Limit (single ended sensing mode)	N_{DFD} CC	-	-	50	cycles	
Data Flash Erase Disturb Limit (complement sensing mode)	N_{DFDC} CC	-	-	500	cycles	
UCB Erase Disturb Limit	N_{UCBD} CC	-	-	500	cycles	

Table 3-56 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program time data flash per page [1][2]	t_{PRD} CC	-	-	75	µs	8 Byte
Complete Device Flash Erase Time PFlash and DFlash [1][3] [4] [5]	t_{ER_Dev} CC	-	3	5	s	Valid for less than 1000 cycles, w/o UCB. Derived value for documentation purpose.
Data Flash program time per burst [1][2]	t_{PRDB} CC	-	-	140	µs	32 Byte
Data Flash suspend to read latency [1]	t_{SPNDD} CC	-	-	120	µs	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	-	-	2	µs	
Program Flash Endurance per Logical Sector	N_{E_P} CC	-	-	1000	cycles	Replace logical sector command shall be used if a sector fails during erase or program
Number of erase operations per physical sector in program flash	N_{ERP} CC	-	-	16000	cycles	
Program Flash Retention Time, Sector	t_{RET} CC	20	-	-	years	Max. 1000 erase/program cycles
UCB Retention Time	t_{RTU} CC	20	-	-	years	Max. 100 erase/program cycles per UCB, max 500 erase/program cycles for all UCBs together
Data Flash access delay	t_{DF} CC	-	-	100	ns	see RFLASH of DMU register HF_DWAIT
Data Flash ECC Delay	t_{DFECC} CC	-	-	20	ns	see RECC of DMU register HF_DWAIT
Program Flash access delay	t_{PF} CC	-	-	30	ns	see RFLASH of DMU register HF_PWAIT
Program Flash ECC delay	t_{PFECC} CC	-	-	10	ns	see RECC and CECC of DMU register HF_PWAIT
Number of erase operations on DF0 over lifetime (complement sensing mode) [6]	N_{ERD0C} CC	-	-	4000000	cycles	
Number of erase operations on DF0 over lifetime (single ended sensing mode) [7]	N_{ERD0S} CC	-	-	750000	cycles	

Table 3-56 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase operations on DF1 over lifetime (complement sensing mode) 6)	N_{ERD1C} CC	-	-	2000000	cycles	
Number of erase operations on DF1 over lifetime (single ended sensing mode) 7)	N_{ERD1S} CC	-	-	500000	cycles	
Data Flash Endurance per EEPROMx sector (complement sensing mode) 8)	N_{E_EEP10C} CC	-	-	500000	cycles	Max. data retention time 10 years
DataFlash Endurance per EEPROMx sector (single ended sensing mode) 8)	N_{E_EEP10S} CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Data Flash Endurance per HSMx sector (complement sensing mode) 8)	N_{E_HSMC} CC	-	-	250000	cycles	Max. data retention time 10 years
Data Flash Endurance per HSMx sector (single ended sensing mode) 8)	N_{E_HSMS} CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Junction temperature limit for PFlash program/erase operations	$T_{JPFlash}$ SR	-	-	150	°C	
Data Flash Erase Time per Sector 1)3)5)	t_{ERD1} CC	-	-	0.5	s	Max. 1000 erase/program cycles
Data Flash Erase Time per Sector 1)3)5)	t_{ERDM} CC	-	-	1.5	s	Max allowed cycles, see NE_EEP10 and NE_HSM parameters
DataFlash Adder on Erase Time per 32kByte erase size when using complement sensing mode 1)	$t_{ER\_ADDC32C}$ CC	-	-	50	ms	Adder per 32 kByte on erase time; applicable only when using complement mode

Table 3-56 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Multi-Sector Command 1)3)5)	t_{MERD1} CC	-	-	0.5	s	Max 1000 erase/program cycles; For consecutive logical sectors ≤ 256KBytes
Data Flash Erase Time per Multi-Sector Command 1)3)5)	t_{MERDM} CC	-	-	1.5	s	Max allowed cycles, see NE_EEP10x and NE_HSMx Parameters; For consecutive logical sectors ≤ 256 kByte
Program Flash Access Delay at reduced VDDP3 voltage supply during cranking	$t_{PF\_low\_VDDP3}$ CC	-	-	60	ns	see register DMU_HF_PWAIT.CFLASH
Data Flash Erase Verify time per page (Complement Sensing) 2)	$t_{VER\_PAGE\_DC}$ CC	-	-	10	µs	Time per 8 Byte page for Verify Erased Page command
Data Flash Erase Verify time per page (Single Ended Sensing) 1)	$t_{VER\_PAGE\_DS}$ CC	-	-	10	µs	Time per 8 Byte page for Verify Erased Page command
Program Flash Erase Verify time per page 1)	$t_{VER\_PAGE\_P}$ CC	-	-	10	µs	Time per 32 Byte page for Verify Erased Page command
Data Flash Erase Verify time per sector (Complement Sensing) 1)	$t_{VER\_SEC\_DC}$ CC	-	-	200	µs	Time per 2 KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per sector (Single Ended Sensing) 1)	$t_{VER\_SEC\_DS}$ CC	-	-	360	µs	Time per 4 KB sector for Verify Erased Logical Sector Range command
Program Flash Erase Verify time per sector 1)	$t_{VER\_SEC\_P}$ CC	-	-	360	µs	Time per 16KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per wordline (Complement Sensing) 1)	$t_{VER\_WL\_DC}$ CC	-	-	30	µs	
Data Flash Erase Verify time per wordline (Single Ended Sensing) 1)	$t_{VER\_WL\_DS}$ CC	-	-	50	µs	
Program Flash Erase Verify time per wordline 1)	$t_{VER\_WL\_P}$ CC	-	-	30	µs	

1) Only vaild for f_{FSI} = 100MHz.

2) Time is not dependent on program mode (5V or 3.3V).

3) Under out-of-spec conditions (e.g. over-cycling) or in case of activation of WL oriented defects, the duration of erase processes may be increased by up to 50%.
4) Using 512 kByte / 256 kByte erase commands (PFlash / DFlash).
5) If the DataFlash is operated in Complement Sensing Mode the erase time is increased by erase_size / 32kByte x tER_ADDC32C
6) Allows segmentation of addressable memory into 8 logical sectors; round robin cycling must still be done to consider erase disturb limit N_{DFD}.
7) Allows segmentation of addressable memory into 6 logical sectors; round robin cycling must still be done to consider erase disturb limit N_{DFD}.
8) Only valid when a robust EEPROM emulation algorithm is used. For more details see the Users Manual.

3.27 Quality Declarations

Table 3-57 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Moisture Sensitivity Level	MSL CC	-	-	3		Conforming to Jedec J-STD--020C for 240C
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	-	-	500 [1]	V	for all other balls/pins; conforming to JESD22-C101-C
		-	-	750	V	for corner balls/pins; conforming to JESD22-C101-C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	-	2000 [2]	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins according to Human Body Model (HBM)	V_{HBM1} SR	-	-	2000	V	
Operation Lifetime	t_{OP} CC	-	-	24500	hour	see below temperature profile as an example

1) Pads of the AGBT interface are limited to a maximum value of 250V.

2) Pads of the AGBT interface are limited to a maximum value of 1000V.

Example Temperature Profile

The following temperature profile is an example. Application specific temperature profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-58 Example Temperature Profile

T_J=	Duration [h]	Comment
≤ 170°C	≤ 30	
≤ 160°C	≤ 120	
≤ 150°C	≤ 220	
≤ 140°C	≤ 350	
≤ 130°C	≤ 780	
≤ 120°C	≤ 1600	
≤ 110°C	≤ 3000	
≤ 100°C	≤ 7000	
≤ 90°C	≤ 8000	
≤ 80°C	≤ 2400	
≤ 70°C	≤ 1000	
	≤ 24500	total time

Table 3-59 Example Inactive Lifetime Temperature Profile

T_J=	Duration [h]	Comment
≤ 55°C	≤ 150700	

3.28 Package Outline

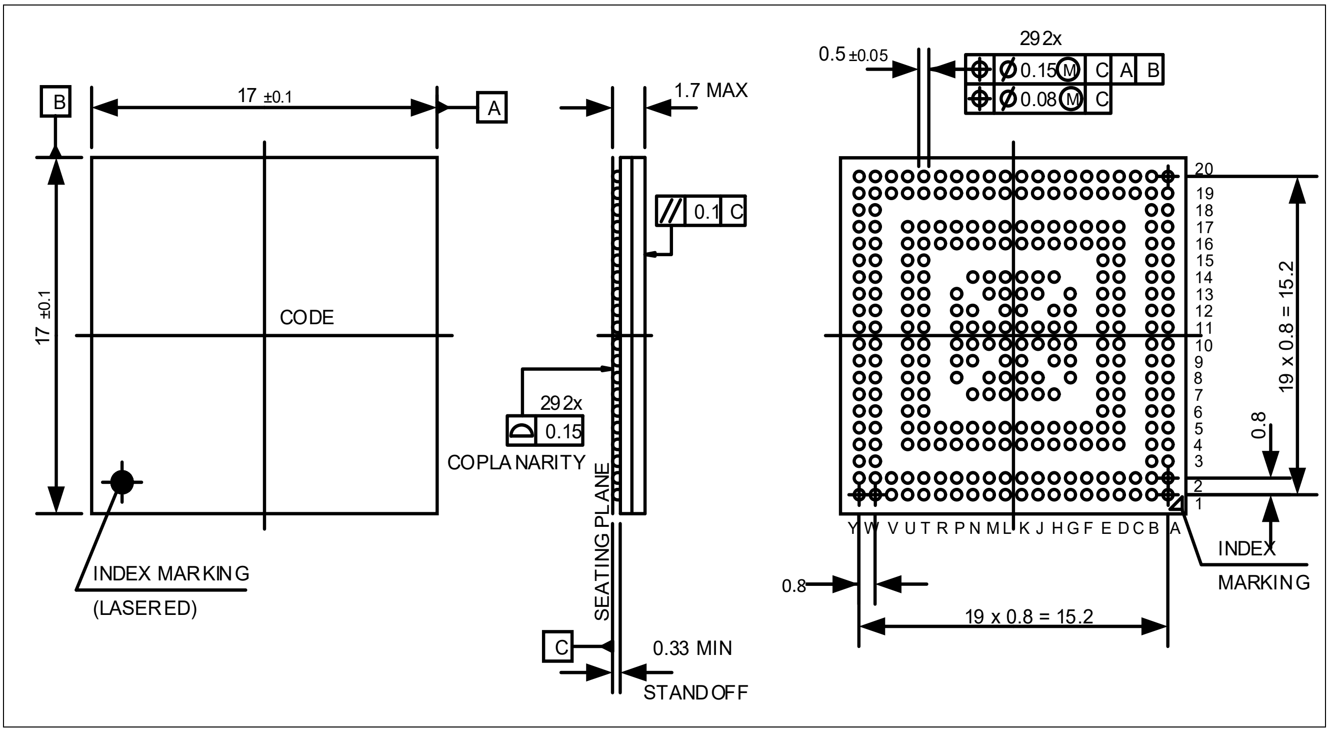


Figure 3-23 Package Outlines LFBGA-292

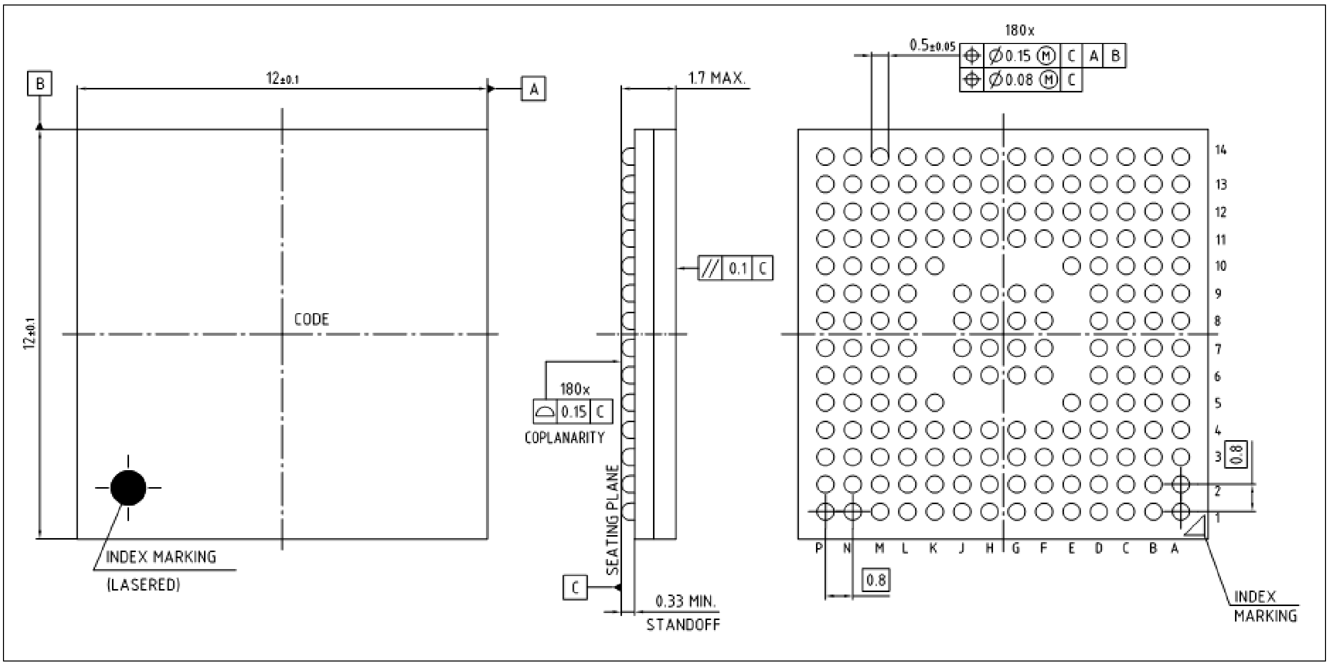


Figure 3-24 Package Outlines LFBGA-180

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

3.28.1 Package Parameters

Table 3-60 Package Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance (junction to ambient) [1]	RTH_JA CC	-	-	22	K/W	LFBGA180; Bottom Cooling
		-	-	14	K/W	LFBGA180; Top Cooling
		-	-	21	K/W	LFBGA292; Bottom Cooling
		-	-	13	K/W	LFBGA292; Top Cooling
Thermal resistance (junction to case bottom) [1]	RTH_JCB CC	-	-	4	K/W	LFBGA180
		-	-	4.5	K/W	LFBGA292
Thermal resistance (junction to case top) [1]	RTH_JCT CC	-	-	6	K/W	LFBGA180
		-	-	5	K/W	LFBGA292

1) The top and bottom thermal resistances between the case and the ambient (RTH_CTA, RTH_CBA) are to be combined with the thermal resistances between the junction and the case given above (RTH_JCT, RTH_JCB), in order to calculate the total thermal resistance between the junction and the ambient (RTH_JA). The thermal resistances between the case and the ambient (RTH_CTA, RTH_CBA) depend on the external system (PCB, case) characteristics and are under user responsibility.
The junction temperature can be calculated using the following equation: TJ = TA + RTH_JA * PD, where the RTH_JA is the total thermal resistance between the junction and the ambient.
Thermal resistances as measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1).

4 History

Version 0.4 is the first version of this document.

4.1 Changes from Version 0.4 to Version 0.6

- Changes in table 'Driver Mode Selection for Fast Pads' of Standard Pads
  - Change row ‘speed grade 4’ from ‘Reserved do not use this combination’ to ‘RGMII driver’
- Pin reliability in Overload
  - refined the phrase “full operation life-time is not exceeded” to “allowed time interval (defined in Note ...”
- High Performance LVDS Pads
  - changed “LVDSH” to “LVDS”
- Package parameters
  - changed Table layout “package parameters”
- Quality declarations
  - added Table “Example inactive lifetime”
  - added footnotes to table ‘Quality parameters’
- VADC 5V
  - updated preamble
  - updated figure ”Equivalent Circuitry for Analog Inpupts”
  - Change max value of Q_{AINS} from 3.5 pC to 4.4 pC
  - Add parameter *dVDDK*
  - Change note of V_{DDK} from '' to 'Measured at low temperature.'
  - Change note of R_{PDD} from '' to 'Measured at pad input voltage V_{IN} = V_{DDM} / 2.'
  - Change note of *TUE* from '12-bit resolution' to '12-bit resolution for primary/secondary groups, 10-bit resolution for fast compare channels'
  - Change note of t_{SCAL} from '100 ns' to '300 ns'
  - Change max value of Q_{AINS} from 3.8 pC to 4.8 pC
  - Change min value of t_{S} from 200 ns to 600 ns
  - Change note of t_{S} from '400 ns' to '800 ns'
- Current Consumption
  - Update footnote of $C_{\mathrm{urrent\ Consumption}}$ to 'Incase of FFT at maximum frequency with more accuracy, the current consumption would be higher.'
  - Change max value of I_{DDP3RAIL} from 60 mA to 45 mA
- Changes in table 'Module Current Consumption' of Current Consumption
  - Change max value of $I_{\mathrm{DDP3ERASE}}$ from 20 mA to 25 mA
  - Add parameter $I_{\mathrm{DDP3ERASE}}$
  - Change description of $I_{\mathrm{DDP3ERASE}}$ from 'Current adder for' to 'I_{DDP3} supply current for erasing of a Pflash or Dflash bank'
  - Change typ value of I_{SCRSB} from 0.190 mA to 0.150 mA
  - Change max value of I_{DDP3PROG} from 20 mA to 25 mA

  - Change note of I_{DDM} from 'real power pattern; current for EVADC modules only and EDSADC modules are inactive; 2 EVADC modules active.' to 'real power pattern; current for EVADC modules; 2 EVADC modules active.'
  - Change note of I_{DDM} from 'max power pattern; current for EVADC modules only and EDSADC modules are inactive; all EVADC modules active.' to 'max power pattern; current for EVADC modules; all EVADC modules active.'
  - Change note of $I_{DDPORST}$ from 'real power pattern; T_J=125°C' to 'V_{DD} = 1.275V; T_J=125°C'
  - Change max value of $I_{DDPORST}$ from 171 mA to 160 mA
- Changes in table 'Module Core Current Consumption' of Current Consumption
  - Change note of $I_{DDLBIST}$ from 'PATTERNS=0x00280, FREQU=5, SPLITSH=4' to 'LBIST Configuration A'
  - Change note of I_{DDSPU} from 'CTRL.DIV = 01 ; FFT clocked at half SPU Clock @150 MHz' to 'CTRL.DIV = 01 ; FFT clocked at half SPU Clock; FFT 512 points.'
  - Change note of $I_{DDTOTDC3}$ from 'real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 3.3V; T_J=160°C' to 'real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 3.3V; T_J=150°C'
  - Change note of $I_{DDTOTDC5}$ from 'real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 5V; T_J=160°C' to 'real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 5V; T_J=150°C'
  - Change note of I_{DDRAIL} from 'max power pattern' to 'ADAS max power pattern'
  - Change note of I_{DDRAIL} from 'ADAS power pattern' to 'ADAS real power pattern'
  - Change note of $I_{DDPORST}$ from ''real power pattern; T_J=150°C'' to ''V_{DD} = 1.275V; T_J=150°C''
  - Change note of $I_{DDPORST}$ from '290 mA' to '270 mA'
- Flash
  - Change typ value of t_{ER_Dev} from 10.4 s to 3 s
  - Change max value of t_{ER_Dev} from 18.5 s to 5 s
  - Change max value of t_{PRPB5_PF} from 16 s to 4 s
  - Change note of N_{E_EEP10S} from 'max data retention time 10y' to 'Retention time and Tj according below example temperature profile'
  - Add new parameter condition N_{E_EEP10S} from 'max data retention time 20 y, Tj=110°C'
  - Add new parameter condition N_{E_EEP10S} from 'max data retention time 8.2y, Tj=125°C'
  - Change note of N_{E_HSMS} from 'max data retention time 10y' to 'Retention time and Tj according below example temperature profile'
  - Add new parameter condition N_{E_HSMS} from 'max data retention time 20 y, Tj=110°C'
  - Add new parameter condition N_{E_HSM0S} from 'max data retention time 8.2y, Tj=125°C'
- PMS/EVR33 LDO
  - Change note of $dVout/dVin$ from '$dVin/dT$=1V/ms; dV= 3.6 to 5V; I_{MAX}=60mA' to '$dVin/dT$=1V/ms; dV= 3.6 to 5V; I_{MAX}=60mA; ΔV_{OUTTC} is included'
  - Change max value of $dVout/dVin$ from 20 mV to 40 mV
  - Change note of $dVout/dVin$ from '$dVin/dT$=1V/ms; dV= 5 to 3.6V; I_{MAX}=60mA' to '$dVin/dT$=1V/ms; dV= 5 to 3.6V; I_{MAX}=60mA; ΔV_{OUTTC} is included'
  - Change min value of $dVout/dVin$ from -20 mV to -40 mV
  - Change note of C_{OUT} from '0.65 µF' to '1.45 µF'
  - Change note of C_{OUT} from '1 µF' to '1.45 µF'
  - Change note of C_{OUT} from '1.35 µF' to '3 µF'
  - Change typ value of C_{OUT} from 2,2 µF to 2.2 µF
  - Add parameter $dVOUTTC$

  - Change note of t_{STR} from '' to 'Normal RUN mode'
  - Added footnote 7) for dV_{OUT} / dI_{OUT}
- Changes in table 'EVRC SMPS'
  - Changed condition of parameter dV_{DDDCT} / dI_{OUT}
- Changes in table 'Slow 3.3V GPIO' of Standard Pads
  - Change max value of V_{IL} from 0.44 * $V_{EXT/FLEX}$ V to 0.42 * $V_{EXT/FLEX}$ V
  - Change note of I_{PUH} from 'V_{IH}; AL and TTL (degraded, used for CIF); exept VGATE1P and T_J > 150°C' to 'V_{IH}; AL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C'
  - Change note of I_{PUH} from 'V_{IL}; AL and TTL and TTL (degraded, used for CIF); exept VGATE1P and T_J > 150°C' to 'V_{IL}; AL and TTL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C'
  - Change note of I_{PUH} from 'V_{IH}; TTL; exept VGATE1P and T_J > 150°C' to 'V_{IH}; TTL; exept VGATE1P; except VGATE1N and T_J > 150°C'
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
  - Change min value of I_{OZ} from -250 nA to -400 nA
  - Change note of I_{OZ} from '250 nA' to '400 nA'
  - Change min value of I_{OZ} from -300 nA to -600 nA
  - Change max value of I_{OZ} from 300 nA to 600 nA
  - Change min value of I_{OZ} from -500 nA to -750 nA
  - Change note of I_{OZ} from '500 nA' to '750 nA'
  - Change min value of I_{OZ} from -350 nA to -300 nA
  - Change note of I_{OZ} from '350 nA' to '300 nA'
  - Change min value of I_{OZ} from -550 nA to -400 nA
  - Change note of I_{OZ} from '550 nA' to '400 nA'
  - Change note of I_{OZ} from '-700 nA' to '-600 nA'
  - Change max value of I_{OZ} from 700 nA to 600 nA
  - Change note of I_{OZ} from '-1100 nA' to '-750 nA'
  - Change max value of I_{OZ} from 1100 nA to 750 nA
  - Change max value of I_{OZ} from 11000 nA to 18000 nA
  - Change min value of I_{OZ} from -11000 nA to -18000 nA
  - Change max value of I_{OZ} from 22000 nA to 38000 nA
  - Change note of I_{OZ} from '-22000 nA' to '-38000 nA'
- Changes in table 'Fast 3.3V GPIO' of Standard Pads
  - Change max value of V_{IL} from 0.44 * $V_{EXT/FLEX}$ V to 0.42 * $V_{EXT/FLEX}$ V
  - Change max value of I_{OZ} from 750 nA to 1100 nA
  - Change min value of I_{OZ} from -750 nA to -1100 nA
  - Change min value of I_{OZ} from -5000 nA to -6000 nA
  - Change max value of I_{OZ} from 5000 nA to 6000 nA
  - Change note of I_{OZ} from '-1300 nA' to '-2000 nA'
  - Change max value of I_{OZ} from 1300 nA to 2000 nA
  - Change note of I_{OZ} from '-2000 nA' to '-2500 nA'
  - Change max value of I_{OZ} from 2000 nA to 2500 nA

  - Change note of I_{OZ} from '-9000 nA' to '-13500 nA'
  - Change note of I_{OZ} from '9000 nA' to '13500 nA'
  - Change note of I_{OZ} from '-2300 nA' to '-1100 nA'
  - Change note of I_{OZ} from '-5000 nA' to '-2000 nA'
  - Change note of I_{OZ} from '2300 nA' to '1100 nA'
  - Change max value of I_{OZ} from 5000 nA to 2000 nA
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
- Changes in table 'RFast 3.3V pad' of Standard Pads
  - Change max value of V_{IL} from 0.44 * $V_{EXT/FLEX}$ V to 0.42 * $V_{EXT/FLEX}$ V
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
- Changes in table 'Fast 5V GPIO' of Standard Pads
  - Change note of I_{OZ} from '750 nA' to '1100 nA'
  - Change min value of I_{OZ} from -750 nA to -1100 nA
  - Change min value of I_{OZ} from -5000 nA to -6000 nA
  - Change max value of I_{OZ} from 5000 nA to 6000 nA
  - Change note of I_{OZ} from '-1300 nA' to '-2000 nA'
  - Change max value of I_{OZ} from 1300 nA to 2000 nA
  - Change note of I_{OZ} from '-2000 nA' to '-2500 nA'
  - Change note of I_{OZ} from '2000 nA' to '2500 nA'
  - Change min value of I_{OZ} from -9000 nA to -13500 nA
  - Change note of I_{OZ} from '9000 nA' to '13500 nA'
  - Change note of I_{OZ} from '-2300 nA' to '-1100 nA'
  - Change note of I_{OZ} from '-5000 nA' to '-2000 nA'
  - Change note of I_{OZ} from '2300 nA' to '1100 nA'
  - Change note of I_{OZ} from '5000 nA' to '2000 nA'
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
- Changes in table 'Slow 5V GPIO' of Standard Pads
  - Change max value of I_{OZ} from 250 nA to 400 nA
  - Change min value of I_{OZ} from -250 nA to -400 nA
  - Change note of I_{OZ} from '350 nA' to '600 nA'
  - Change note of I_{OZ} from '-350 nA' to '-600 nA'
  - Change min value of I_{OZ} from -500 nA to -750 nA
  - Change max value of I_{OZ} from 500 nA to 750 nA
  - Change note of I_{PUH} from 'V_{IH}; AL or TTL; exept VGATE1P and T_J > 150°C' to 'V_{IH};AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C'
  - Change note of I_{PUH} from 'V_{IL}; AL or TTL; exept VGATE1P and T_J > 150°C' to 'V_{IL}; AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C'
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
  - Change min value of I_{OZ} from -350 nA to -300 nA

  - Change max value of I_{OZ} from 350 nA to 300 nA
  - Change min value of I_{OZ} from -550 nA to -400 nA
  - Change note of I_{OZ} from '550 nA' to '400 nA'
  - Change min value of I_{OZ} from -700 nA to -600 nA
  - Change note of I_{OZ} from '700 nA' to '600 nA'
  - Change note of I_{OZ} from '-1100 nA' to '-750 nA'
  - Change max value of I_{OZ} from 1100 nA to 750 nA
  - Change max value of I_{OZ} from 11000 nA to 18000 nA
  - Change note of I_{OZ} from '-11000 nA' to '-18000 nA'
  - Change max value of I_{OZ} from 22000 nA to 38000 nA
  - Change min value of I_{OZ} from -22000 nA to -38000 nA
- Changes in table 'Class D' of Standard Pads
  - Change note of I_{OZ} from "$T_J \leq 150°C$; PDD option available, or AltRef option available and EDSADC channel connected" to "$T_J \leq 150°C$; PDD option available"
  - Change note of I_{OZ} from '-350 nA' to '-300 nA'
  - Change note of I_{OZ} from '350 nA' to '300 nA'
  - Change note of I_{OZ} from '$T_J \leq 170°C$; PDD option available, or AltRef option available and EDSADC channel connected' to '$T_J \leq 170°C$; PDD option available'
  - Change min value of I_{OZ} from -700 nA to -600 nA
  - Change max value of I_{OZ} from 700 nA to 600 nA
- Changes in table 'Class S 5V' of Standard Pads
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
- Changes in table 'RFast 5V GPIO' of Standard Pads
  - Change description of t_{SET} from 'Pad set-up time' to 'Pad set-up time to get an software update of the configuration active'
- Reset
  - Change max value of t_{BS} from 1 ms to 1.05 ms
  - Change max value of t_{BWP} from 1 ms to 1.3 ms
  - Change max value of t_B from 350 us to 400 us
  - Change note of $t_{SUPHOLD}$ from 'external supplies are V_{EVRSB}, V_{EXT}, V_{FLEX}, V_{EBU}, V_{DDM}, V_{DDP3} and V_{DD}' to 'external supplies are V_{EVRSB}, V_{EXT}, V_{FLEX}, V_{DDM}, V_{DDP3} and V_{DD}'
  - Change note of t_{BP} from 'Firmware execution time after warm PORST without EVR ramp-up; RAM initialization and HSM boot time is not included' to 'Firmware execution time after PORST release without EVR ramp-up; RAM initialization and HSM boot time is not included'
  - Change note of t_{LBIST} from 'PATTERNS=0x00040, FREQU=5, SPLITSH=4' to 'LBIST Configuration A'
  - Change description of t_{BP} from 'Power on Reset Boot Time' to 'Cold Power on Reset Boot Time'
- PLL Peripheral
  - Add parameter *JABS25*
  - Change note of *DP* from 'f_{DCO} = 640 MHz' to 'f_{DCO} = 640 MHz or f_{DCO} = 800 MHz'
  - Change note of D_{RMS} from 'measured over 1 µs; f_{REF} = 20 MHz; f_{DCO} = 640 MHz' to 'measured over 1 µs; f_{REF} = 20 MHz and f_{DCO} = 640 MHz or f_{REF} = 25 MHz and f_{DCO} = 800 MHz'
- Changes in table 'DTS Core' of DTS

  - Add parameter ΔT
- Changes in table 'LVDS - IEEE standard LVDS general purpose link (GPL)' of LVDS Pads
  - Change note of R_{in} from '1600 mV < $V_I \leq$ 2000 mV' to '$V_I \leq$ 2000 mV'
- Changes in table 'Overload Parameters' of Overload
  - Change note of I_{IN} from 'except LVDS pins' to 'except LVDS pins; limited to max. Operation Livetime hours'
  - Change note of I_{INLVDS} from '' to 'limited to max. Operation Livetime hours'
  - Change note of I_{ID} from 'All power supply voltages V_{DDx} = 0' to 'All power supply voltages V_{DDx} = 0; limited to max. Inactive Livetime hours'
  - Change note of I_{OUT} from '100% duty cycle; output driver = medium' to '100% duty cycle; output driver = medium; limited to max. Operation Livetime hours'
  - Change note of I_{OUT} from '100% duty cycle; output driver = strong' to '100% duty cycle; output driver = strong; limited to max. Operation Livetime hours'
- Absolute Maximum Ratings
  - Change description of V_{DDM} from 'Voltage at V_{DDM}, V_{EXT} and V_{FLEX} power supply pins with respect to V_{SS}' to 'Voltage at V_{DDM}, V_{EXT}, V_{FLEX} and V_{EVRSB} power supply pins with respect to V_{SS}'
  - Change max value of V_{DD} from 7V to 6.75V
  - Change max value of V_{IN} from 7V to 6.75V
- ED current consumption
  - Removed parameter I_{DDAGBT}
- AGBT timings
  - Added comment that AGBT is only for lab measurements.

4.2 Changes from Version 0.6 to Version 0.61

Changes in chapter “Pin Definition and Functions”

- Changes in chapter 'LFBGA292 ADAS Package Variants Pin Configuration of TC35x'
  - Changes in LFBGA-292 ADAS Package Variant 'Port 00 Functions' table; P00.0, P00.1, P00.2, P00.3, P00.4, P00.5
  - Changes in LFBGA-292 ADAS Package Variant 'Port 02 Functions' table; P02.0, P02.1, P02.2, P02.3, P02.4, P02.5, P02.8
  - Changes in LFBGA-292 ADAS Package Variant 'Port 10 Functions' table; P10.2, P10.3, P10.5, P10.6, P10.7, P10.8
  - Changes in LFBGA-292 ADAS Package Variant 'Port 11 Functions' table; P11.0, P11.1, P11.4, P11.5, P11.7, P11.8, P11.9, P11.10, P11.11, P11.12, P11.13
  - Changes in LFBGA-292 ADAS Package Variant 'Port 12 Functions' table; P12.0, P12.1
  - Changes in LFBGA-292 ADAS Package Variant 'Port 14 Functions' table; P14.0, P14.1, P14.2, P14.3, P14.4, P14.5, P14.6, P14.7, P14.8, P14.9, P14.10
  - Changes in LFBGA-292 ADAS Package Variant 'Port 15 Functions' table; P15.0, P15.1, P15.2, P15.3, P15.4, P15.5
  - Changes in LFBGA-292 ADAS Package Variant 'Port 20 Functions' table; P20.0, P20.3, P20.6, P20.7, P20.8, P20.9, P20.10
  - Changes in LFBGA-292 ADAS Package Variant 'Port 21 Functions' table; P21.0, P21.1
  - Changes in LFBGA-292 ADAS Package Variant 'Port 22 Functions' table; P22.4, P22.5
  - Changes in LFBGA-292 ADAS Package Variant 'Port 23 Functions' table; P23.0, P23.1, P23.2, P23.3

  - Changes in LFBGA-292 ADAS Package Variant 'Port 32 Functions' table; P32.2, P32.3, P32.4, P32.5, P32.6
  - Changes in LFBGA-292 ADAS Package Variant 'Port 33 Functions' table; P33.4, P33.5, P33.7, P33.8, P33.9, P33.10, P33.12, P33.13
  - Changes in LFBGA-292 ADAS Package Variant 'Port 34 Functions' table; P34.1, P34.2
  - Changes in LFBGA-292 ADAS Package Variant 'System I/O' table; Ball L7, K7, P10, P11, L14, K14, G11, G10, G17
- Added chapter 'LFBGA-180 ADAS Package Variants Pin Configuration of TC35x'
- Added chapter 'Sequence of Pads in Pad Frame'
- Changes in chapter 'Legend'
  - Added link to file TC35xpd_IO_Spirit_v1.0.0.1.20.xml
  - Changed description - Column “Buffer Type”: PU2 and PD2'

Changes in chapter “Electrical Specification”

- Changed wording in sub-chapter “Parameter Interpretation”
- Changes in table 'Absolute Maximum Ratings'
  - Added footnote 2) for V_{DD}
  - Changed order of footnotes
- Changes in table 'Pin Reliability in Overload'
  - Changed wording in chapter statements
- Changes in table 'Overload Parameters'
  - Changed parameter condition of I_{IN}
  - Removed note for I_{INLVDS}
  - Removed note for I_{INANA}
  - Removed parameter I_{ID}
  - Changed parameter condition of I_{OUT}
  - Changed parameter condition of K_{OVAP}
- Changes in table 'Operating Conditions'
  - Added footnote 1) for V_{DD}
  - Changed order of footnotes
- Changes in table 'PORST Pad'
  - Changed value name of parameter '*HYS*'
  - Changed parameter condition of I_{OZ}
  - Added values for parameter V_{IH}
  - Added values for parameter V_{IL}
  - Added footnote 2) for I_{PDL}
- Changes in table 'Fast 5V GPIO'
  - Changed note of t_{RF}
  - Changed value name of parameter '*HYS*'
  - Changed parameter condition of I_{OZ}
  - Combined equal values of I_{OZ} in single lines
  - Changed value name of parameter V_{IH}
  - Changed value name of parameter V_{IL}

  - Changed parameter condition of V_{ILD}
  - Changed footnote 2) for t_{RF}
  - Added footnote 4) for I_{PUH}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
- Changes in table 'Fast 3.3V GPIO'
  - Changed note of t_{RF}
  - Changed value name of parameter '*HYS*'
  - Changed parameter condition of I_{OZ}
  - Combined equal values of I_{OZ} in single lines
  - Changed value name of parameter V_{IH}
  - Changed value name of parameter V_{IL}
  - Changed parameter condition of V_{ILD}
  - Changed footnote 2) for t_{RF}
  - Added footnote 4) for I_{PUH}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
- Changes in table 'Slow 5V GPIO'
  - Changed value name of parameter '*HYS*'
  - Changed parameter condition of I_{OZ}
  - Combined equal values of I_{OZ} in single lines
  - Changed value names for parameter V_{IH}
  - Changed value names for parameter V_{IL}
  - Changed parameter condition of V_{ILD}
  - Changed footnote 2) for t_{RF}
  - Added footnote 4) for I_{PUH}
  - Removed footnote 4) for I_{OZ}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
- Changes in table 'Slow 3.3V GPIO'
  - Changed value name of parameter '*HYS*'
  - Changed parameter condition of I_{OZ}
  - Combined equal values of I_{OZ} in single lines
  - Changed value name of parameter V_{IH}
  - Changed value name of parameter V_{IL}
  - Changed parameter condition of V_{ILD}
  - Changed footnote 2) for t_{RF}
  - Removed footnote 4) for I_{OZ}
  - Added footnote 4) for I_{PUH}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
- Changes in table 'RFast 5V GPIO'

  - Changed parameter condition of t_{RF}
  - Changed value name of parameter 'HYS'
  - Changed parameter condition of I_{OZ}
  - Changed value name of parameter V_{IH}
  - Changed value name of parameter V_{IL}
  - Changed parameter condition of V_{ILD}
  - Changed footnote 2) for t_{RF}
  - Added footnote 4) for I_{PUH}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
- Changes in table 'RFast 3.3V pad'
  - Changed parameter condition of t_{RF}
  - Changed value name of parameter 'HYS'
  - Changed parameter condition of I_{OZ}
  - Changed value name of parameter V_{IH}
  - Changed value name of parameter V_{IL}
  - Changed parameter condition of V_{ILD}
  - Changed footnote 2) for t_{RF}
  - Added footnote 4) for I_{PUH}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
  - Changed driver setting in table 'Driver Mode Selection for Fast Pads'
- Changes in table 'ADC Reference Pads'
  - Removed values for parameter I_{OZ2}
- Changes in table 'VADC 5V'
  - Changed value and naming of parameter V_{AREF}
  - Added values for parameter V_{AREF}
  - Added footnote 1) for V_{AREF}
  - Added footnote 9) for Q_{CONV}
  - Changed order of footnotes
- Changes in table 'OSC_XTAL'
  - Removed parameter V_{IHBX}
  - Removed parameter V_{ILBX}
  - Added values for parameter DC_{X1}
  - Added values for parameter J_{ABSX1}
  - Added values for parameter SR_{XTAL1}
  - Added footnote 3) for DC_{X1} ,J_{ABSX1} ,SR_{XTAL1}
- Changes in table 'Back-up Clock'
  - Changed value of parameter f_{SB}
  - Changed footnote 1) for parameter f_{BACKT}
- Changes in table 'DTS PMS'
  - Added condition for parameter T_{NL}

- Changes in table 'DTS Core'
  - Added condition for parameter T_{NL}
- Changes in table 'Current Consumption'
  - Changed parameter name of I_{DDRAIL}
  - Changed footnote 3) for $I_{EXTFLEX}$
- Changes in table 'Module Current Consumption'
  - Changed value of parameter $I_{DDP3PROG}$
  - Changed and added values of parameter $I_{EXTLVDS}$
  - Changed value of parameter $I_{SCRIDLE}$
- Changes in table 'Module Core Current Consumption'
  - Changed condition of parameter $I_{DDLBIST}$
  - Changed footnote 1) for I_{DDHSM}
  - Added footnote 4) for $I_{DDLBIST}$
- Changes in chapter “Power Supply Infrastructure and Supply Start-up”
  - Changed figure and description for 'Single Supply Mode (a)'
  - Changed figure and description for 'Single Supply Mode (e)'
  - Changed figure and description for 'Single Supply Mode (d)'
  - Changed figure and description for 'Single Supply Mode (h)'
- Changes in table 'Reset'
  - Added parameter for $t_{WARMRSTSEQ}$
  - Changed parameter of t_{LBIST}
  - Added footnote 2) for t_{EVRPOR}
- Changes in table 'EVR33 LDO'
  - Added footnote 7) for *dVout/dIout*
- Changes in table 'Supply Monitors'
  - Changed parameter of V_{EXTMON}
  - Changed footnote 2) for $V_{EXTPRIUV}$, $V_{DDP3PRIUV}$, $V_{DDPRIUV}$
  - Added footnote 4) for V_{EXTMON}
  - Added footnote 5) for V_{EXTMON}, $V_{DDP3MON}$, V_{DDMON}
- Changes in table 'EVRC SMPS'
  - Changed values and conditions for f_{DCDC}
  - Changed value for ΔV_{DDDC}
  - Changed condition for dV_{DDDCT} / dI_{OUT}
- Changes in table 'EVRC SMPS External Components'
  - Removed values and conditions of C_{OUT}
  - Added values and conditions of L_{DC}
- Changed naming of chapter “Phase Locked Loop (PLL)” to “System Phase Locked Loop (SYS_PLL)”
- Changes in table “PLL System”
  - Removed parameter of f_{MV}
- Changes in table “PLL Peripheral”
  - Changed parameter of D_{PP}
  - Added parameter for D_{PPI}

- Changes in table “Master Mode Timing, LVDS Output Pads for Data and Clock”
  - Added footnote 1) for all parameters
- Changes in table “Receive Parameters”
  - Changed parameter naming for $t_{dCCRxD10}$
- Changes in table “Flash”
  - Changed parameter naming for N_{DFD}
  - Added parameter for N_{DFDC}
  - Added parameter for N_{UCBD}
  - Changed condition of parameter t_{RTU}
  - Added parameter for $t_{VER\_PAGE\_DC}$
  - Added parameter for $t_{VER\_PAGE\_DS}$
  - Removed parameter for $t_{VER\_PAGE\_D}$
  - Changed order of footnotes
- Changes in table “Quality Parameters”
  - Changed parameter naming for V_{HBM1}
- Removed table for “ED Current Consumption”
- Changes in chapter “Package Outline”
  - Added figure Package Outlines LF-BGA-180
- Changes in table “Package Parameters”
  - Added values for RTH_JA, RTH_JCB, RTH_JCT

4.3 Changes from Version 0.61 to Version 0.7

Changes in chapter Summary of Features, table “Platform Feature Overview”

- Added package LFBGA-180

Changes in chapter “Pin Definitions and Functions”

- Changed wording for packages LFBGA-292 and LFBGA-180
- Changes in table “Pin Definition and Functions: LFBGA-292”
  - Changes in table “System I/O” - Changed buffer type for symbol AGBTCLKN (VSS), ball L7
  - Changes in table “System I/O” - Changed buffer type for symbol AGBTCLKP (VSS), ball K7
  - Changes in table “System I/O” - Changed buffer type for symbol AGBTTXN (VSS), ball P10
  - Changes in table “System I/O” - Changed buffer type for symbol AGBTTXP (VSS), ball P11
  - Changes in sub-chapter “Legend” - new IO-Spirit version

Changes in chapter “Electrical Specification”

- Changes in table “Overload Parameters”
  - Changed note for parameter K_{OVAN}
  - Added footnote number of parameter K_{OVAN}
  - Changed note for parameter K_{OVAP}
  - Added footnote number of parameter K_{OVAP}
  - Added footnote 2)

- Changes in table “Fast 5V GPIO”
  - Deleted parameter V_{ILD}
- Changes in table “Fast 3.3V GPIO”
  - Deleted parameter V_{ILD}
- Changes in table “Slow 5V GPIO”
  - Deleted parameter V_{ILD}
- Changes in table “Slow 3.3V GPIO”
  - Deleted parameter V_{ILD}
- Changes in table “RFast 5V GPIO”
  - Deleted parameter V_{ILD}
- Changes in table “RFast 3.3V pad”
  - Deleted parameter V_{ILD}
- Changes in table “LVDS - IEEE standard LVDS general purpose link (GPL)”
  - Changed value for parameter V_I
  - Changed value in note of parameter R_{in}
- Changes in table “VADC 5V”
  - Changed values for parameter V_{DDK}
  - Changed note of parameter V_{AIN}
- Changes in table “OSC_XTAL”
  - Changed value for parameter J_{ABSX1}
- Changes in sub-chapter "Power Supply Current"
  - Changed description of "Realistic power pattern"
  - Added description of "Maximum power pattern"
- Changes in table “Current Consumption”
  - Changed value for parameter $I_{EXTFLEX}$
  - Added value for parameter for $I_{DDTOTDC3}$
  - Removed parameter for $I_{DDTOTDC5}$
  - Changed footnote 1)
- Changes in table “Module Current Consumption”
  - Changed footnote 4)
- Changes in table “Module Core Current Consumption”
  - Changed footnote 2)
  - Changed condition for I_{DDSPU1}, I_{DDSPU2}, $I_{DDSPULJ1}$, $I_{DDSPULJ2}$
- Changes in table “Reset”
  - Changed value for parameter t_{BWP}
  - Changed value for parameter t_{SCR}
- Changes in table “Supply Monitors”
  - Changed note of parameter V_{RST33}
  - Changed value and note of parameter V_{RSTC}
- Changes in sub-chapter “Package Outline”
  - Changed wording of image captions
- Changes in table “Package Parameters”

  - Changed value for parameter RTH_JA
  - Added values of parameter RTH_JA for package LFBGA-180
  - Added values of parameter RTH_JCB for package LFBGA-180
  - Added values of parameter RTH_JCT for package LFBGA-180
  - Split condition for RTH_JA into Top Cooling and Buttom Cooling

4.4 Changes from Version 0.7 to Version 0.71

Changes in chapter "Revision History"

- Added version hints for Data Sheet

Changes in chapter "Pin Definitions and Functions"

- Added explanation following table "Pad List"

Changes in chapter "Electrical Specification"

- Changes in sub-chapter "High performance LVDS Pads"
  - Added notes to table "LVDS - IEEE standard LVDS general purpose link (GPL)"
- Changes in sub-chapter "Power Supply Current"
  - Changed value of parameter I_{EVRSB}
  - Changed footnote 6) of table "Current Consumption"
- Changes in sub-chapter "System Phase Locked Loop (SYS_PLL)"
  - Changed value of parameter f_{REV} in table "PLL System"
  - Changed footnote 6) of table "Current Consumption"
- Changes in sub-chapter "ETH RGMII Parameters"
  - Added figure for "ETH RGMII TX Signal Timing (Delay on Destination (DoD))"
  - Added figure for "ETH RGMII RX Signal Timing (Delay on Source (DoS))"
- Changes in sub-chapter "Package Outline"
  - Changed figure numbers for Package Outlines LFBGA-292 and LFBGA-180
  - Added figure title of package outline for LFBGA-180
- Changes in sub-chapter "Package Parameters"
  - Changed notes of parameter RTH_JA in table "Package Parameters"

4.5 Changes from Version 0.71 to Version 1.0

Changes in chapter "Summary of Features", table "Platform Feature Overview"

- Changed number of Data Flash Instances to 2
- Removed ASIL Statement
- Added LFBGA-180 package and renamed LF-BGA-292 to LFBGA-292

Changes in chapter "Pin Definitions and Functions"

- Changes in sub-chapter "Sequence of Pads in Padframe"
  - Changed "Pad Type" for Pads: AGBTCLKN, AGBTCLKP, AGBTTXN, AGBTTXP

Changes in chapter "Electrical Specification"

- Changes in sub-chapter "Absolute Maximum Ratings"

  - Added Footnote 5) to parameter “Input current on any pin during overload condition”
- Changes in sub-chapter “Pin Reliability in Overload”
  - Removed parameter K_{OVDN} - “Overload coupling factor for digital inputs, negative” for TX pin as TX does not exist
  - Removed parameter K_{OVDP} - “Overload coupling factor for digital inputs, positive” for TX pin as TX does not exist
- Changes in sub-chapter “5V / 3.3V switchable Pads”
  - Removed comment in Note / Test Condition“ no analog input” for parameter I_{OZ} - “Input leackage current of Slow 5V GPIO”
  - Removed comment in Note / Test Condition“ no analog input” for parameter I_{OZ} - “Input leackage current of Slow 3.3V GPIO”
  - Added characteristics for Class S 5V and Class S 3.3V Pads
- Changes in sub-chapter “High performance LVDS Pads”
  - Changed wording in description
- Changes in sub-chapter “Power Supply Current”
  - Changed “Note/Test Condition” for parameter I_{DDM} -”Sum of external I_{DDM} supply currents” in table “Current Consumption” by removing “EDSADC” as module does not exist
  - Removed max. limit for parameter $I_{EXTLVDS}$ -”I_{EXT} supply current added by LVDS pads in LVDS mode” in table “Module Current Consumption” and adapted “Note/Test Condition” from “3 pairs of LVDS pins” to “ 2 pairs of LVDS pins”
  - Added sub-chapter “Calculating the 1.25V Current Consumption”
- Changes in sub-chapter “Reset Timing”
  - Changed max. limit for parameter t_{PIP} - “Ports inactive after PORST reset active”
- Changes in sub-chapter “EVR”
  - Added statement for number of allowed supply ramp cycles
  - Added digital thresholds to table “Supply Monitors” in column “Note/Test Condition” for parameter V_{EXTMON}, $V_{DDP3MON}$, V_{DDMONO}
- Changes in sub-chapter “Quality Declarations”
  - Increased max. limit for parameter V_{HBM1} - “ESD susceptibility of the LVDS pins according to Human Body Model (HBM)”
- Changes in sub-chapter “Parameters Specific to Emulation Part only”
  - sub-chapter removed
- Changes in sub-chapter “Package Outline”
  - Changed package names in figure titles from “LF-BGA-292” to “LFBGA-292” and “LF-BGA-180” to “LFBGA-180”

4.6 Changes from Version 1.0 to Version 1.1

- **Added the term “ on all Data Sheet pages**
  –
- **Changes in chapter “Revision History”**
  - Chronology completed
  –
- **Changes in chapter “Summary of Features”**

  - Changed wording for “DFLASH”
  - Added description for “AEC-Q100”
  - Added description for “ISO 26262 Safety Element”
  - Added description for Data Flash in table “Platform Feature Overview”
  - Added ASIL level to table “Platform Feature Overview”
  - Added footnote 1) for parameter Debug/ AGBT in table “Platform Feature Overview”
  - Added footnote 1) to table “Platform Feature Overview”
  -
- **Changes in chapter “TC35x Pin Definition and Functions”**
  - Added notes to table “System I/O” for “LFBGA-292 Package Variant”
  - Added notes to table “System I/O” for “LFBGA-180 Package Variant”
  - Changed pad type for pad names AGBT (144), AGBT (145), AGBT (148), AGBT (149) in Pad List of sub-chapter “Sequence of Pads in Pad Frame”
  - Deleted redundant wording in footnotes for sub-chapter “Sequence of Pads in Pad Frame”
  -
- **Changes in chapter “Electrical Specification”**
  - Changed parameter definition for ΣI_{IN} in table “Absolute Maximum Ratings”
  - Typos corrected in footnotes for sub-chapter “Absolute Maximum Ratings”
  - Changed table link numbering in sub-chapter “Pin Reliability in Overload”
  - Typo corrected for parameter I_{INSA} in table “Overload Parameters” of sub-chapter “Pin Reliability in Overload
  - Changed values for parameter GETH frequency in table “Operating Conditions”
  - Changed note for parameter t_{TX_ASYM} in table “Fast 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Fast 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Slow 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Slow 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “RFast 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “RFast 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Deleted tables “Class S 5V” and “Class S 3.3V” of sub-chapter “5V/3.3V switchable Pads” as they are not part of the product. This results in changing of subsequent table numbering
  - Typos corrected in footnotes for table “LVDS – IEEE standard LVDS general purpose link (GPL)” in sub-chapter “High performance LVDS Pads”
  - Added footnote sentence for table “LVDS – IEEE standard LVDS general purpose link (GPL)” in sub-chapter “High performance LVDS Pads”
  - Typo corrected for parameter dV_{CSD} in table “VADC 5V” in sub-chapter “VADC Parameters”
  - Changed footnote 3) and 6) of table “VADC 5V” in sub-chapter “VADC Parameters”
  - Changed footnote 7) of table “VADC 5V” in sub-chapter “VADC Parameters”
  - Changed figure “Equivalent Circuitry for Analog Inputs” in sub-chapter “VADC Parameters”
  - Changed spelling in footnote 2) for table “OSC_XTAL” in sub-chapter “MHz Oscillator”
  - Changed footnote 2) for table “Current Consumption” in sub-chapter “Power Supply Current”
  - Added footnote 7) to parameter *PD* in table “Current Consumption” for sub-chapter “Power Supply Current”
  - Added footnote 7) for table “Current Consumption” in sub-chapter “Power Supply Current”
  - Typos corrected in sub-chapter “Calculating the 1.25V Current Consumption”

- Added sentence to sub-chapter “Supply Ramp-up and Ramp-down Behavior”
- Changed/added value for parameter t_{PI} in table “Reset” for sub-chapter “Reset Timing”
- Typos corrected in footnotes for table “Supply Ramp” in sub-chapter “EVR”
- Changed value (from Max. to Typ.) for parameter R_{ON} in table “EVRC SMPS External components” for sub-chapter “EVR”
- Deleted value for parameter t_{52} in table “Master Mode Timing, LVDS output pads for data and clock” in sub-chapter “QSPI Timings, Master and Slave Mode”
- Changed values (from Min. to Typ.) for parameter t_7 in table “ETH MII Signal Timing Parameters” for sub-chapter “ETH MII Parameters”
- Changed symbols for parameters t_{13}, t_{14}, t_{15} in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Changed value (from Min. to Typ.) for parameter t_{13} in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Added footnote 3) to parameters t_{16}, t_{17} in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Added footnote 3) for table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Deleted parameter t_{81} in table “Skew Calibration Related” in sub-chapter “Radar Interface Timing”
- Changed values for parameters t_{82} and t_{83} in table “Skew Calibration Related” in sub-chapter “Radar Interface Timing”
- Deleted notes for parameters t_{82} and t_{83} in table “Skew Calibration Related” in sub-chapter “Radar Interface Timing”

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