RELIABILITY REPORT

FOR

MAX8685AETD+

PLASTIC ENCAPSULATED DEVICES

July 9, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX8685AETD+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX8685 family charges high-voltage photoflash capacitors quickly, while limiting peak drain from the battery, through an efficient flyback switching regulator. The internal n-channel MOSFET improves efficiency over competing bipolar designs by lowering switch-voltage dropout. An integrated insulated gate bipolar transistor (IGBT) driver enables flash discharge and reduces external component count. The device includes an open-drain active-low DONE output to indicate when the photoflash voltage has reached regulation. The device automatically refreshes the output voltage every 16s, thus efficiently maintains the capacitor charge level with minimum battery drain. The MAX8685A/MAX8685F feature an undervoltage input (UVI) monitor. UVI monitors the supply voltage and suspends switching if the input voltage drops below a programmed threshold. The MAX8685A/MAX8685F also feature a voltage-monitor output that provides a scaled replica of the output voltage. The voltage-monitor output is used for interfacing with a microprocessor's internal A/D converter to assist in implementing red-eye reduction. The MAX8685C/MAX8685D, with fixed peak-primary current limits of 1A and 1.6A, respectively, are offered in a 2mm x 3mm, 8-pin TDFN package. The MAX8685A/MAX8685F, with resistor-programmable current limits of up to 2A (max) and 2.6A (max), respectively, are offered in a 3mm x 3mm, 14-pin TDFN package. All devices operate over the -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	Xenon Photoflash Charger with IGBT Driver and Voltage Monitor
B. Process:	S4
C. Number of Device Transistors:	6702
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Thailand
F. Date of Initial Production:	January 19, 2007

III. Packaging Information

A. Package Type:	14-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2637
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8.3°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8.3°C/W

IV. Die Information

A. Dimensions:	50 X 58 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide
C. Interconnect:	Al/0.5%Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 47 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.8 \times 10^{-9}$

$\lambda = 22.8$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S45 Process results in a FIT Rate of 2.33 @ 25C and 28.16 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PP88 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX8685AETD+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	47	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data