19-3661; Rev 1; 8/05

EVALUATION KIT AVAILABLE

Configurable, Single-/Dual-Output, Synchronous Buck Controller for High-Current Applications

General Description

The MAX5066 is a two-phase, configurable single- or dual-output buck controller with an input voltage range of 4.75V to 5.5V or from 5V to 28V. Each phase of the MAX5066 is designed for 180° operation. A mode pin allows for a dual-output supply or connecting two phases together for a single-output, high-current supply. Each output channel of the MAX5066 drives n-channel MOSFETs and is capable of providing more than 25A of load current. The MAX5066 uses average current-mode control with a switching frequency up to 1MHz per phase where each phase is 180° out of phase with respect to the other. Out-of-phase operation results in significantly reduced input capacitor ripple current and output voltage ripple in dual-phase, single-output voltage applications. Each buck regulator output has its own high-performance current and voltage-error amplifier that can be compensated for optimum output filter L-C values and transient response.

The MAX5066 offers two enable inputs with accurate turn-on thresholds to allow for output voltage sequencing of the two outputs. The device's switching frequency can be programmed from 100kHz to 1MHz with an external resistor. The MAX5066 can be synchronized to an external clock. Each output voltage is adjustable from 0.61V to 5.5V. Additional features include thermal shutdown, "hiccup mode" short-circuit protection. Use the MAX5066 with adaptive voltage positioning for applications that require a fast transient response, or accurate output voltage regulation.

The MAX5066 is available in a thermally enhanced 28-pin TSSOP package capable of dissipating 1.9W. The device is rated for operation over the -40°C to +85°C extended, or -40°C to +125°C automotive temperature range.

Applications

High-End Desktop Computers

Graphics Cards

Networking Systems

Point-of-Load High-Current/High-Density Telecom DC-DC Regulators

RAID Systems

Features

- **4.75V to 5.5V or 5V to 28V Input**
- **Dual-Output Synchronous Buck Controller**
- **Configurable for Two Separate Outputs or One Single Output**
- **Each Output is Capable of Up to 25A Output Current**
- **Average Current-Mode Control Provides Accurate Current Limit**
- **180° Interleaved Operation Reduces Size of Input Filter Capacitors**
- **Limits Reverse Current Sinking When Operated in Parallel Mode**
- **Each Output is Adjustable from 0.61V to 5.5V**
- **Independently Programmable Adaptive Voltage Positioning**
- **Independent Shutdown for Each Output**
- **100kHz to 1MHz per Phase Programmable Switching Frequency**
- **Oscillator Frequency Synchronization from 200kHz to 2MHz**
- **Hiccup Mode Overcurrent Protection**
- **Overtemperature Shutdown**
- **Thermally Enhanced 28-Pin TSSOP Package Capable of Dissipating 1.9W**
- **Operates Over -40°C to +85°C or -40°C to +125°C Temperature Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5066EUI	-40°C to +85°C	28 TSSOP-EP*
MAX5066AUI	-40°C to +125°C	28 TSSOP-EP*

*Exposed Pad

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ABSOLUTE MAXIMUM RATINGS

IN to AGND .....-0.3V to +30V
BST_ to AGND .....-0.3V to +35V
DH_ to LX_ .....-0.3V to ($V_{BST\_}$ - $V_{LX\_}$) + 0.3V
DL_ to PGND .....-0.3V to (V_{DD} + 0.3V)
BST_ to LX_ .....-0.3V to +6V
V_{DD} to PGND .....-0.3V to +6V
AGND to PGND .....-0.3V to +0.3V
REG, RT/CLKIN, CSP_, CSN_ to AGND .....-0.3V to +6V
All Other Pins to AGND .....-0.3V to (V_{REG} + 0.3V)
REG Continuous Output Current
(Limited by Power Dissipation, No Thermal or Short-Circuit Protection).....67mA
REF Continuous Output Current 200µA
Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP (derate 23.8mW/°C above +70°C) 1904mW
Package Thermal Resistance (θ_{JC}) .....2°C/W
Operating Temperature Ranges
MAX5066EUI .....-40°C to +85°C
MAX5066AUI .....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{REG} = V_{DD} = $V_{EN\_}$ = +5V, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted, circuit of Figure 6. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM SPECIFICATIONS						
Input Voltage Range	V_{IN}		5		28	V
		IN and REG shorted together for +5V operation	4.75		5.5	
Quiescent Supply Current	I_{IN}	f_{OSC} = 500kHz, DH_, DL_ = open		4	20	mA
STARTUP/INTERNAL REGULATOR OUTPUT (REG)						
REG Undervoltage Lockout	UVLO	V_{REG} rising	4.0	4.15	4.5	V
Hysteresis	V_{HYST}			200		mV
REG Output Accuracy		V_{IN} = 5.8V to 28V, I_{SOURCE} = 0 to 65mA	4.75	5.10	5.30	V
REG Dropout		V_{IN} < 5.8V, I_{SOURCE} = 60mA			0.5	V
INTERNAL REFERENCE						
Internal Reference Voltage	$V_{EAN\_}$	EAN_ connected to EAOUT_ (Note 2)		0.6135		V
Internal Reference Voltage Accuracy	$V_{EAN\_}$	V_{IN} = V_{REG} = 4.75V to 5.5V or V_{IN} = 5V to 28V, EAN_ connected to EAOUT_ (Note 2)	-0.9		+0.9	%
EXTERNAL REFERENCE VOLTAGE OUTPUT (REF)						
Accuracy	V_{REF}	I_{REF} = 100µA	3.23	3.3	3.37	V
Load Regulation		I_{REF} = 0 to 200µA	3.2		3.4	V
MOSFET DRIVERS						
p-Channel Output Driver Impedance	R_{ON_P}			1.35	4	Ω
n-Channel Output Driver Impedance	R_{ON_N}			0.45	1.35	Ω
Output Driver Source Current	$I_{DH\_}$, $I_{DL\_}$			2.5		A
Output Driver Sink Current	$I_{DH\_}$, $I_{DL\_}$			8		A
Nonoverlap Time (Dead Time)	t_{NO}	$C_{DH\_}$ or $C_{DL\_}$ = 5nF		30		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{REG} = V_{DD} = $V_{EN\_}$ = +5V, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted, circuit of Figure 6. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OSCILLATOR							
Switching Frequency	f_{SW}	1MHz (max) switching frequency per phase	R_{RT} = 12.4kΩ		1000		kHz
			R_{RT} = 127kΩ		100		
Switching Frequency Accuracy		f_{SW} = 250kHz nominal, R_{RT} = 50kΩ		-7.5		+7.5	%
		f_{SW} = 1MHz nominal, R_{RT} = 12.4kΩ		-10		+10	
RT/CLKIN Output Voltage	$V_{RT/CLKIN}$				1.225		V
RT/CLKIN Current Sourcing Capability	$I_{RT/CLKIN}$				0.5		mA
RT/CLKIN Logic-High Threshold	$V_{RT/CLKIN\_H}$			2.4			V
RT/CLKIN Logic-Low Threshold	$V_{RT/CLKIN\_L}$					0.8	V
RT/CLKIN High Pulse Width	$t_{RT/CLKIN}$				30		ns
RT/CLKIN Synchronization Frequency Range	$f_{RT/CLKIN}$			200		2000	kHz
CURRENT LIMIT							
Average Current-Limit Threshold	$V_{CL\_}$	$V_{CSP\_}$ - $V_{CSN\_}$		20.4	22.5	24.75	mV
Reverse Current-Limit Threshold	$V_{RCL\_}$	$V_{CSP\_}$ - $V_{CSN\_}$		-3.13	-1.63	-0.1	mV
Cycle-by-Cycle Current-Limit Threshold	$V_{CLpk\_}$	$V_{CSP\_}$ - $V_{CSN\_}$			52.5		mV
Cycle-by-Cycle Current-Limit Response Time	t_R				260		ns
DIGITAL FAULT INTEGRATION (DF_)							
Number of Switching Cycles to Shutdown in Current-Limit	$NS_{DF\_}$				32,768		Clock cycles
Number of Switching Cycles to Recover from Shutdown	$NR_{DF\_}$				524,288		Clock cycles
CURRENT-SENSE AMPLIFIER							
CSP_ to CSN_ Input Resistance	$R_{CS\_}$				1.9835		kΩ
Common-Mode Range	$V_{CMR(CS)}$	V_{IN} = V_{REG} = 4.75V to 5.5V or V_{IN} = 5V to 10V		-0.3		+3.6	V
		V_{IN} = 7V to 28V		-0.3		+5.5	V
Input Offset Voltage	$V_{OS(CS)}$				100		µV
Amplifier Gain	$A_{V(CS)}$				36		V/V
-3dB Bandwidth	f_{-3dB}				4		MHz
CSP_ Input Bias Current	$I_{CSA(IN)}$	$V_{CSP\_}$ = 5.5V, sinking				120	µA
		$V_{CSP\_}$ = 0V, sourcing				30	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{REG} = V_{DD} = $V_{EN\_}$ = +5V, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted, circuit of Figure 6. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-ERROR AMPLIFIER (CEA_)						
Transconductance	g_M			550		µS
Open-Loop Gain	$A_{VOL(CEA)}$	No load		50		dB
VOLTAGE ERROR AMPLIFIER (EAOUT_)						
Open-Loop Gain	$A_{VOL(EA)}$			70		dB
Unity-Gain Bandwidth	f_{UGEA}			3		MHz
EAN_ Input Bias Current	$I_{BIAS(EA)}$	$V_{EAN\_}$ = 2.0V		100		nA
Error Amplifier Output Clamping High Voltage	$V_{CLMP\_HI (EA)}$	With respect to V_{CM}		1.14		V
Error Amplifier Output Clamping Low Voltage	$V_{CLMP\_LO (EA)}$	With respect to V_{CM}		-0.234		V
EN_ INPUTS						
EN_ Input High Voltage	V_{ENH}	EN rising	1.204	1.222	1.240	V
EN_ Hysteresis				0.05		
EN_ Input Leakage Current	I_{EN}		-1		+1	µA
MODE INPUT						
MODE Logic-High Threshold	V_{MODE_H}		2.4			V
MODE Logic-Low Threshold	V_{MODE_L}				0.8	V
MODE Input Pulldown	$I_{PULLDWN}$			5		µA
THERMAL SHUTDOWN						
Thermal Shutdown	T_{SHDN}			160		°C
Thermal Shutdown Hysteresis	T_{HYST}			10		

Note 1: The device is 100% production tested at T_A = +85°C (MAX5066EUI) and T_A = T_J = +125°C (MAX5066AUI). Limits at -40°C and +25°C are guaranteed by design.

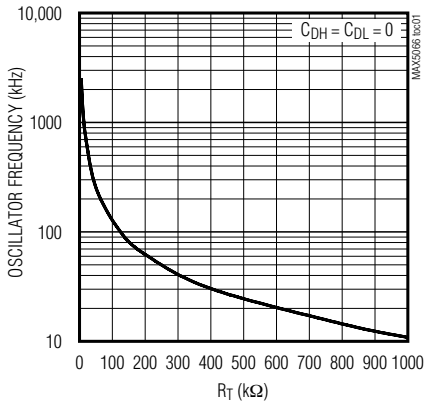
Note 2: The internal reference voltage accuracy is measured at the negative input of the error amplifiers (EAN_). Output voltage accuracy must include external resistor-divider tolerances.

Configurable, Single-/Dual-Output, Synchronous Buck Controller for High-Current Applications

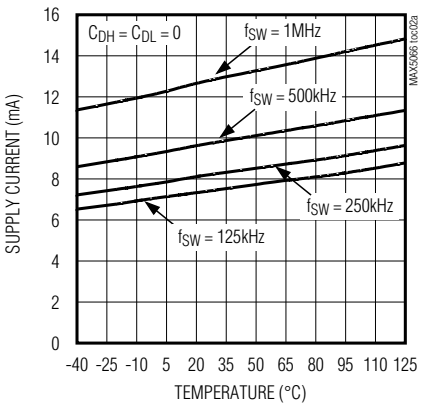
Typical Operating Characteristics

(Circuit of Figure 6, T_A = +25°C, unless otherwise noted. V_{IN} = 12V, V_{OUT1} = 0.8V, V_{OUT2} = 1.3V, f_{SW} = 500kHz per phase.)

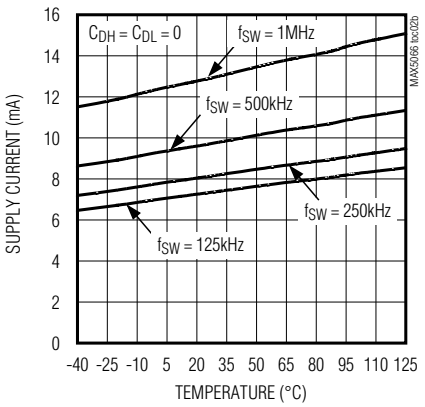
OSCILLATOR FREQUENCY vs. R_T



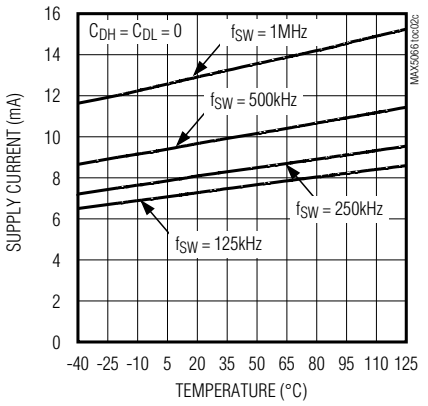
SUPPLY CURRENT vs. TEMPERATURE AND FREQUENCY (V_{IN} = 5V)



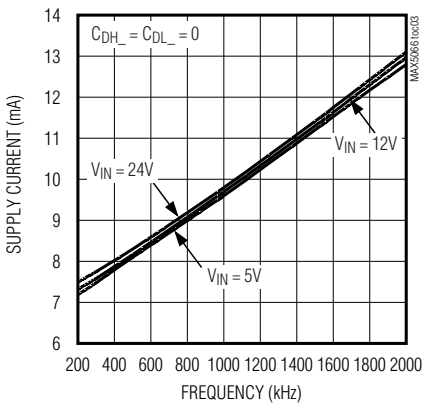
SUPPLY CURRENT vs. TEMPERATURE AND FREQUENCY (V_{IN} = 12V)



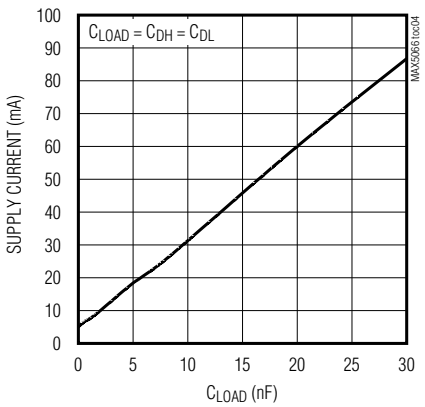
SUPPLY CURRENT vs. TEMPERATURE AND FREQUENCY (V_{IN} = 24V)



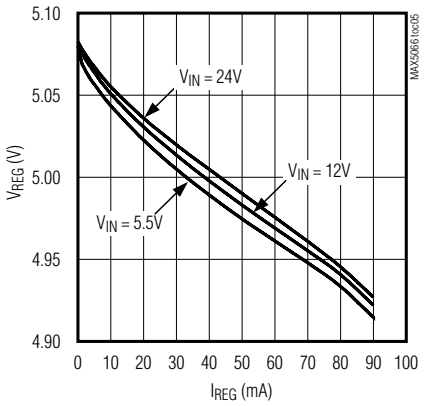
SUPPLY CURRENT vs. OSCILLATOR FREQUENCY



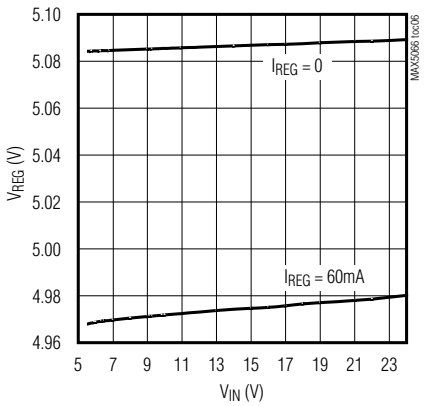
SUPPLY CURRENT vs. DRIVER LOAD CAPACITANCE



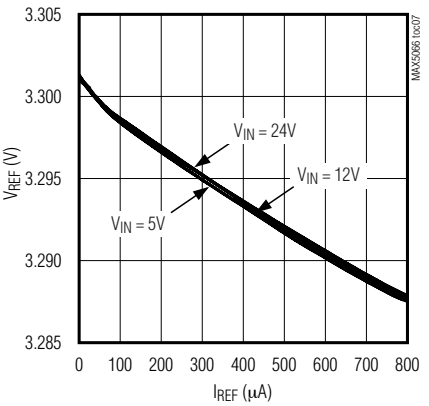
REG LOAD REGULATION



REG LINE REGULATION



REF LOAD REGULATION

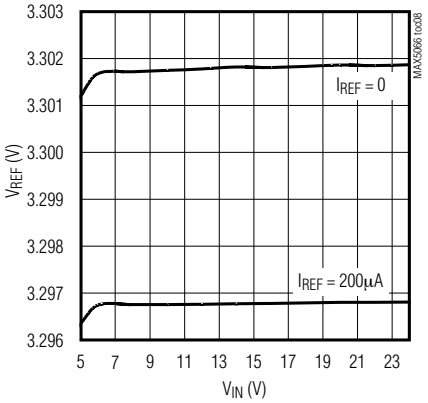


Configurable, Single-/Dual-Output, Synchronous Buck Controller for High-Current Applications

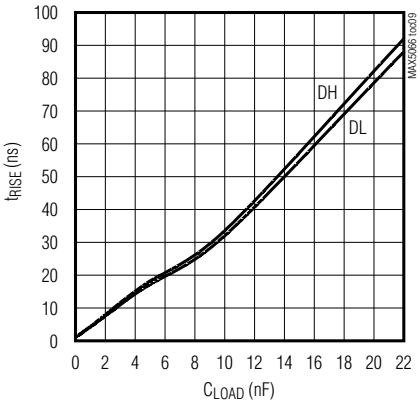
Typical Operating Characteristics (continued)

(Circuit of Figure 6, T_A = +25°C, unless otherwise noted. V_{IN} = 12V, V_{OUT1} = 0.8V, V_{OUT2} = 1.3V, f_{SW} = 500kHz per phase.)

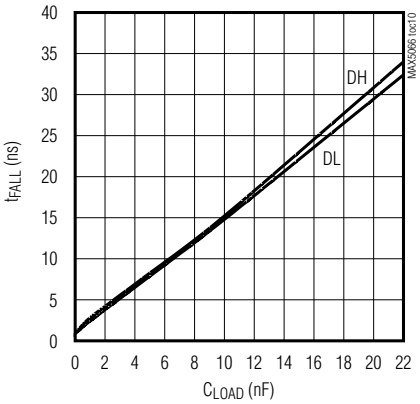
REF LINE REGULATION



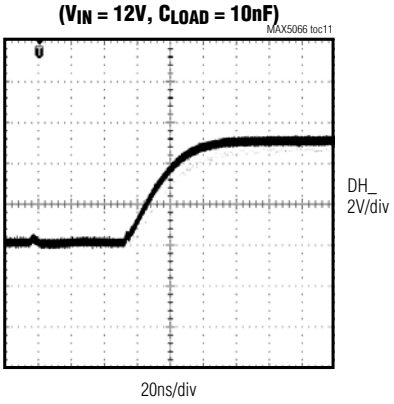
DRIVER RISE TIME vs. LOAD CAPACITANCE



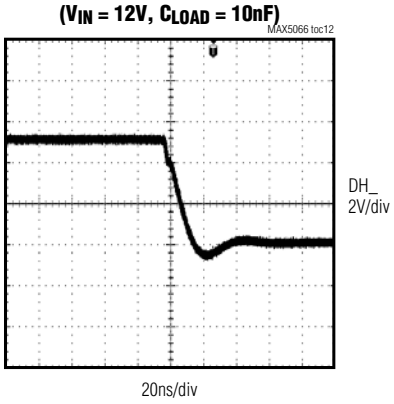
DRIVER FALL TIME vs. LOAD CAPACITANCE



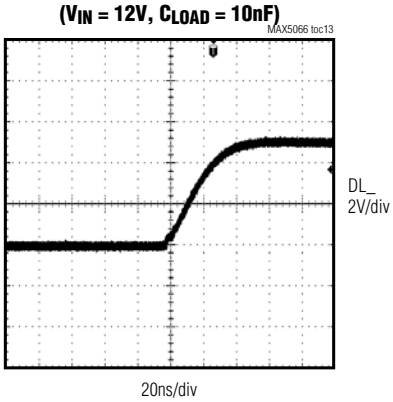
HIGH-SIDE DRIVER RISE TIME (V_{IN} = 12V, C_{LOAD} = 10nF)



HIGH-SIDE DRIVER FALL TIME (V_{IN} = 12V, C_{LOAD} = 10nF)



LOW-SIDE DRIVER RISE TIME (V_{IN} = 12V, C_{LOAD} = 10nF)

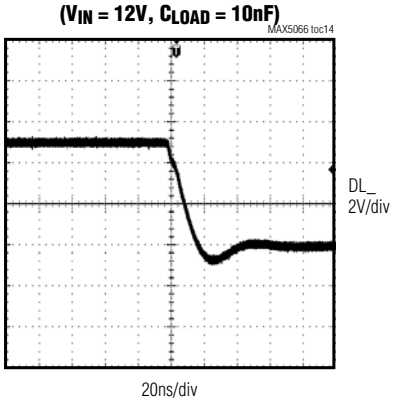


Configurable, Single-/Dual-Output, Synchronous Buck Controller for High-Current Applications

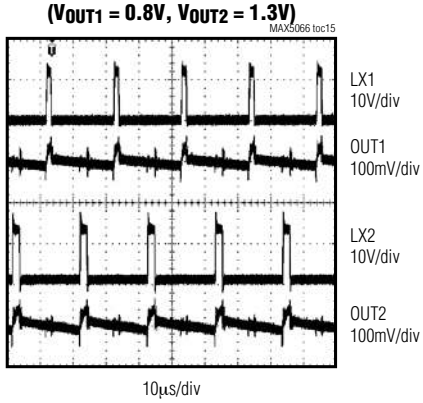
Typical Operating Characteristics (continued)

(Circuit of Figure 6, T_A = +25°C, unless otherwise noted. V_{IN} = 12V, V_{OUT1} = 0.8V, V_{OUT2} = 1.3V, f_{SW} = 500kHz per phase.)

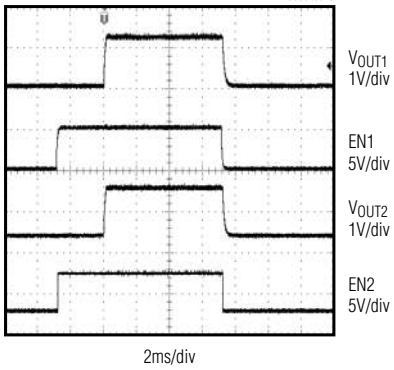
LOW-SIDE DRIVER FALL TIME
(V_{IN} = 12V, C_{LOAD} = 10nF)



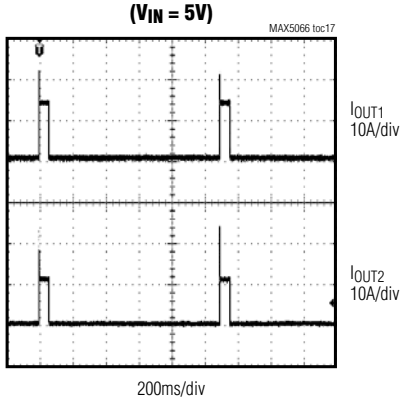
OUT1/OUT2 OUT-OF-PHASE WAVEFORMS
(V_{OUT1} = 0.8V, V_{OUT2} = 1.3V)



TURN-ON/-OFF WAVEFORMS
(I_{OUT1} = I_{OUT2} = 10A)



SHORT-CIRCUIT CURRENT WAVEFORMS
(V_{IN} = 5V)



Configurable, Single-/Dual-Output, Synchronous Buck Controller for High-Current Applications

Pin Description

PIN	NAME	FUNCTION
1	CSN2	Current-Sense Differential Amplifier Negative Input for Output2. Connect CSN2 to the negative terminal of the sense resistor. The differential voltage between CSP2 and CSN2 is internally amplified by the current-sense amplifier ($A_{V(CS)}$ = 36V/V).
2	CSP2	Current-Sense Differential Amplifier Positive Input for Output2. Connect CSP2 to the positive terminal of the sense resistor. The differential voltage between CSP2 and CSN2 is internally amplified by the current-sense amplifier ($A_{V(CS)}$ = 36V/V).
3	EAOUT2	Voltage Error-Amplifier Output2. Connect to an external gain-setting feedback resistor. The error-amplifier gain determines the output voltage load regulation for adaptive voltage positioning. This output also serves as the compensation network connection from EAOUT2 to EAN2. A resistive network results in a drooped output voltage regulation characteristic. An integrator configuration results in very tight output voltage regulation (see the *Adaptive Voltage Positioning* section).
4	EAN2	Voltage Error-Amplifier Inverting Input for Output2. Connect a resistive divider from V_{OUT2} to EAN2 to AGND to set the output voltage. A compensation network connects from EAOUT2 to EAN2. A resistive network results in a drooped output-voltage-regulation characteristic. An integrator configuration results in very tight output-voltage regulation (see the *Adaptive Voltage Positioning* section).
5	CLP2	Current-Error Amplifier Output2. Compensate the current loop by connecting an R-C network from CLP2 to AGND.
6	REF	3.3V Reference Output. Bypass REF to AGND with a minimum 0.1µF ceramic capacitor. REF can source up to 200µA for external loads.
7	RT/CLKIN	External Clock Input or Internal Frequency-Setting Connection. Connect a resistor from RT/CLKIN to AGND to set the switching frequency. Connect an external clock at RT/CLKIN for external frequency synchronization.
8	AGND	Analog Ground
9	MODE	Mode Function Input. MODE selects between a single-output dual phase or a dual-output buck regulator. When MODE is grounded, VEA1 and VEA2 connect to CEA1 and CEA2, respectively (see Figure 1) and the device operates as a two-output, out-of-phase buck regulator. When MODE is connected to REG (logic high), VEA2 is disconnected and VEA1 is routed to both CEA1 and CEA2.
10	CLP1	Current-Error Amplifier Output1. Compensate the current loop by connecting an R-C network from CLP1 to AGND.
11	EAN1	Voltage Error Amplifier Inverting Input for Output1. Connect a resistive divider from V_{OUT1} to EAN1 to regulate the output voltage. A compensation network connects from EAOUT1 to EAN1. A resistive network results in a drooped output-voltage-regulation characteristic. An integrator configuration results in very tight output voltage regulation (see the *Adaptive Voltage Positioning* section).
12	EAOUT1	Voltage Error Amplifier Output1. Connect to an external gain-setting feedback resistor. The error amplifier gain determines the output-voltage-load regulation for adaptive voltage positioning. This output also serves as the compensation network connection from EAOUT1 to EAN1. A resistive network results in a drooped output-voltage-regulation characteristic. An integrator configuration results in very tight output-voltage regulation (see the *Adaptive Voltage Positioning* section).
13	CSP1	Current-Sense Differential Amplifier Positive Input for Output1. Connect CSP1 to the positive terminal of the sense resistor. The differential voltage between CSP1 and CSN1 is internally amplified by the current-sense amplifier ($A_{V(CS)}$ = 36V/V).

Pin Description (continued)

PIN	NAME	FUNCTION
14	CSN1	Current-Sense Differential Amplifier Negative Input for Output1. Connect CSN1 to the negative terminal of the sense resistor. The differential voltage between CSP1 and CSN1 is internally amplified by the current-sense amplifier ($A_{V(CS)}$ = 36V/V).
15	EN1	Output 1 Enable. A logic-low shuts down channel 1's MOSFET drivers. EN1 can be used for output sequencing.
16	BST1	Boost Flying Capacitor Connection. Reservoir capacitor connection for the high-side MOSFET driver supply. Connect a 0.47µF ceramic capacitor between BST1 and LX1.
17	DH1	High-Side Gate Driver Output1. DH1 drives the gate of the high-side MOSFET.
18	LX1	External inductor connection and source connection for the high-side MOSFET for Output1. LX1 also serves as the return terminal for the high-side MOSFET driver.
19	DL1	Low-Side Gate Driver Output1. Gate driver output for the synchronous MOSFET.
20	V_{DD}	Supply Voltage for Low-Side Drivers. REG powers V_{DD}. Connect a parallel combination of 0.1µF and 1µF ceramic capacitors from V_{DD} to PGND and a 1Ω resistor from V_{DD} to REG to filter out the high-peak currents of the driver from the internal circuitry.
21	REG	Internal 5V Regulator Output. REG is derived internally from IN and is used to power the internal bias circuitry. Bypass REG to AGND with a 4.7µF ceramic capacitor.
22	IN	Supply Voltage Connection. Connect IN to a 5V to 28V input supply.
23	PGND	Power Ground. Source connection for the low-side MOSFET. Connect V_{DD}'s bypass capacitor returns to PGND.
24	DL2	Low-Side Gate Driver Output2. Gate driver for the synchronous MOSFET.
25	LX2	External inductor connection and source connection for the high-side MOSFET for Output2. Also serves as the return terminal for the high-side MOSFET driver.
26	DH2	High-Side Gate Driver Output2. DH2 drives the gate of the high-side MOSFET.
27	BST2	Boost Flying Capacitor Connection. Reservoir capacitor connection for the high-side MOSFET driver supply. Connect a 0.47µF ceramic capacitor between BST2 and LX2.
28	EN2	Output 2 Enable. A logic-low shuts down channel 2's MOSFET drivers. EN2 can be used for output sequencing.
EP	EP	Exposed Pad. Connect exposed pad to ground plane.

Detailed Description

The MAX5066 switching power-supply controller can be configured in two ways. With the MODE input high, it operates as a single-output, dual-phase, step-down switching regulator where each output is 180° out of phase. With the MODE pin connected low, the MAX5066 operates as a dual-output, step-down switching regulator. The average current-mode control topology of the MAX5066 offers high-noise immunity while having benefits similar to those of peak current-mode control. Average current-mode control has the intrinsic ability to accurately limit the average current sourced by the converter during a fault condition. When a fault condition occurs, the error amplifier output voltage (EAOUT1 or EAOUT2) that connects to the positive input of the transconductance amplifier (CA1 or CA2) is clamped thus limiting the output current.

The MAX5066 contains all blocks necessary for two independently regulated average current-mode PWM regulators. It has two voltage error amplifiers (VEA1 and VEA2), two current-error amplifiers (CEA1 and CEA2), two current-sensing amplifiers (CA1 and CA2), two PWM comparators (CPWM1 and CPWM2), and drivers for both low- and high-side power MOSFETs (see Figure 1). Each PWM section is also equipped with a pulse-by-pulse, current-limit protection and a fault integration block for hiccup protection.

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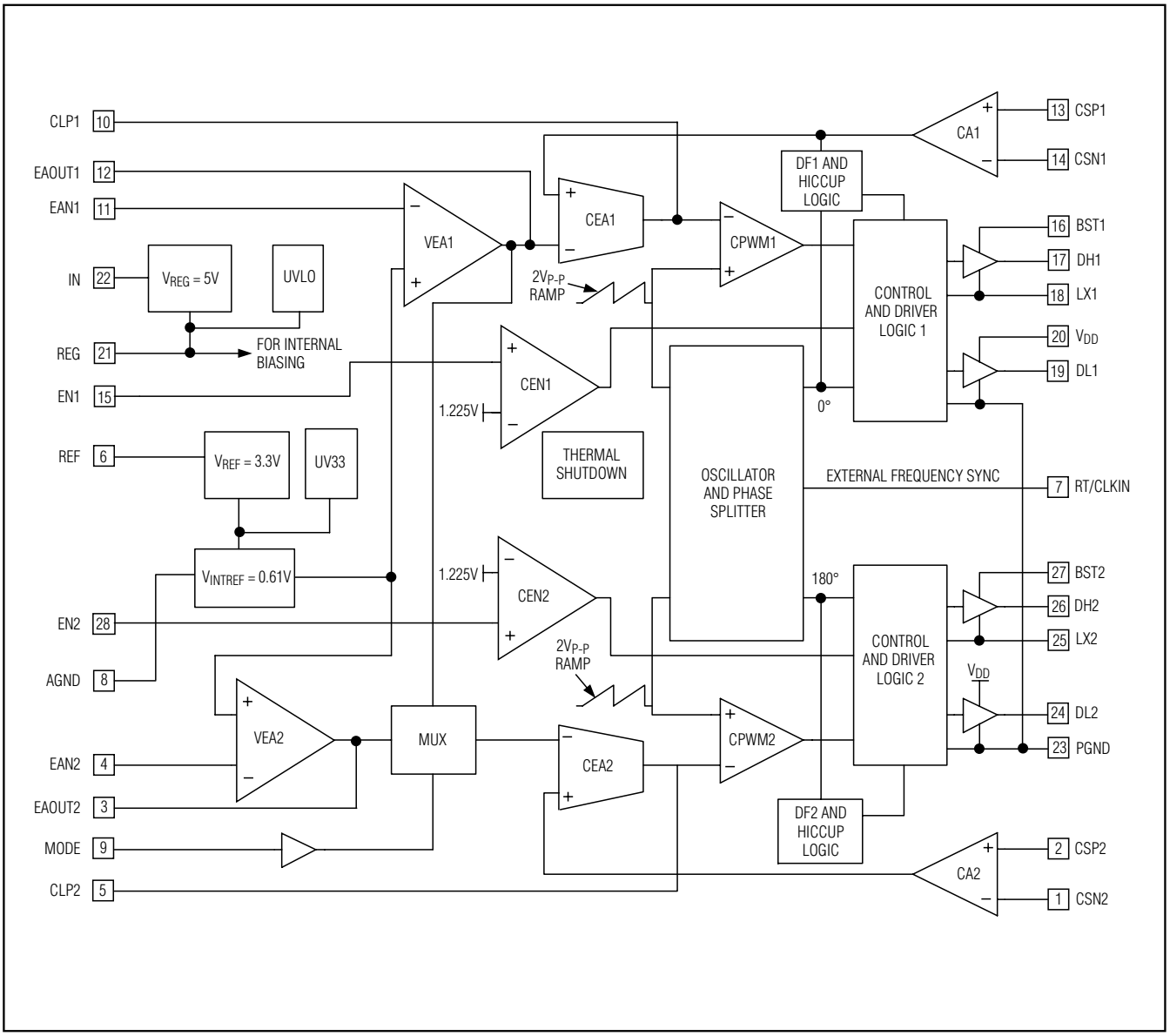

Figure 1. Block Diagram

Two enable comparators (CEN1 and CEN2) are available to control and sequence the two PWM sections through the enable (EN1 or EN2) inputs. An oscillator, with an externally programmable frequency generates two clock pulse trains and two ramps for both PWM sections. The two clocks and the two ramps are 180° out of phase with each other.

A linear regulator (REG) generates the 5V to supply the device. This regulator has the output-current capability necessary to provide for the MAX5066's internal circuitry and the power for the external MOSFET's gate drivers. A low-current linear regulator (REF) provides a precise 3.3V reference output and is capable of driving loads of up to 200µA. Internal UVLO circuitry ensures that the MAX5066 starts up only when V_{REG} and V_{REF} are at the correct voltage levels to guarantee safe operation of the IC and of the power MOSFETs.

Finally, a thermal-shutdown feature protects the device during thermal faults and shuts down the MAX5066 when the die temperature exceeds +160°C.

Dual-Output/Dual-Phase Select (MODE)

The MAX5066 can operate as a dual-output independently regulated buck converter, or as a dual-phase, single-output buck converter. The MODE input selects between the two operating modes. When MODE is grounded (logic low), VEA1 and VEA2 connect to CEA1 and CEA2, respectively (see Figure 1) and the device operates as a two-output DC-DC converter. When MODE is connected to REG (logic high), VEA2 is disconnected and VEA1 is routed to both CEA1 and CEA2 and the device works as a dual-phase, single-output buck regulator with each output 180° out of phase with respect to each other.

Supply Voltage Connections (V_{IN}/V_{REG})

The MAX5066 accepts a wide input voltage range at IN of 5V to 28V. An internal linear regulator steps down V_{IN} to 5.1V (typ) and provides power to the MAX5066. The output of this regulator is available at REG. For V_{IN} = 4.75V to 5.5V, connect IN and REG together externally. REG can supply up to 65mA for external loads. Bypass REG to AGND with a 4.7µF ceramic capacitor for high-frequency noise rejection and stable operation.

REG supplies the current for both the MAX5066's internal circuitry and for the MOSFET gate drivers (when connected externally to V_{DD}), and can source up to 65mA. Calculate the maximum bias current (I_{BIAS}) for the MAX5066:

$$I_{BIAS} = I_{IN} + f_{SW} \times (Q_{GQ1} + Q_{GQ2} + Q_{GQ3} + Q_{GQ4})$$

where I_{IN} is the quiescent supply current into IN (4mA, typ), Q_{GQ1}, Q_{GQ2}, Q_{GQ3}, Q_{GQ4} are the total gate charges of MOSFETs Q1 through Q4 at V_{GS} = 5V (see Figure 6), and f_{SW} is the switching frequency of each individual phase.

Low-Side MOSFET Driver Supply (V_{DD})

V_{DD} is the power input for the low-side MOSFET drivers. Connect the regulator output REG externally to V_{DD} through an R-C lowpass filter. Use a 1Ω resistor and a parallel combination of 1µF and 0.1µF ceramic capacitors to filter out the high peak currents of the MOSFET drivers from the sensitive internal circuitry.

High-Side MOSFET Drive Supply (BST_)

BST1 and BST2 supply the power for the high-side MOSFET drivers for output 1 and output 2, respectively. Connect BST1 and BST2 to V_{DD} through rectifier diodes D1 and D2 (see Figure 6). Connect a 0.1µF ceramic capacitor between BST_ and LX_.

Minimize the trace inductance from BST_ and V_{DD} to rectifier diodes, D1 and D2, and from BST_ and LX_ to the boost capacitors, C8 and C9 (see Figure 6). This is accomplished by using short, wide trace lengths.

Undervoltage Lockout (UVLO)/ Power-On Reset (POR)/Soft-Start

The MAX5066 includes an undervoltage lockout (UVLO) with hysteresis, and a power-on reset circuit for converter turn-on and monotonic rise of the output voltage. The UVLO threshold monitors V_{REG} and is internally set between 4.0V and 4.5V with 200mV of hysteresis. Hysteresis eliminates "chattering" during startup. Most of the internal circuitry, including the oscillator, turns on when V_{REG} reaches 4.5V. The MAX5066 draws up to 4mA (typ) of current before V_{REG} reaches the UVLO threshold.

The compensation network at the current-error amplifiers (CLP1 and CLP2) provides an inherent soft-start of the output voltage. It includes (R14 and C10) in parallel with C11 at CLP1 and (R15 and C12) in parallel with C13 at CLP2 (see Figure 6). The voltage at the current-error amplifier output limits the maximum current available to charge the output capacitors. The capacitor at CLP_ in conjunction with the finite output-drive current of the current-error amplifier yields a finite rise time for the output current and thus the output voltage.

Setting the Switching Frequency (f_{SW})

An internal oscillator generates the 180° out-of-phase clock signals required for both PWM modulators. The oscillator also generates the $2V_{P-P}$ voltage ramps necessary for the PWM comparators. The oscillator frequency can be set from 200kHz to 2MHz by an external resistor (R_T) connected from RT/CLKIN to AGND (see Figure 6). The equation below shows the relationship between R_T and the switching frequency:

$$f_{OSC} = \frac{2.5 \times 10^{10}}{R_{RT}} Hz$$

where R_{RT} is in ohms and $f_{SW(PER\ PHASE)} = f_{OSC}/2$.

Use RT/CLKIN as a clock input to synchronize the MAX5066 to an external frequency ($f_{RT/CLKIN}$). Applying an external clock to RT/CLKIN allows each PWM section to work at a frequency equal to $f_{RT/CLKIN}/2$. An internal comparator with a 1.6V threshold detects $f_{RT/CLKIN}$. If $f_{RT/CLKIN}$ is present, internal logic switches from the internal oscillator clock, to the clock present at RT/CLKIN.

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Hiccup Fault Protection

The MAX5066 includes overload fault protection circuitry that prevents damage to the power MOSFETs. The fault protection consists of two digital fault integration blocks that enable "hiccuping" under overcurrent conditions. This circuit works as follows: for every clock cycle the current-limit threshold is exceeded, the fault integration counter increments by one count. Thus, if the current-limit condition persists, then the counter reaches its shutdown threshold in 32,768 counts and shuts down the external MOSFETs. When the MAX5066 shuts down due to a fault, the counter begins to count down, (since the current-limit condition has ended), once every 16 clock cycles. Thus, the device counts down for 524,288 clock cycles. At this point, switching resumes. This produces an effective duty cycle of 6.25% power-up and 93.75% power-down under fault conditions. With a switching frequency set to 250kHz, power-up and power-down times are approximately 131ms and 2.09s, respectively.

Control Loop

The MAX5066 uses an average current-mode control topology to regulate the output voltage. The control loop consists of an inner current loop and an outer voltage loop. The inner current loop controls the output current, while the outer voltage loop controls the output voltage. The inner current loop absorbs the inductor pole, reducing the order of the outer voltage loop to that of a single-pole system. Figure 2 is the block diagram of OUT1's control loop.

The current loop consists of a current-sense resistor, R_{SENSE}, a current-sense amplifier (CA1), a current-error amplifier (CEA1), an oscillator providing the carrier ramp, and a PWM comparator (CPWM1). The precision current-sense amplifier (CA1) amplifies the sense voltage across R_{SENSE} by a factor of 36. The inverting input to CEA1 senses the output of CA1. The output of CEA1 is the difference between the voltage-error amplifier output (EAOUT1) and the gained-up voltage from CA1. The RC compensation network connected to CLP1 provides external frequency compensation for the respective CEA1 (see the *Compensation* section). The start of every clock cycle enables the high-side driver and initiates a PWM on-cycle. Comparator CPWM1 compares the output voltage from CEA1 against a 0 to 2V ramp from the

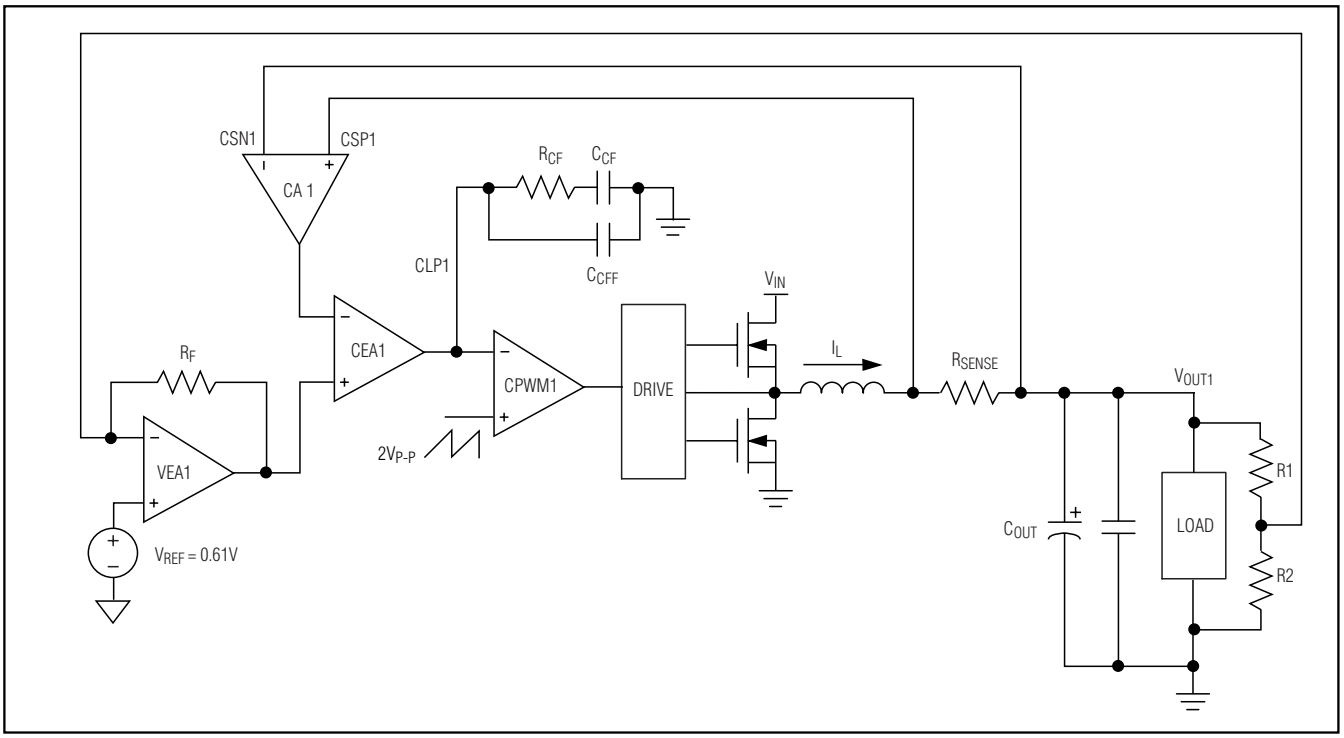

Figure 2. Current and Voltage Loops

oscillator. The PWM on-cycle terminates when the ramp voltage exceeds the error voltage from the current-error amplifier (CEA1).

The outer voltage control loop consists of the voltage-error amplifier (VEA1). The noninverting input (EAN1) is externally connected to the midpoint of a resistive voltage-divider from OUT1 to EAN1 to AGND. The voltage loop gain is set by using an external resistor from the output of this amplifier (EAOUT1) to its inverting input (EAN1). The noninverting input of (VEA1) is connected to the 0.61V internal reference.

Peak-Current Comparator

The peak-current comparator (see Figure 3) monitors the voltage across the current-sense resistor (R_{SENSE}) and provides a fast cycle-by-cycle current limit with a threshold of 52.5mV. Note that the average current-limit threshold of 22.5mV still limits the output current during short-circuit conditions. To prevent inductor saturation, select an output inductor with a saturation current specification greater than the average current limit of 22.5mV/R_{SENSE}. Proper inductor selection ensures that only extreme conditions trip the peak-current comparator, such as a damaged output inductor. The typical propagation delay of the peak current-limit comparator is 260ns.

Current-Error Amplifier

The MAX5066 has two dedicated transconductance current-error amplifiers CEA1 and CEA2 with a typical g_M of 550µS and 320µA output sink and source capability. The current-error amplifier outputs (CLP1 and CLP2) serve as the inverting input to the PWM comparators. CLP1 and CLP2 are externally accessible to provide frequency compensation for the inner current loops (see C_{CFF}, C_{CF}, and R_{CF} in Figure 2). Compensate the current-error amplifier such that the inductor current down slope, which becomes the up slope at the inverting input of the PWM comparator, is less than the slope of the internally generated voltage ramp (see the *Compensation* section).

PWM Comparator and R-S Flip-Flop

The PWM comparator (CPWM1 or CPWM2) sets the duty cycle for each cycle by comparing the current-error amplifier output to a $2V_{P-P}$ ramp. At the start of each clock cycle an R-S flip-flop resets and the high-side drivers (DH1 and DH2) turn on. The comparator sets the flip-flop as soon as the ramp voltage exceeds the current-error amplifier output voltage, thus terminating the on cycle.

Voltage Error Amplifier

The voltage-error amplifier (VEA_) sets the gain of the voltage control loop. Its output clamps to 1.14V and -0.234V relative to V_{CM} = 0.61V. Set the MAX5066 output voltage by connecting a voltage-divider from the output to EAN_ to GND (see Figure 4). At no load the output of the voltage error amplifier is zero.

Use the equation below to calculate the no load voltage:

$$V_{OUT(NL)} = 0.6135 \times \left(1+\frac{R_1}{R_2}\right)$$

The voltage at full load is given by:

$$V_{OUT(FL)} = 0.6135 \times \left(1+\frac{R_1}{R_2}\right) - \Delta V_{OUT}$$

where ΔV_{OUT} is the voltage-positioning window described in the *Adaptive Voltage Positioning* section.

Adaptive Voltage Positioning

Powering new-generation ICs requires new techniques to reduce cost, size, and power dissipation. Voltage positioning (Figure 5) reduces the total number of output capacitors to meet a given transient response requirement. Setting the no-load output voltage slightly higher than the output voltage during nominally loaded conditions allows a larger downward voltage excursion when the output current suddenly increases. Regulating at a lower output voltage under a heavy load allows a larger upward-voltage excursion when the output current suddenly decreases. A larger allowed voltage-step excursion reduces the required number of output capacitors and/or allows the use of higher ESR capacitors.

The internal 0.61V reference in the MAX5066 has a tolerance of ±0.9%. If we use 0.1% resistors for R_1 and R_2, we still have another 4% available for the variation in the output voltage from nominal. This available voltage range allows us to reduce the total number of output capacitors to meet a given transient response requirement. This results in a voltage-positioning window as shown in Figure 5.

From the allowable voltage-positioning window we can calculate the value of R_F from the equation below.

$$R_F = \frac{I_{OUT} \times R_{SENSE} \times 36 \times R_1}{\Delta V_{OUT}}$$

where ΔV_{OUT} is the allowable voltage-positioning window, R_{SENSE} is the sense resistor, 36 is the current-sense amplifier gain, and R_1 is as shown in Figure 4.

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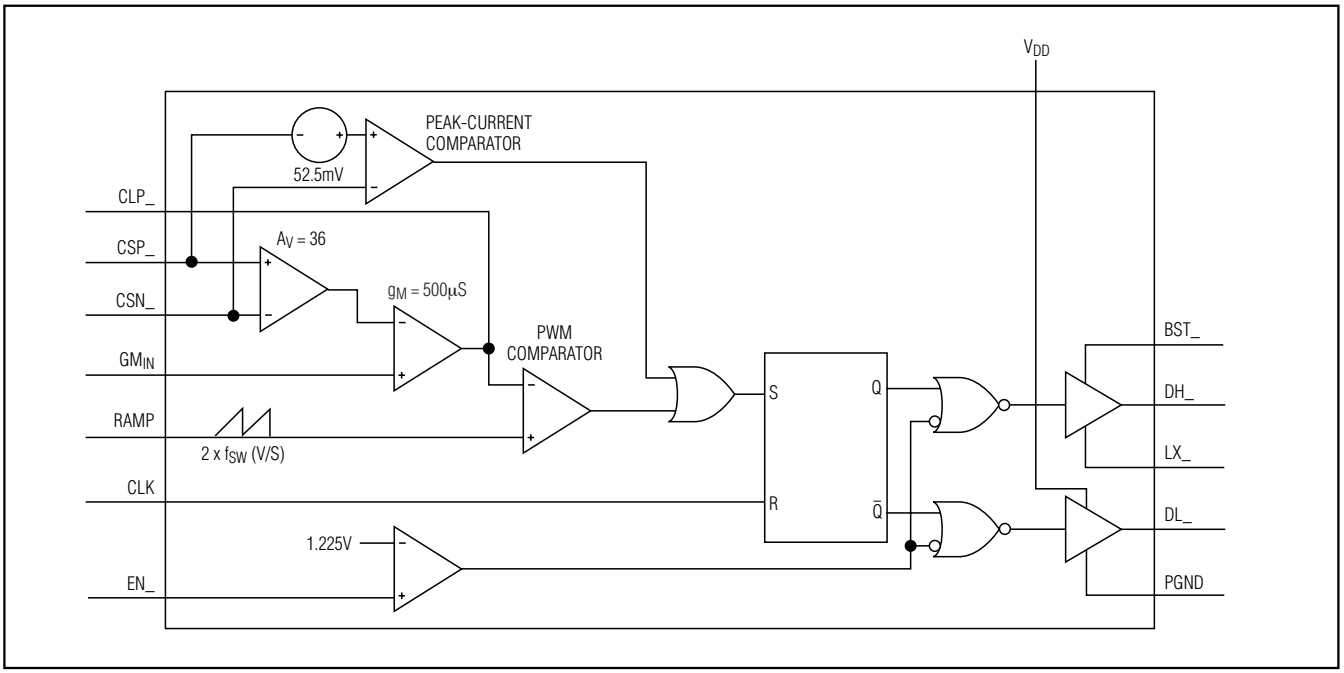

Figure 3. Current Comparator and MOSFET Driver Logic

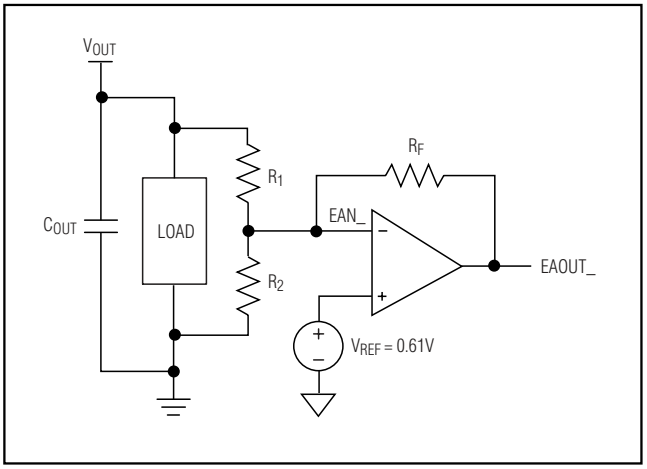

Figure 4. Voltage Error Amplifier

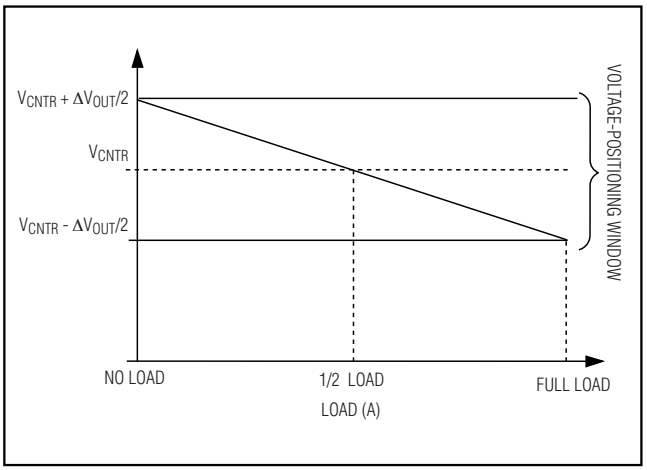

Figure 5. Defining the Voltage-Positioning Window

MOSFET Gate Drivers (DH_, DL_)

The high-side drivers (DH1 and DH2) and low-side drivers (DL1 and DL2) drive the gates of external n-channel MOSFETs. The high-peak sink and source current capability of these drivers provides ample drive for the fast rise and fall times of the switching MOSFETs. Faster rise and fall times result in reduced switching losses. For low-output, voltage-regulating applications where the duty cycle is less than 50%, choose high-side MOSFETs (Q2 and Q4, Figure 6) with a moderate $R_{DS(ON)}$ and a very low gate charge. Choose low-side MOSFETs (Q1 and Q3, Figure 6) with very low $R_{DS(ON)}$ and moderate gate charge. The driver block also includes a logic circuit that provides an adaptive nonoverlap time (30ns typical) to

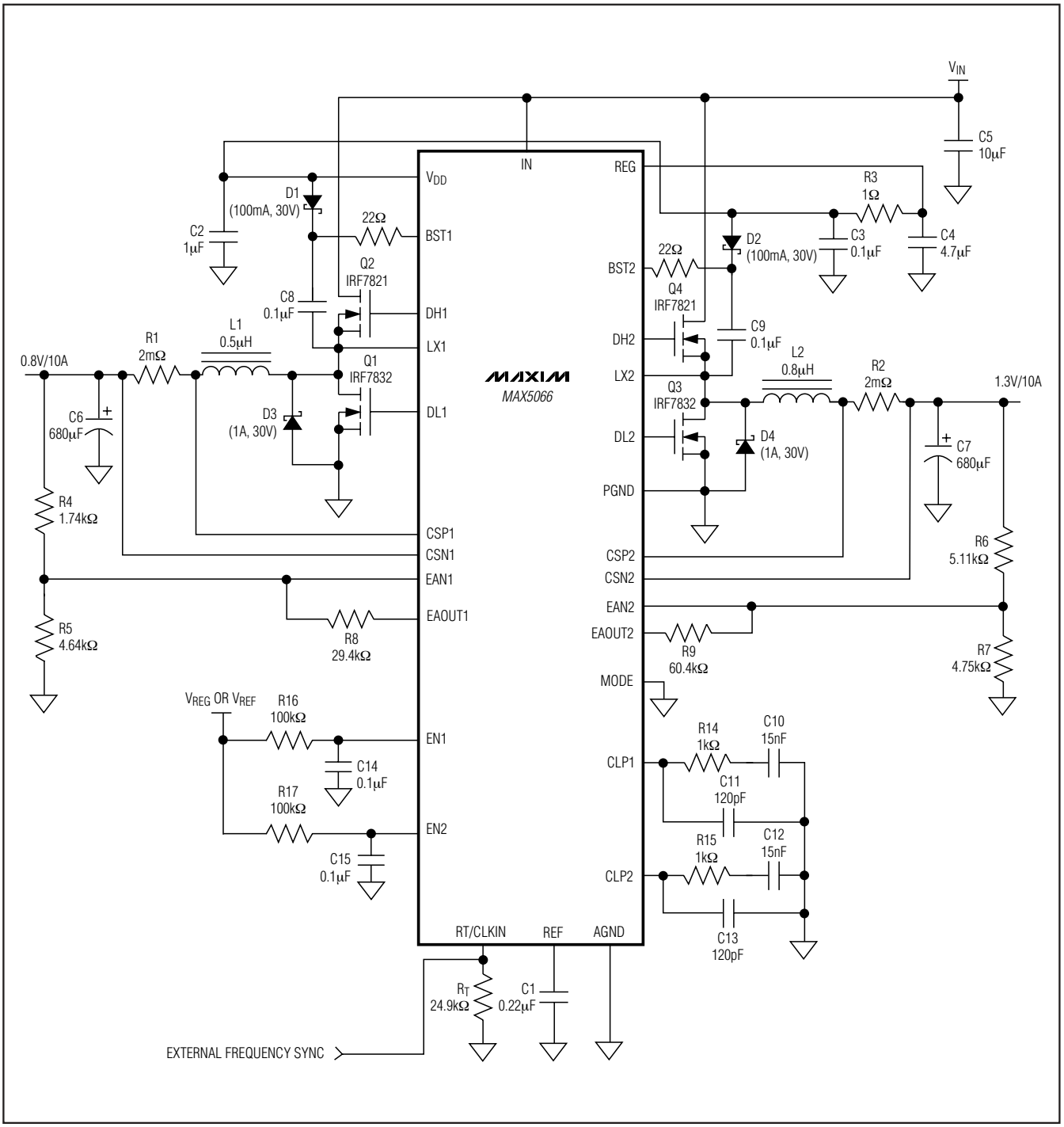

Figure 6. Dual-Output Buck Regulator

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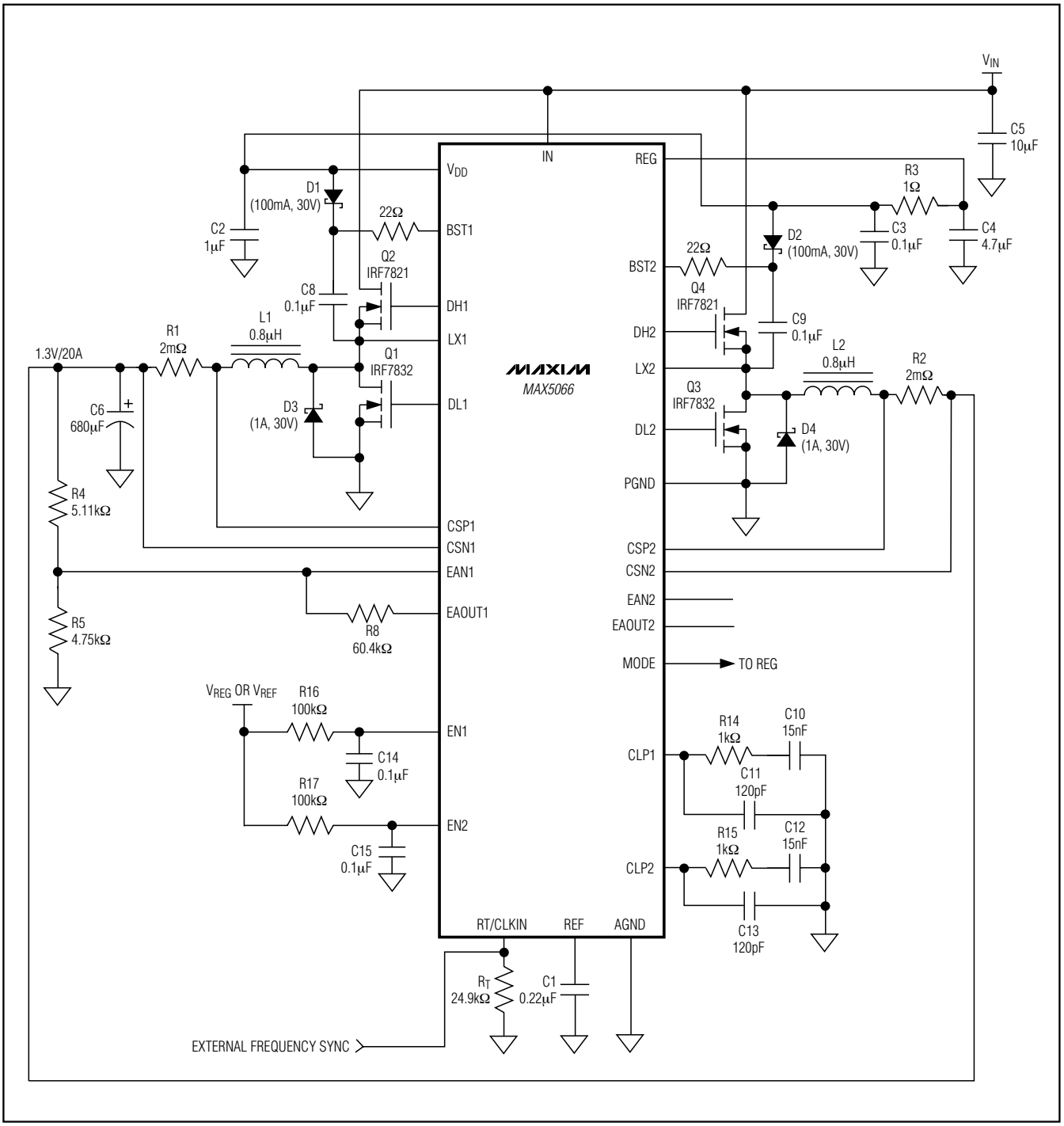

Figure 7. Dual-Phase, Single-Output Buck Regulator

prevent shoot-through currents during transition. Figure 7 shows the dual-phase, single-output buck regulator.

Design Procedures

Inductor Selection

The switching frequency per phase, peak-to-peak ripple current in each phase, and allowable voltage ripple at the output, determine the inductance value. Selecting higher switching frequencies reduces the inductance requirement, but at the cost of lower efficiency due to the charge/discharge cycle of the gate and drain capacitances in the switching MOSFETs. The situation worsens at higher input voltages, since capacitive switching losses are proportional to the square of the input voltage. Lower switching frequencies on the other hand will increase the peak-to-peak inductor ripple current (ΔI_L) and therefore increase the MOSFET conduction losses (see the *Power MOSFET Selection* section for a detailed description of MOSFET power loss).

When using higher inductor ripple current, the ripple cancellation in the multiphase topology, reduces the input and output capacitor RMS ripple current. Use the following equation to determine the minimum inductance value:

$$L = \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Choose ΔI_L to be equal to about 30% of the output current per channel. Since ΔI_L affects the output-ripple voltage, the inductance value may need minor adjustment after choosing the output capacitors for full-rated efficiency. Choose inductors from the standard high-current, surface-mount inductor series available from various manufacturers. Particular applications may require custom-made inductors. Use high-frequency core material for custom inductors. High ΔI_L causes large peak-to-peak flux excursion increasing the core losses at higher frequencies. The high-frequency operation coupled with high ΔI_L, reduces the required minimum inductance and even makes the use of planar inductors possible. The advantages of using planar magnetics include low-profile design, excellent current sharing between phases due to the tight control of parasitics, and low cost. For example, the minimum inductance at V_{IN} = 12V, V_{OUT} = 0.8V, ΔI_L = 3A, and f_{SW} = 500kHz is 0.5µH.

The average current-mode control feature of the MAX5066 limits the maximum inductor current, which prevents the inductor from saturating. Choose an inductor with a saturating current greater than the worst-case peak inductor current:

$$I_{L\_PEAK} = \frac{24.75 \times 10^{-3}}{R_{SENSE}} + \frac{\Delta I_L}{2}$$

where 24.75mV is the maximum average current-limit threshold for the current-sense amplifier and R_{SENSE} is the sense resistor.

Power MOSFET Selection

When choosing the MOSFETs, consider the total gate charge, $R_{DS(ON)}$, power dissipation, the maximum drain-to-source voltage, and package thermal impedance. The product of the MOSFET gate charge and on-resistance is a figure of merit, with a lower number signifying better performance. Choose MOSFETs optimized for high-frequency switching applications. The average gate-drive current from the MAX5066's output is proportional to the total capacitance it drives at DH1, DH2, DL1, and DL2. The power dissipated in the MAX5066 is proportional to the input voltage and the average drive current. See the *Supply Voltage Connection (V_{IN}/V_{REG})* and the *Low-Side MOSFET Drives Supply (V_{DD})* sections to determine the maximum total gate charge allowed from all driver outputs together.

The losses may be broken into four categories: conduction loss, gate drive loss, switching loss and output loss. The following simplified power loss equation is true for both MOSFETs in the synchronous buck-converter:

$$P_{LOSS} = P_{CONDUCTION} + P_{GATEDRIVE} + P_{SWITCH} + P_{OUTPUT}$$

For the low-side MOSFET, the P_{SWITCH} term becomes virtually zero because the body diode of the MOSFET is conducting before the MOSFET is turned on.

Tables 1 and 2 describe the different losses and shows an approximation of the losses during that period.

Input Capacitance

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source, dictate the capacitance requirement. Increasing the number of phases increases the effective switching frequency and lowers the peak-to-average current ratio, yielding lower input capacitance requirement. It can be shown that the

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Table 1. High-Side MOSFET Losses

LOSS	DESCRIPTION	SEGMENT LOSS
Conduction Loss	Losses associated with MOSFET on-time and on-resistance. I_{RMS} is a function of load current and duty cycle.	$P_{CONDUCTION} = I_{RMS}2 \times R_{DS(ON)}$ where $I_{RMS} \approx \sqrt{\frac{V_{OUT}}{V_{IN}}} \times I_{LOAD}$
Gate Drive Loss	Losses associated with charging and discharging the gate capacitance of the MOSFET every cycle. Use the MOSFET's (Q_G) specification.	$P_{GATEDRIVE} = V_{DD} \times Q_G \times f_{SW}$
Switching Loss	Losses during the drain voltage and drain current transitions for every switching cycle. Losses occur only during the Q_{GS2} and Q_{GD} time period and not during the initial Q_{GS1} period. The initial Q_{GS1} period is the rise in the gate voltage from zero to V_{TH}. R_{DH} is the high-side MOSFET driver's on-resistance and R_{GATE} is the internal gate resistance of the high-side MOSFET (Q_{GD} and Q_{GS2} are found in the MOSFET data sheet).	$P_{SWITCH} = V_{IN} \times I_{LOAD} \times f_{SW} \times \frac{(Q_{GS2} + Q_{GD})}{I_{GATE}}$ where $I_{GATE} = \frac{V_{DD}}{2 \times (R_{DH} + R_{GATE})}$
Output Loss	Losses associated with Q_{OSS} of the MOSFET occur every cycle when the high-side MOSFET turns on. The losses are caused by both MOSFETs but are dissipated in the high-side MOSFET.	$P_{OUTPUT} = \frac{Q_{OSS(HS)} + Q_{OSS(LS)}}{2} \times V_{IN} \times f_{SW}$

worst-case RMS current occurs when only one controller section is operating. The controller section with the highest output power needs to be used in determining the maximum input RMS ripple current requirement. Increasing the output current drawn from the other out-of-phase controller section results in reducing the input ripple current. A low-ESR input capacitor that can handle the maximum input RMS ripple current of one channel must be used. The maximum RMS capacitor ripple current is given by:

$$I_{CIN(RMS)} \approx I_{MAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where I_{MAX} is the full load current of the regulator. V_{OUT} is the output voltage of the same regulator and C_{IN} is C5 in Figure 6. The ESR of the input capacitors wastes power from the input and heats up the capacitor. Reducing the ESR is important to maintain a high overall efficiency and in reducing the heating of the capacitors.

Output Capacitors

The worst-case peak-to-peak inductor ripple current, the allowable peak-to-peak output ripple voltage, and the maximum deviation of the output voltage during step loads determine the capacitance and the ESR requirements for the output capacitors. The output ripple can be approximated as the inductor current ripple multiplied by the output capacitor's ESR (R_{ESR_OUT}). The peak-to-peak inductor current ripple is given by:

$$\Delta I_L = \frac{V_{OUT}(1 - D)}{L \times f_{SW}}$$

During a load step, the allowable deviation of the output voltage during the fast transient load dictates the output capacitance and ESR. The output capacitors supply the load step until the controller responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the regulator. The resistive drop across the capacitor's ESR and capacitor discharge causes a voltage drop during a

Table 2. Low-Side MOSFET Losses

LOSS	DESCRIPTION	SEGMENT LOSSES
Conduction Loss	Losses associated with MOSFET on-time, I_{RMS} is a function of load current and duty cycle.	$P_{CONDUCTION} = I_{RMS}2 \times R_{DS(ON)}$ where $I_{RMS} \approx \sqrt{\frac{V_{IN} - V_{OUT}}{V_{IN}}} \times I_{LOAD}$
Gate Drive Loss	Losses associated with charging and discharging the gate of the MOSFET every cycle. There is no Q_{GD} charging involved in this MOSFET due to the zero-voltage turn-on. The charge involved is (Q_G - Q_{GD}).	$P_{GATEDRIVE} = V_{DD} \times (Q_G - Q_{GD}) \times f_{SW}$

Note: *The gate drive losses are distributed between the drivers and the MOSFETs in the ratio of the gate driver's resistance and the MOSFET's internal gate resistance.*

load step. Use a combination of SP polymer and ceramic capacitors for better transient load and ripple/noise performance.

Keep the maximum output-voltage deviation less than or equal to the adaptive voltage-positioning window (ΔV_{OUT}). During a load step, assume a 50% contribution each from the output capacitance discharge and the voltage drop across the ESR ($\Delta V_{OUT} = \Delta V_{ESR\_OUT} + \Delta V_{Q\_OUT}$). Use the following equations to calculate the required ESR and capacitance value:

$$R_{ESR\_OUT} = \frac{\Delta V_{ESR\_OUT}}{I_{LOAD\_STEP}}$$

$$C_{OUT} = \frac{I_{LOAD\_STEP} \times t_{RESPONSE}}{\Delta V_{Q\_OUT}}$$

where I_{LOAD_STEP} is the step in load current and $t_{RESPONSE}$ is the response time of the controller. Controller response time depends on the control-loop bandwidth. C_{OUT} is C6 and C7 in Figure 6.

Current Limit

The average current-mode control technique of the MAX5066 accurately limits the maximum average output current per phase. The MAX5066 senses the voltage across the sense resistor and limits the maximum inductor current accordingly. Use the equations below to calculate the current-sense resistor values:

$$I_{LOAD(MAX)} = \frac{24.75 \times 10^{-3}}{R_{SENSE}}$$

Due to tolerances involved, the minimum average voltage at which the voltage across the current-sense resistor is clamped is 20.4mV. Therefore, the minimum average current limit is set at:

$$I_{LIMIT(MIN)} = \frac{20.4 \times 10^{-3}}{R_{SENSE}}$$

For example, the current-sense resistor:

$$R_{SENSE} = \frac{20.4mV}{10A} = 2.04m\Omega$$

for a maximum output current of 10A. The standard value is 2mΩ. Also, adjust the value of the current-sense resistor to compensate for parasitics associated with the PC board. Select a noninductive resistor with appropriate wattage rating.

The second type of current limit is the peak current limit as explained in the *Peak-Current Comparator* section.

The third current-protection circuit is the hiccup fault protection as explained in the *Hiccup Fault Protection* section. The average current during a short at the output is given by:

$$I_{AVG(SHORT)} = \frac{1.41 \times 10^{-3}}{R_{SENSE}}$$

Reverse Current Limit

The MAX5066 limits the reverse current when the output capacitor voltage is higher than the preset output voltage. Calculate the maximum reverse current limit based on V_{CLAMP_LO} and the current-sense resistor R_{SENSE}.

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$$I_{REVERSE} = \frac{1.63 \times 10^{-3}}{R_{SENSE}}$$

Output-Voltage Setting

The output voltage is set by the combination of resistors R1, R2, and R_F as described in the *Voltage Error Amplifier* section. First select a value for resistor R2. Then calculate the value of R1 from the following equation:

$$R1 = \frac{(V_{OUT(NL)} - 0.6135)}{0.6135} \times R2$$

where $V_{OUT(NL)}$ is the voltage at no load. Then find the value of R_F from the following equation:

$$R_F = \frac{I_{OUT} \times R_{SENSE} \times 36 \times R_1}{\Delta V_{OUT}}$$

where ΔV_{OUT} is the allowable drop in voltage from no load to full load. R_F is R8 and R9, R1 is R4 and R6, R2 is R5 and R7 in Figure 6.

Compensation

The MAX5066 uses an average current-mode control scheme to regulate the output voltage (see Figure 2). The main control loop consists of an inner current loop and an outer voltage loop. The voltage error amplifier (VEA1 and VEA2) provides the controlling voltage for the current loop in each phase. The output inductor is "hidden" inside the inner current loop. This simplifies the design of the outer voltage control loop and also improves the power-supply dynamics. The objective of the inner current loop is to control the average inductor current. The gain-bandwidth characteristic of the current loop can be tailored for optimum performance by the compensation network at the output of the current-error amplifier (CEA1 or CEA2). Compared with peak current-mode control, the current-loop gain crossover frequency, f_C, can be made approximately the same, but the gain at low frequencies is much higher. This results in the following advantages over peak current-mode control.

1) The average current tracks the programmed current with a high degree of accuracy.
2) Slope compensation is not required, but there is a limit to the loop gain at the switching frequency in order to achieve stability.
3) Noise immunity is excellent.
4) The average current-mode method can be used to sense and control the current in any circuit branch.

For stability of the current loop, the amplified inductor-current downslope at the negative input of the PWM comparator (CPWM1 and CPWM2) must not exceed the ramp slope at the comparator's positive input. This puts an upper limit on the current-error amplifier gain at the switching frequency. The inductor current downslope is given by V_{OUT}/L where L is the value of the inductor (L1 and L2 in Figure 6) and V_{OUT} is the output voltage. The amplified inductor current downslope at the negative input of the PWM comparator is given by:

$$\frac{\Delta V_L}{\Delta t} = \frac{V_{OUT}}{L} \times R_{SENSE} \times 36 \times g_M \times R_{CF}$$

where R_{SENSE} is the current-sense resistor (R1 and R2 in Figure 6) and $g_M \times R_{CF}$ is the gain of the current-error amplifier (CEA_) at the switching frequency. The slope of the ramp at the positive input of the PWM comparator is $2V \times f_{SW}$. Use the following equation to calculate the maximum value of R_{CF} (R14 or R15 in Figure 6).

$$R_{CF} \le \frac{2 \times f_{SW} \times L}{V_{OUT} \times R_{SENSE} \times 36 \times g_M} \quad (1)$$

The highest crossover frequency f_{CMAX} is given by:

$$f_{CMAX} = \frac{f_{SW} \times V_{IN}}{2\pi \times V_{OUT}}$$

or alternatively:

$$f_{SW} = \frac{f_{CMAX} \times 2\pi \times V_{OUT}}{V_{IN}}$$

Equation (1) can now be rewritten as:

$$R_{CF} = \frac{\pi \times f_C \times L}{V_{IN} \times R_S \times 9 \times g_M} \quad (2)$$

In practical applications, pick the crossover frequency (f_C) in the range of:

$$\frac{f_{SW}}{10} < f_C < \frac{f_{SW}}{2}.$$

First calculate R_{CF} in equation 2 above. Calculate C_{CF} such that:

$$C_{CF} = \frac{10}{2 \times \pi \times f_C \times R_{CF}}$$

where C_{CF} is C10 and C12 in Figure 6.

Calculate C_{CFF} such that:

$$C_{CFF} = \frac{1}{2 \times \pi \times f_C \times 10 \times R_{CF}}$$

where C_{CFF} is C11 and C13 in Figure 6.

Applications Information

Independant Turn-On and Off

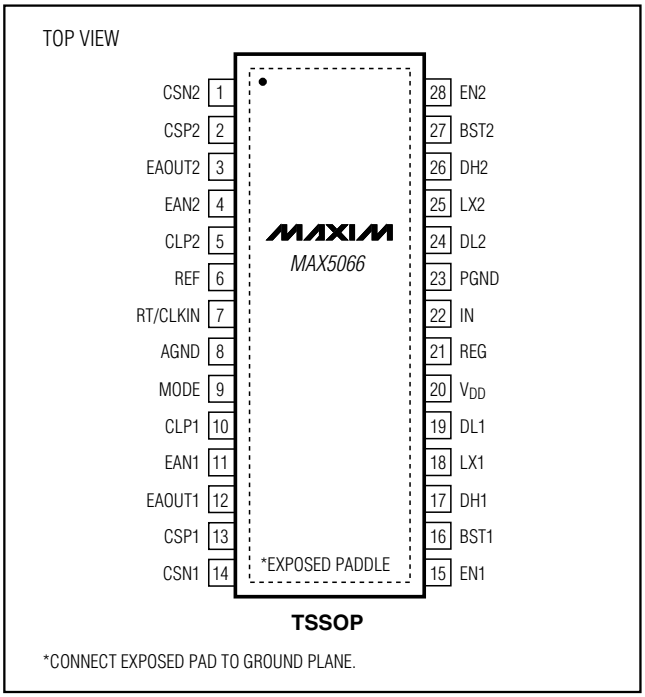
The MAX5066 can be used to regulate two outputs from one controller. Each of the two outputs can be turned on and off independently of one another by controlling the enable input of each phase (EN1 and EN2). A logic-low on each enable pin shuts down the MOSFET drivers for that phase. When the voltage on the enable pin exceeds 1.2V, the drivers are turned on and the output can come up to regulation. This method of turning on the outputs allows the MAX5066 to be used for power sequencing.

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low losses, low output noise, and clean and stable operation. This is especially true for dual-phase converters where one channel can affect the other. Use the following guidelines for PC board layout:

1) Place the V_{DD}, REG, and the BST1 and BST2 bypass capacitors close to the MAX5066.
2) Minimize all high-current switching loops.
3) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PC boards (2oz or higher) to enhance efficiency and minimize trace inductance and resistance.
4) Run the current-sense lines CSP_ and CSN_ very close to each other to minimize loop areas. Do not cross these critical signal lines through power circuitry. Sense the current right at the pads of the current-sense resistors.
5) Place the bank of output capacitors close to the load.
6) Isolate the power components on the top side from the analog components on the bottom side with a ground plane in between.
7) Provide enough copper area around the switching MOSFETs, inductors, and sense resistors to aid in thermal dissipation and reducing resistance.
8) Distribute the power components evenly across the top side for proper heat dissipation.
9) Keep AGND and PGND isolated and connect them at one single point close to the IC. Do not connect them together anywhere else.
10) Place all input bypass capacitors for each input as close to each other as is practical.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 6252

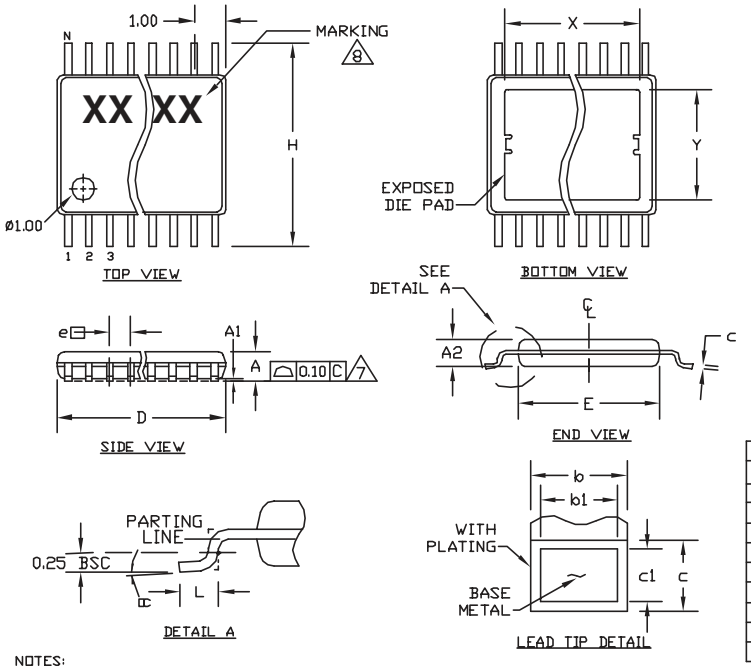
PROCESS: BiCMOS

Configurable, Single-/Dual-Output, Synchronous Buck Controller for High-Current Applications

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP 4.4mm BODY.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.00	0.15	0.000	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	0.112	0.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT-1	14	D	4.90	5.10	0.193	0.201
		X	2.95	3.25	0.116	0.128
ABT	16	D	4.90	5.10	0.193	0.201
		X	2.85	3.15	0.112	0.124
ACT	20	D	6.40	6.60	0.252	0.260
		X	4.00	4.34	0.157	0.171
AET	28	D	9.60	9.80	0.378	0.386
		X	5.35	5.65	0.211	0.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0108	E	1/1