CAT6241

LDO Voltage Regulator - Adjustable CMOS

1 A

Description

The CAT6241 is a low dropout CMOS voltage regulator providing up to 1000 mA of output current with fast response to load current and line voltage changes. CAT6241 offers a user adjustable output voltage from 0.5 V to 5.0 V and its low quiescent current make CAT6241 ideal for energy conscious designs. CAT6241 is available in space saving 2 mm x 2 mm UDFN−8 and 3 mm x 3 mm WDFN−6 packages, each with a power pad for heat sinking to the PCB.

Features

- Guaranteed 1000 mA Continuous Output Current
- V_{OUT}: 0.5 V to 5.0 V, Minimum V_{IN}: 1.6 V
- Dropout Voltage of 350 mV Typical at 1000 mA
- ±2.0% Output Voltage Accuracy at Room Temperature
- No−load Ground Current of 70 μA Typical
- Full−load Ground Current of 140 μA Typical
- “Zero” Current Shutdown Mode
- Under Voltage Lockout
- Stable with Ceramic Output Capacitors
- Current Limit and Thermal Protection
- 2 mm x 2 mm UDFN−8 and 3 mm x 3 mm WDFN−6 Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- DSP Core and I/O Voltages
- FPGAs, ASICs
- PDAs, Mobile Phones, GPS
- Camcorders and Cameras
- Hard Disk Drives

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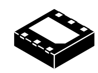
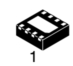
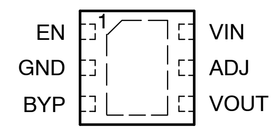


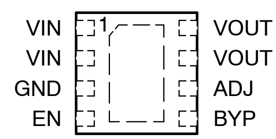
WDFN−6
3 x 3 mm
CASE 511AP



UDFN−8
2 x 2 mm
CASE 517AW

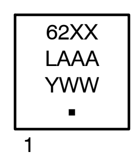
PIN CONNECTIONS



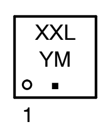


(Top Views)

MARKING DIAGRAMS



(WDFN−6)



(UDFN−8)

XX	= Specific Device Code
62XX	= Specific Device Code
L	= Assembly Location Code
AAA	= Assembly Lot Number (Last Three Digits)
Y	= Production Year (Last Digit)
M	= Production Month (1−9, O, N, D)
WW	= Production Week (Two Digits)
▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

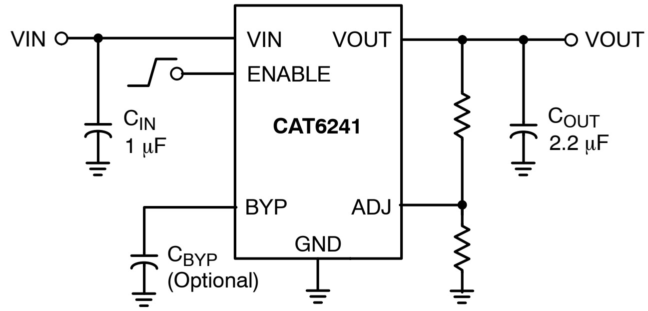


Figure 1. Application Schematic

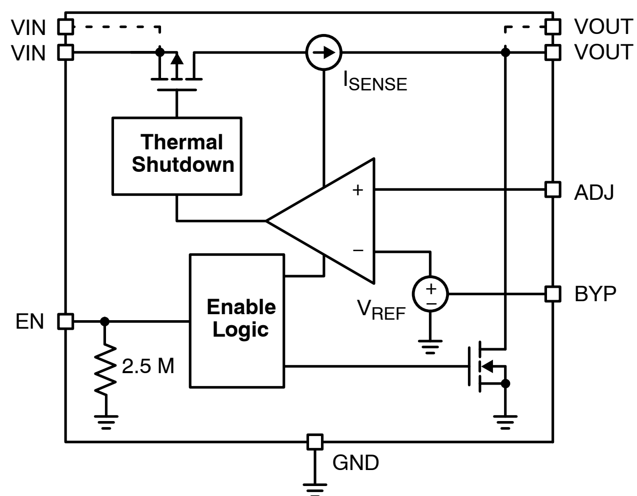


Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin # WDFN−6	Pin # UDFN−8	Pin Name	Description
1	4	EN	The Enable Input. An active HIGH input, turning ON the LDO. This input should be tied to V_{IN} if the LDO is not intended to be shut off during normal operation. A pull−down 2.5 MΩ resistor maintains the circuit in the OFF state if the pin is left open.
2, PAD	3, PAD	GND	Power Supply Ground; Device Substrate. The center pad is internally connected to Ground and as such can cause short circuits to signal traces running beneath the IC. This pad is intended for heat sinking the IC to the PCB and is typically connected to the PCB ground plane.
3	5	BYP	Bypass input. Placing a capacitor of 100 pF to 470 pF between BYP and ground reduces noise on $V_{OUT.}$ This capacitor is optional.
4	7, 8	V_{OUT}	Regulated Output Voltage. A protection block eliminates any current flow from output to input if $V_{OUT} > V_{IN}$. Connect both pins for specified dropout performance.
5	6	ADJ	Output Voltage Adjust Input. This input ties to the common point of a resistor divider which determines the regulator's output voltage. See Applications section for details on selecting resistor values.
6	1, 2	V_{IN}	Positive Power Supply Input. Supplies power for V_{OUT} as well as the regulator's internal circuitry. Connect both pins for specified dropout performance.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{IN}	−0.3 to 6.0	V
Output Voltage Range	V_{OUT}	−0.3 to 6.0	V
Enable Input Range	EN	−0.3 to 5.5 V or (V_{IN} + 0.3), whichever is lower	V
Adjust Input Range	ADJ	−0.3 to 5.5 V	V
Bypass Input Range	BYP	−0.3 to 5.5 V or (V_{IN} + 0.3), whichever is lower	V
Power Dissipation	PD	Internally Limited	mW
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating range.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WDFN−6, 3 x 3 mm			°C/W
Thermal Resistance, Junction−to−Air: 1 in^2/1 oz. copper (Note 4)	$R_{\theta JA}$	55	
Thermal Reference, Junction−to−Case (Note 4)	$R_{\psi JL}$	10	

4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. OPERATING RANGES (Note 5)

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 6)	V_{IN}	1.6	5.5	V
Output Current	I_{OUT}	0.1	1000	mA
Output Voltage	V_{OUT}	0.5	5.0	V
Ambient Temperature	T_A	−40	85	°C

5. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating range.
6. Minimum V_{IN_MIN} = 1.6 V or (V_{OUT} + V_{DO}), whichever is higher.

Table 5. ELECTRICAL CHARACTERISTICS (V_{IN} = (V_{OUT} + 1 V) or V_{IN_MIN}, whichever is higher, C_{IN} = 1 μF, C_{OUT} = 2.2 μF, for typical values T_A = 25°C, for **Bold** values T_A = −40°C to 85°C; unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INPUT / OUTPUT						
V_{IN}	Input Voltage		**1.6**		**5.5**	V
V_{OUT}	Output Voltage Range		**0.5**		**5.0**	V
$V_{OUT-ACC}$	Output Voltage Accuracy	Initial accuracy, I_{OUT} = 1 mA	−2		2	%
			−3		**3**	
V_{ADJ}	Voltage at ADJ input		**0.485**	**0.5**	**0.515**	V
TC_{OUT}	Output Voltage Temp. Coefficient			**50**		ppm/°C
I_{OUT}	Output Current		0.0001	1		A

Table 5. ELECTRICAL CHARACTERISTICS (V_{IN} = (V_{OUT} + 1 V) or V_{IN_MIN}, whichever is higher, C_{IN} = 1 μF, C_{OUT} = 2.2 μF, for typical values T_A = 25°C, for **Bold** values T_A = −40°C to 85°C; unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INPUT / OUTPUT						
V_{R-LINE}	Line Regulation	V_{IN} = V_{OUT} + 1.0 V to 5.5 V, I_{OUT} = 10 mA	−0.3	±0.08	0.3	%/V
		V_{IN} = V_{OUT} + 1.0 V to 5.5 V, I_{OUT} = 10 mA	**−0.45**		**0.45**	
V_{R-LOAD}	Load Regulation $V_{OUT} \geq 0.8$ V	I_{OUT} = 100 μA to 1000 mA		1.5	2	%
		I_{OUT} = 100 μA to 1000 mA			**3**	
V_{DO}	V_{OUT} = 1.2 V	I_{OUT} = 300 mA T_A = 25°C			460	mV
	V_{OUT} = 2.5 V				110	
	V_{OUT} = 3.3 V				85	
	V_{OUT} = 1.2 V	I_{OUT} = 1 A T_A = 25°C			700	
	V_{OUT} = 2.5 V				350	
	V_{OUT} = 3.3 V				275	
I_{ADJ}	ADJ Input Current				100	nA
I_{GND}	Ground Current	I_{OUT} = 0 μA		70		μA
		I_{OUT} = 0 μA			**100**	
		I_{OUT} = 1000 mA		140	200	
		I_{OUT} = 1000 mA			**250**	
I_{GND-SD}	Shutdown Ground Current	V_{EN} < 0.4 V			**5**	μA
ISC	Output short circuit current limit	V_{OUT} = 0 V		900		mA
PSRR AND NOISE						
PSRR	Power Supply Rejection Ratio	f = 1 kHz, BYP = 470 pF, I_{OUT} = 10 mA		54		dB
		f = 20 kHz, BYP = 470 pF, I_{OUT} = 10 mA		42		
e_N	Output Noise Voltage for 1.2 V output	BW = 10 Hz to 100 kHz BYP = 470 pF, I_{OUT} = 10 mA		45		μVrms
UVLO, R_{OUT} AND ESR						
V_{UVLO}	Under voltage lockout threshold			1.4	**1.55**	V
R_{OUT-SH}	ON resistance of Discharge Transistor			150		Ω
ESR	C_{OUT} equivalent series resistance		5		500	mΩ
ENABLE INPUT						
V_{HI}	Logic High Level	V_{IN} = 1.6 to 5.5 V	**1.6**			V
V_{LO}	Logic Low Level	V_{IN} = 1.6 to 5.5 V			**0.4**	V
I_{EN}	Enable Input Current	V_{EN} = 0.4 V		0.15	**1**	μA
		V_{EN} = V_{IN} = 2.5 V		1	**3**	
R_{EN}	Enable pull−down resistor			2.5		MΩ
TIMING						
T_{ON}	Turn−On Time	C_{BYP} = 0 pF		230		μs
		C_{BYP} = 470 pF		1600		
THERMAL PROTECTION						
T_{SD}	Thermal Shutdown			145		°C
T_{HYS}	Thermal Hysteresis			10		°C

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. Output current capability depends upon the value of both V_{IN} and V_{OUT}. For $V_{OUT} \leq 0.8$ V, output current capability is 90% of ISC (see Figure 13). For $V_{OUT} > 0.8$ V, current capability is 1 A for $V_{IN} \geq 1.8$ V.

TYPICAL CHARACTERISTICS

(shown for $V_{ADJ} = V_{OUT} = 0.5$ V, $V_{IN} = 1.6$ V, $I_{OUT} = 1$ mA, $C_{IN} = 1$ μF, $C_{OUT} = 4.7$ μF, $C_{BYP} = 0$, and $T_A = 25°C$ unless otherwise specified.)

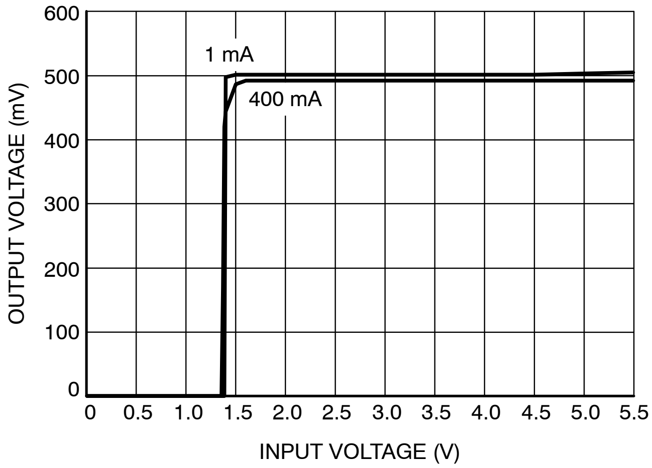


Figure 3. Dropout Characteristics

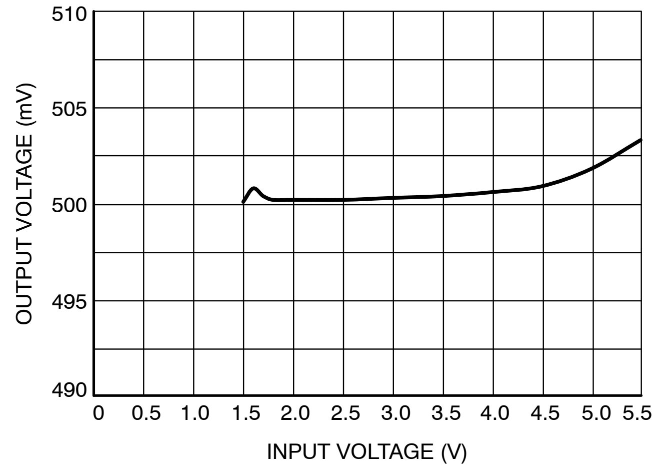


Figure 4. Line Regulation

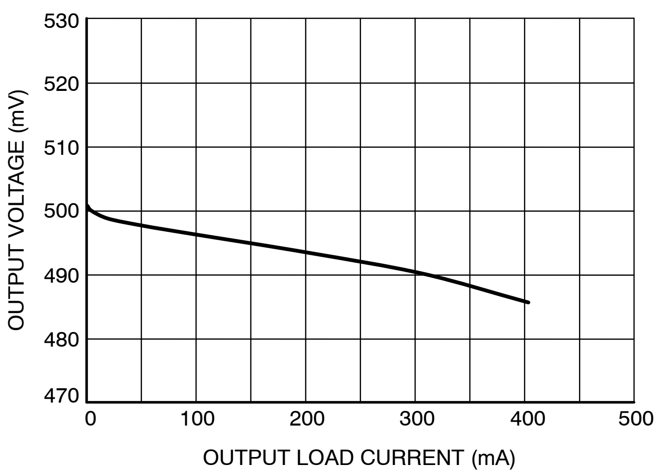


Figure 5. Load Regulation

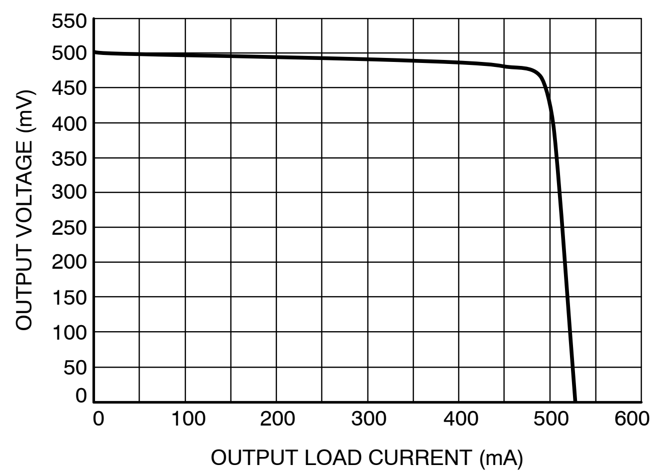


Figure 6. Output Current Capability

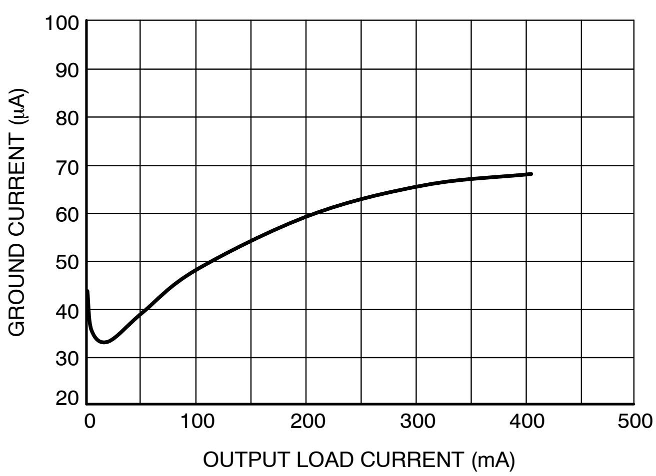


Figure 7. Ground Current vs. Load Current

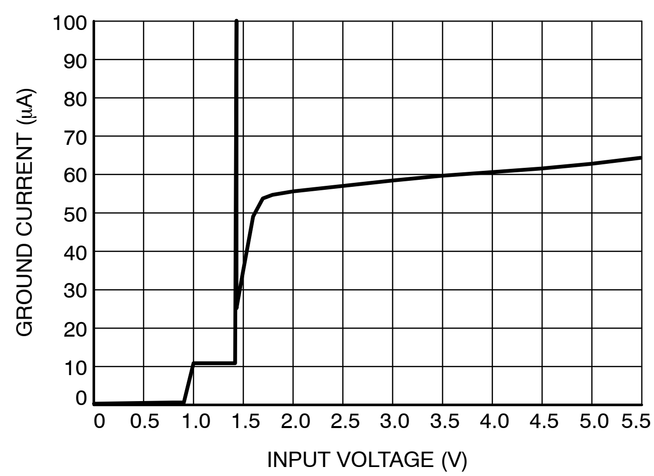


Figure 8. Ground Current vs. Input Voltage

TYPICAL CHARACTERISTICS

(shown for $V_{ADJ} = V_{OUT} = 0.5$ V, $V_{IN} = 1.6$ V, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 4.7$ µF, $C_{BYP} = 0$, and $T_A = 25°C$ unless otherwise specified.)

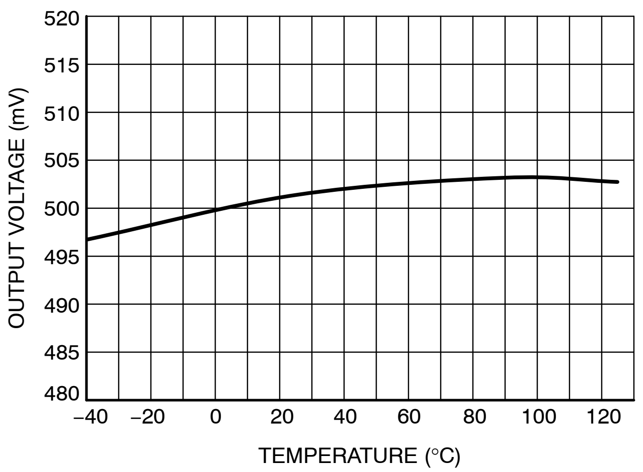


Figure 9. Output Voltage vs. Temperature

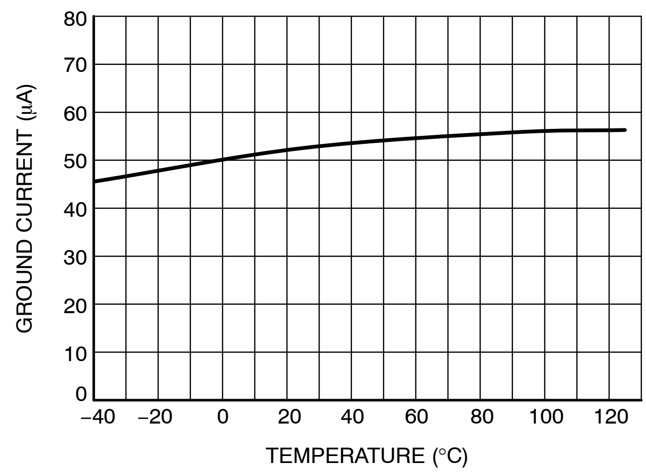


Figure 10. Ground Current vs. Temperature

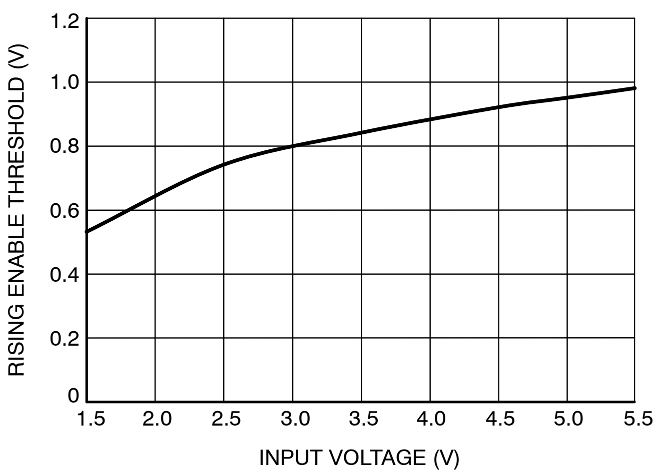


Figure 11. Rising Enable Threshold vs. Input Voltage

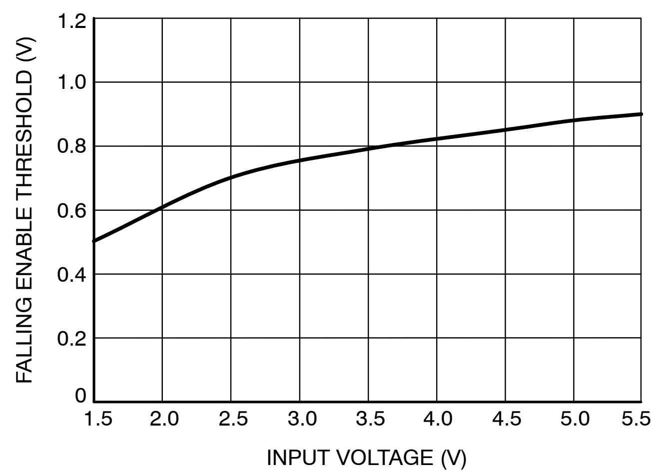


Figure 12. Falling Enable Threshold vs. Input Voltage

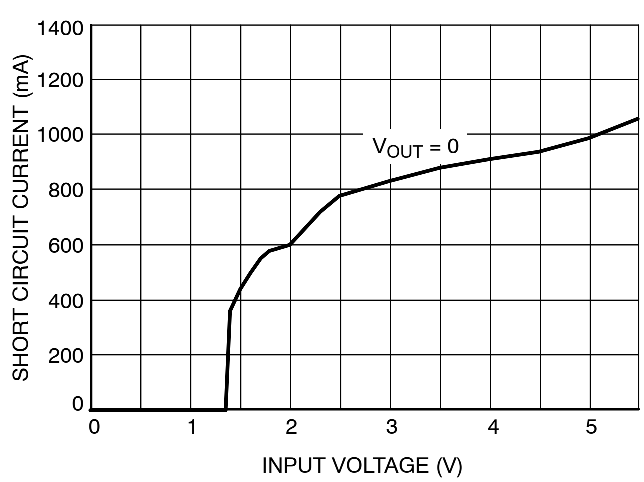


Figure 13. Output Short−circuit Current vs. Input Voltage

TRANSIENT CHARACTERISTICS

(shown for V_{OUT} = 0.5 V, V_{IN} = 1.6 V, I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, C_{BYP} = 0, and T_A = 25°C unless otherwise specified.)

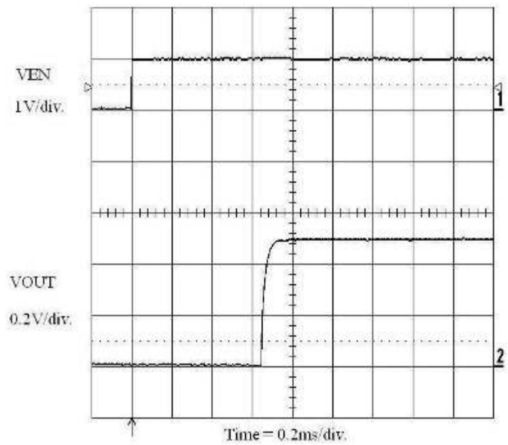


Figure 14. Enable Turn−on (1 mA Load)

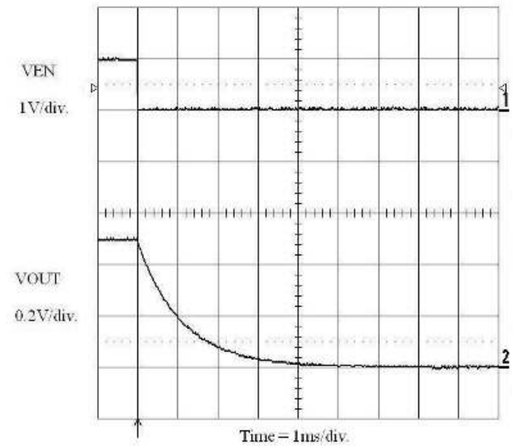


Figure 15. Enable Turn−off (1 mA Load)

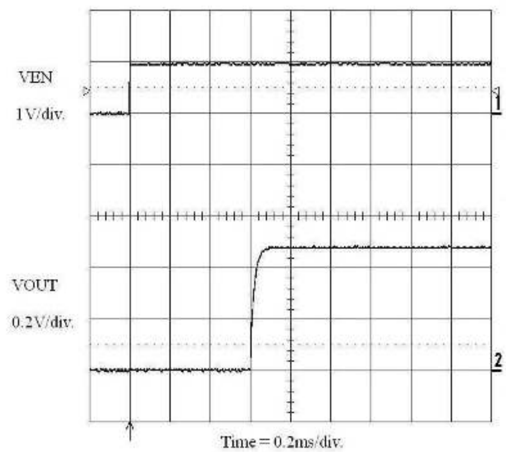


Figure 16. Enable Turn−on (350 mA Load)

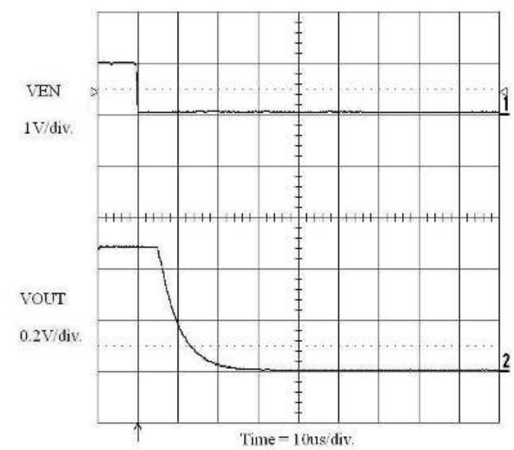


Figure 17. Enable Turn−off (350 mA Load)

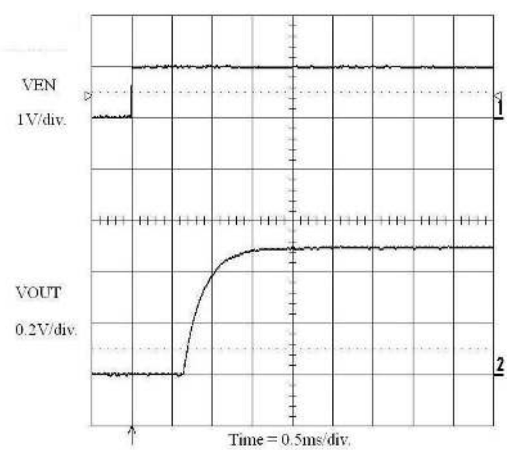


Figure 18. Enable Turn−on (1 mA Load) C_{BYP} = 470 pF

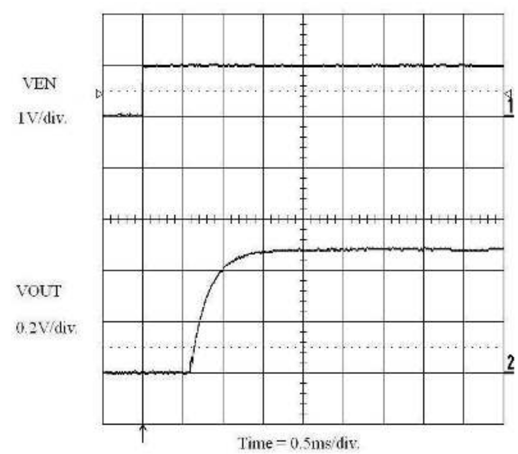


Figure 19. Enable Turn−on (350 mA Load) C_{BYP} = 470 pF

TRANSIENT CHARACTERISTICS

(shown for V_{OUT} = 0.5 V, V_{IN} = 1.6 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF, C_{BYP} = 0, and T_A = 25°C unless otherwise specified.)

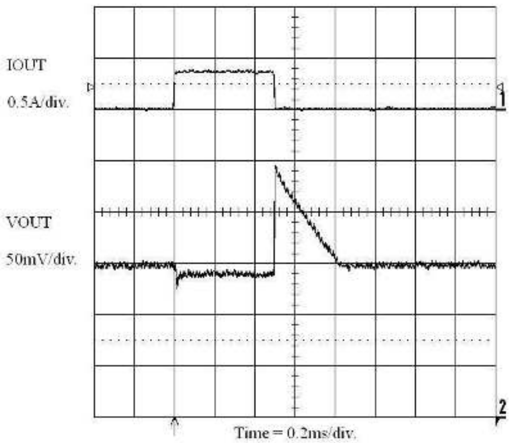


Figure 20. Load Transient Response (1 mA to 350 mA)

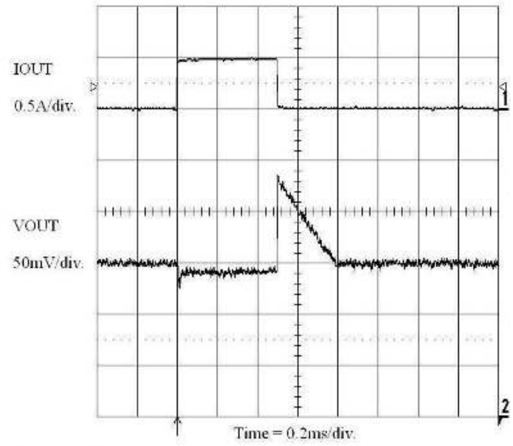


Figure 21. Load Transient Response (1 mA to 500 mA) V_{IN} = 1.8 V

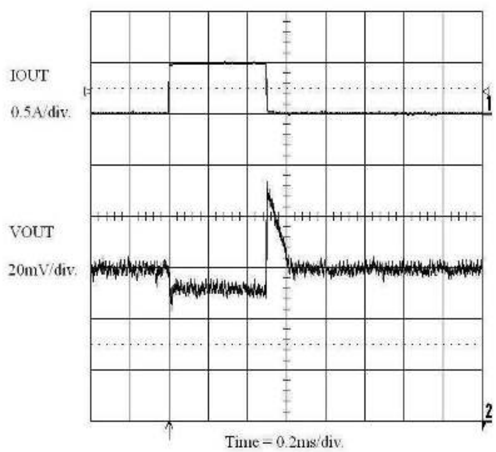


Figure 22. Load Transient Response (1 mA to 500 mA) V_{IN} = 1.9 V

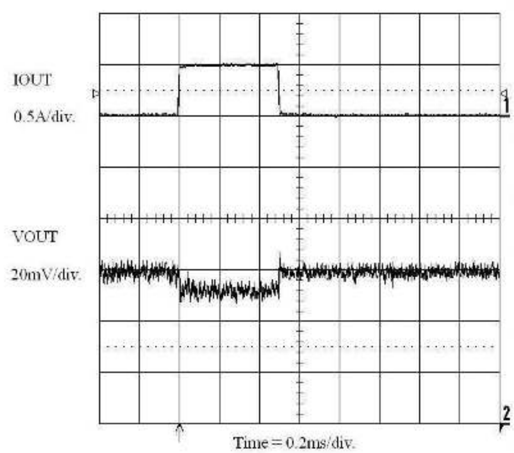


Figure 23. Load Transient Response (1 mA to 500 mA) V_{IN} = 2.0 V

TYPICAL CHARACTERISTICS

(shown for V_{OUT} = 1.0 V, V_{IN} = 2.0 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF, C_{BYP} = 0, and T_A = 25°C unless otherwise specified.)

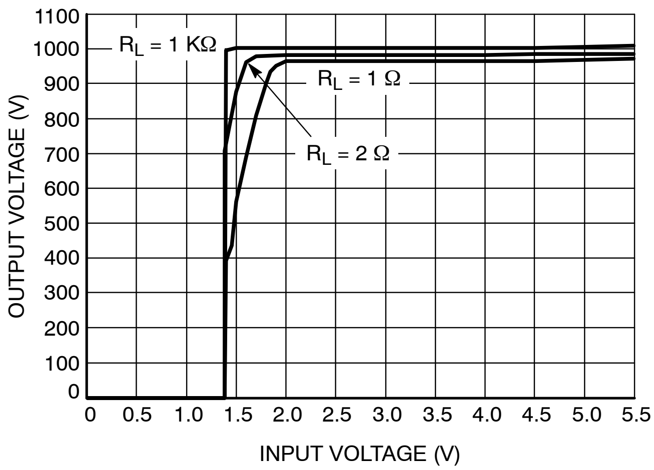


Figure 24. Dropout Characteristics

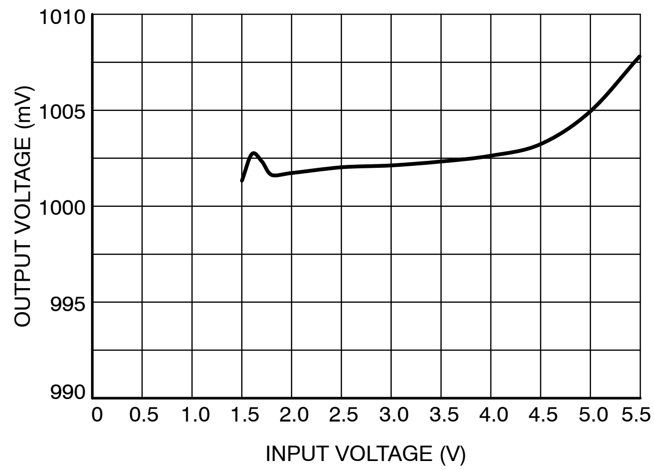


Figure 25. Line Regulation

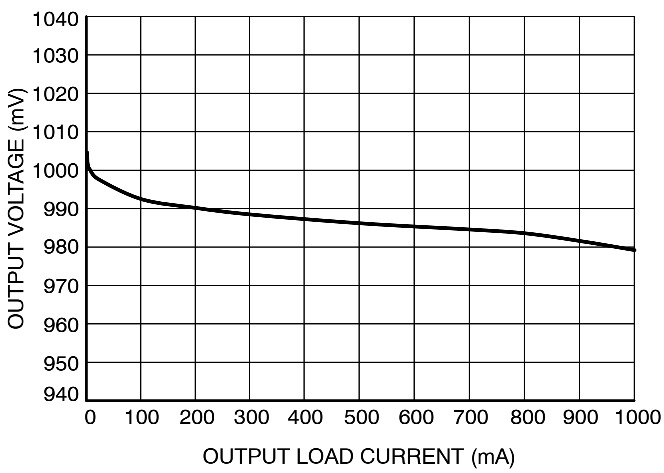


Figure 26. Load Regulation

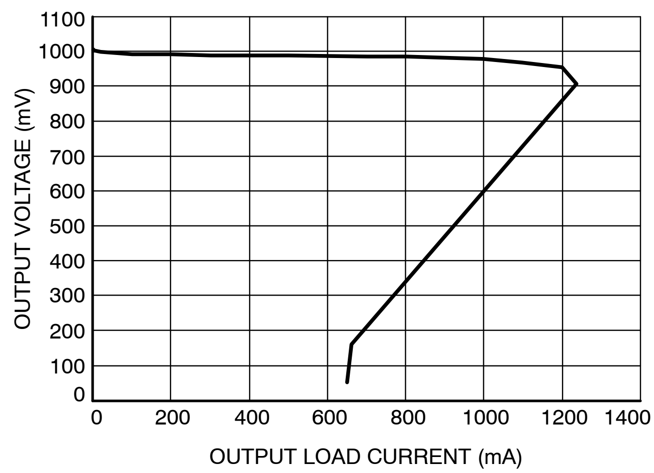


Figure 27. Output Current Capability

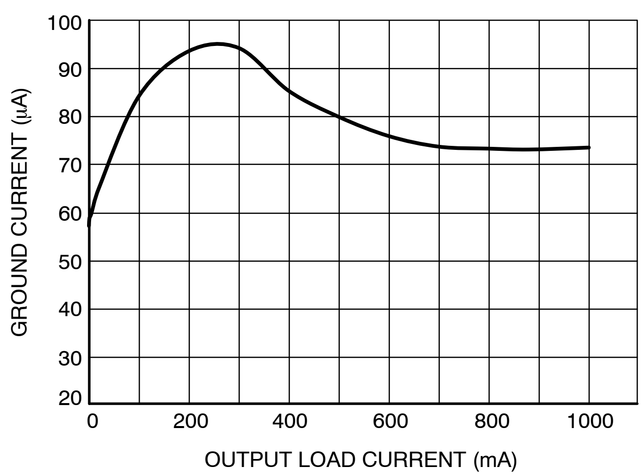


Figure 28. Ground Current vs. Load Current

TRANSIENT CHARACTERISTICS

(shown for V_{OUT} = 1.0 V, V_{IN} = 2.0 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF, C_{BYP} = 0, and T_A = 25°C unless otherwise specified.)

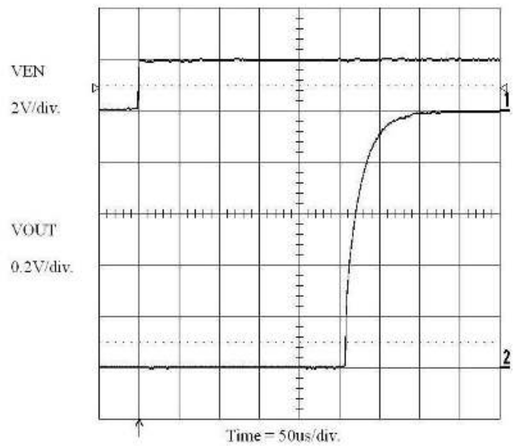


Figure 29. Enable Turn−on (1 mA Load)

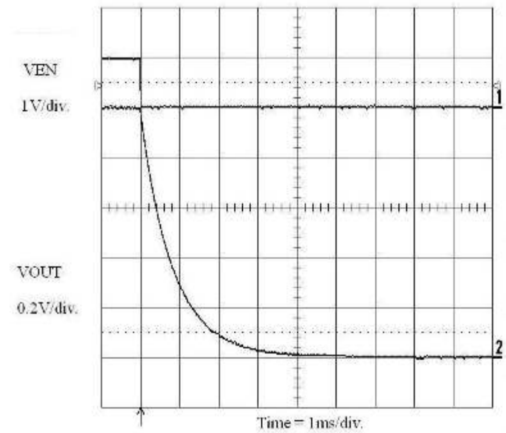


Figure 30. Enable Turn−off (1 mA Load)

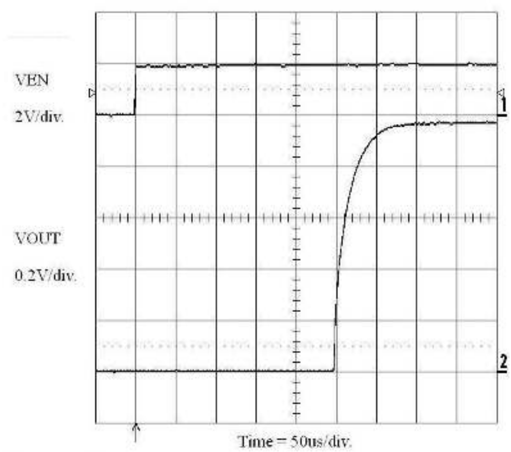


Figure 31. Enable Turn−on (1 A Load)

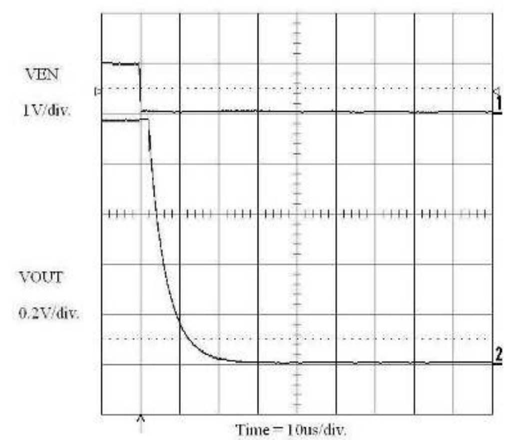


Figure 32. Enable Turn−off (1 A Load)

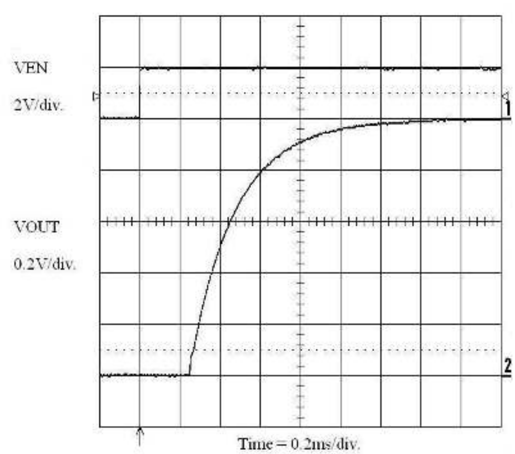


Figure 33. Enable Turn−on (1 mA Load)
C_{BYP} = 470 pF

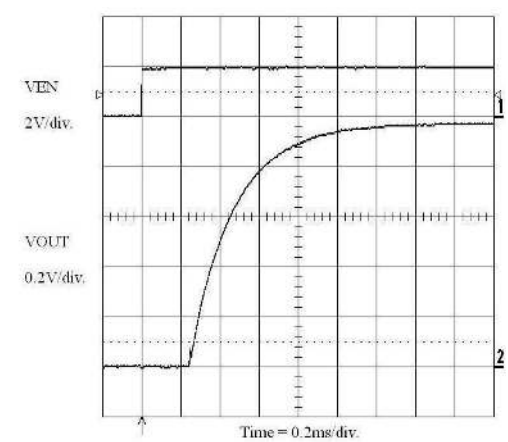


Figure 34. Enable Turn−on (1 A Load)
C_{BYP} = 470 pF

TRANSIENT CHARACTERISTICS

(shown for V_{OUT} = 1.0 V, V_{IN} = 2.0 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF, C_{BYP} = 0, and T_A = 25°C unless otherwise specified.)

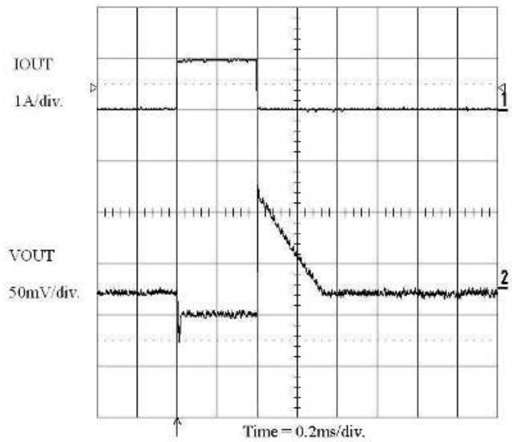


Figure 35. Load Transient Response (1 mA to 1 A)

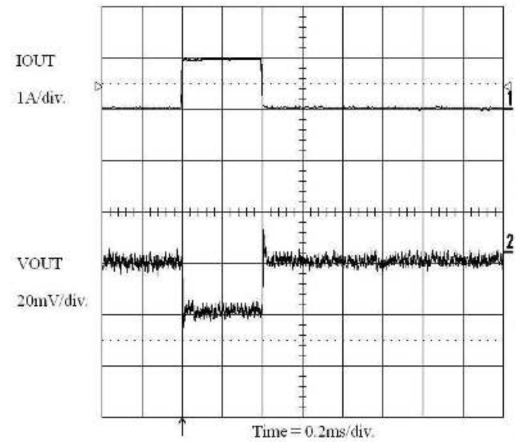


Figure 36. Load Transient Response (1 mA to 1 A) V_{IN} = 2.2 V

PIN FUNCTIONS

V_{IN}

Positive Power Input. Power is supplied to the device through the V_{IN} pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general it is advisable to include a small bypass capacitor adjacent to the regulator. In battery−powered circuits this is particularly important because the output impedance of a battery rises with frequency, so a bypass capacitor in the range of 1 μF to 10 μF is recommended.

GND

Ground. The negative voltage of the input power source. The center pad on the back of the package is also electrically ground. This pad is used for cooling the device by making connection to the buried ground plane through solder filled vias or by contact with a topside copper surface exposed to free flowing air.

ENABLE

ENABLE is an active high logic input which controls the regulator's the output state. If ENABLE < 0.4 V the regulator is shutdown and V_{OUT} = 0 V. If ENABLE > 1.6 V the regulator is active and supplying power to the load.

If the regulator is intended to operate continuously and won't be shut down from time to time ENABLE should be tied to V_{IN}.

BYP

The Bypass Capacitor input is used to decrease output voltage noise by placing a capacitor between BYP and ground. The recommended range of capacitance is from 100 pF to 470 pF. Values larger than this will provide no additional improvement and will further extend CAT6241's startup time.

A bypass capacitor is not required for operation and BYP may be left open or floating if no capacitor is used but DO NOT ground BYP as this will interfere with the error amplifier's functioning.

ADJ

ADJ = Adjust and is the voltage control input. ADJ connects to the center point of a resistor divider which determines the CAT6241's output voltage. See Applications Section for resistor selection guidelines.

V_{OUT}

V_{OUT} is the regulator's output and supplies power to the load. V_{OUT} can be shut off via the ENABLE input. All CAT6241 members are designed to block reverse current, meaning anytime V_{OUT} becomes greater than V_{IN} the pass FET will be shut off so there is no reverse current flow from output to input. CAT6241 is also equipped with an output discharge transistor that is turned ON anytime ENABLE is at a logic Low. This transistor ensures V_{OUT} discharges to 0 V when the regulator is shutdown. This is especially important when powering digital circuitry because if V_{OUT} fails to reach 0 V their POR (power−ON reset) circuitry may not trigger and scrambled data or unpredictable operations may result.

A minimum output capacitor of 2.2 μF should be placed between V_{OUT} and GND to insure stable operation. Increasing the size of C_{OUT}, up to 22 μF, will improve transient response to large changes in load current.

APPLICATIONS INFORMATION

Input Decoupling (C_{IN})

A ceramic or tantalum 1 μF capacitor is recommended and should be connected close to the CAT6241's package. Higher capacitance and lower ESR will improve the overall line and load transient response.

Output Decoupling (C_{OUT})

The minimum output decoupling value is 2.2 μF and can be augmented to fulfill stringent load transient requirements. Larger values, up to 22 μF, improve noise rejection and load regulation transient response. The CAT6241 is a highly stable regulator and performs well over a wide range of Equivalent Series Resistances (ESR) with ceramic chip capacitors.

No−Load Regulation Considerations

The CAT6241 adjustable regulator will operate properly under conditions where the only load current is through the resistor divider that sets the output voltage. However, in the case where the CAT6241 is configured to provide a 0.5 V output, there is no resistor divider and the ADJ pin is connected to VOUT. If the part is enabled under no−load conditions, leakage current through the pass transistor at junction temperatures above 85°C can approach several microamperes, especially as junction temperature approaches 150°C. If this leakage current is not directed into a load, the output voltage will rise above nominal until a load is applied. For this reason it is recommended that a minimum load of 100 μA be present at all times. Normally the voltage setting resistor divider will serve this function but if no divider is used (VOUT = 0.5 V) then an external load of 5 KΩ should be provided.

Output Voltage Adjust

The output voltage can be adjusted from 0.5 V to 5.0 V using resistors between the output and the ADJ input. The output voltage and resistors are chosen using Equation 1 and Equation 2.

$$V_{OUT} = 0.5\left(1 + \frac{R_1}{R_2}\right) + \left(I_{ADJ} \times R_1\right) \qquad \text{(eq. 1)}$$

$$R_2 \cong \frac{0.5\ \text{V}}{I_{DIV}} \qquad \text{(eq. 2)}$$

$$R_1 \cong R_2\left(\frac{V_{OUT}}{0.5\ \text{V}} - 1\right) \qquad \text{(eq. 3)}$$

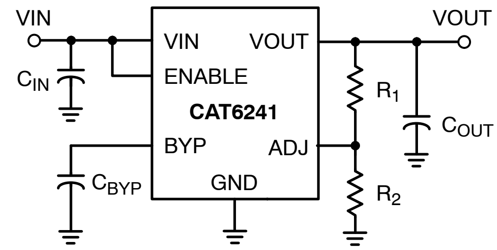


Figure 37. Adjustable Output Resistor Divider

Input bias current, I_{ADJ}, for all practical designs can be ignored (I_{ADJ} = 0). Considering that the lowest recommended I_{OUT} value is 100 μA, then, when there is no load on V_{OUT}, $I_{divider}$ must be 100 μA to keep CAT6241 in regulation. This then sets R2's value using Equation 2 to 5 KΩ, which minimizes output noise. Use Equation 3 to find the required value for R1. If needed, lower values for IDIV can be considered, but not lower than 10 μA. The trade−off will be worse values for both load regulation and TCOUT.

Thermal Considerations

As power in the CAT6241 increases, it may become necessary to provide thermal relief. The maximum power dissipation supported by this device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the CAT6241 has good thermal conductivity through the PCB, the junction temperature will be relatively low even with high power applications. The maximum dissipation the CAT6241 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 4)}$$

Since T_J is not recommended to exceed 125°C, then with CAT6241 soldered to 645 mm^2 (1 sq inch), 1 oz copper area, FR4 PCB material can dissipate in excess of 1 W when the ambient temperature (T_A) is 25°C. Note that this assumes the pad in the center of the package is soldered to the dissipating copper foil. See Figure below for $R_{\theta JA}$ versus PCB area for heat dissipating areas smaller than 645 mm^2. Power dissipation can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND} + I_{OUT}) + I_{OUT}(V_{IN} - V_{OUT}) \qquad \text{(eq. 5)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + (V_{OUT} \times I_{OUT})}{I_{OUT} + I_{GND}} \qquad \text{(eq. 6)}$$

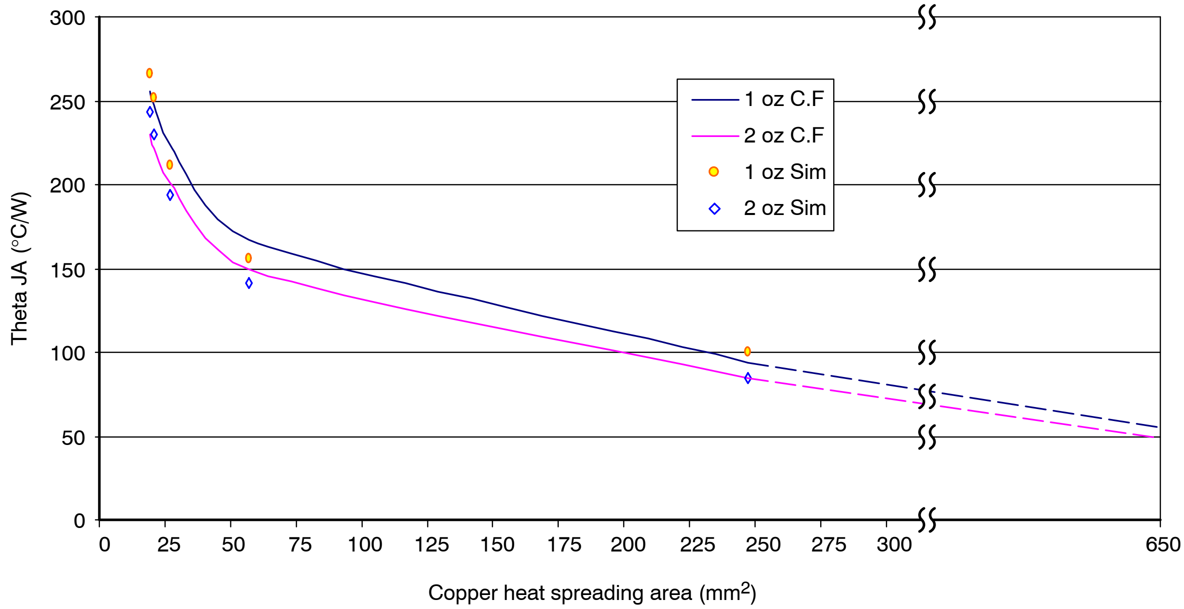


Figure 38. Thermal Resistance vs. PCB Copper Area for 3 mm x 3 mm WDFN Package

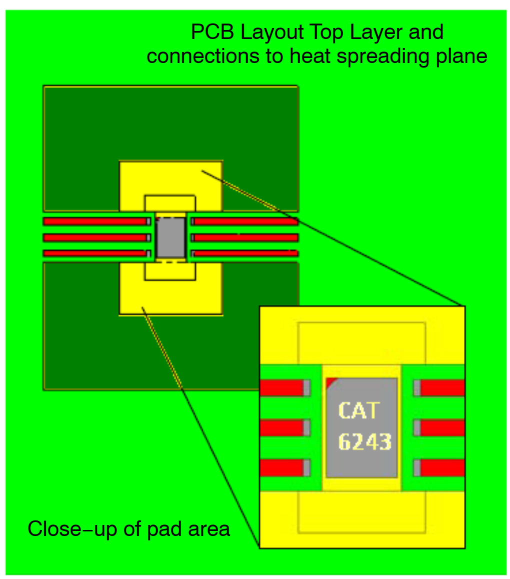


Figure 39. Topside Copper Foil Pattern for Heat Dissipation

Design Hints

V_{IN} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high due to narrow trace width or long length, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the input and output capacitors, as close as possible to the CAT6241, and keep traces between power source and load as short as possible.

SCALE 2:1

UDFN8, 2x2
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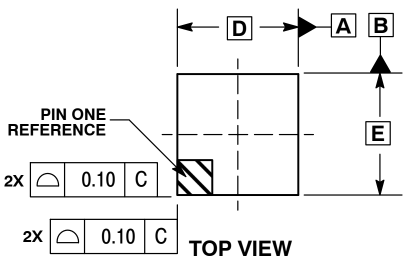
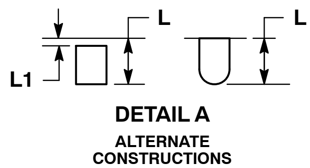
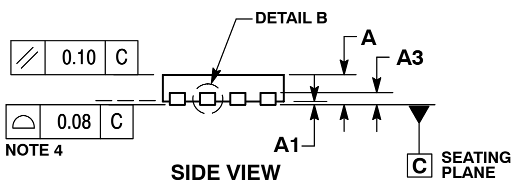
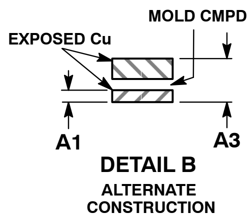


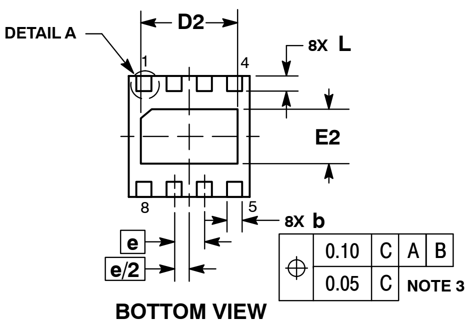




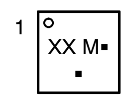


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.18	0.30
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.50 BSC	
L	0.20	0.45
L1	---	0.15



GENERIC MARKING DIAGRAM*

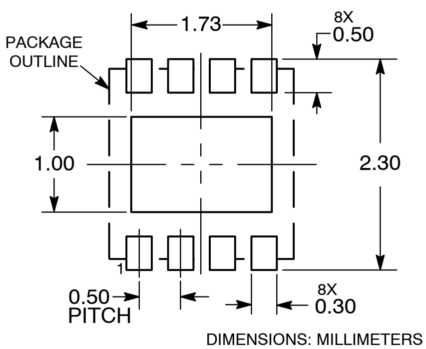


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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