

7-46-07.05

**MOTOROLA  
SEMICONDUCTOR  
TECHNICAL DATA**

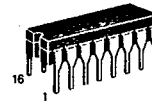
**MC54/74HC174**

**Hex D Flip-Flop with Common  
Clock and Reset  
High-Performance Silicon-Gate CMOS**

The MC54/74HC174 is identical in pinout to the LS174. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 162 FETs or 40.5 Equivalent Gates



**J SUFFIX  
CERAMIC  
CASE 620-09**



**N SUFFIX  
PLASTIC  
CASE 648-06**



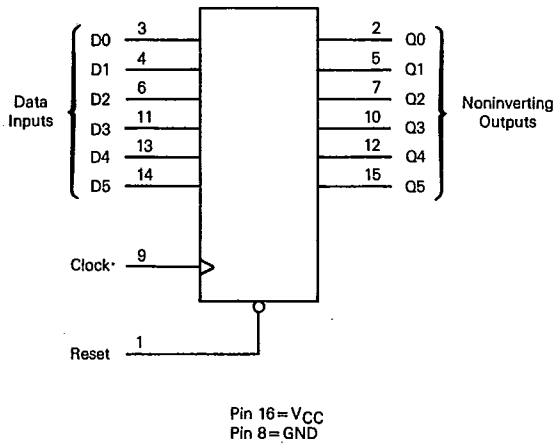
**D SUFFIX  
SOIC  
CASE 751B-03**

**ORDERING INFORMATION**

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
Dimensions in Chapter 7.

**LOGIC DIAGRAM**



**PIN ASSIGNMENT**

Reset	1	16	V <sub>CC</sub>
Q0	2	15	Q5
D0	3	14	D5
D1	4	13	D4
Q1	5	12	Q4
D2	6	11	D3
Q2	7	10	Q3
GND	8	9	Clock

**FUNCTION TABLE**

Inputs		Output	
Reset	Clock	D	Q
L	X	X	L
H		H	H
H		L	L
H	L	X	no change
H		X	no change

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## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C  
Ceramic DIP: -10 mW/°C from 100° to 125°C  
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V	
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> =2.0 V V <sub>CC</sub> =4.5 V V <sub>CC</sub> =6.0 V	0 0 0	1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> =0.1 V or V <sub>CC</sub> -0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	5.9	5.9	5.9	
			6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V <sub>in</sub> =V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	6.0	0.1	0.1	0.1	
			6.0	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> =V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> =V <sub>CC</sub> or GND I <sub>out</sub> =0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

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AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
$f_{max}$	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
$t_{PHL}$	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
$C_{in}$	Maximum Input Capacitance	—	10	10	10	pF

## NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, VCC = 5.0 V		pF
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TIMING REQUIREMENTS (Input  $t_r = t_f = 6$  ns)

Symbol	Parameter	VCC V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
$t_{su}$	Minimum Setup Time, Data to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
$t_h$	Minimum Hold Time, Clock to Data (Figure 3)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
$t_{rec}$	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
$t_w$	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_w$	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
$t_r$ , $t_f$	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

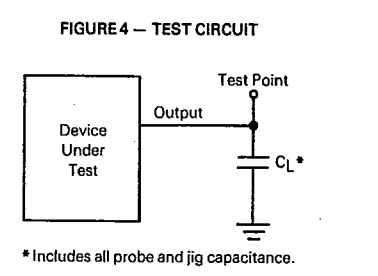
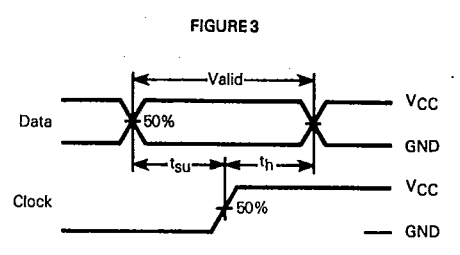
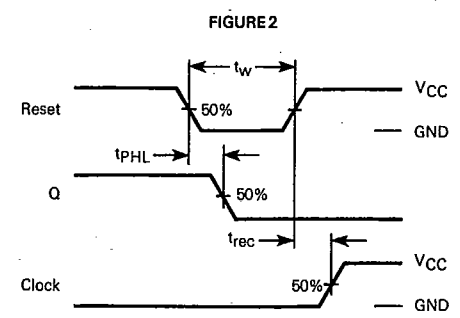
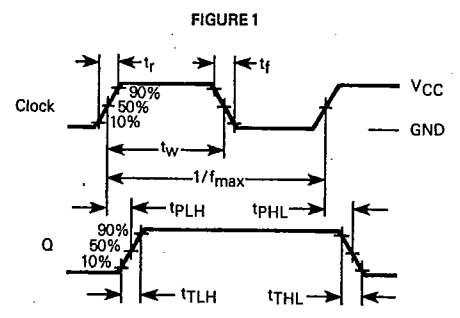
NOTE: Information on typical parametric values can be found in Chapter 4.

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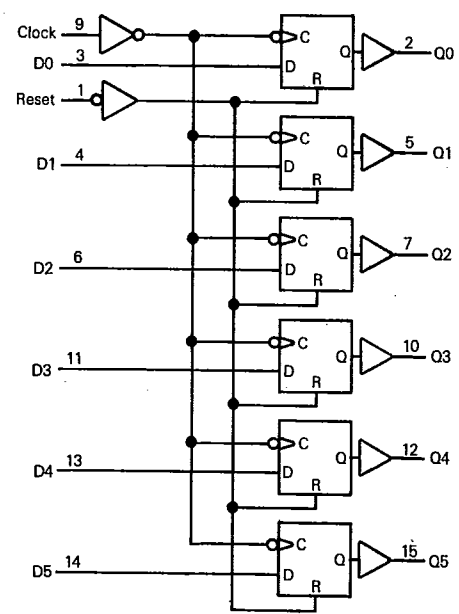
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SWITCHING WAVEFORMS



EXPANDED LOGIC DIAGRAM



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