

**Circuits from the Lab™**  
Reference Circuits

*Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit [www.analog.com/CN0348](http://www.analog.com/CN0348).*

### Devices Connected/Referenced

AD5541A	Serial-Input, Voltage Output, Unbuffered 16-Bit DAC
ADA4500-2	Rail-to-Rail Input/Output, Zero Input Crossover Distortion Amplifier
ADR4550	Ultralow Noise, High Accuracy, 5 V Voltage Reference

## 16-Bit Single-Supply Buffered Voltage Output Digital-to Analog Conversion with Less Than $\pm 1$ LSB Integral and Differential Nonlinearity

### EVALUATION AND DESIGN SUPPORT

#### Circuit Evaluation Boards

[CN-0348 Circuit Evaluation Board \(EVAL-CN0348-SDPZ\)](#)

[System Demonstration Platform \(EVAL-SDP-CB1Z\)](#)

#### Design and Integration Files

[Schematics](#), [Layout Files](#), [Bill of Materials](#)

### CIRCUIT FUNCTION AND BENEFITS

The circuit in Figure 1 is a complete single-supply, 16-bit buffered voltage output DAC that maintains  $\pm 1$  LSB integral and differential nonlinearity by utilizing a CMOS DAC followed by an innovative amplifier that has no crossover distortion.

The circuit eliminates the crossover nonlinearity associated with most rail-to-rail op amps that can be as high as 4 or 5 LSBs for a 16-bit system.

This industry-leading solution is ideal for industrial process control and instrumentation applications where a compact, single-supply, low cost, and highly linear 16-bit buffered voltage source is required.

Total power dissipation for the three active devices is less than 25 mW typical when operating on a single 6 V supply.

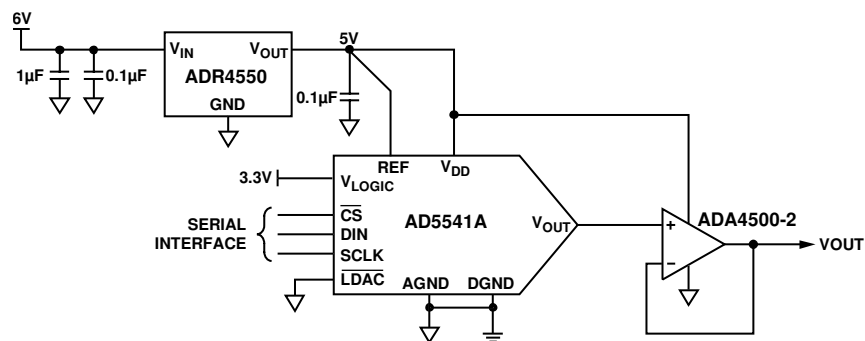


Figure 1.  $\pm 1$  LSB Linear 16-Bit Buffered Voltage Output DAC (Simplified Schematic, All Connections and Decoupling Not Shown)

#### Rev. 0

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## CIRCUIT DESCRIPTION

Figure 1 shows the single supply signal chain that consists of a voltage reference, a digital-to-analog converter (DAC) and a DAC buffer. The reference voltage of the DAC is equal to the supply voltage,  $V_{DD}$ , to maximize dynamic output range and signal-to-noise ratio. With this configuration, a rail-to-rail input and output buffer amplifier is required.

The DAC is the [AD5541A](#) 16-bit, serial input, voltage output segmented R/2R CMOS DAC. The output voltage of the DAC is dependent on the reference voltage, as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where

$D$  is the decimal data word loaded in the DAC register.

$N$  is the number of bits.

For a reference of 5 V, and  $N = 16$ , the equation simplifies to the following:

$$V_{OUT} = \frac{5 \times D}{2^{16}} = \frac{5 \times D}{65,536}$$

This gives a  $V_{OUT}$  of 2.5 V at mid-scale, and 5 V at full-scale.

The LSB size is  $5 \text{ V}/65,536 = 76.3 \text{ } \mu\text{V}$ .

One LSB at 16 bits is also 0.0015% of full-scale or 15 ppm FS.

The [ADR4550](#) voltage reference provides a high precision, low noise (2.8  $\mu\text{V}$  p-p, 0.1 Hz to 10 Hz) and stable reference to the DAC. The [ADR4550](#) uses an innovative core topology to achieve high accuracy while offering industry-leading temperature stability and noise performance. The low output voltage temperature coefficient (2 ppm/ $^{\circ}\text{C}$  maximum) and low long-term output voltage drift of the device also improve system accuracy over time and temperature variations.

The initial room temperature accuracy of the [ADR4550B](#) is  $\pm 0.02\%$  maximum, which is approximately 14 LSBs at 16 bits. This initial error can be removed with a system calibration. The voltage reference drives the REF pin of the DAC as well as provides power to the DAC and the output buffer. As a result, it must supply up to 3.9 mA of load current. The [ADR4550](#) can drive up to 10 mA with 25 ppm/mA load current regulation.

The [ADR4550](#) reference should be placed as close to the REF pin of the DAC as possible to minimize the length of the output traces, and therefore, the error introduced by the voltage drop. Current flowing through a PCB trace produces an IR voltage drop, and with longer traces, this voltage drop can be several millivolts or more, introducing a considerable error. A 1 inch long, 0.005 inch wide trace of 1oz copper has a resistance of approximately 100 m $\Omega$  at room temperature. With a load current of 10 mA, this can introduce a 1 mV error.

The [ADA4500-2](#) is selected as the output buffer. This device is a high precision amplifier with maximum offset voltage of 120  $\mu\text{V}$ , offset drift of less than 5.5  $\mu\text{V}/^{\circ}\text{C}$ , 0.1 Hz to 10 Hz noise of 2  $\mu\text{V}$  p-p, and maximum input bias current of 2 pA. Its key feature of rail-to-rail input and output swing with zero crossover distortion makes it a suitable candidate as a DAC buffer.

A typical rail-to-rail input amplifier uses two differential pairs to achieve rail-to-rail input swing (see [Tutorial MT-035](#)). One differential pair is active at the higher range of the input common-mode voltage, and the other pair is active at the lower end. This classic dual differential pair topology introduces crossover distortion during the handoff of one differential pair to the other. The change in offset voltage causes nonlinearity when the amplifier is used as a DAC buffer. The [ADA4500-2](#) uses an integrated charge pump in its input structure to achieve rail-to-rail input swing without the need for a second differential pair. Therefore, it does not exhibit crossover distortion. Using a zero crossover distortion amplifier in this single supply system provides wide dynamic output range while maintaining linearity over the input common mode/input digital code range. Details of the operation of the [ADA4500-2](#) can be found on the [ADA4500-2](#) data sheet.

The output impedance of the DAC is constant (typically 6.25 k $\Omega$ ) and code-independent. However, the output buffer should have a high input impedance (low input bias current) to minimize errors. The [ADA4500-2](#) is a suitable candidate with high input impedance and 2 pA maximum of input bias current at room temperature, and 190 pA maximum of input bias current over temperature. This results in 1.2  $\mu\text{V}$  of worst-case error due to input bias current, which is much less than 1 LSB.

The [AD5541A](#) is available 10-lead MSOP or 10-lead LFCSP. The [ADR4550](#) is available in 8-lead SOIC, and the [ADA4500-2](#) is available in 8-lead MSOP or 8-lead LFCSP.

Measured results show that the combination of the [AD5541A](#), [ADR4550](#) and [ADA4500-2](#) is an excellent solution for high accuracy, low noise performance applications. The [ADA4500-2](#) maintains the linearity of the DAC with no crossover distortion.

### **Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) Measurements**

INL error is the deviation in LSB of the actual DAC transfer function from an idealized transfer function. DNL error is the difference between an actual step size and the ideal value of 1 LSB. This system solution provides a 16-bit resolution with  $\pm 1$  LSB DNL and INL. Figure 2 and Figure 3 show the DNL and INL performance of the circuit.

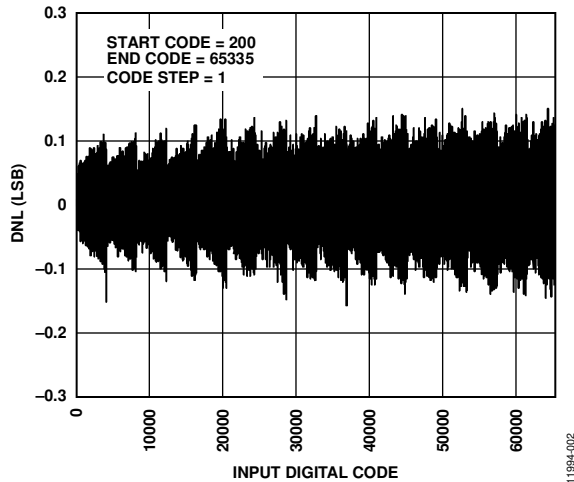


Figure 2. Differential Non Linearity (DNL)

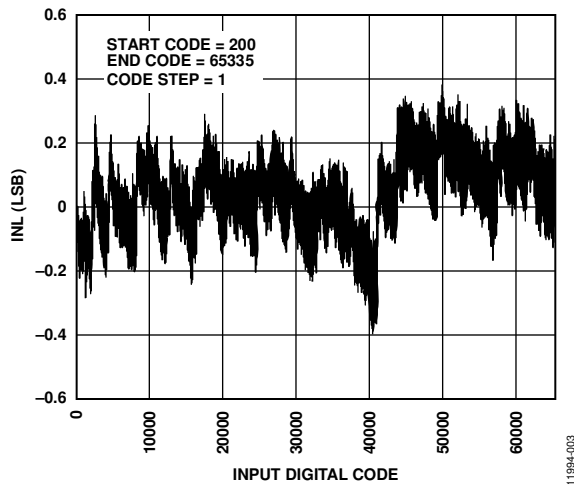


Figure 3. Integral Non Linearity (INL)

Note that the DNL and INL measurements exclude the 200 codes (approximately 15 mV) from either end of the range. This is because the rail-to-rail output stage becomes nonlinear over this region as described in [Tutorial MT-035](#).

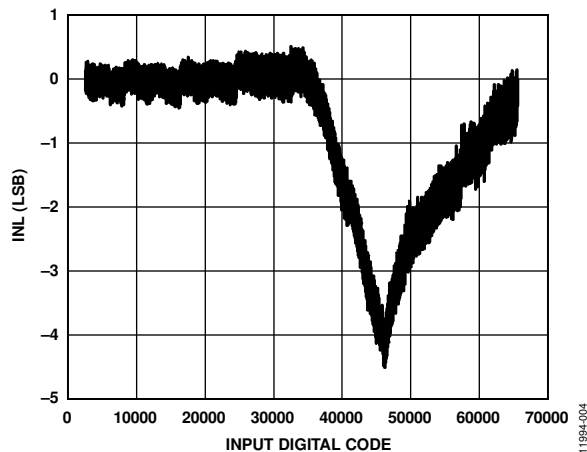


Figure 4. DAC Nonlinearity when Using Op Amp Buffer with Traditional Rail-to-Rail Input Stage.

Figure 4 shows the nonlinearity introduced by using an op amp with a traditional rail-to-rail input stage. Note that the peak error of about 4 LSBs occurs when the common-mode voltage is about 1.7 V away from the +5 V supply rail.

### Board Layout Considerations

It is important to carefully consider the power supply and ground return layout on the board. The printed circuit board should have separate analog and digital sections. If the circuit is used in a system where multiple devices require an analog ground to digital ground connection, make the connection at only one point. Power supplies to all components should be bypassed with at least 0.1  $\mu$ F capacitors. These bypass capacitors should be as physically close as possible to the device, with the capacitor ideally right up against the device. The 0.1  $\mu$ F capacitor should be chosen to have low effective series resistance (ESR) and low effective series inductance (ESL), such as ceramic capacitors. This 0.1  $\mu$ F capacitor provides a low impedance path to ground for transient currents. The power supply line should also have as large a trace as possible to provide a low impedance supply path. Proper layout, grounding, and decoupling techniques should be used to achieve optimum performance (see [Tutorial MT-031, Grounding Data Converters and Solving the Mystery of AGND and DGND](#) and [Tutorial MT-101, Decoupling Techniques](#)).

### COMMON VARIATIONS

For a lower power consumption solution (at lower speed), use the [ADA4505-1/ADA4505-2/ADA4505-4](#) as the output buffer. The [ADA4505](#) family is a micropower, zero-crossover distortion amplifier with low input bias current.

The [ADR425](#), [ADR435](#) and [ADR445](#) are suitable candidates to provide the 5 V reference. They feature high accuracy, low noise and accept input voltages up to 18 V.

For bipolar output swing, use the [AD5512A/AD5542A](#). These are single, 12-/16-bit, unbuffered voltage output digital-to-analog converters (DAC) that allow bipolar mode operation.

Another solution to avoid crossover distortion at the expense of a reduced output range would be to use a lower reference voltage, for example the 2.5 V [ADR4525](#), with the same supply voltage (5 V). This ensures that the crossover point of a typical rail-to-rail input amplifier (with dual differential pair topology) is out of the input digital code range.

Circuit Notes [CN-0181](#) and [CN-0169](#) also show other alternatives for digital-to-analog conversion using the [AD5541A](#).

## CIRCUIT EVALUATION AND TEST

This circuit uses the [EVAL-CN0348-SDPZ](#) circuit board and the [EVAL-SDP-CB1Z](#) system demonstration platform (SDP) evaluation board. The two boards have 120-pin mating connectors, allowing for the quick setup and evaluation of the circuit's performance. The [EVAL-CN0348-SDPZ](#) board contains the circuit to be evaluated, as described in this note, and the SDP evaluation board is used with the [CN-0348](#) evaluation software to capture the data from the [EVAL-CN0348-SDPZ](#) circuit board.

### Equipment Needed

- PC with a USB port and Windows XP or Windows Vista (32-bit), or Windows 7 (32-bit)
- [EVAL-CN0348-SDPZ](#) circuit evaluation board
- [EVAL-SDP-CB1Z](#) SDP evaluation board
- [CN-0348](#) evaluation software
- Power supply: 6 V to 18 V, or 6 V wall wart.
- Agilent 3458A Multimeter or equivalent.
- A GPIB-to-USB cable (only required for capturing analog data from the DAC and transferring it to the PC).

### Getting Started

Load the evaluation software by placing the CN0348 Evaluation Software disc in the CD drive of the PC. Using My Computer, locate the drive that contains the evaluation software disc.

### Functional Block Diagram

See Figure 5 shows the functional block diagram of the test setup.

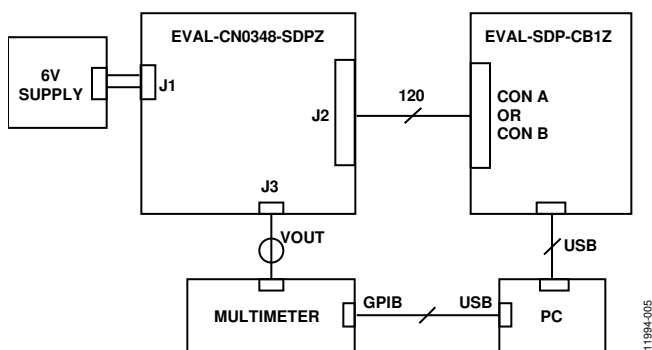


Figure 5. Test Setup Functional Block Diagram

### Setup

Connect the 120-pin connector on the [EVAL-CN0348-SDPZ](#) circuit board to the connector marked CON A on the [EVAL-SDP-CB1Z](#) evaluation (SDP) board. Use nylon hardware to secure the two boards firmly, using the holes provided at the ends of the 120-pin connectors.

With power to the supply off, connect a +6 V (up to +18 V) power supply to the pins marked V+ and AGND on the board (J1). Connect the USB cable supplied with the SDP board to the USB port on the PC. Do not connect the USB cable to the mini USB connector on the SDP board at this time.

### Test

Apply power to the V+ supply connected to [EVAL-CN0348-SDPZ](#) circuit board. Connect the USB cable from the PC to the USB mini-connector on the SDP board and launch the evaluation software. The software can communicate to the SDP board if the Analog Devices System Development Platform driver is listed in the Device Manager.

After USB communications are established, the SDP board can be used to send, receive, and capture serial data from the [EVAL-CN0348-SDPZ](#) board.

Figure 6 is a photo of the [EVAL-CN0348-SDPZ](#) evaluation board.

Information and details regarding test setup and how to use the evaluation software for data capture can be found in the [CN-0348 Software User Guide](#).

Information regarding the SDP board can be found in the [SDP User Guide](#).

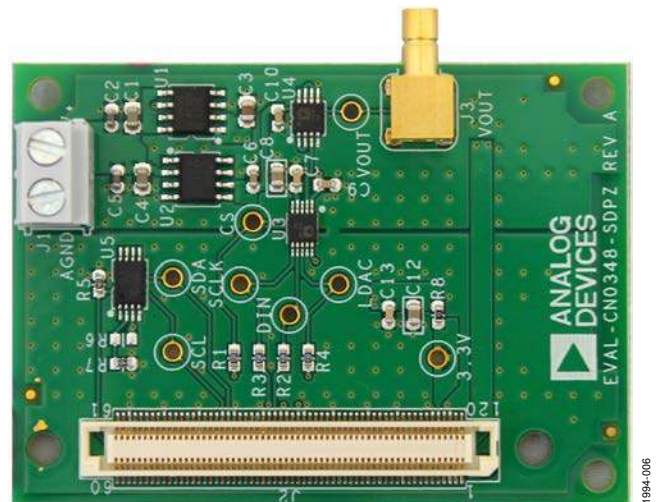


Figure 6. [EVAL-CN0348-SDPZ](#) Evaluation Board

**LEARN MORE**

CN-0348 Design Support Package:

<http://www.analog.com/CN0348-DesignSupport>

Kester, Walt. *The Data Conversion Handbook*, Chapters 3 and 7, Analog Devices. 2005.

MT-015 Tutorial, *Basic DAC Architectures II: Binary DACs*. Analog Devices.

MT-016 Tutorial, *Basic DAC Architectures III: Segmented DACs*, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND*. Analog Devices.

MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

**Data Sheets and Evaluation Boards**

AD5541A Data sheet

ADA4500-2 Data sheet

ADR4550 Data sheet

**REVISION HISTORY**

1/14—Revision 0: Initial Version

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