



TSH31

280MHz BANDWIDTH MOS INPUT SINGLE OPERATIONAL AMPLIFIER

- VERY LOW INPUT CURRENT : 2pA typ
- GAIN BANDWIDTH PRODUCT : 280MHz
- GAIN OF 2 STABILITY
- SLEW RATE : 300V/μs
- STANDARD PIN OUT

DESCRIPTION

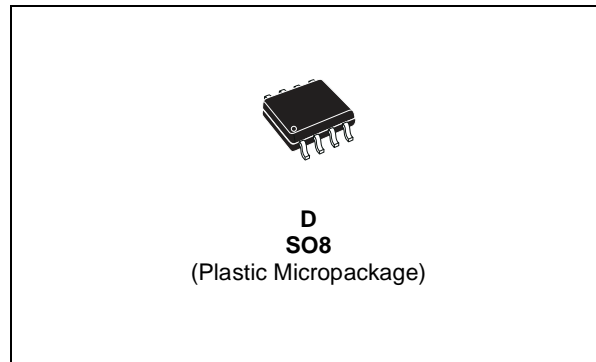
The TSH31 is a low cost wide bandwidth single operational amplifier featuring extremely low input current of 2pA typ.

Other features as high slew rate, fast settling time and high linearity make it suitable for many applications requiring speed and very high input impedance as photo cell amplifier, Fet probe, high speed precision integrator, sample and hold circuit.

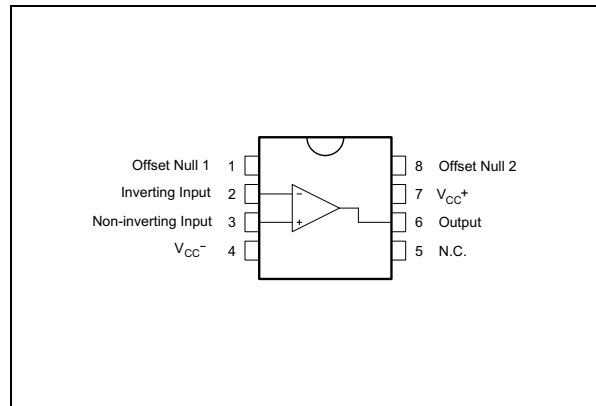
ORDER CODE

Part Number	Temperature Range	Package
		D
TSH31I	-40°C, +125°C	•

D = Small Outline Package (SO) - also available in Tape & Reel (DT)

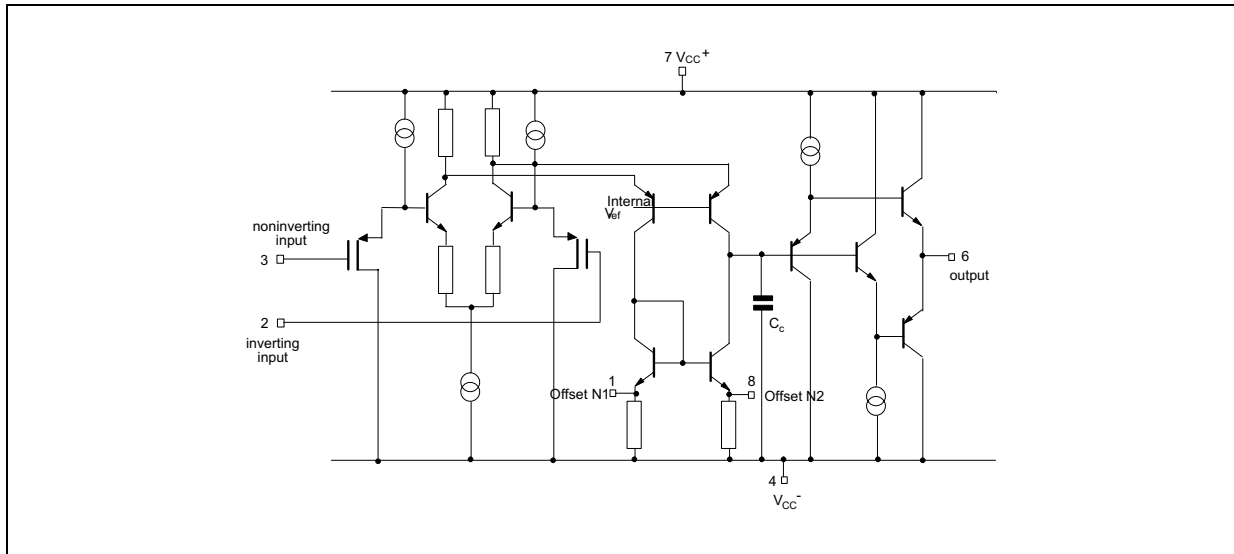


PIN CONNECTIONS (top view)

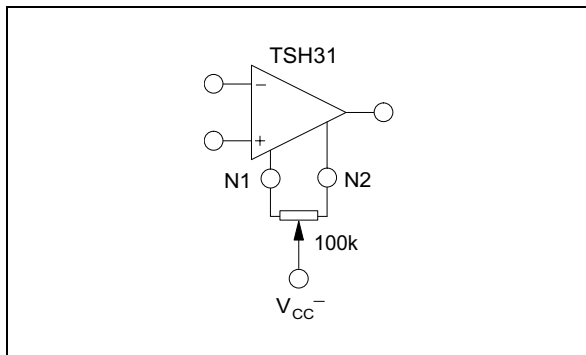


TSH31

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 7	V
V_{id}	Differential Input Voltage	± 5	V
V_i	Input Voltage	± 5	V
I_{in}	Current On Offset Null Pins	± 20	μ A
T_{oper}	Operating Free-Air Temperature range	-40 to +125	$^{\circ}$ C

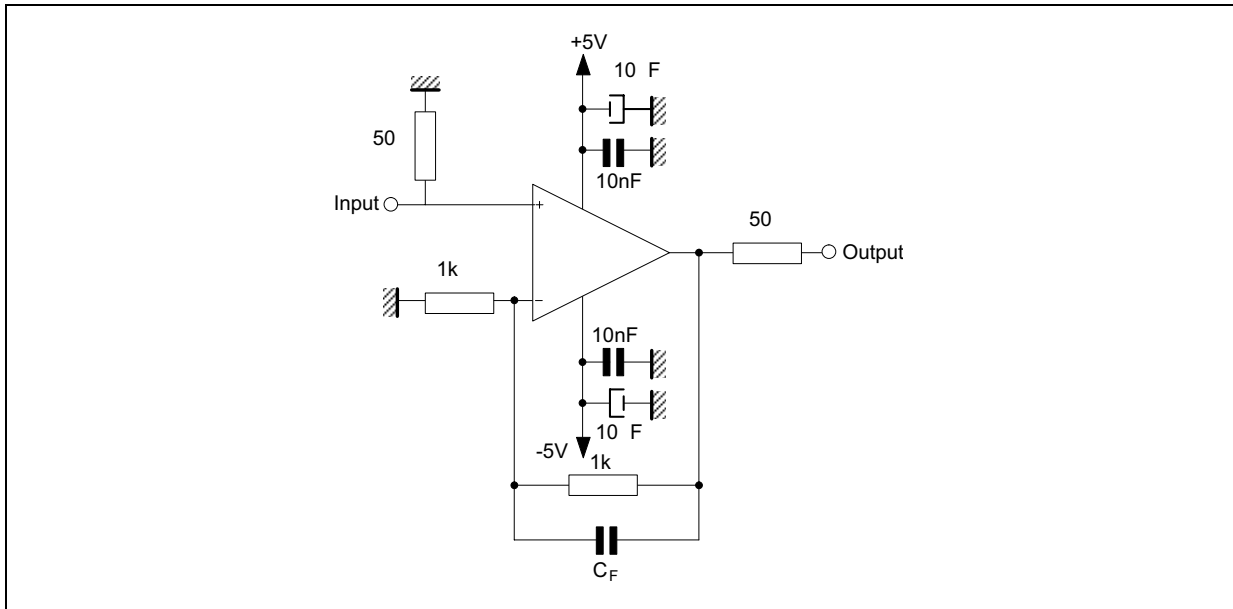
OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	± 3 to ± 6	V
V_{ic}	Common Mode Input Voltage Range	V_{CC-} to $V_{CC+} - 3$	V

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage		3	15	mV
DV_{io}	Input Offset Voltage Drift $T_{min.} \leq T_{amb} \leq T_{max.}$		20		$\mu V/^{\circ}C$
I_{ib}	Input Bias Current		2	300	pA
I_{io}	Input Offset Current		2	200	pA
I_{CC}	Supply Current, no load $V_{CC} = \pm 5V$		20	40	mA
A_{vd}	Large Signal Voltage Gain $V_o = \pm 2.5V$ $R_L = 100\Omega$	200	800		V/V
V_{icm}	Input Common Mode Voltage Range	-5 to +2	-5.5 to +2.5		V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm min.}$	55	95		dB
SVR	Supply Voltage Rejection Ratio $V_{CC} = \pm 5V$ to $\pm 3V$	45	65		dB
V_o	Output Voltage $R_L = 100\Omega$	± 2.5	+3.5 -3.7		V
I_o	Output Short Circuit Current $V_{id} = \pm 1V$, $V_o = 0V$		± 70		mA
GBP	Gain Bandwidth Product $A_{VCL} = 100$, $R_L = 100\Omega$, $f = 7.5MHz$		280		MHz
SR	Slew Rate $V_{in} = \pm 2V$, $A_{VCL} = 1$, $R_L = 100\Omega$		300		V/ μs
e_n	Equivalent Input Voltage Noise $f = 1MHz$		20		nV/ \sqrt{Hz}
ϕ_m	Phase Margin $A_{VM} = 1$, $R_L = 100\Omega$, $C_L = 15pF$		40		Degrees

EVALUATION CIRCUIT



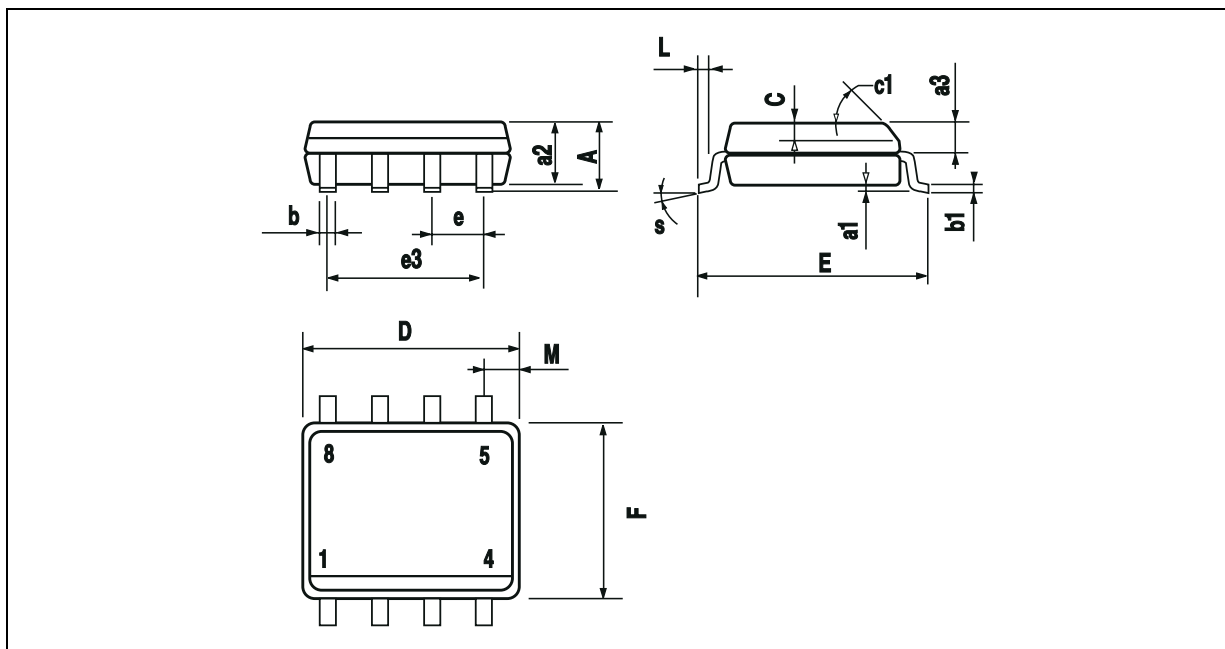
PRINTED CIRCUIT LAYOUT

As for any high frequency device, a few rules must be observed when designing the PCB to get the best performances from this high speed op amp.

From the most to the least important points :

- Each power supply lead has to be bypassed to ground with a 10nF ceramic capacitor very close to the device and a 10 μ F tantalum capacitor.
- To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- All leads must be wide and as short as possible especially for op amp inputs. This is in order to decrease parasitic capacitance and inductance.
- Use small resistor values to decrease time constant with parasitic capacitance.
- Choose component sizes as small as possible (SMD).
- On output, decrease capacitor load so as to avoid circuit stability being degraded which may cause oscillation. You can also add a serial resistor in order to minimise its influence.
- One can add in parallel with feedback resistor a few pF ceramic capacitor C_F adjusted to optimize the settling time.

PACKAGE MECHANICAL DATA
8 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

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