A product Line of
Diodes Incorporated

PI6LC48H04

PCIe® 4.0 and Ethernet Clock Generator with 4 HCSL Outputs

Features

- PCIe® 4.0/3.0/2.0/1.0 compliant
  - PCIe 4.0 Phase jitter - 0.45ps RMS
- LVDS compatible outputs
- Supply voltage of 3.3V±5% and 2.5V±5%
- 25MHz crystal or clock input frequency
- HCSL outputs, 0.7V low power differential pair
- Jitter 35ps cycle-to-cycle (typ)
- RMS phase jitter 12kHz ~ 20MHz @ 100MHz - 0.32ps (typ)
- RMS phase jitter 12kHz ~ 20MHz @ 125MHz, 156.25MHz, 200MHz - 0.3ps (typ)
- Industrial temperature range
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

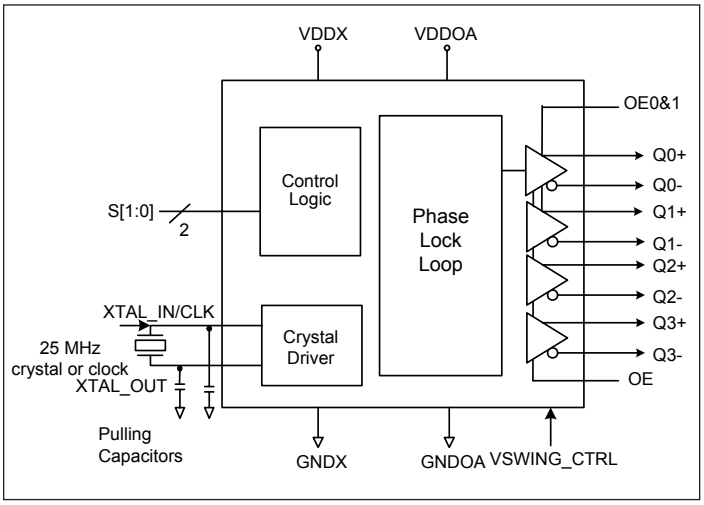
  https://www.diodes.com/quality/product-definitions/
- Packaging: (Pb-free and Green)
  - 20-pin TSSOP (L20)

Description

The PI6LC48H04 is a clock generator compliant to PCI Express® 4.0/3.0/2.0/1.0, Ethernet and other requirements. The device is used for networking or embedded systems.

The PI6LC48H04 provides four differential (Low Power HCSL) or LVDS outputs. Using Diodes' patented Phase Locked Loop (PLL) techniques, the device takes a 25MHz crystal input and produces four pairs of differential outputs (HCSL) at 156.25MHz, 100MHz, 125MHz, 133.33MHz and 200MHz clock frequencies.

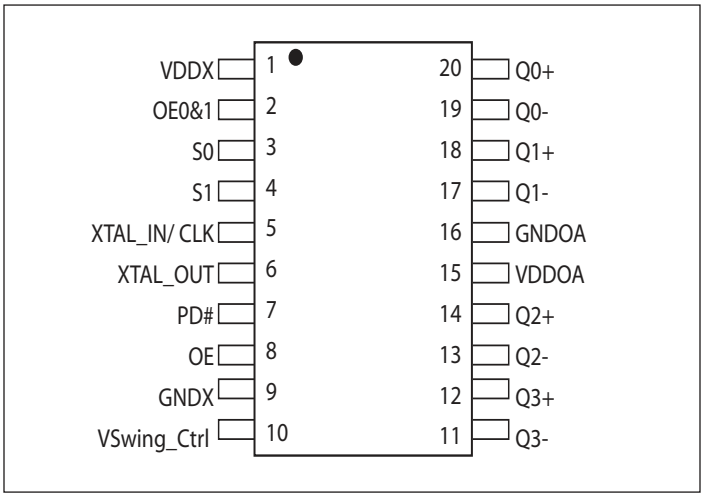
Block Diagram



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin #	Pin Name	I/O Type		Description
1	VDDX	Power		Crystal supply pin.
2	OE0&1	Input	Pull-up	Output enable pin for Q0+/- and Q1+/-. When HIGH, output is enabled and active. When LOW, output is disabled and in high impedance state. Don't care if OE is LOW. Internal 343kΩ pull-up resistor.
3	S0	Input	Pull-up	Frequency select pin. Internal 343kΩ pull-up resistor.
4	S1	Input	Pull-up	Frequency select pin. Internal 343kΩ pull-up resistor.
5	XTAL_IN/CLK	Input		Crystal or clock input. Connect to a 25MHz crystal or single ended clock.
6	XTAL_OUT	Output		Crystal output. Leave unconnected for clock input.
7	PD#	Input	Pull-up	Power down pin. When HIGH, the device is in normal operation. When LOW, the device is in power down mode and all outputs are in high impedance state. Internal 343kΩ pull-up resistor.
8	OE	Input	Pull-up	Output enable pin for all outputs. When HIGH, Q2+/- and Q3+/- are enabled and active and Q0+/- and Q1+/- depends on OE0&1. When LOW, all outputs are disabled and in high impedance state and not dependent on OE0&1. Internal 343kΩ pull-up resistor.
9	GNDX	Power		Crystal ground.
10	VSWING_CTRL	Input	Pull-up/ pull down	VOH selection pin for all outputs. Tri-level selection for different voltage swings.
11, 12	Q3-, Q3+	Output		Low power HCSL clock output 3.
13, 14	Q2-, Q2+	Output		Low power HCSL clock output 2.
15	VDDOA	Power		Analog and output supply pin.
16	GNDOA	Power		Analog and output ground.
17, 18	Q1-, Q1+	Output		Low power HCSL clock output 1.
19, 20	Q0-, Q0+	Output		Low power HCSL clock output 0.

Table 1: Output Select Table (25MHz Xtal Input)

S1	S0	CLK(MHz)
0	0	156.25
0	1	100
1	0	125
1	1	200 (Default)

Table 1a: Output Select Table (Generating Other Frequencies)

Xtal Input Freq.	S1	S0	CLK(MHz)
21.33MHz	0	0	133.3MHz
26.66MHz	1	0	133.3MHz

Note: Above frequencies are only for the provided settings. Do not deviate from provided S1, S0 settings. For any other output frequencies, please contact Diodes.

Table 2: Output Enable Table

OE	OE0&1	Q0+/-	Q1+/-	Q2+/-	Q3+/-
0	0	HiZ	HiZ	HiZ	HiZ
0	1	HiZ	HiZ	HiZ	HiZ
1	0	HiZ	HiZ	Active	Active
1 (Default)	1 (Default)	Active	Active	Active	Active

Table 3: VSWING_CTRL Select Table

VSWING_CTRL	Output Amplitude (V)
0	0.63
Open (default)	0.75
1	0.87

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential	4.6V
All Inputs	-0.5V to V_{DD}+0.5V
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
ESD Protection (HBM)	2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Specifications

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured with respect to GND)	3.135	3.3	3.465	V
	2.375	2.5	2.625	V

DC Characteristics (T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
V_{IH}	Input High Voltage(1)	OE, S0, S1, OE0&1, PD# @ VDD=3.3V	2.0		V_{DD} +0.3	V
		OE, S0, S1, OE0&1, PD# @ VDD=2.5V	1.7		V_{DD} +0.3	V
		VSWING_CTRL @ VDD = 3.3V and 2.5V	V_{DD} x 0.7		V_{DD} +0.3	V
V_{IL}	Input Low Voltage(1)	OE, S0, S1, OE0&1, PD# @ VDD=3.3V	GND -0.3		0.8	V
		OE, S0, S1, OE0&1, PD# @ VDD=2.5V	GND -0.3		0.7	V
		VSWING_CTRL @ VDD = 3.3V and 2.5V	GND -0.3		V_{DD} x 0.3	V
I_{IH}	Input High Current	OE, S0, S1, OE0&1, PD# with Vin = V_{DD}	-5		5	µA
		VSWING_CTRL with Vin = V_{DD}			150	
I_{IL}	Input Low Current	OE, S0, S1, OE0&1, PD# with Vin = 0	-20		20	
		VSWING_CTRL with Vin = 0	-150			
I_{DD}(2)	Operating Supply Current	C_L = 2pF			120	mA
I_{DDOE}		OE = LOW			65	mA
I_{DDPD}	Power Down Supply Current				50	µA
C_{IN}	Input Capacitance	@ 25MHz			7	pF
C_{OUT}	Output Capacitance	@ 25MHz			6	pF

Notes:

1. Single edge is monotonic when transition through region.
2. Total current consumption of device, inclusive of I_{DDOE}

HCSL Output AC Characteristics (V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{IN}	Input Frequency			25		MHz
F_{OUT}	Output Frequency		100		200	MHz
V_{OH}	Output High Voltage (1,2)	100 MHz HCSL output @ V_{DD} = 3.3V	660	800	900	mV
V_{OL}	Output Low Voltage(1,2)	100 MHz HCSL output @ V_{DD} = 3.3V	-150	0		mV
V_{CPA}	Crossing Point Voltage(1,2)	Absolute @100MHz	250	350	550	mV
V_{CN}	Crossing Point Voltage(1,2,4)	Variation over all edges@100MHz			140	mV
J_{CC}	Jitter, Cycle-to-Cycle(1,3)			35	60	ps
J_{Period}	Period jitter			26	40	ps
J_{Phase}	RMS Phase Jitter, (Random)	100MHz 25MHz Xtal input, 12kHz - 20MHz		0.32	0.5	ps
		125MHz 25MHz Xtal input, 12kHz - 20MHz		0.3	0.5	ps
		156.25MHz 25MHz Xtal input, 12kHz - 20MHz		0.3	0.5	ps
		200MHz 25MHz Xtal input, 12kHz - 20MHz		0.3	0.5	ps
$J_{RMS2.0}$	PCIe 2.0 RMS Jitter	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps
$J_{RMS3.0}$	PCIe 3.0 RMS Jitter	PLL L-BW @ 2M & 5M 1st H3		1.42	3	ps
		PLL L-BW @ 2M & 4M 1st H3		2.05	3	ps
		PLL H-BW @ 2M & 5M 1st H3		0.45	1	ps
		PLL H-BW @ 2M & 4M 1st H3		0.45	1	ps
$J_{RMS4.0}$	PCIe 4.0 RMS Jitter	PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)		0.37	0.45	ps
t_{OR}	Rise Time(1,2)	From 0.175V to 0.525V	175		700	ps
t_{OF}	Fall Time(1,2)	From 0.525V to 0.175V	175		700	ps
t_{RF}	Slew Rate	Differential Slew Rate +150mV / -150mV	1.1	2.7	5.5	V/ns
T_{SKEW}	Skew between outputs	At Crossing Point Voltage			25	ps
$T_{DUTY-CYCLE}$	Duty Cycle(1,3)		45		55	%
T_{OE}	Output Enable Time(5)	All outputs			10	µs
T_{OT}	Output Disable Time(5)	All outputs			10	µs
t_{STABLE}	Stabilization Time	From Power-up V_{DD}=3.3V		20		ms

Notes:
1. CL = 2 pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

HCSL Output AC Characteristics (V_{DD} = 2.5V ±5%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{IN}	Input Frequency			25		MHz
F_{OUT}	Output Frequency		100		200	MHz
V_{OH}	Output High Voltage (1,2)	100 MHz HCSL output @ V_{DD} = 2.5V	660	800	900	mV
V_{OL}	Output Low Voltage(1,2)	100 MHz HCSL output @ V_{DD} = 2.5V	-150	0		mV
V_{CPA}	Crossing Point Voltage(1,2)	Absolute @100MHz	250	350	550	mV
V_{CN}	Crossing Point Voltage(1,2,4)	Variation over all edges@100MHz			140	mV
J_{CC}	Jitter, Cycle-to-Cycle(1,3)			35	60	ps
J_{Period}	Period jitter			26	40	ps
J_{Phase}	RMS Phase Jitter, (Random)	100MHz 25MHz Xtal input, 12kHz - 20MHz		0.32	0.5	ps
		125MHz 25MHz Xtal input, 12kHz - 20MHz		0.3	0.5	ps
		156.25MHz 25MHz Xtal input, 12kHz - 20MHz		0.3	0.5	ps
		200MHz 25MHz Xtal input, 12kHz - 20MHz		0.3	0.5	ps
$J_{RMS2.0}$	PCIe 2.0 RMS Jitter	PCIe 2.0 Test Method @ 100MHz Output			3.1	ps
$J_{RMS3.0}$	PCIe 3.0 RMS Jitter	PLL L-BW @ 2M & 5M 1st H3		1.42	3	ps
		PLL L-BW @ 2M & 4M 1st H3		2.05	3	ps
		PLL H-BW @ 2M & 5M 1st H3		0.45	1	ps
		PLL H-BW @ 2M & 4M 1st H3		0.45	1	ps
$J_{RMS4.0}$	PCIe 4.0 RMS Jitter	PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)		0.37	0.45	ps
t_{OR}	Rise Time(1,2)	From 0.175V to 0.525V	175		700	ps
t_{OF}	Fall Time(1,2)	From 0.525V to 0.175V	175		700	ps
t_{RF}	Slew Rate	Differential Slew Rate +150mV / -150mV	1.1	2.7	5.5	V/ns
T_{SKEW}	Skew between outputs	At Crossing Point Voltage			25	ps
$T_{DUTY-CYCLE}$	Duty Cycle(1,3)		45		55	%
T_{OE}	Output Enable Time(5)	All outputs			10	µs
T_{OT}	Output Disable Time(5)	All outputs			10	µs
t_{STABLE}	Stabilization Time	From Power-up V_{DD}=2.5V		20		ms

Notes:
1. CL = 2 pF
2. Single-ended waveform
3. Differential waveform
4. Measured at the crossing point
5. CLK pins are tri-stated when OE is LOW

Application Information

Decoupling Capacitors

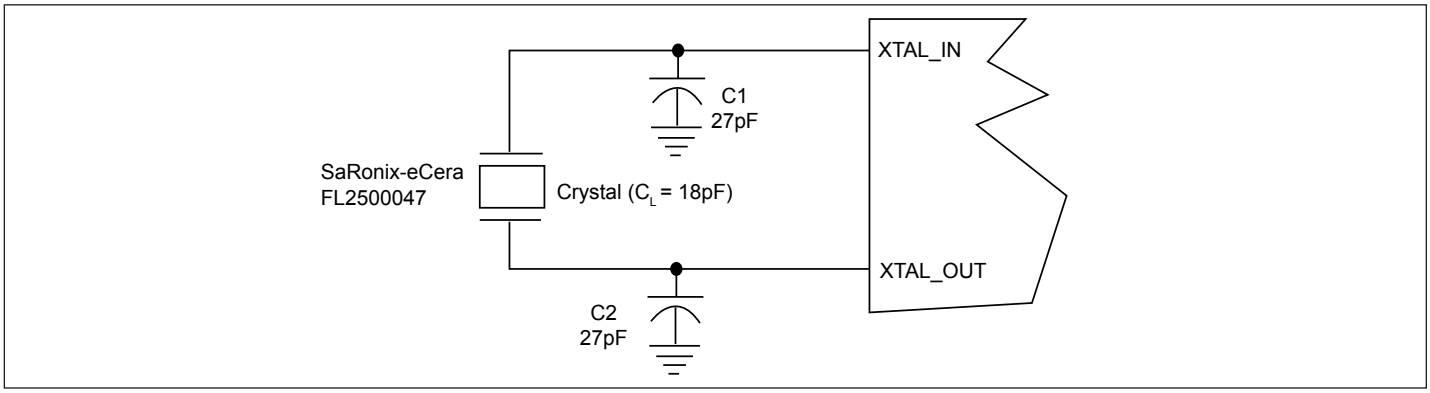
Decoupling capacitors of 0.01µF should be connected between each V_{DD} pin and the ground plane and placed as close to the V_{DD} pin as possible.

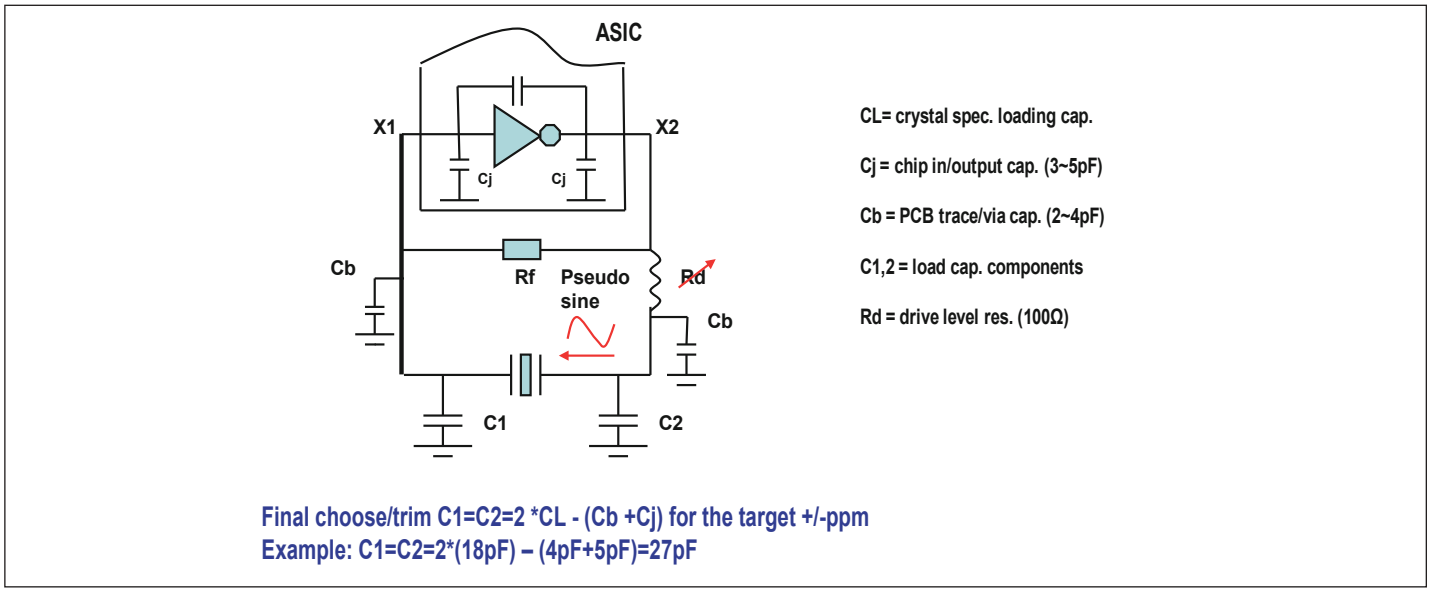
Crystal

Use a 25MHz fundamental mode parallel resonant crystal with less than 300PPM of error across temperature.

Crystal Circuit Connection

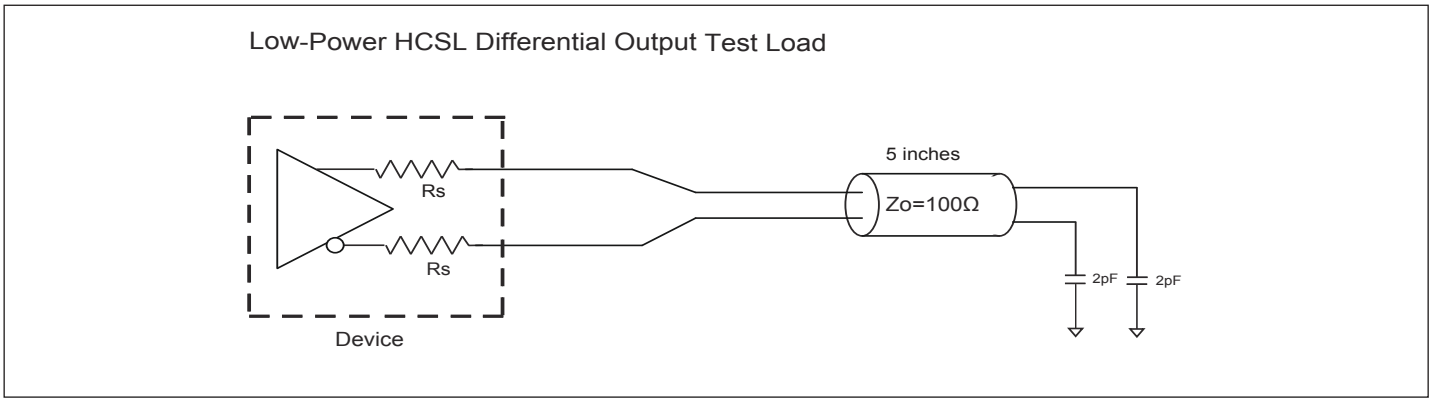
The following diagram shows crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 27pF, C2= 27pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.



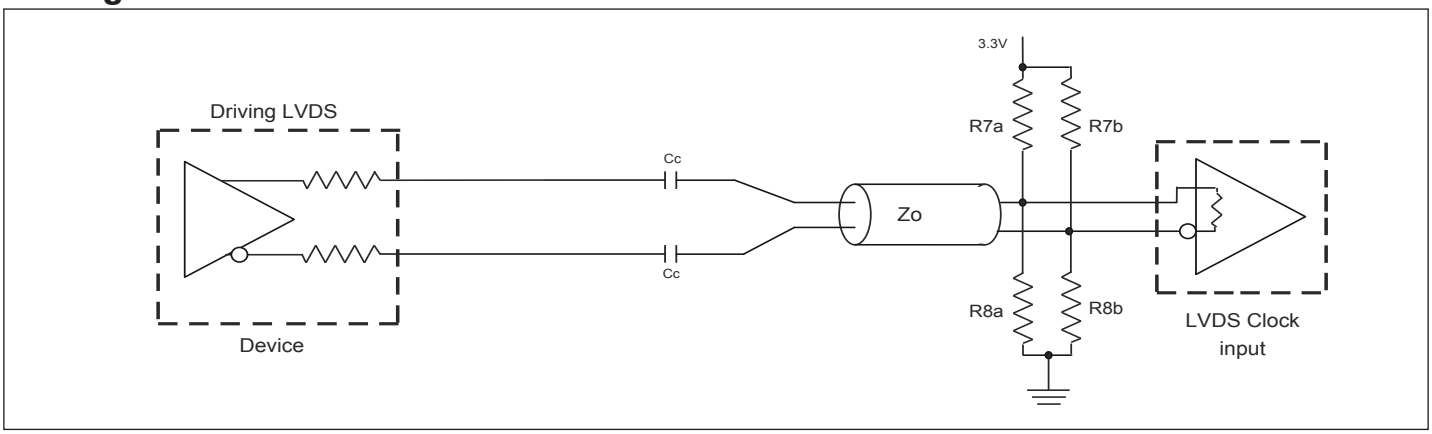


Final choose/trim C1=C2=2 *CL - (Cb +Cj) for the target +/-ppm
Example: C1=C2=2*(18pF) – (4pF+5pF)=27pF

Test Loads



Driving LVDS



Driving LVDS Inputs

Component	Value	
	Receiver has termination	Receiver does not have termination
R7a, R7b	10K Ω	140 Ω
R8a, R8b	5.6K Ω	75 Ω
Cc	0.1 uF	0.1 uF
Vcm	1.2 volts	1.2 volts

Thermal Characteristics

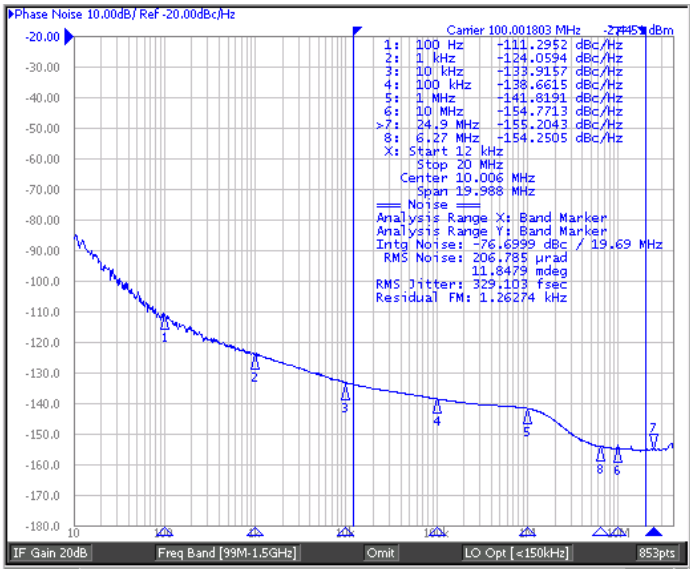
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
θ_{JA}	Thermal Resistance Junction to Ambient	Still air			84	°C/W
θ_{JC}	Thermal Resistance Junction to Case				17	°C/W

Recomended Crystal Specification

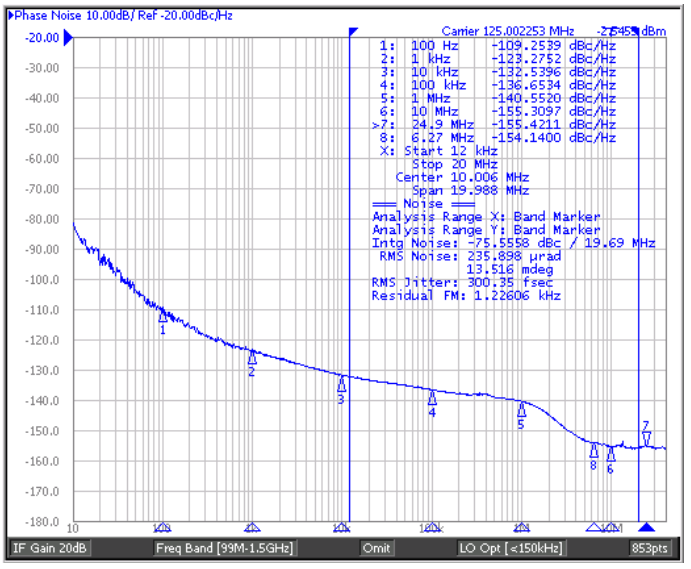
Pericom recommends:
a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm
b) FY2500107, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm
c) FL2500038, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm

Phase Noise Plot

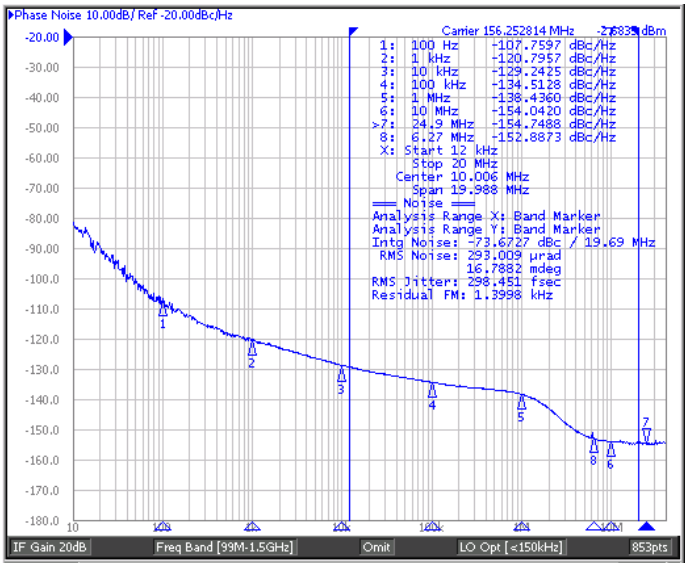
100MHz



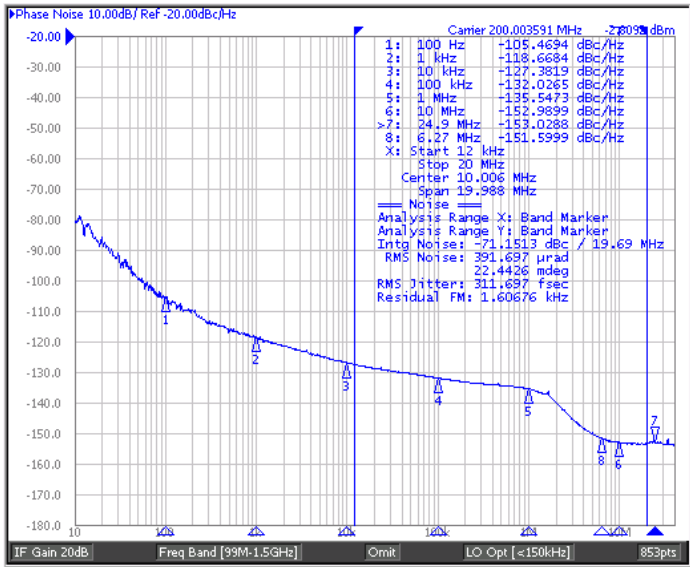
125MHz



156.25MHz

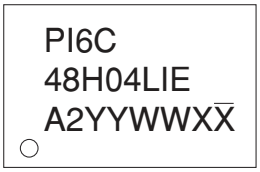


200MHz



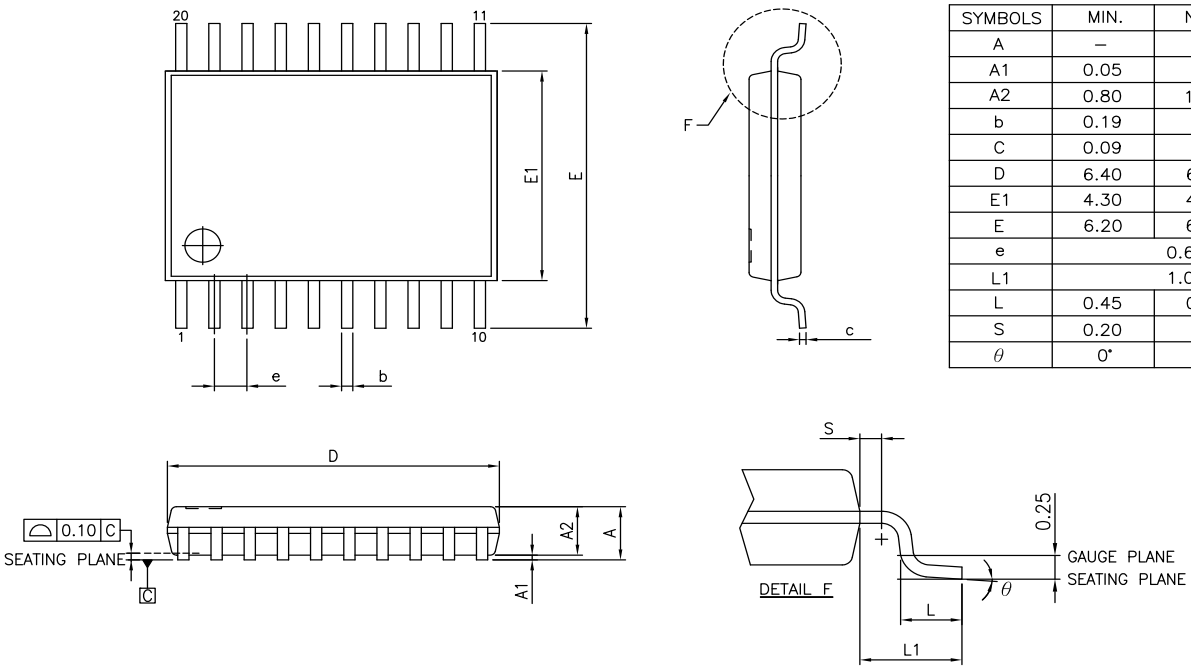
Part Marking

L Package



A2: BD Option
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Site Code

Packaging Mechanical: 20-TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO–153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

DATE: 03/31/16

DESCRIPTION: 20-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L20)

DOCUMENT CONTROL #: PD-1311 REVISION: G

16-0074

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description	Operating Temperature
PI6LC48H04LIEX	L	20-Pin, 173mil Wide (TSSOP)	Industrial

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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