

## LM148JAN Quad 741 Op Amps

 Check for Samples: [LM148JAN](#)

### FEATURES

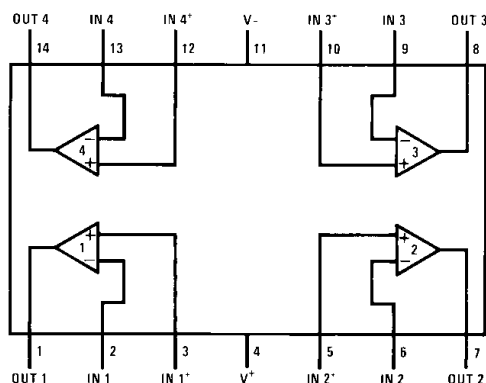
- 741 Op Amp Operating Characteristics
- Class AB Output Stage—No Crossover Distortion
- Pin Compatible with the LM124
- Overload Protection for Inputs and Outputs
- Low Supply Current Drain: 0.6 mA/Amplifier
- Low Input Offset Voltage: 1 mV
- Low Input Offset Current: 4 nA
- Low Input Bias Current 30 nA
- High Degree of Isolation between Amplifiers: 120 dB
- Gain Bandwidth Product (Unity Gain): 1.0 MHz

### DESCRIPTION

The LM148 is a true quad LM741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar LM741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single LM741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard LM741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple LM741 or LM1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

### Connection Diagram



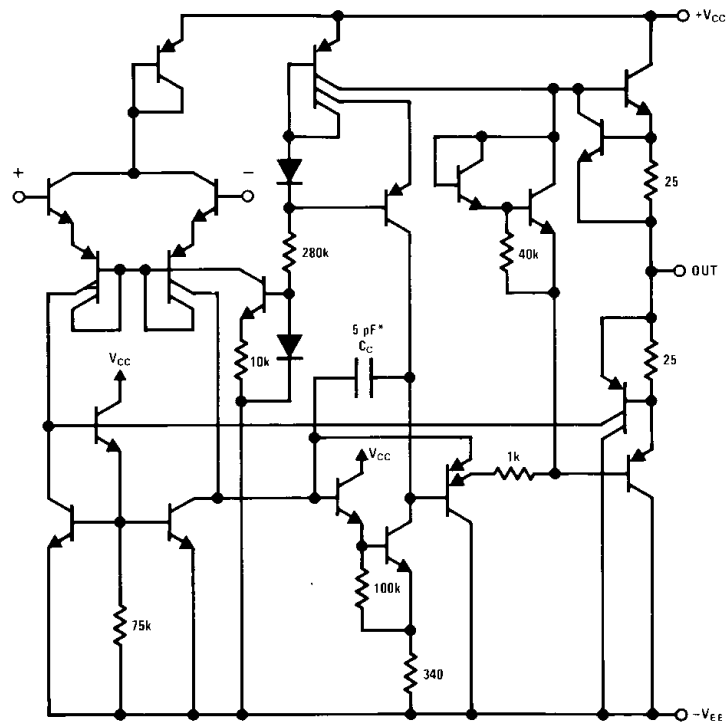
**Figure 1. Top View**  
See Package Number J0014A, NAD0014B, NAC0014A



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## Schematic Diagram



\* 1 pF in the LM149



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage		±22V	
Input Voltage Range		±20V	
Input Current Range		-0.1mA to 10mA	
Differential Input Voltage <sup>(2)</sup>		±30V	
Output Short Circuit Duration <sup>(3)</sup>		Continuous	
Power Dissipation ( $P_d$ at 25°C) <sup>(4)</sup>		CDIP	400mW
		CLGA (NAD0014B)	350mW
Thermal Resistance	$\theta_{JA}$	CDIP (Still Air)	103°C/W
		CDIP (500LF/ Min Air flow)	52°C/W
		CLGA (NAD0014B) (Still Air)	140°C/W
		CLGA (NAD0014B) (500LF/ Min Air flow)	100°C/W
	$\theta_{JC}$	CLGA (NAC0014A) (Still Air)	176°C/W
		CLGA (NAC0014A) (500LF/ Min Air flow)	116°C/W
		CDIP	19°C/W
		CLGA (NAD0014B)	25°C/W
Package Weight (typical)		CLGA (NAC0014A)	25°C/W
	CDIP		TBD
	CLGA (NAD0014B)		465mg
		CLGA (NAC0014A)	415mg
Maximum Junction Temperature ( $T_{JMAX}$ )		175°C	
Operating Temperature Range		-55°C ≤ $T_A$ ≤ +125°C	
Storage Temperature Range		-65°C ≤ $T_A$ ≤ +150°C	
Lead Temperature (Soldering, 10 sec.) Ceramic		300°C	
ESD tolerance <sup>(5)</sup>		500V	

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) The differential input voltage range shall not exceed the supply voltage range.
- (3) Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
- (4) The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum available power dissipation at any temperature is  $P_d = (T_{JMAX} - T_A)/\theta_{JA}$  or the number given in the Absolute Maximum Ratings, whichever is less.
- (5) Human body model, 1.5 kΩ in series with 100 pF.

**Quality Conformance Inspection**

MIL-STD-883, Method 5005 — Group A

Subgroup	Description	Temp ( °C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25

## Quality Conformance Inspection (continued)

MIL-STD-883, Method 5005 — Group A

Subgroup	Description	Temp ( °C)
10	Switching tests at	+125
11	Switching tests at	-55

## Electrical Characteristics

DC PARAMETERS (The following conditions apply to all parameters, unless otherwise specified.)

 $\pm V_{CC} = \pm 20V$ ,  $V_{CM} = 0V$ , measure each amplifier.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
$V_{IO}$	Input Offset Voltage	$+V_{CC} = 35V$ , $-V_{CC} = -5V$ , $V_{CM} = -15V$		-5.0	+5.0	mV	1
				-6.0	+6.0	mV	2, 3
		$+V_{CC} = 5V$ , $-V_{CC} = -35V$ , $V_{CM} = +15V$		-5.0	+5.0	mV	1
				-6.0	+6.0	mV	2, 3
		$+V_{CC} = 5V$ , $-V_{CC} = -5V$ ,		-5.0	+5.0	mV	1
				-6.0	+6.0	mV	2, 3
Delta $V_{IO}$ / Delta $T$	Input Offset Voltage Temperature Stability	$25^{\circ}C \leq T_A \leq 125^{\circ}C$	See <sup>(1)</sup>	-25	25	$\mu V/^{\circ}C$	2
		$-55^{\circ}C \leq T_A \leq 25^{\circ}C$	See <sup>(1)</sup>	-25	25	$\mu V/^{\circ}C$	3
$I_{IO}$	Input Offset Current	$+V_{CC} = 35V$ , $-V_{CC} = -5V$ , $V_{CM} = -15V$		-25	+25	nA	1, 2
				-75	+75	nA	3
		$+V_{CC} = 5V$ , $-V_{CC} = -35V$ , $V_{CM} = +15V$		-25	+25	nA	1, 2
				-75	+75	nA	3
		$+V_{CC} = 5V$ , $-V_{CC} = -5V$ ,		-25	+25	nA	1, 2
				-75	+75	nA	3
Delta $I_{IO}$ / Delta $T$	Input Offset Current Temperature Stability	$25^{\circ}C \leq T_A \leq 125^{\circ}C$	See <sup>(1)</sup>	-200	200	$\mu A/^{\circ}C$	2
		$-55^{\circ}C \leq T_A \leq 25^{\circ}C$	See <sup>(1)</sup>	-400	400	$\mu A/^{\circ}C$	3
$\pm I_{IB}$	Input Bias Current	$+V_{CC} = 35V$ , $-V_{CC} = -5V$ , $V_{CM} = -15V$		-0.1	100	nA	1, 2
				-0.1	325	nA	3
		$+V_{CC} = 5V$ , $-V_{CC} = -35V$ , $V_{CM} = +15V$		-0.1	100	nA	1, 2
				-0.1	325	nA	3
		$+V_{CC} = 5V$ , $-V_{CC} = -5V$ ,		-0.1	100	nA	1, 2
				-0.1	325	nA	3
PSRR+	Power Supply Rejection Ratio	$-V_{CC} = -20V$ , $+V_{CC} = 20V$ to $10V$	See <sup>(2)</sup>	-100	100	$\mu V/V$	1, 2, 3
PSRR-	Power Supply Rejection Ratio	$+V_{CC} = 20V$ , $-V_{CC} = -20V$ to $-10V$	See <sup>(2)</sup>	-100	100	$\mu V/V$	1, 2, 3
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 15V$ , $\pm 5V \leq V_{CC} \leq \pm 35V$		76		dB	1, 2, 3

(1) Calculated parameter.

(2) Datalogs as  $\mu V$

## Electrical Characteristics

AC / DC PARAMETERS (The following conditions apply to all parameters, unless otherwise specified.)

$\pm V_{CC} = \pm 20V$ ,  $V_{CM} = 0V$ , measure each amplifier.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
+ I <sub>OS</sub>	Short Circuit Current	+V <sub>CC</sub> = 15V, -V <sub>CC</sub> = -15V, V <sub>CM</sub> = -10V		-55		mA	1, 2
				-75		mA	3
- I <sub>OS</sub>	Short Circuit Current	+V <sub>CC</sub> = 15V, -V <sub>CC</sub> = -15V, V <sub>CM</sub> = +10V			55	mA	1, 2
					75	mA	3
I <sub>CC</sub>	Power Supply Current	+V <sub>CC</sub> = 15V, -V <sub>CC</sub> = -15V			3.6	mA	1
					4.5	mA	2, 3
-A <sub>VS</sub>	Open Loop Voltage Gain	V <sub>OUT</sub> = -15V, R <sub>L</sub> = 10KΩ		50		V/mV	4
				25		V/mV	5, 6
		V <sub>OUT</sub> = -15V, R <sub>L</sub> = 2KΩ		50		V/mV	4
				25		V/mV	5, 6
+A <sub>VS</sub>	Open Loop Voltage Gain	V <sub>OUT</sub> = +15V, R <sub>L</sub> = 10KΩ		50		V/mV	4
				25		V/mV	5, 6
		V <sub>OUT</sub> = +15V, R <sub>L</sub> = 2KΩ		50		V/mV	4
				25		V/mV	5, 6
A <sub>VS</sub>	Open Loop Voltage Gain	V <sub>CC</sub> = ±5V, V <sub>OUT</sub> = ±2V, R <sub>L</sub> = 10KΩ		10		V/mV	4, 5, 6
		V <sub>CC</sub> = ±5V, V <sub>OUT</sub> = ±2V, R <sub>L</sub> = 2KΩ		10		V/mV	4, 5, 6
+V <sub>OP</sub>	Output Voltage Swing	R <sub>L</sub> = 10KΩ		+16		V	4, 5, 6
		R <sub>L</sub> = 2KΩ		+15		V	4, 5, 6
-V <sub>OP</sub>	Output Voltage Swing	R <sub>L</sub> = 10KΩ			-16	V	4, 5, 6
		R <sub>L</sub> = 2KΩ			-15	V	4, 5, 6
TR <sub>TR</sub>	Transient Response Time	V <sub>IN</sub> = 50mV, A <sub>V</sub> = 1			1	μS	7, 8A, 8B
TR <sub>OS</sub>	Transient Response Time	V <sub>IN</sub> = 50mV, A <sub>V</sub> = 1			25	%	7, 8A, 8B
±SR	Slew Rate	V <sub>IN</sub> = -5V to +5V, A <sub>V</sub> = 1		0.2		V/μS	7, 8A, 8B
		V <sub>IN</sub> = +5V to -5V, A <sub>V</sub> = 1		0.2		V/μS	7, 8A, 8B

## Electrical Characteristics

AC PARAMETERS (The following conditions apply to all parameters, unless otherwise specified.)

$\pm V_{CC} = \pm 20V$ ,  $V_{CM} = 0V$ , measure each amplifier.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
NI <sub>BB</sub>	Noise (Broadband)	BW = 10Hz to 5KHz			15	μV <sub>RMS</sub>	7
NI <sub>PC</sub>	Noise (Popcorn)	R <sub>S</sub> = 20KΩ			40	μV <sub>PK</sub>	7
C <sub>S</sub>	Channel Separation	V <sub>IN</sub> = ±10V, A to B, R <sub>L</sub> = 2KΩ		80		dB	7
		V <sub>IN</sub> = ±10V, A to C, R <sub>L</sub> = 2KΩ		80		dB	7
		V <sub>IN</sub> = ±10V, A to D, R <sub>L</sub> = 2KΩ		80		dB	7
		V <sub>IN</sub> = ±10V, B to A, R <sub>L</sub> = 2KΩ		80		dB	7
		V <sub>IN</sub> = ±10V, B to C, R <sub>L</sub> = 2KΩ		80		dB	7
		V <sub>IN</sub> = ±10V, B to D, R <sub>L</sub> = 2KΩ		80		dB	7
		V <sub>IN</sub> = ±10V, C to A, R <sub>L</sub> = 2KΩ		80		dB	7
		V <sub>IN</sub> = ±10V, C to B, R <sub>L</sub> = 2KΩ		80		dB	7
		V <sub>IN</sub> = ±10V, C to D, R <sub>L</sub> = 2KΩ		80		dB	7
		V <sub>IN</sub> = ±10V, D to A, R <sub>L</sub> = 2KΩ		80		dB	7
		V <sub>IN</sub> = ±10V, D to B, R <sub>L</sub> = 2KΩ		80		dB	7
		V <sub>IN</sub> = ±10V, D to C, R <sub>L</sub> = 2KΩ		80		dB	7

### Electrical Characteristics

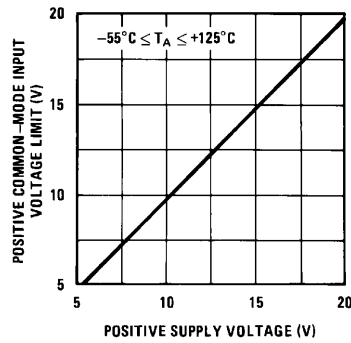
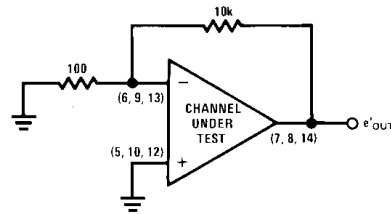
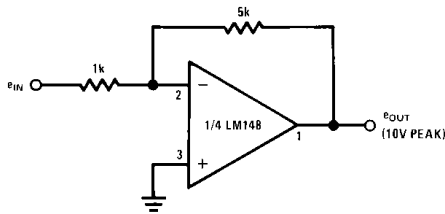
DC DRIFT PARAMETERS (The following conditions apply to all parameters, unless otherwise specified.)

$\pm V_{CC} = \pm 20V$ ,  $V_{CM} = 0V$ , measure each amplifier. Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
$V_{IO}$	Input Offset Voltage			-1	1	mV	1
$\pm I_{IB}$	Input Bias Current			-15	15	nA	1

### Cross Talk Test Circuit

$V_S = \pm 15V$



Typical Performance Characteristics

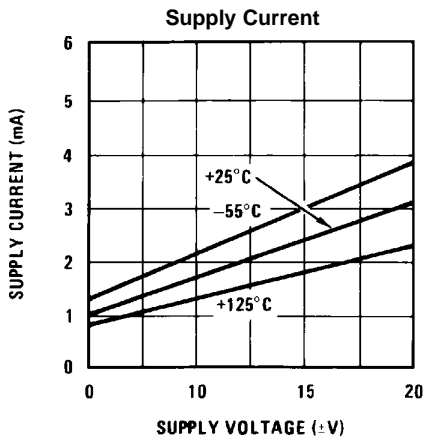


Figure 2.

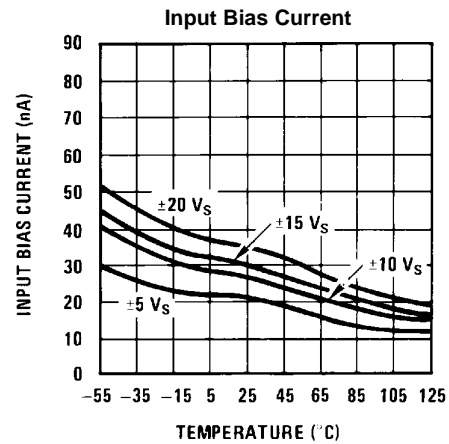


Figure 3.

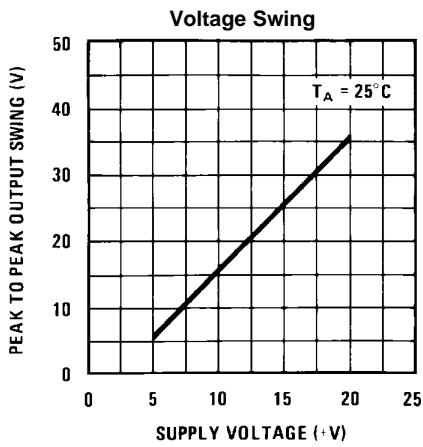


Figure 4.

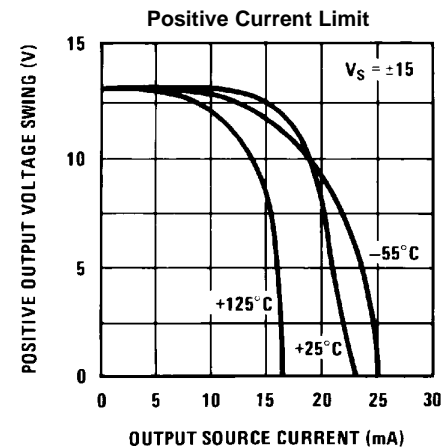


Figure 5.

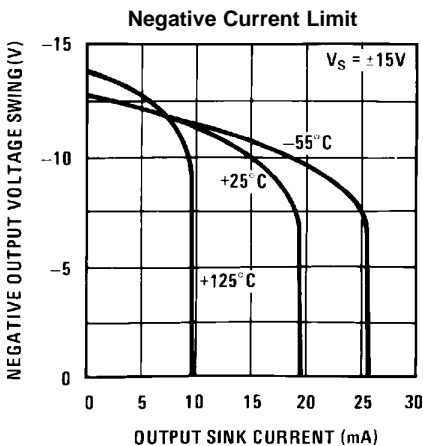


Figure 6.

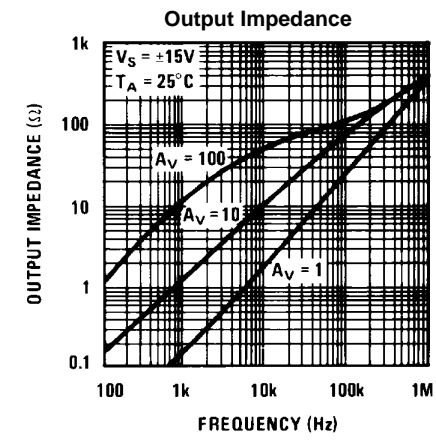


Figure 7.

Typical Performance Characteristics (continued)

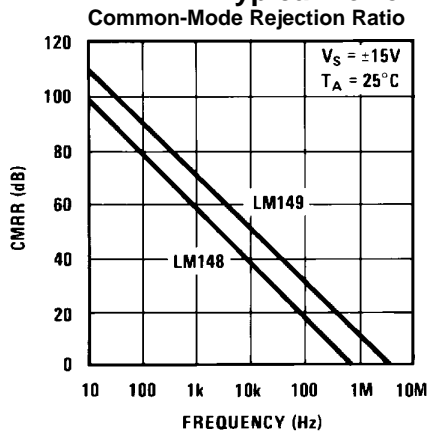


Figure 8.

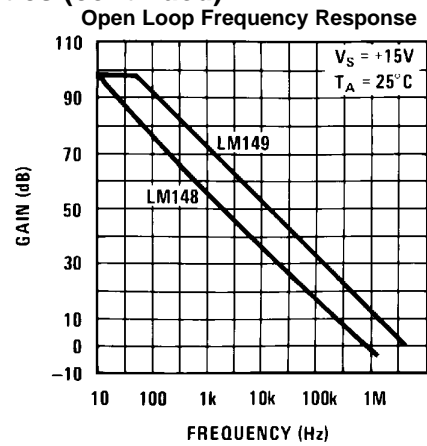


Figure 9.

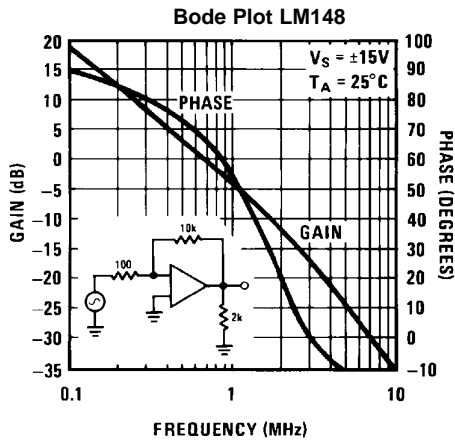


Figure 10.

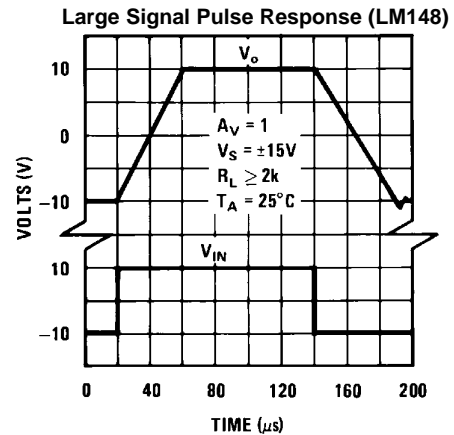


Figure 11.

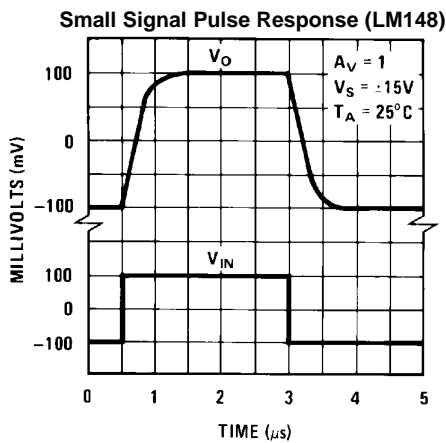


Figure 12.

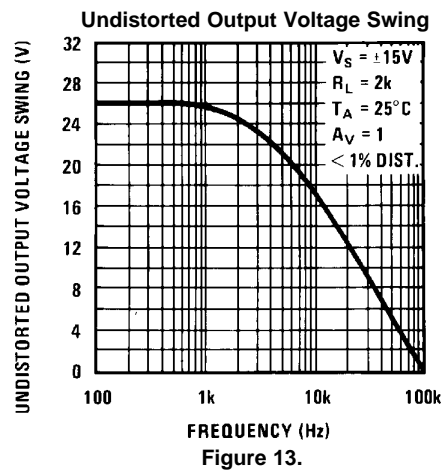


Figure 13.



Typical Performance Characteristics (continued)

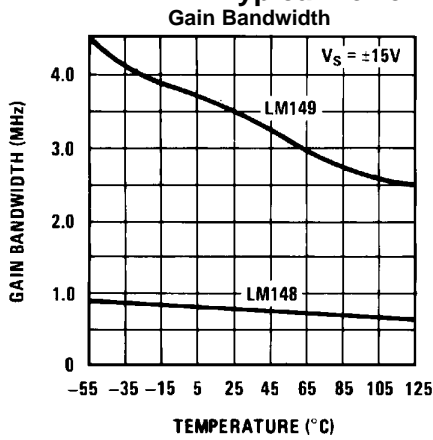


Figure 14.

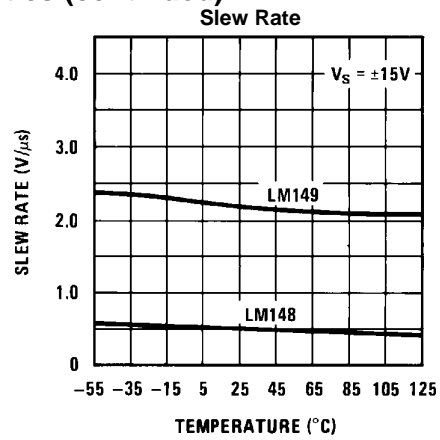


Figure 15.

Inverting Large Signal Pulse Response (LM148)

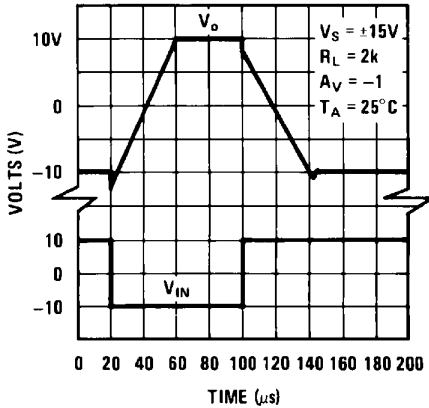


Figure 16.

Input Noise Voltage and Noise Current

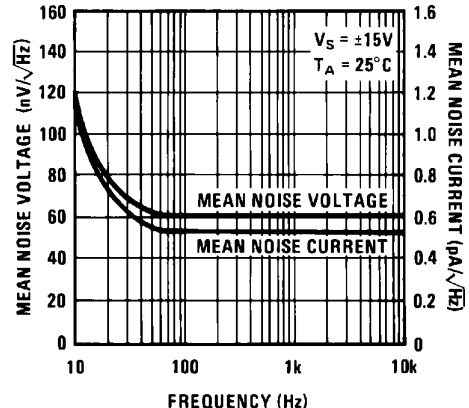


Figure 17.

Positive Common-Mode Input Voltage Limit

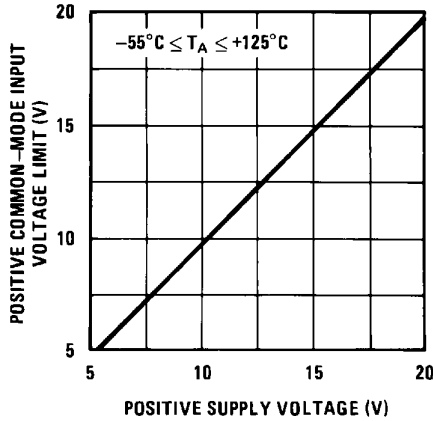


Figure 18.

Negative Common-Mode Input Voltage Limit

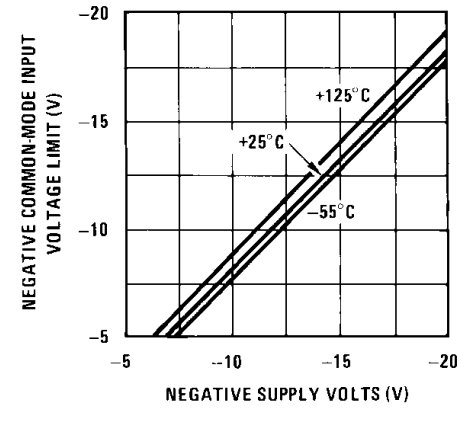


Figure 19.

## APPLICATION HINTS

The LM148 series are quad low power LM741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the LM741 op amp. In those applications where LM741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

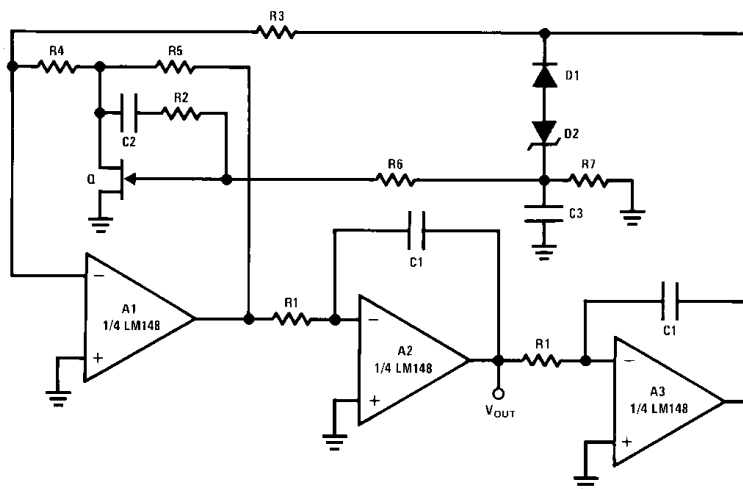
Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications—LM148



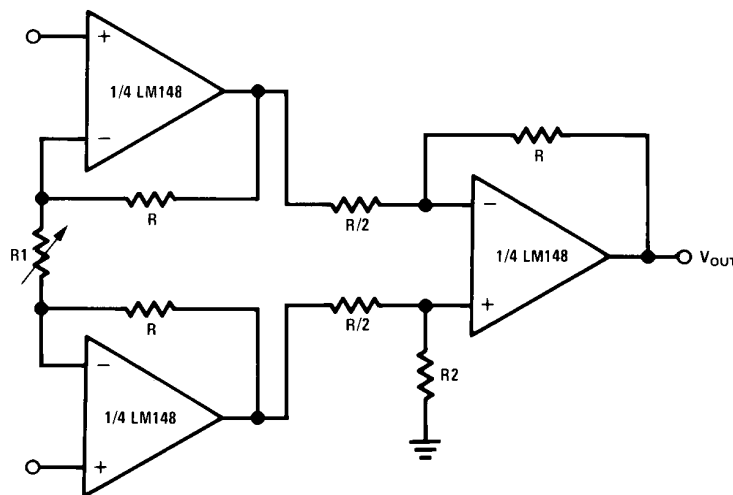
$$f = \frac{1}{2\pi R_1 C_1} \times \sqrt{K}, K = \frac{R_4 R_5}{R_3} \left( \frac{1}{r_{DS}} + \frac{1}{R_4} + \frac{1}{R_5} \right), r_{DS} \approx \frac{R_{ON}}{\left( 1 - \frac{V_{GS}}{V_P} \right)^{1/2}}$$

$f_{MAX} = 5 \text{ kHz}$ , THD  $\leq 0.03\%$

$R_1 = 100\text{k pot}$ ,  $C_1 = 0.0047 \mu\text{F}$ ,  $C_2 = 0.01 \mu\text{F}$ ,  $C_3 = 0.1 \mu\text{F}$ ,  $R_2 = R_6 = R_7 = 1\text{M}$ ,  
 $R_3 = 5.1\text{k}$ ,  $R_4 = 12\Omega$ ,  $R_5 = 240\Omega$ ,  $Q = \text{NS5102}$ ,  $D_1 = 1\text{N914}$ ,  $D_2 = 3.6\text{V avalanche diode (ex. LM103)}$ ,  $V_S = \pm 15\text{V}$

A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

Figure 20. One Decade Low Distortion Sine Wave Generator

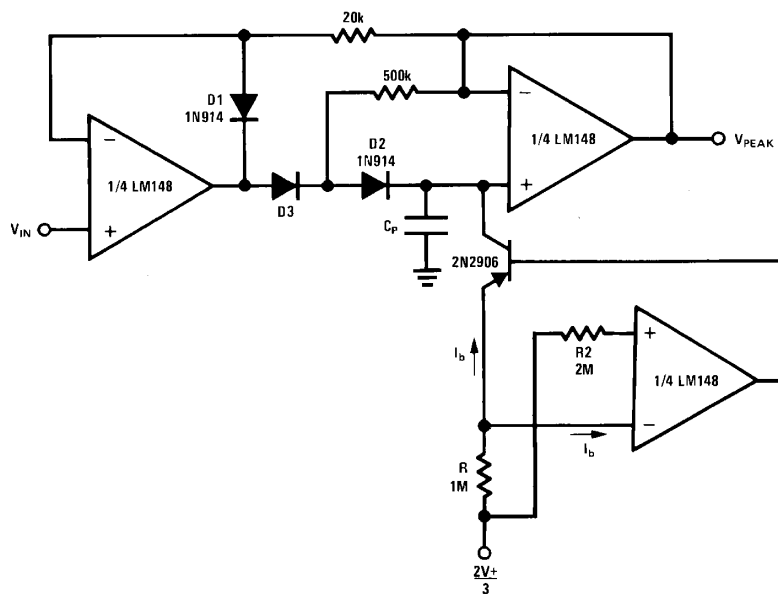


$$V_{OUT} = 2 \left( \frac{2R}{R_1} + 1 \right) \cdot V_S - 3V \leq V_{IN CM} < V_S^+ - 3V,$$

$V_S = \pm 15\text{V}$

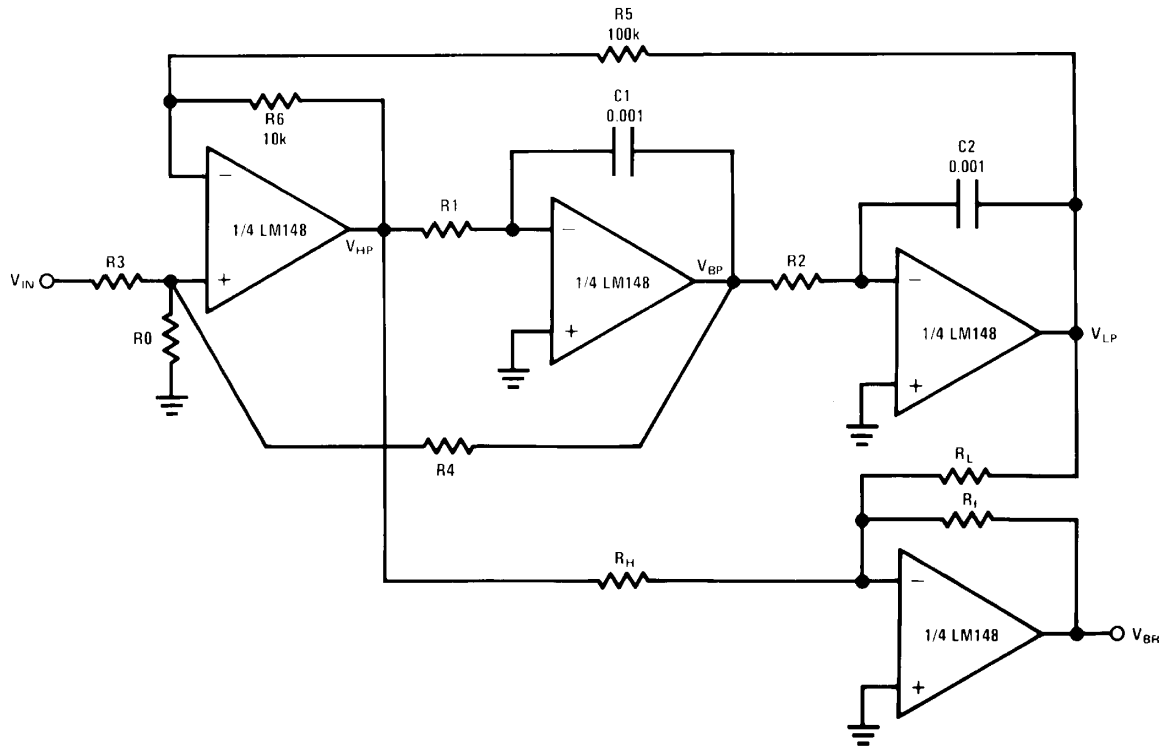
$R = R_2$ , trim  $R_2$  to boost CMRR

Figure 21. Low Cost Instrumentation Amplifier



Adjust R for minimum drift  
 D3 low leakage diode  
 D1 added to improve speed  
 $V_S = \pm 15V$

**Figure 22. Low Drift Peak Detector with Bias Current Compensation**



Tune Q through R0,  
For predictable results:  $f_0 Q \leq 4 \times 10^4$   
Use Band Pass output to tune for Q

$$\frac{V(s)}{V_{IN}(s)} = \frac{N(s)}{D(s)}, D(s) = s^2 + \frac{s\omega_0}{Q} + \omega_0^2$$

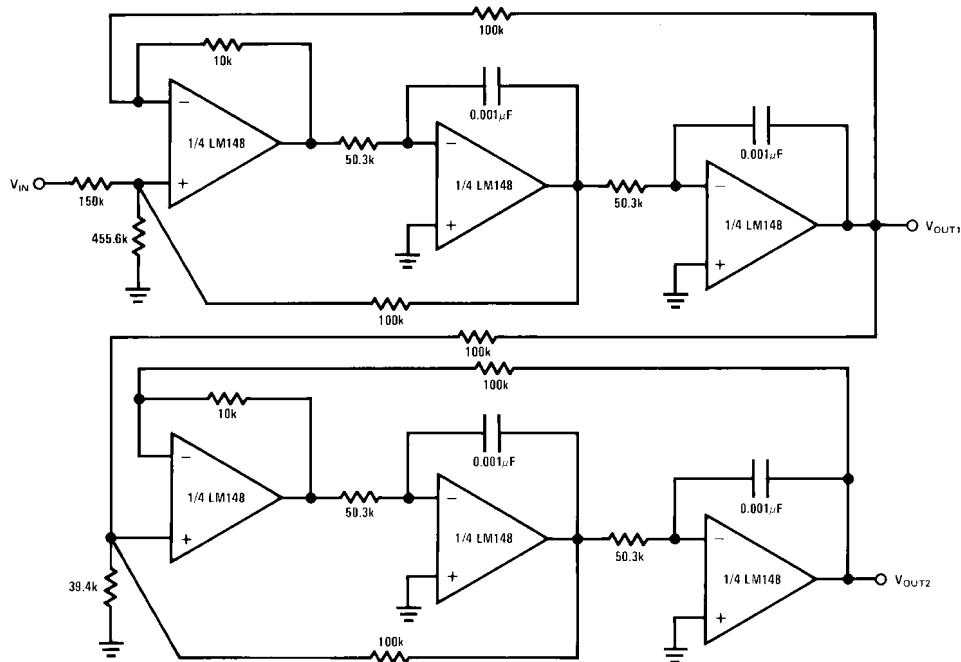
$$N_{HP}(s) = s^2 H_{OHP}, N_{BP}(s) = \frac{s\omega_0 H_{OBP}}{Q}, N_{LP} = \omega_0^2 H_{OLP}$$

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{R6}{R5} \frac{1}{t_1 t_2}}, t_1 = R_1 C_1, Q = \left( \frac{1 + R4|R3 + R4|R0}{1 + R6|R5} \right) \left( \frac{R6 t_1}{R5 t_2} \right)^{1/2}$$

$$f_{NOTCH} = \frac{1}{2\pi} \left( \frac{R_H}{R_L t_1 t_2} \right)^{1/2}, H_{OHP} = \frac{1 + R6|R5}{1 + R3|R0 + R3|R4}, H_{OBP} = \frac{1 + R4|R3 + R4|R0}{1 + R3|R0 + R3|R4}$$

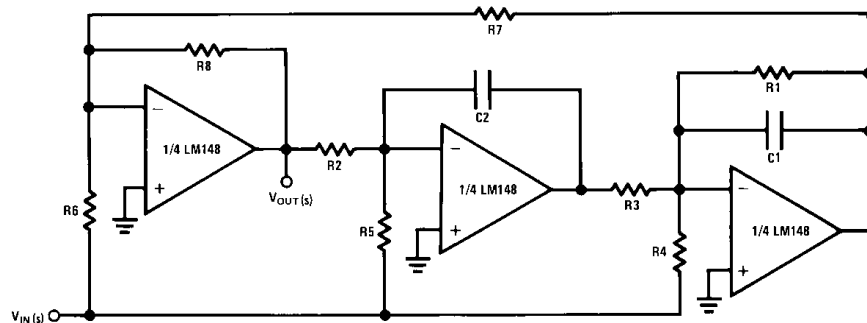
$$H_{OLP} = \frac{1 + R5|R6}{1 + R3|R0 + R3|R4}$$

Figure 23. Universal State-Variable Filter



Use general equations, and tune each section separately  
 $Q_{1stSECTION} = 0.541$ ,  $Q_{2ndSECTION} = 1.306$   
 The response should have 0 dB peaking

Figure 24. A 1 kHz 4 Pole Butterworth

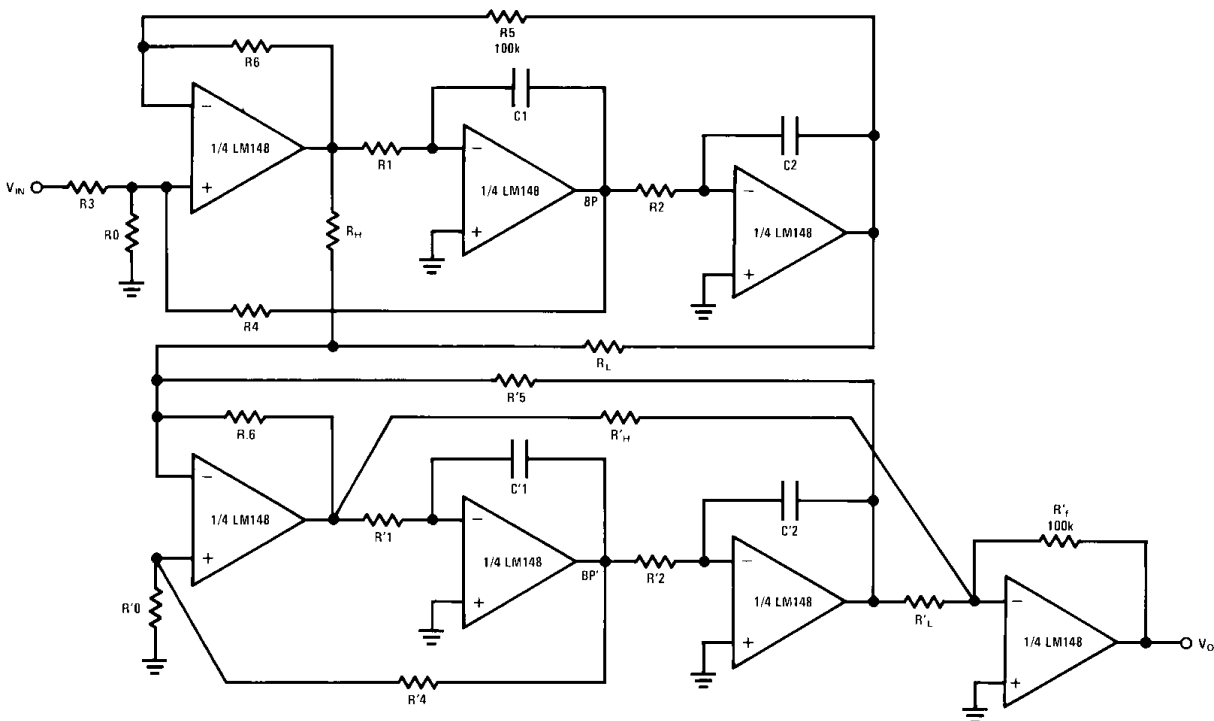


$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}}, \quad f_o = \frac{1}{2\pi} \sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}}, \quad f_{NOTCH} = \frac{1}{2\pi} \sqrt{\frac{R6}{R3R5R7C1C2}}$$

Necessary condition for notch:  $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex:  $f_{NOTCH} = 3$  kHz,  $Q = 5$ ,  $R1 = 270k$ ,  $R2 = R3 = 20k$ ,  $R4 = 27k$ ,  $R5 = 20k$ ,  $R6 = R8 = 10k$ ,  $R7 = 100k$ ,  $C1 = C2 = 0.001 \mu F$   
 Better noise performance than the state-space approach.

Figure 25. A 3 Amplifier Bi-Quad Notch Filter

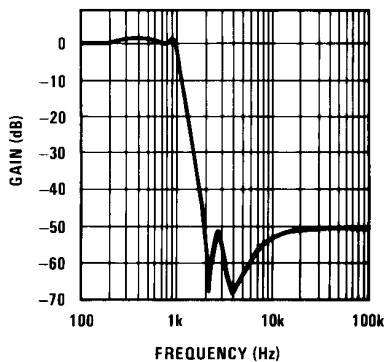


$R1C1 = R2C2 = t$   
 $R'1C'1 = R'2C'2 = t'$   
 $f_c = 1 \text{ kHz}$ ,  $f_s = 2 \text{ kHz}$ ,  $f_p = 0.543$ ,  $f_z = 2.14$ ,  $Q = 0.841$ ,  $f'_p = 0.987$ ,  $f'_z = 4.92$ ,  $Q' = 4.403$ , normalized to ripple BW

$$f = \frac{1}{2\pi R1C1} \times \sqrt{K}, K = \frac{R4R5}{R3} \left( \frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5} \right), r_{DS} \approx \frac{R_{ON}}{\left( 1 - \frac{V_{GS}}{V_P} \right)^{1/2}}$$

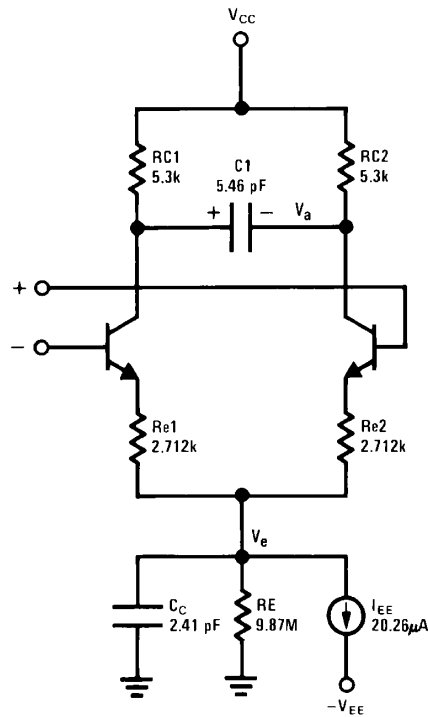
Use the BP outputs to tune Q, Q', tune the 2 sections separately  
 $R1 = R2 = 92.6k$ ,  $R3 = R4 = R5 = 100k$ ,  $R6 = 10k$ ,  $R0 = 107.8k$ ,  $R_L = 100k$ ,  $R_H = 155.1k$ ,  
 $R'1 = R'2 = 50.9k$ ,  $R'4 = R'5 = 100k$ ,  $R'6 = 10k$ ,  $R'0 = 5.78k$ ,  $R'_L = 100k$ ,  $R'_H = 248.12k$ ,  $R'f = 100k$ . All capacitors are  $0.001 \mu F$ .

**Figure 26. A 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)**



**Figure 27. Lowpass Response**

Typical Simulation



For more details, see IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974

$$\alpha_1 = 112I_S = 8 \times 10^{-16}$$

$$\alpha_2 = 144 \cdot C_2 = 6 \text{ pF for LM149}$$

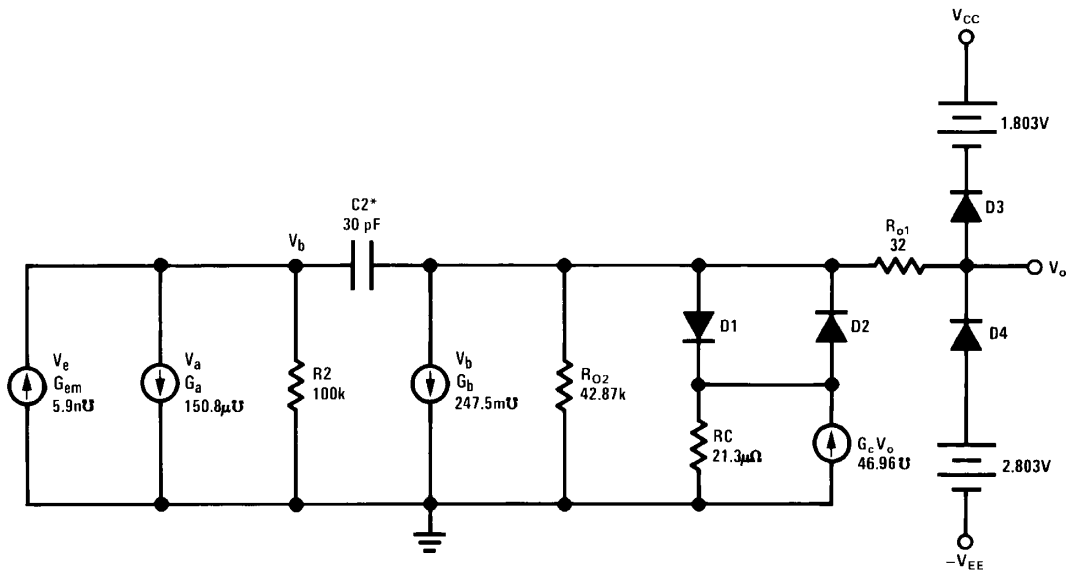


Figure 28. LM148, LM741 Macromodel for Computer Simulation



**REVISION HISTORY SECTION**

<b>Date Released</b>	<b>Revision</b>	<b>Section</b>	<b>Originator</b>	<b>Changes</b>
02/15/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheet converted into one Corp. data sheet format. MJLM148-X, Rev. 0C1. MDS data sheet will be archived.
03/20/13	A	All		Changed layout of National Data Sheet to TI format

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JL148BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	JL148BCA JM38510/11001BCA Q	<a href="#">Samples</a>
JL148SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	JL148SCA JM38510/11001SCA Q	<a href="#">Samples</a>
JM38510/11001BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	JL148BCA JM38510/11001BCA Q	<a href="#">Samples</a>
JM38510/11001SCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	JL148SCA JM38510/11001SCA Q	<a href="#">Samples</a>
M38510/11001BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	JL148BCA JM38510/11001BCA Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF LM148JAN, LM148JAN-SP :**

- Military : [LM148JAN](#)
- Space : [LM148JAN-SP](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

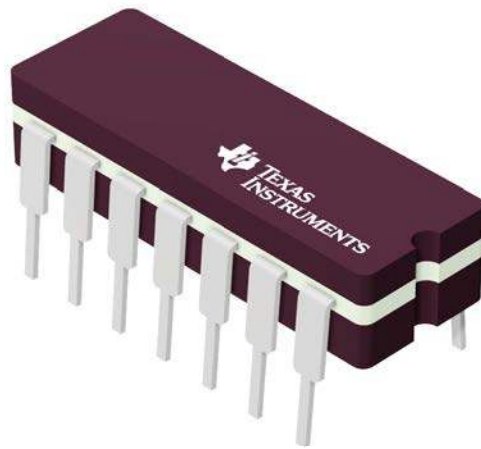
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JL148BCA	J	CDIP	14	25	506.98	15.24	13440	NA
JL148SCA	J	CDIP	14	25	506.98	15.24	13440	NA
JM38510/11001BCA	J	CDIP	14	25	506.98	15.24	13440	NA
JM38510/11001SCA	J	CDIP	14	25	506.98	15.24	13440	NA
M38510/11001BCA	J	CDIP	14	25	506.98	15.24	13440	NA

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

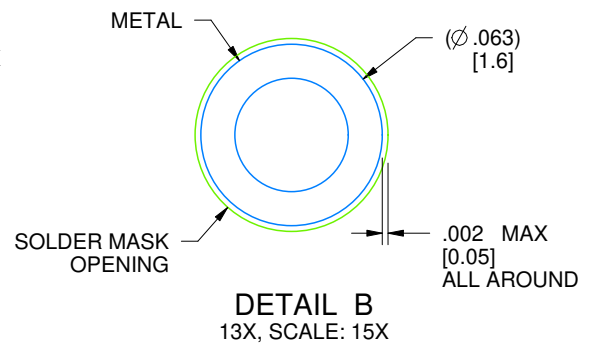
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

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