ZARLINK SEMICONDUCTOR

ZL38015
Voice Processor

Data Sheet

June 2007

A full Design Manual is available to qualified customers. To register, please send an email to VoiceProcessing@Zarlink.com.

Ordering Information

ZL38015QCG1	100 Pin LQFP	Trays, Bake & Drypack

*Pb Free Matte Tin

-40°C to +85°C

Features

- 100 MHz (200 MIPs) Zarlink voice processor with Butterfly hardware accelerator and breakpoint/interrupt controller
- On-board Data (26 Kbytes), Instruction (24 Kbytes RAM and Boot (3 Kbytes) ROM
- 2048 tap Filter co-processor shared across up to 16 separate functions in 128 tap increments
- Primary PCM port supports TDM (ST BUS, GCI or McBSP framing) or SSI modes at bit rates of 128, 256, 512, 1024, 2048, 4096, 8192 or 16384 Kb/sec
- Separate slave (microcontroller) and master (Flash) SPI ports, maximum clock rate = 25 MHz
- Watchdog and 2 auxiliary timers
- 11 General Purpose Input/Output (GPIO) pins
- General purpose UART port
- Bootloadable for future Zarlink software upgrades
- External oscillator or crystal/ceramic resonator
- 1.2 V Core; 3.3 V IO with 5 V-tolerant inputs
- IEEE-1149.1 compatible JTAG port

Applications

- Wireless Local Loop base stations and controllers
- Voice telephony gateways
- Digital, VoIP based and wireless PBX systems
- Echo Canceller pools
- Customer Premise equipment
- Integrated access devices
- SOHO gateways

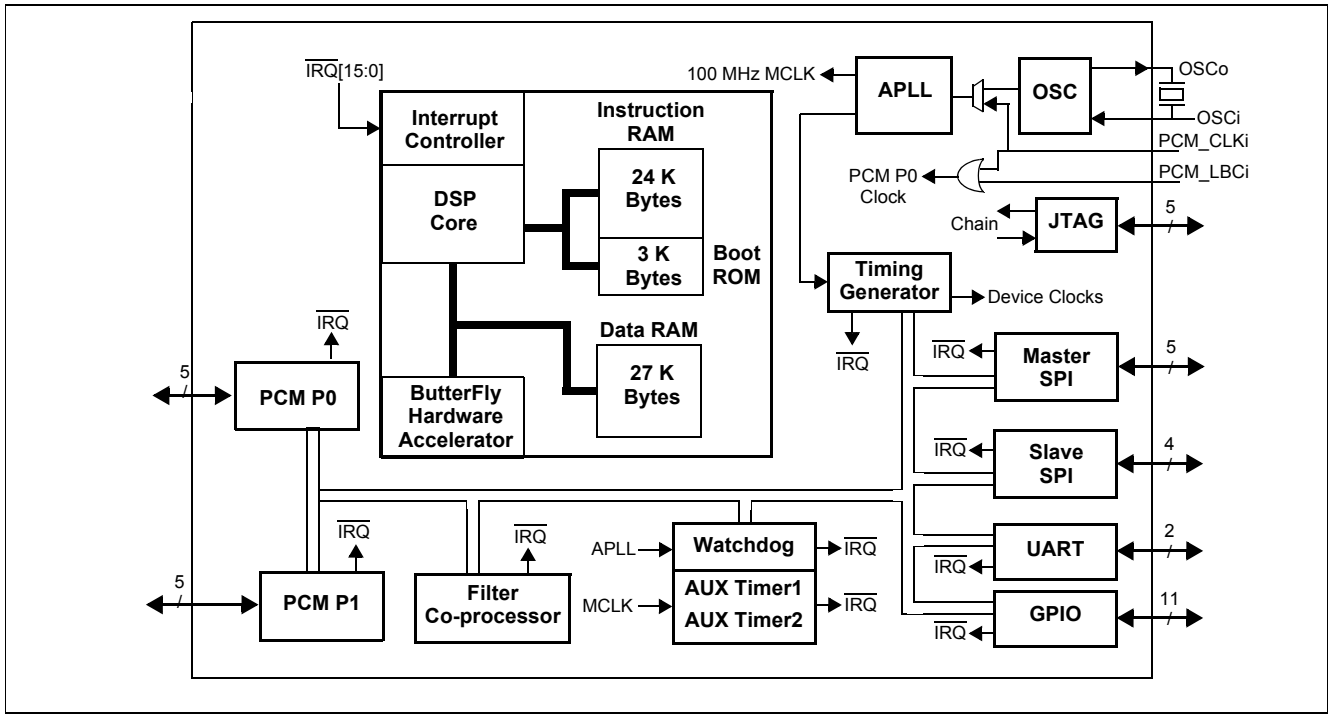

Figure 1 - Functional Block Diagram

Description

The ZL38015 is a four channel Voice-Processor hardware platform designed to support advanced voice and digital signal processing applications available from Zarlink Semiconductor. The ZL38015 platform integrates Zarlink's Voice Processor (ZVP) DSP Core with a number of internal peripherals including: 2 PCM ports, a 2048 tap Filter Co-processor, 2 Auxiliary Timers and a Watchdog Timer, 9 GPIO pins, UART, Slave SPI and Master SPI ports and a master/slave timing block.

The firmware products and manuals available at the release of this data sheet is the ZLS38233: 4 Channel Voice Echo Cancellor (VEC) with integrated DTMF Transceiver (Tx/Rx). If these applications do not meet your requirements, please contact your local Zarlink Sales Office for the latest firmware releases.

1.0 Functional Description

The ZL38015 is a hardware platform designed to support advanced voice processing applications available from Zarlink Semiconductor. These applications are resident in external memory and are down-loaded by the ZL38015 resident boot code during initialization.

The firmware products and manuals available at the release of this data sheet is the ZLS38233: 4 Channel Voice Echo Cancellor with DTMF Transceiver.

The ZL38015 platform integrates Zarlink's Voice Processor (ZVP) DSP Core with a number of internal peripherals. These peripherals include the following:

- Two PCM ports - ST BUS, GCI, McBSP or SSI operation
- A 2048 tap Filter Co-processor (LMS, FIR and FAP realizations)
- Two Auxiliary Timers and a Watchdog Timer
- 11 GPIO pins
- A UART interface
- A Slave SPI port and a Master SPI port
- A timing block that supports master and slave operation
- An IEEE - 1149.1 compatible JTAG port

The DSP Core can process up to four 8-bit voice channels, two 16-bit voice channels or two 8-bit and one 16-bit voice channel.