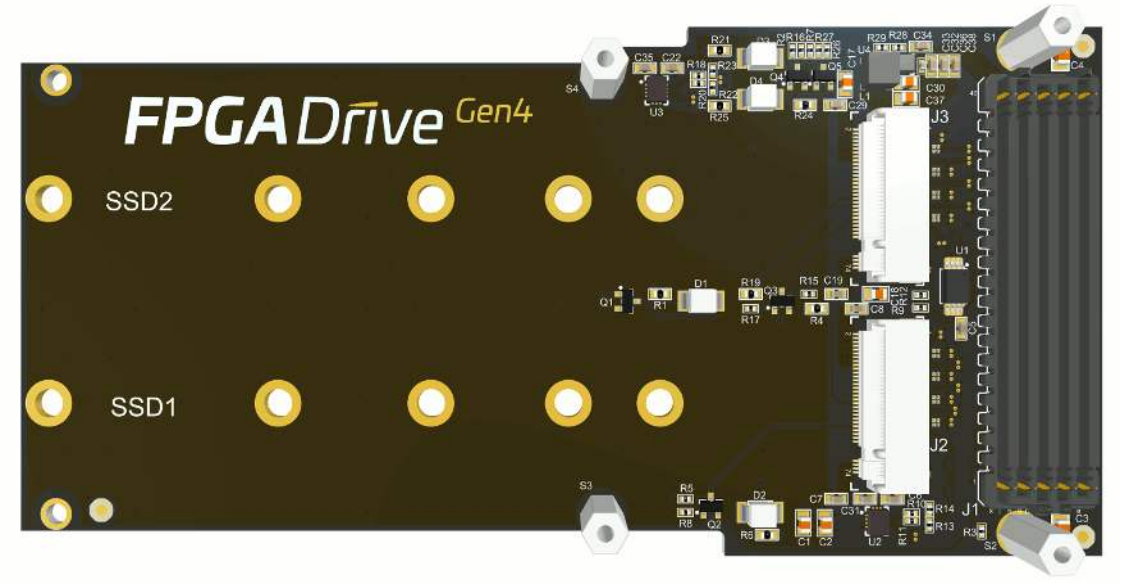
FPGA Drive FMC Gen4

Overview

Description

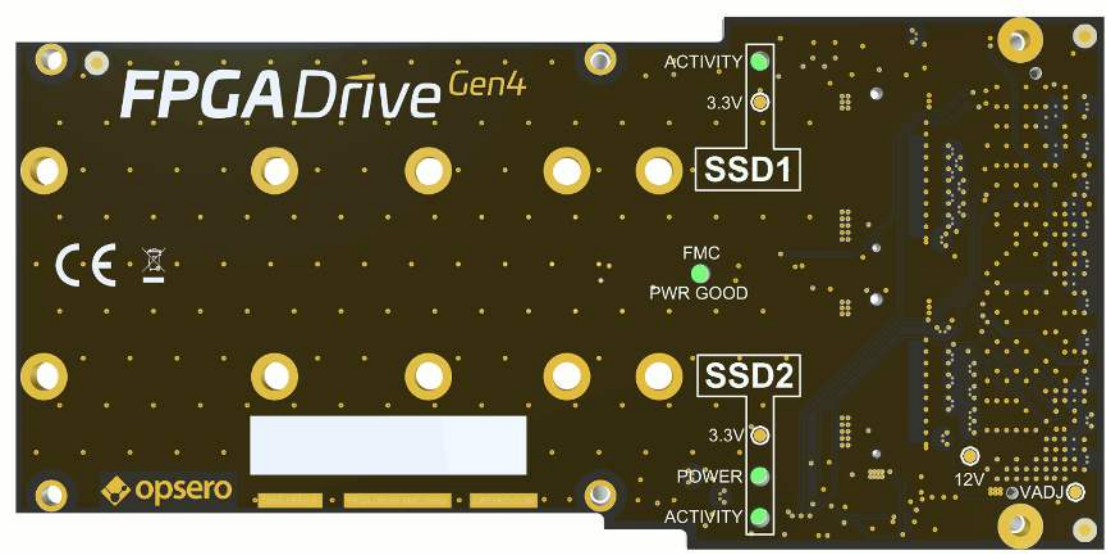
FPGA Drive FMC Gen4 is an adapter that allows M.2 NVMe PCIe SSDs to be connected to FPGA and MPSoC based development boards. The adapter uses the FPGA Mezzanine Card (FMC) form factor for connection with FPGA and MPSoC development boards via the FMC connector. It has 2x M-key M.2 sockets and can carry M.2 PCIe SSDs of length 42mm, 60mm, 80mm or 110mm. Each M.2 socket has its own independent connection to the FPGA for maximum throughput and can support a 4-lane PCIe connection up to Gen4.

Top view



FPGA Drive FMC Gen4 top

Bottom view



FPGA Drive FMC Gen4 bottom

Features

- 2x M-key M.2 connectors for PCIe NVMe SSDs
- Support and example designs for multiple development boards
- Supports up to PCIe Gen4 speeds
- FMC pinout conforms to VITA 57.1 FMC Standard
- Standalone example designs
- PetaLinux example designs

Supported development boards

For a list of all the FPGA and MPSoC development boards that are compatible with the FPGA Drive FMC Gen4, please refer to the list of compatible boards. For a list of boards for which we currently have a reference design, please refer to the list of supported boards in the reference design documentation.

Supported SSDs

The FPGA Drive FMC Gen4 has been designed to support all standard M-key M.2 NVMe SSDs for PCIe Gen1 to Gen4. However, certain software incompatibility issues can arise when using some SSDs and can depend on the version of PetaLinux used, the version of NVMe built into the SSD, the transceiver settings in the Vivado design,

and other factors. To help guide your selection of SSD, the documentation for the reference designs contains a list of SSDs that have been tested with the FPGA Drive FMC Gen4.

Ordering

The FPGA Drive FMC Gen4 can be ordered from the vendors listed below. The links under the part number column will take you to the corresponding order page.

Vendor	Part name	Part number
Opsero	FPGA Drive FMC Gen4	OP063
Digi-Key	FPGA Drive FMC Gen4	OP063

Included with the FPGA Drive FMC Gen4 are:

- 2x machine screws for fixing the SSDs to the mezzanine card * 2x M.2 loopback modules (PN: OP057)

Note that the FPGA Drive FMC Gen4 does NOT come with SSDs.

Pin Configuration

Pinout table

The FPGA Drive FMC Gen4 has a high pin count FPGA Mezzanine Card (FMC) connector, providing the connections to the FPGA on the development board. The following table defines the pinout of the FMC connector and describes each pin's purpose on this mezzanine card.

To avoid confusion, we have chosen not to label the PCIe lanes as being TX or RX; instead we have labelled them with the direction in which the signal flows (eg. FPGA-to-SSD1 means that the FPGA transmits this signal and the SSD1 receives).

Pin	Pin name	Net	Description
A1	GND	GND	Ground
A2	DP1_M2C_P	SSDA2FPGA_1_P	PCIe lane 1 positive (SSD1-to-FPGA)
A3	DP1_M2C_N	SSDA2FPGA_1_N	PCIe lane 1 negative (SSD1-to-FPGA)

A4	GND	GND	Ground
A5	GND	GND	Ground
A6	DP2_M2C_P	SSDA2FPGA_2_P	PCIe lane 2 positive (SSD1-to-FPGA)
A7	DP2_M2C_N	SSDA2FPGA_2_N	PCIe lane 2 negative (SSD1-to-FPGA)
A8	GND	GND	Ground
A9	GND	GND	Ground
A10	DP3_M2C_P	SSDA2FPGA_3_P	PCIe lane 3 positive (SSD1-to-FPGA)
A11	DP3_M2C_N	SSDA2FPGA_3_N	PCIe lane 3 negative (SSD1-to-FPGA)
A12	GND	GND	Ground
A13	GND	GND	Ground
A14	DP4_M2C_P	SSDB2FPGA_0_P	PCIe lane 0 positive (SSD2-to-FPGA)
A15	DP4_M2C_N	SSDB2FPGA_0_N	PCIe lane 0 negative (SSD2-to-FPGA)
A16	GND	GND	Ground
A17	GND	GND	Ground
A18	DP5_M2C_P	SSDB2FPGA_1_P	PCIe lane 1 positive (SSD2-to-FPGA)
A19	DP5_M2C_N	SSDB2FPGA_1_N	PCIe lane 1 negative (SSD2-to-FPGA)
A20	GND	GND	Ground
A21	GND	GND	Ground
A22	DP1_C2M_P	FPGA2SSDA_1_P	PCIe lane 1 positive (FPGA-to-SSD1)

A23	DP1_C2M_N	FPGA2SSDA_1_N	PCIe lane 1 negative (FPGA-to-SSD1)
A24	GND	GND	Ground
A25	GND	GND	Ground
A26	DP2_C2M_P	FPGA2SSDA_2_P	PCIe lane 2 positive (FPGA-to-SSD1)
A27	DP2_C2M_N	FPGA2SSDA_2_N	PCIe lane 2 negative (FPGA-to-SSD1)
A28	GND	GND	Ground
A29	GND	GND	Ground
A30	DP3_C2M_P	FPGA2SSDA_3_P	PCIe lane 3 positive (FPGA-to-SSD1)
A31	DP3_C2M_N	FPGA2SSDA_3_N	PCIe lane 3 negative (FPGA-to-SSD1)
A32	GND	GND	Ground
A33	GND	GND	Ground
A34	DP4_C2M_P	FPGA2SSDB_0_P	PCIe lane 0 positive (FPGA-to-SSD2)
A35	DP4_C2M_N	FPGA2SSDB_0_N	PCIe lane 0 negative (FPGA-to-SSD2)
A36	GND	GND	Ground
A37	GND	GND	Ground
A38	DP5_C2M_P	FPGA2SSDB_1_P	PCIe lane 1 positive (FPGA-to-SSD2)
A39	DP5_C2M_N	FPGA2SSDB_1_N	PCIe lane 1 negative (FPGA-to-SSD2)
A40	GND	GND	Ground
B1	CLK_DIR	N/C	Not connected

B2	GND	GND	Ground
B3	GND	GND	Ground
B4	DP9_M2C_P	N/C	Not connected
B5	DP9_M2C_N	N/C	Not connected
B6	GND	GND	Ground
B7	GND	GND	Ground
B8	DP8_M2C_P	N/C	Not connected
B9	DP8_M2C_N	N/C	Not connected
B10	GND	GND	Ground
B11	GND	GND	Ground
B12	DP7_M2C_P	SSDB2FPGA_3_P	PCIe lane 3 positive (SSD2-to-FPGA)
B13	DP7_M2C_N	SSDB2FPGA_3_N	PCIe lane 3 negative (SSD2-to-FPGA)
B14	GND	GND	Ground
B15	GND	GND	Ground
B16	DP6_M2C_P	SSDB2FPGA_2_P	PCIe lane 2 positive (SSD2-to-FPGA)
B17	DP6_M2C_N	SSDB2FPGA_2_N	PCIe lane 2 negative (SSD2-to-FPGA)
B18	GND	GND	Ground
B19	GND	GND	Ground
B20	GBTCLK1_M2C_P	REFCLKB_FPGA_P	100MHz PCIe reference clock for the FPGA
B21	GBTCLK1_M2C_N	REFCLKB_FPGA_N	100MHz PCIe reference clock for the FPGA
B22	GND	GND	Ground

B23	GND	GND	Ground
B24	DP9_C2M_P	N/C	Not connected
B25	DP9_C2M_N	N/C	Not connected
B26	GND	GND	Ground
B27	GND	GND	Ground
B28	DP8_C2M_P	N/C	Not connected
B29	DP8_C2M_N	N/C	Not connected
B30	GND	GND	Ground
B31	GND	GND	Ground
B32	DP7_C2M_P	FPGA2SSDB_3_P	PCIe lane 3 positive (FPGA-to-SSD2)
B33	DP7_C2M_N	FPGA2SSDB_3_N	PCIe lane 3 negative (FPGA-to-SSD2)
B34	GND	GND	Ground
B35	GND	GND	Ground
B36	DP6_C2M_P	FPGA2SSDB_2_P	PCIe lane 2 positive (FPGA-to-SSD2)
B37	DP6_C2M_N	FPGA2SSDB_2_N	PCIe lane 2 negative (FPGA-to-SSD2)
B38	GND	GND	Ground
B39	GND	GND	Ground
B40	RES0	N/C	Not connected
C1	GND	GND	Ground
C2	DP0_C2M_P	FPGA2SSDA_0_P	PCIe lane 0 positive (FPGA-to-SSD1)
C3	DP0_C2M_N	FPGA2SSDA_0_N	PCIe lane 0 negative (FPGA-to-SSD1)

C4	GND	GND	Ground
C5	GND	GND	Ground
C6	DP0_M2C_P	SSDA2FPGA_0_P	PCIe lane 0 positive (SSD1-to-FPGA)
C7	DP0_M2C_N	SSDA2FPGA_0_N	PCIe lane 0 negative (SSD1-to-FPGA)
C8	GND	GND	Ground
C9	GND	GND	Ground
C10	LA06_P	N/C	Not connected
C11	LA06_N	N/C	Not connected
C12	GND	GND	Ground
C13	GND	GND	Ground
C14	LA10_P	N/C	Not connected
C15	LA10_N	N/C	Not connected
C16	GND	GND	Ground
C17	GND	GND	Ground
C18	LA14_P	N/C	Not connected
C19	LA14_N	N/C	Not connected
C20	GND	GND	Ground
C21	GND	GND	Ground
C22	LA18_P_CC	N/C	Not connected
C23	LA18_N_CC	N/C	Not connected
C24	GND	GND	Ground
C25	GND	GND	Ground
C26	LA27_P	N/C	Not connected

C27	LA27_N	N/C	Not connected
C28	GND	GND	Ground
C29	GND	GND	Ground
C30	SCL	I2C_SCL	I2C Clock (FPGA-to-PHY)
C31	SDA	I2C_SDA	I2C Data (bidirectional)
C32	GND	GND	Ground
C33	GND	GND	Ground
C34	GA0	GA0	EEPROM Address Bit 1 (A1)
C35	12P0V_1	12V0	12VDC (Not used)
C36	GND	GND	Ground
C37	12P0V_2	12V0	12VDC (Not used)
C38	GND	GND	Ground
C39	3P3V_1	3V3	3.3VDC
C40	GND	GND	Ground
D1	PG_C2M	PG	Power Good (Driven by carrier)
D2	GND	GND	Ground
D3	GND	GND	Ground
D4	GBTCLK0_M2C_P	REFCLKA_FPGA_P	100MHz PCIe reference clock for the FPGA
D5	GBTCLK0_M2C_N	REFCLKA_FPGA_P	100MHz PCIe reference clock for the FPGA
D6	GND	GND	Ground
D7	GND	GND	Ground
D8	LA01_P_CC	N/C	Not connected
D9	LA01_N_CC	N/C	Not connected

D10	GND	GND	Ground
D11	LA05_P	N/C	Not connected
D12	LA05_N	N/C	Not connected
D13	GND	GND	Ground
D14	LA09_P	N/C	Not connected
D15	LA09_N	N/C	Not connected
D16	GND	GND	Ground
D17	LA13_P	N/C	Not connected
D18	LA13_N	N/C	Not connected
D19	GND	GND	Ground
D20	LA17_P_CC	RSVD	Reserved for production testing
D21	LA17_N_CC	RSVD	Reserved for production testing
D22	GND	GND	Ground
D23	LA23_P	N/C	Not connected
D24	LA23_N	N/C	Not connected
D25	GND	GND	Ground
D26	LA26_P	N/C	Not connected
D27	LA26_N	N/C	Not connected
D28	GND	GND	Ground
D29	TCK	N/C	Not used
D30	TDI	TDI-TDO	JTAG TDI (Connects to TDO to close JTAG chain)
D31	TDO	TDI-TDO	JTAG TDO (Connects to TDI to close JTAG chain)
D32	3P3VAUX	3V3AUX	3.3VDC Power supply for EEPROM

D33	TMS	N/C	Not used
D34	TRST_L	N/C	Not used
D35	GA1	GA1	EEPROM Address Bit 0 (A0)
D36	3P3V_2	3V3	3.3VDC
D37	GND	GND	Ground
D38	3P3V_3	3V3	3.3VDC
D39	GND	GND	Ground
D40	3P3V_4	3V3	3.3VDC
G1	GND	GND	Ground
G2	CLK1_M2C_P	N/C	Not used
G3	CLK1_M2C_N	N/C	Not used
G4	GND	GND	Ground
G5	GND	GND	Ground
G6	LA00_P_CC	PERST_A	PCIe reset for SSD1 (active high)
G7	LA00_N_CC	PEDET_A	PCIe detect for SSD1
G8	GND	GND	Ground
G9	LA03_P	N/C	Not connected
G10	LA03_N	N/C	Not connected
G11	GND	GND	Ground
G12	LA08_P	N/C	Not connected
G13	LA08_N	N/C	Not connected
G14	GND	GND	Ground
G15	LA12_P	N/C	Not connected
G16	LA12_N	N/C	Not connected

G17	GND	GND	Ground
G18	LA16_P	N/C	Not connected
G19	LA16_N	N/C	Not connected
G20	GND	GND	Ground
G21	LA20_P	N/C	Not connected
G22	LA20_N	N/C	Not connected
G23	GND	GND	Ground
G24	LA22_P	N/C	Not connected
G25	LA22_N	N/C	Not connected
G26	GND	GND	Ground
G27	LA25_P	N/C	Not connected
G28	LA25_N	N/C	Not connected
G29	GND	GND	Ground
G30	LA29_P	N/C	Not connected
G31	LA29_N	N/C	Not connected
G32	GND	GND	Ground
G33	LA31_P	N/C	Not connected
G34	LA31_N	N/C	Not connected
G35	GND	GND	Ground
G36	LA33_P	N/C	Not connected
G37	LA33_N	N/C	Not connected
G38	GND	GND	Ground
G39	VADJ_3	VADJ	I/O Supply Voltage (1.2VDC)
G40	GND	GND	Ground

H1	VREF_A_M2C	N/C	Not used
H2	PRSNT_M2C_L	GND	Ground
H3	GND	GND	Ground
H4	CLK0_M2C_P	N/C	Not used
H5	CLK0_M2C_N	N/C	Not used
H6	GND	GND	Ground
H7	LA02_P	N/C	Not connected
H8	LA02_N	N/C	Not connected
H9	GND	GND	Ground
H10	LA04_P	PERST_B	PCIe reset for SSD2 (active high)
H11	LA04_N	PEDET_B	PCIe detect for SSD2
H12	GND	GND	Ground
H13	LA07_P	DISABLE_SSD2_PWR	Disable switching regulator for SSD2 (0=Enable,1=Disable)
H14	LA07_N	N/C	Not used
H15	GND	GND	Ground
H16	LA11_P	N/C	Not connected
H17	LA11_N	N/C	Not connected
H18	GND	GND	Ground
H19	LA15_P	N/C	Not connected
H20	LA15_N	N/C	Not connected
H21	GND	GND	Ground
H22	LA19_P	N/C	Not connected
H23	LA19_N	N/C	Not connected

H24	GND	GND	Ground
H25	LA21_P	N/C	Not connected
H26	LA21_N	N/C	Not connected
H27	GND	GND	Ground
H28	LA24_P	N/C	Not connected
H29	LA24_N	N/C	Not connected
H30	GND	GND	Ground
H31	LA28_P	N/C	Not connected
H32	LA28_N	N/C	Not connected
H33	GND	GND	Ground
H34	LA30_P	N/C	Not connected
H35	LA30_N	N/C	Not connected
H36	GND	GND	Ground
H37	LA32_P	N/C	Not connected
H38	LA32_N	N/C	Not connected
H39	GND	GND	Ground
H40	VADJ_4	VADJ	I/O Supply Voltage (1.2VDC)

Rows E,F,J and K of the HPC connector were left out of the above table. On the mezzanine card, these rows are left unconnected, with the exception of the ground and VADJ pins which are connected appropriately.

Specifications

Recommended Operating Conditions

SUPPLY VOLTAGE	MIN	TYP	MAX	UNIT
12 VDC	+11.4	+12	+12.6	V

3.3 VDC	+3.14	+3.3	+3.46	V
VADJ 1.8VDC	+1.71	+1.8	+1.89	V

Power Consumption

The specifications below refer to the total current draw on each of the power supplies while the FPGA Drive FMC Gen4 is connected to a development board and has 2x SSDs connected.

SUPPLY	UTILIZATION	MIN	TYP	MAX	UNIT
12 VDC	Dual write		281		mA
12 VDC	Dual read		199		mA
3.3 VDC	Dual write		969		mA
3.3 VDC	Dual read		688		mA
VADJ 1.8 VDC	Dual write		<1		mA
VADJ 1.8 VDC	Dual read		<1		mA

- Tests performed at ambient temperature of 25 degrees C
- Tests performed using the ZCU106 development board
- Tests performed using 2x Samsung 980 PRO SSDs
- Both SSDs were exercised using dd under PetaLinux
- Measured write speed was 167MBytes/s (1.7% of rated write speed)
- Measured read speed was 240MBytes/s (1.7% of rated read speed)

Note that the FPGA Drive FMC Gen4 example design will also produce an increase in power consumption of the FPGA/MPSoC on the development board due to the use of FPGA and hardware resources.

Thermal Information

We have not performed comprehensive thermal testing on the FPGA Drive FMC Gen4, however we recommend that it be operated under ambient temperatures between 0 and 70 degrees C. This advice is based on the recommended ambient operating temperatures of a basket of NVMe SSDs currently on the market. The active devices on the mezzanine card itself have operating ranges that exceed those of the typical SSD and are listed in the table below.

Component Ambient Operating Temperatures

DEVICE	MIN	MAX	UNIT
ON Semi, Digital FET N-Channel, FDV303N	-55	150	C
TI, 3-17V 2-3A Buck Converter, TPS62913RPUR	-40	150	C
MicroChip, 2x Output PCIe Clock Generator, DSC557-0334FI1	-40	85	C
ST, 2K EEPROM, M24C02-FDW6TP	-40	85	C
Amphenol, PCIe M.2 connector, MDT420M02003	-40	80	C

Components that are not listed in the table above (such as resistors, capacitors) are selected to have minimum operating temperature that is lower than -20 degrees C, and maximum operating temperature that is greater than 70 degrees C.

I2C (EEPROM) Timing

The serial EEPROM (part number ST, 2K EEPROM, M24C02-FDW6TP) has a maximum operating clock frequency of 400 kHz.

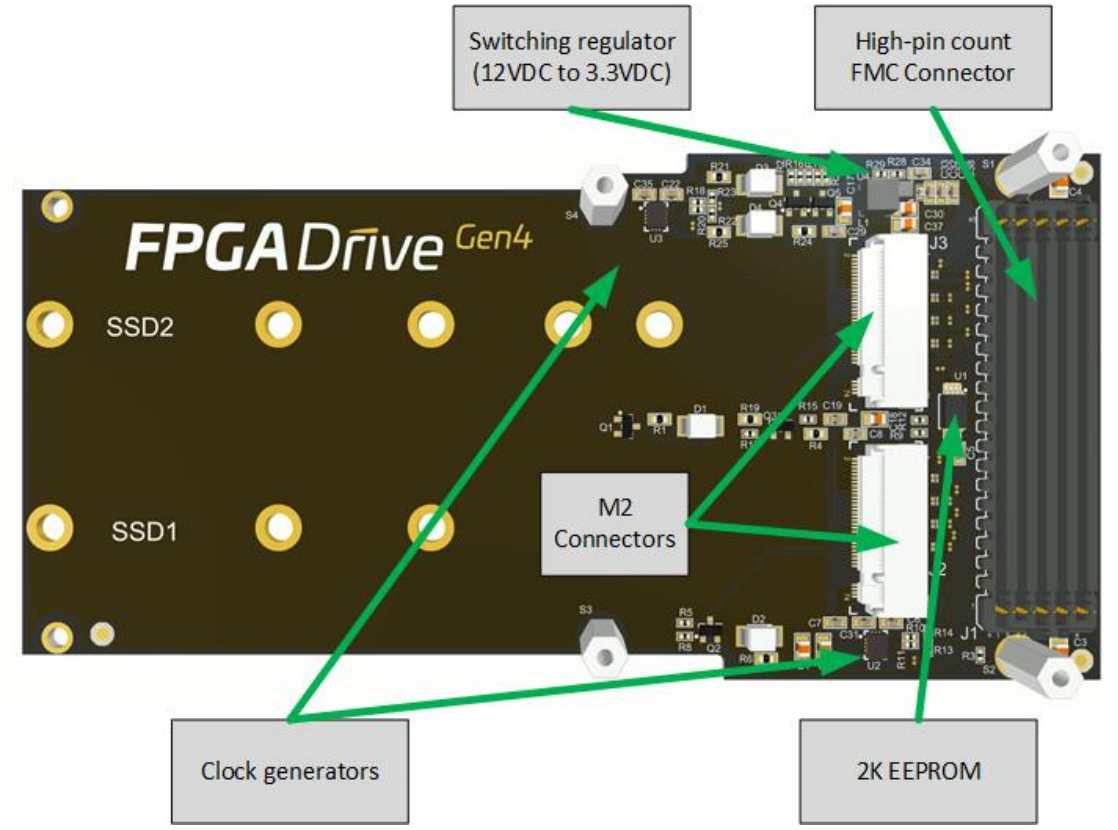
Certifications

- RoHS
- CE
- UKCA

Detailed Description

Hardware Overview

The figure below illustrates the various hardware components that are located on the top-side of the FPGA Drive FMC Gen4.



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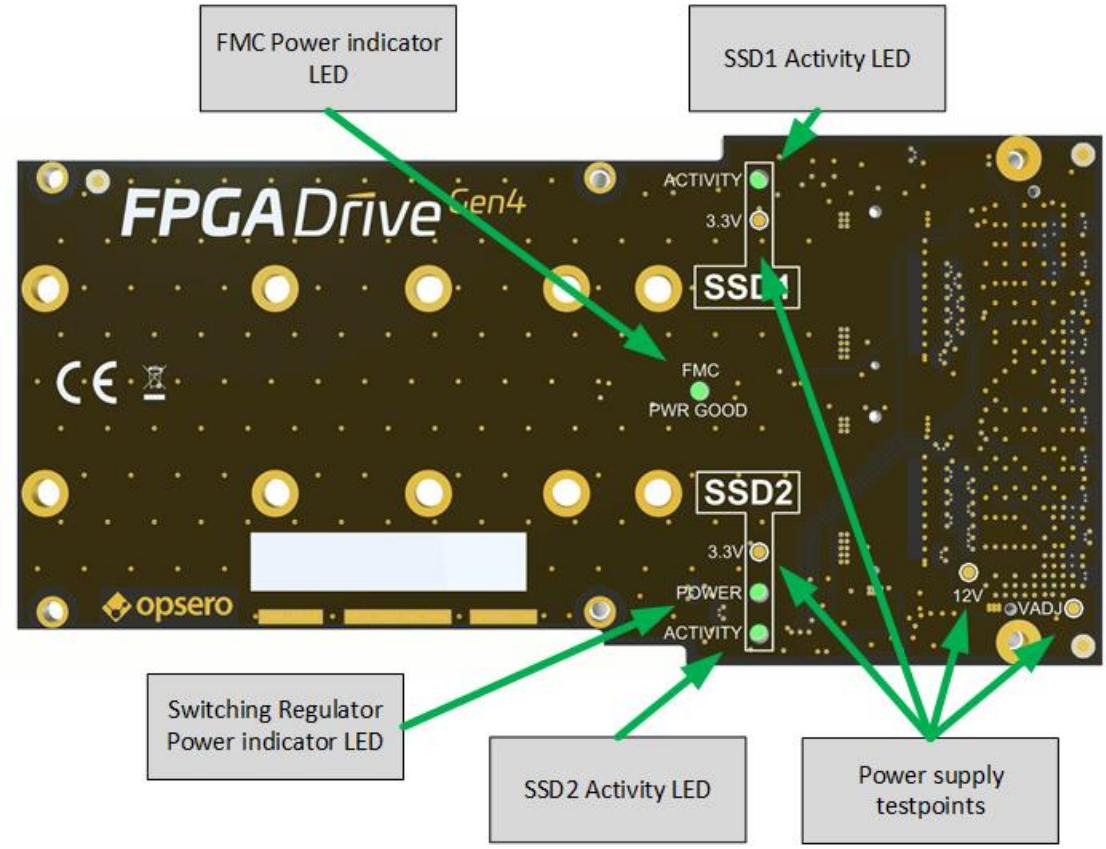
The main components on the top-side of the mezzanine card are:

- 2x M-key M.2 socket connectors (for the SSDs)
- High Pin Count FMC Connector
- 2K EEPROM
- 2x PCIe Clock oscillators (100MHz)
- Switching regulator

The figure below illustrates the various hardware components that are located on the bottom-side of the mezzanine card.



The main components on the bottom-side of the mezzanine card are:

- FMC Power indicator LED
- Switching regulator power indicator LED
- SSD activity LEDs
- Test points for power supplies

M.2 connectors

The NVMe PCIe SSDs connect to the mezzanine card through 2x M-key M.2 connectors (Amphenol, PCIe M.2 connector, MDT420M02003).

The pinout of the M.2 connector is shown in the table below:

Pin #	Pin name	Connection	Pin #	Pin name	Connection
1	GND	GND	2	3.3V	3V3
3	GND	GND	4	3.3V	3V3

5	PER-N3	SSD2FPGA_3_N	6	N/C	NC
7	PER-P3	SSD2FPGA_3_P	8	N/C	NC
9	GND	GND	10	DAS/DSS#/LED1#	DAS/DSS#
11	PET-N3	FPGA2SSD_3_N	12	3.3V	3V3
13	PET-P3	FPGA2SSD_3_P	14	3.3V	3V3
15	GND	GND	16	3.3V	3V3
17	PER-N2	SSD2FPGA_2_N	18	3.3V	3V3
19	PER-P2	SSD2FPGA_2_P	20	N/C	NC
21	GND	GND	22	N/C	NC
23	PET-N2	FPGA2SSD_2_N	24	N/C	NC
25	PET-P2	FPGA2SSD_2_P	26	N/C	NC
27	GND	GND	28	N/C	NC
29	PER-N1	SSD2FPGA_1_N	30	N/C	NC
31	PER-P1	SSD2FPGA_1_P	32	N/C	NC
33	GND	GND	34	N/C	NC
35	PET-N1	FPGA2SSD_1_N	36	N/C	NC
37	PET-P1	FPGA2SSD_1_P	38	DEVSLP	GND
39	GND	GND	40	SMB_CLK	NC
41	PER-N0	SSD2FPGA_0_N	42	SMB_DATA	NC
43	PER-P0	SSD2FPGA_0_P	44	ALERT#	NC
45	GND	GND	46	N/C	NC
47	PET-N0	FPGA2SSD_0_N	48	N/C	NC
49	PET-P0	FPGA2SSD_0_P	50	PERST#	PERST#
51	GND	GND	52	CLKREQ#	NC

53	REFCLK-N	REFCLK_SSD_N	54	PEWAKE#	NC
55	REFCLK-P	REFCLK_SSD_P	56	RSVD	NC
57	GND	GND	58	RSVD	NC
67	N/C	NC	68	SUSCLK	NC
69	PEDET	PEDET	70	3.3V	3V3
71	GND	GND	72	3.3V	3V3
73	GND	GND	74	3.3V	3V3
75	GND	GND			

EEPROM

The EEPROM (ST, 2K EEPROM, M24C02-FDW6TP) stores IPMI FRU data that can be read by the carrier board and contains the following information:

- Manufacturer name (Opsero Electronic Design Inc.)
- Product name
- Product part number
- Serial number
- Power supply requirements

The FRU data is read by some carrier boards to determine the correct VADJ voltage to apply to the mezzanine card. All Opsero FMC products have their EEPROMs programmed with valid FRU data to allow these carrier boards to correctly power them.

Erasing or writing over the contents of the EEPROM can corrupt the IPMI FRU data making the mezzanine card unusable with carrier boards that require the information. We recommend that you do not use the mezzanine card's EEPROM for non-volatile storage but instead use the storage options provided by the carrier board. If you mistakenly erase or corrupt the contents of the EEPROM, you can reprogram it using the Opsero FMC EEPROM Tool. Read more about the FMC EEPROM tool in the User Guide.

High Pin Count FMC Connector

The FPGA Drive FMC Gen4 has a high pin count (HPC) FMC (FPGA Mezzanine Card) connector for interfacing with an FPGA or SoC development board. The part number of

this connector is Samtec, High pin count FMC connector, ASP-134488-01 . This HPC FMC connector can be mated with LPC, HPC or FMC+ carrier connectors.

Note: When mated with an LPC FMC connector, only one SSD is connected, and only with a single lane PCIe interface. To get full functionality from the mezzanine card, it is recommended to use it with fully connected HPC or FMC+ connectors.

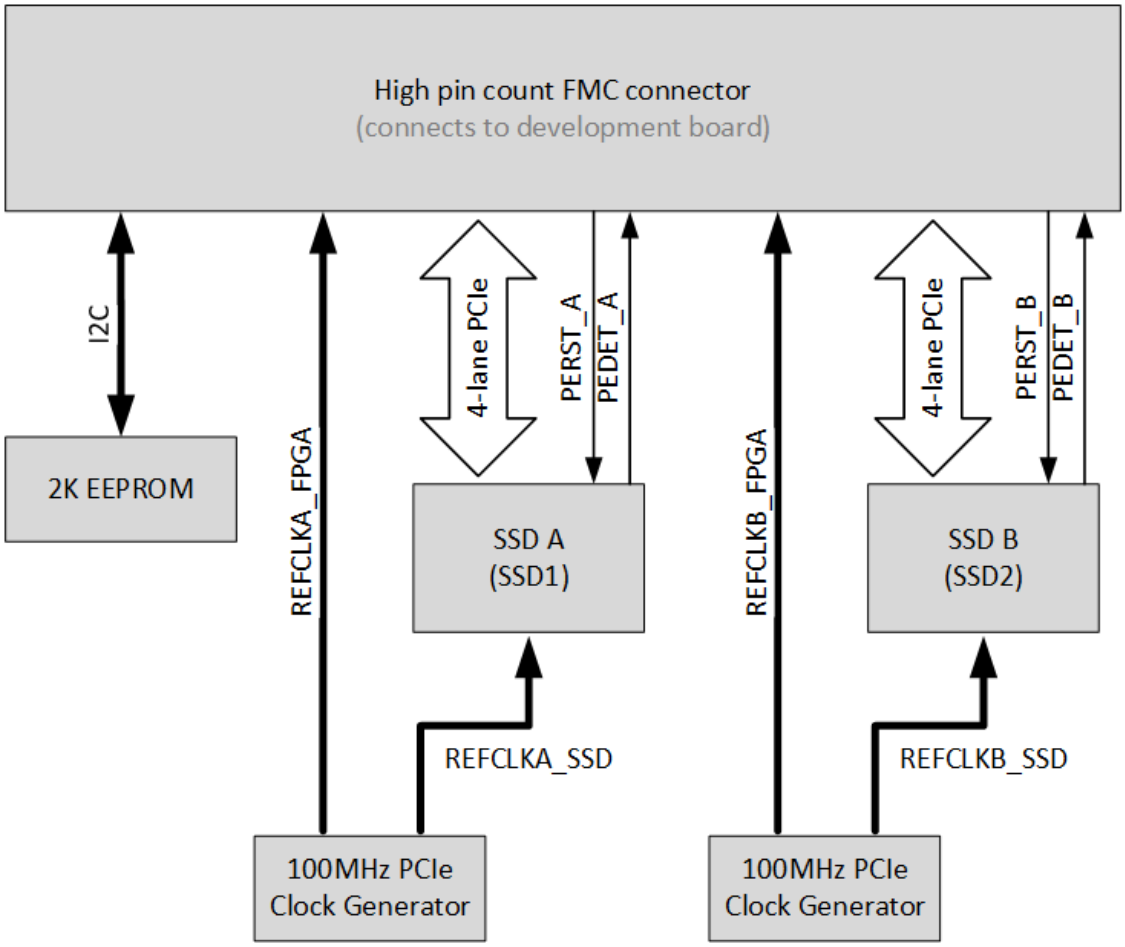
The pinout of this connector conforms to the VITA 57.1 FPGA Mezzanine Card Standard (for more information, see Pin configuration. For more information on the FMC connector and the VITA 57.1 standard, see the Samtec page on VITA 57.1 .

I/O Interfaces

The FMC connector provides power to the FPGA Drive FMC Gen4 and also presents the following I/O signals to the FPGA fabric of the development board:

- 2x 4-lane PCIe interfaces for the SSDs
- 2x PERST active-high reset signals (driven by FPGA)
- 2x PEDET detect signals (driven by mezzanine card)
- 2x LVDS 100MHz PCIe reference clocks
- I2C for EEPROM R/W access

The 2x 4-lane PCIe interfaces are routed to independent gigabit transceivers on the FMC connector for maximum throughput. The figure below illustrates the main connections to the FMC connector. Note that the PERST signals pass through FETs for inversion and level translation, however this circuit is left out of the diagram for clarity.



PCIe interfaces

The 4-lane PCIe interfaces are routed to FMC pins that are dedicated to gigabit transceivers. The connections are shown in the tables below. Note that in this documentation, the label for the first SSD is SSD A (or SSD1) while the second SSD is SSD B (or SSD2).

SSD A (SSD1)

Direction	PCIe lane	FMC Pin	FMC name	Net name
SSD-to-FPGA	0	C6/C7	DP0_M2C_P/N	SSDA2FPGA_0_P/N
	1	A2/A3	DP1_M2C_P/N	SSDA2FPGA_1_P/N
	2	A6/A7	DP2_M2C_P/N	SSDA2FPGA_2_P/N
	3	A10/A11	DP3_M2C_P/N	SSDA2FPGA_3_P/N

FPGA-to-SSD	0	C2/C3	DP0_C2M_P/N	FPGA2SSDA_0_P/N
	1	A22/A23	DP1_C2M_P/N	FPGA2SSDA_1_P/N
	2	A26/A27	DP2_C2M_P/N	FPGA2SSDA_2_P/N
	3	A30/A31	DP3_C2M_P/N	FPGA2SSDA_3_P/N

SSD B (SSD2)

Direction	PCIe lane	FMC Pin	FMC name	Net name
SSD-to-FPGA	0	A14/A15	DP4_M2C_P/N	SSDB2FPGA_0_P/N
	1	A18/A19	DP5_M2C_P/N	SSDB2FPGA_1_P/N
	2	B16/B17	DP6_M2C_P/N	SSDB2FPGA_2_P/N
	3	B12/B13	DP7_M2C_P/N	SSDB2FPGA_3_P/N
FPGA-to-SSD	0	A34/A35	DP4_C2M_P/N	FPGA2SSDB_0_P/N
	1	A38/A39	DP5_C2M_P/N	FPGA2SSDB_1_P/N
	2	B36/B37	DP6_C2M_P/N	FPGA2SSDB_2_P/N
	3	B32/B33	DP7_C2M_P/N	FPGA2SSDB_3_P/N

Reference clocks

The mezzanine card has two clock oscillators (MicroChip, 2x Output PCIe Clock Generator, DSC557-0334FI1), one for each SSD. Each clock oscillator generates two synchronous 100MHz clocks; one LVDS and the other HCSL. The LVDS clocks are fed to the FMC connector, while the HCSL clocks are fed directly to the SSDs.

Synchronous to	FMC Pin	FMC name	Net name
SSD A	D4/D5	GBTCLK0_M2C_P/N	REFCLKA_FPGA_P/N
SSD B	B20/B21	GBTCLK1_M2C_P/N	REFCLKB_FPGA_P/N

PERST

The PERST_A and PERST_B signals are active-high reset signals of SSD A and SSD B respectively, and they are driven by the FPGA. The FPGA drives these signals at VADJ voltage levels, while the SSDs require 3.3VDC active-low signals. For this reason, the mezzanine card has two FET based inverter circuits to perform the level translation and the signal inversion. The FPGA design should drive these signals active-high as shown in the table below:

PERST_A/B	Function
0 (LOW)	SSD operational
1 (HIGH)	SSD in reset

PEDET

The PEDET_A and PEDET_B signals are outputs of the mezzanine card and they can be read by the FPGA if so desired. The purpose of the signal is to indicate whether the connected SSD has a PCIe or SATA interface. The functionality of the output is described in the table below:

PEDET_A/B	Function
0 (LOW)	SATA
1 (HIGH)	PCIe

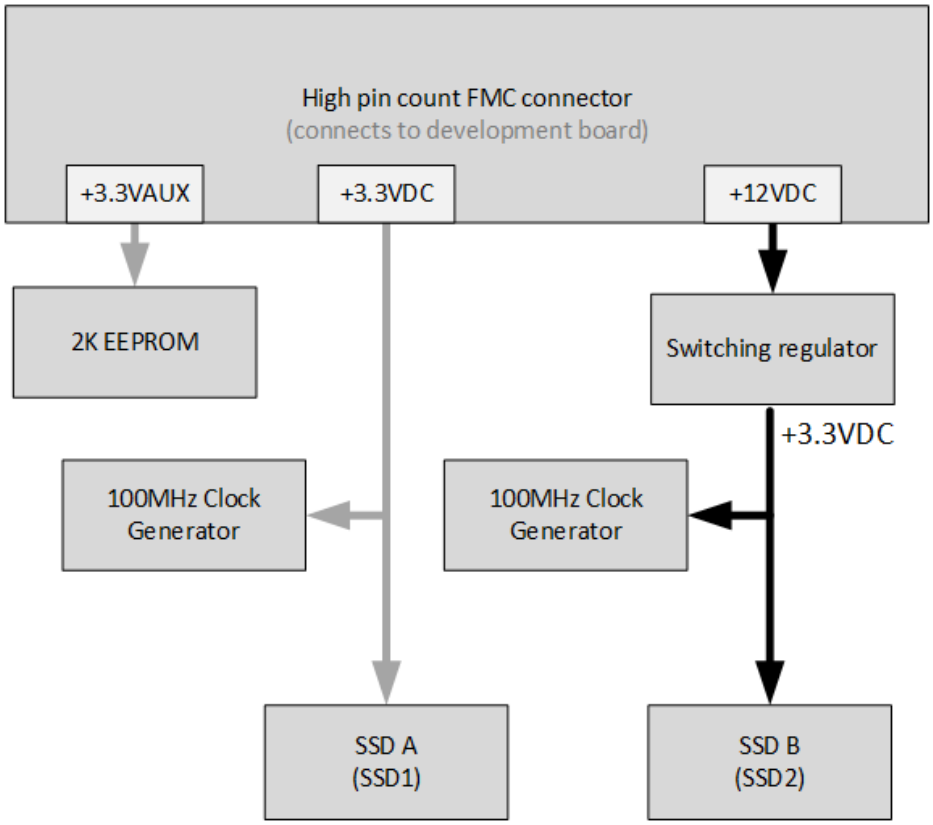
This signal is not used in our example designs and is not required if only using NVMe PCIe SSDs.

Power Supplies

All power required by the FPGA Drive FMC Gen4 is supplied by the development board through the FMC connector:

- +12VDC
- +3.3VDC
- +3.3VAUX (for powering EEPROM only)
- VADJ: +1.8VDC

The mezzanine card powers the first SSD and it's clock generator using the FMC's 3.3VDC supply. It has a switching regulator to power the second SSD and it's clock generator using the FMC's 12VDC supply.



Power supplies

12VDC Supply

The 12VDC supply is used to power the second SSD (SSD B/SSD2) via a buck switching regulator (TI, 3-17V 2-3A Buck Converter, TPS62913RPUR). The switching regulator converts the 12VDC supply to a 3.3VDC supply which powers SSD B (SSD2) and its corresponding 100MHz clock oscillator. The switching regulator can be disabled by driving the DISABLE_SSD2_PWR pin as described in the table below:

DISABLE_SSD2_PWR	Function
0 (LOW)	SSD B power enabled
1 (HIGH)	SSD B power disabled

The DISABLE_SSD2_PWR is controlled via the LA07_P pin of the FMC connector. The mezzanine card has a pull down resistor to hold this pin to ground, enabling the switching regulator, if it is not driven by the FPGA.

An LED indicates when the switching regulator is enabled (ie. when SSD B has power), and it can be seen in the labelled bottom view of the board above.

3.3VDC Supply

The 3.3VDC supply provides power for the first SSD (SSD A/SSD1) and the corresponding 100MHz clock oscillator.

VADJ Supply

The adjustable voltage supply (VADJ), is the I/O voltage that is supplied by all standard FMC carriers. The FPGA Drive FMC Gen4 can accept any VADJ voltage in the range of 1.8V to 3.3V. The mezzanine card has an onboard FRU EEPROM that specifies a VADJ voltage of 1.8V. All carriers with a power management system will read this EEPROM on power-up and apply the voltage specified by the EEPROM. Note that some development boards require the VADJ voltage to be configured by a DIP switch or jumper placement, in which case the user should ensure that it is set to 1.8V.

Power LED and testpoints

Two red LEDs on the mezzanine card are used to indicate when the required power supplies are active. The location of these LEDs can be seen in the labelled bottom view of the board above. The main LED in the middle of the board indicates when the FMC's 12VDC, 3.3VDC and VADJ voltages are active. The second LED indicates when the 3.3VDC supply generated by the switching regulator is active (ie. when the second SSD is powered).

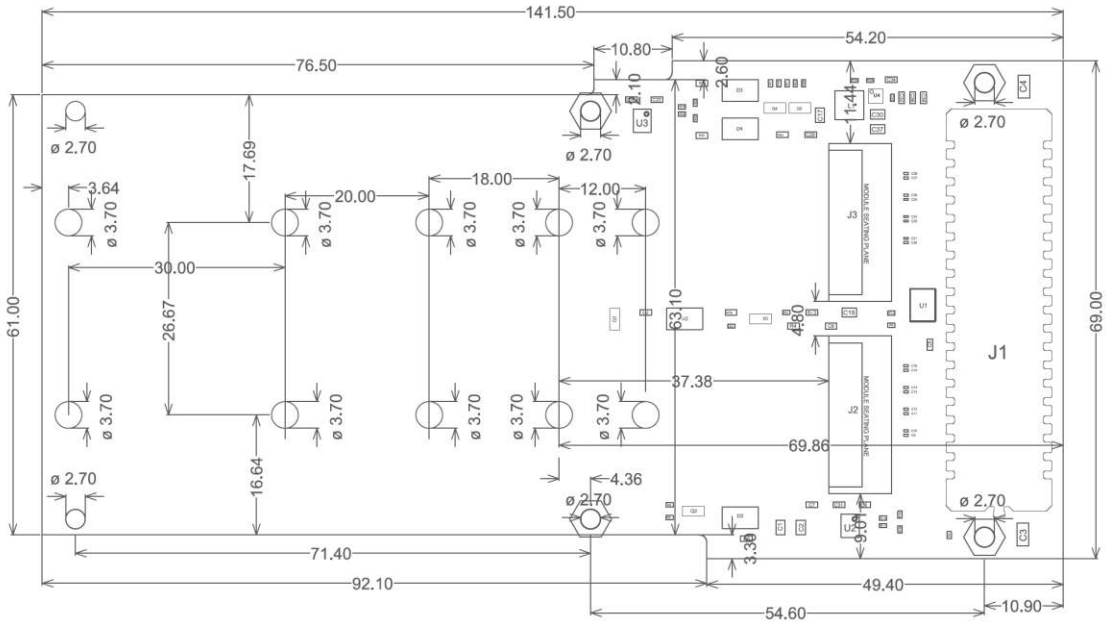
To aid hardware debug, test points are accessible on the bottom side of the mezzanine card for each of the power supplies of the FPGA Drive FMC Gen4.

Mechanical Information

Dimensions

The mechanical dimensions of the FPGA Drive FMC Gen4 are illustrated in the figures below. All dimensions are in millimeters (mm).

The assembly drawings are also available as PDF files that you can download at the provided links.



FPGA Drive FMC Gen4 mechanical drawing

- FPGA Drive FMC Gen4 Rev-A Assembly Drawing PDF

3D Model

The 3D model of the board is available as a STEP file at the link below:

- FPGA Drive FMC Gen4 Rev-A 3D STEP model

Mezzanine fastening hardware

For mechanical fastening of the mezzanine card to the carrier board, the FPGA Drive FMC Gen4 comes with 4x hex standoffs. We **highly recommend** using machine screws on each of these standoffs to fix the mezzanine card to the carrier board.

The hex standoff and machine screw part numbers are listed below:

- Hex standoff, Thread M2.5 x 0.45, Brass, Board-to-board length 10mm
  Part number: V6516C
  Manufacturer: Assmann

- Machine screw, Thread M2.5 x 0.45, Length (below head) 4mm, Stainless steel, Phillips head
  Part number: 90116A105
  Supplier: McMaster-Carr

Getting Started

Minimum setup

To start developing with the FPGA Drive FMC Gen4, we recommend that you get setup with the minimum hardware and software requirements:

1. An FPGA or MPSoC development board from our list of supported boards.
2. One FPGA Drive FMC Gen4.
3. At least one M.2 NVMe SSD (see our list of tested SSDs).
4. Build and run one of our example designs.

Hardware setup

For instructions on attaching the SSDs and connecting the FPGA Drive FMC Gen4 into the carrier board, we have put together the following video:

https://www.youtube.com/watch?v="A-80u63AjiM"

Fastening the mezzanine

FMC mezzanine cards are **not** hot-pluggable; to prevent the mezzanine card from detaching from the carrier while active, we recommend using machine screws to fix the mezzanine card to the carrier board. The screws should be screwed into the mezzanine's hex standoffs from the underside of the carrier board. The details on suitable screws can be found in the mechanical information section.

Software setup

In order to build our example designs, you will need to setup your PC with the AMD Xilinx development tools:

- Vivado ML
- Vitis
- PetaLinux

The Vivado and Vitis tools support most operating systems, whereas the PetaLinux tools can only be installed under Linux.

For the specific versions required, please refer to the release notes in the Git repository of the particular example design you wish to build.

Compatible Boards

The following development boards are compatible with the FPGA Drive FMC Gen4 and can support at least one SSD. If you know of a board that is not listed here and you would like to know if it is compatible, please contact us.

Note that we don't currently have example designs for all of these carrier boards. For a list of carrier boards for which we do have example designs, please refer to the list of supported carriers in the reference design documentation.

Series-7 boards

Carrier	FMC	Ref design	PCIe	SSD 1	SSD 2
AMD Xilinx KC705 Kintex-7 Development board	HPC	Yes	Gen2	4-lanes	Not supported
AMD Xilinx KC705 Kintex-7 Development board	LPC	Yes	Gen2	1-lane [1]	Not supported [2]
AMD Xilinx VC707 Virtex-7 Development board	HPC1	Yes	Gen2	4-lanes	4-lanes
AMD Xilinx VC707 Virtex-7 Development board	HPC2	Yes	Gen2	4-lanes	4-lanes
AMD Xilinx VC709 Virtex-7 Development board	HPC	Yes	Gen3	4-lanes	4-lanes
AMD Xilinx ZC706 Zynq-7000 Development board	HPC	Yes	Gen2	4-lanes	Not supported [3]
AMD Xilinx ZC706 Zynq-7000 Development board	LPC	Yes	Gen2	1-lane [4]	Not supported [5]

[1] LPC connectors can only support 1-lane PCIe

[2] LPC connectors can only support 1-lane PCIe

[3] Zynq-7000 devices only have 1 PCIe block

[4] LPC connectors can only support 1-lane PCIe

[5] LPC connectors can only support 1-lane PCIe

Avnet PicoZed FMC Carrier Card V2 Zynq-7000 Development Board	LPC	Yes	Gen2	1-lane [6]	Not supported [7]

UltraScale boards

Carrier	FMC	Ref design	PCIe	SSD 1	SSD 2
AMD Xilinx KCU105 Kintex UltraScale Development board	HPC	Yes	Gen3	4-lanes	4-lanes
AMD Xilinx KCU105 Kintex UltraScale Development board	LPC	Yes	Gen3	1-lane [8]	Not supported [9]
AMD Xilinx VCU108 Virtex UltraScale Development board	HPC0	No	Gen3	4-lanes	4-lanes
AMD Xilinx VCU108 Virtex UltraScale Development board	HPC1	No	Gen3	4-lanes	4-lanes

Zynq Ultrascale+ boards

Carrier	FMC	Ref design	PCIe	SSD 1	SSD 2
AMD Xilinx ZCU104 Zynq UltraScale+ Development board	LPC	Yes	Gen3	1-lane [10]	Not supported [11]

[6] LPC connectors can only support 1-lane PCIe

[7] LPC connectors can only support 1-lane PCIe

[8] LPC connectors can only support 1-lane PCIe

[9] LPC connectors can only support 1-lane PCIe

[10] LPC connectors can only support 1-lane PCIe

[11] LPC connectors can only support 1-lane PCIe

AMD Xilinx ZCU102 Zynq UltraScale+ Development board	HPC0	No	Gen3	4-lanes [12]	4-lanes [13]
AMD Xilinx ZCU102 Zynq UltraScale+ Development board	HPC1	No	Gen3	4-lanes [14]	4-lanes [15]
AMD Xilinx ZCU106 Zynq UltraScale+ Development board	HPC0	Yes	Gen3	4-lanes	4-lanes
AMD Xilinx ZCU106 Zynq UltraScale+ Development board	HPC1	Yes	Gen3	1-lanes	Not supported
AMD Xilinx ZCU111 Zynq UltraScale+ Development board	FMC+	Yes	Gen3	4-lanes	4-lanes
Avnet UltraZed EV Carrier Zynq UltraScale+ Development board	HPC	Yes	Gen3	4-lanes	4-lanes
Trenz UltraITX+ Baseboard Zynq UltraScale+ Development board	HPC	No	Gen3	4-lanes [16]	4-lanes [17]

Ultrascale+ boards

Carrier	FMC	Ref design	PCIe	SSD 1	SSD 2

[12] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

[13] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

[14] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

[15] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

[16] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

[17] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

AMD Xilinx VCU118 Virtex UltraScale+ Development board	HPC	No	Gen3	Not supported	Not supported
AMD Xilinx VCU118 Virtex UltraScale+ Development board	FMC+	No	Gen3	4-lanes	4-lanes

Versal boards

Carrier	FMC	Ref design	PCIe	SSD 1	SSD 2
AMD Xilinx VCK190 Versal AI Core Development board	FMC+1	No	Gen4	4-lanes	4-lanes
AMD Xilinx VCK190 Versal AI Core Development board	FMC+2	No	Gen4	4-lanes	4-lanes
AMD Xilinx VMK180 Versal Prime Series Development board	FMC+1	No	Gen4	4-lanes	4-lanes
AMD Xilinx VMK180 Versal Prime Series Development board	FMC+2	No	Gen4	4-lanes	4-lanes

Compatibility requirements

If you need to determine the compatibility of a development board that is not listed here, or you are designing a carrier board to mate with the FPGA Drive FMC Gen4, you can check your board against the list of requirements below.

VADJ

The carrier board must have the ability to supply a VADJ voltage between 1.8VDC and 3.3VDC.

Gigabit transceivers

The FPGA or MPSoC device must have gigabit transceivers and they must be routed to the FMC connector. For support of both SSDs, transceivers DP0-DP7 must all be connected to the FPGA. In the AMD Xilinx devices, the transceivers are typically grouped into quads containing 4 transceivers. Ideally, each SSD should be connected to a single quad and the lane ordering should match the MGT ordering as shown in the tables below:

Quad 1

The first quad should be connected to SSD A (SSD1) as follows:

FPGA pin	PCIe lane	FMC Pin	FMC name	Net name
MGT_RXP/N0	0	C6/C7	DP0_M2C_P/N	SSDA2FPGA_0_P/N
MGT_TXP/N0	0	C2/C3	DP0_C2M_P/N	FPGA2SSDA_0_P/N
MGT_RXP/N1	1	A2/A3	DP1_M2C_P/N	SSDA2FPGA_1_P/N
MGT_TXP/N1	1	A22/A23	DP1_C2M_P/N	FPGA2SSDA_1_P/N
MGT_RXP/N2	2	A6/A7	DP2_M2C_P/N	SSDA2FPGA_2_P/N
MGT_TXP/N2	2	A26/A27	DP2_C2M_P/N	FPGA2SSDA_2_P/N
MGT_RXP/N3	3	A10/A11	DP3_M2C_P/N	SSDA2FPGA_3_P/N
MGT_TXP/N3	3	A30/A31	DP3_C2M_P/N	FPGA2SSDA_3_P/N

The clock reference for this SSD (FMC pins GBTCLK0_M2C_P/N) should be connected to MGTREFCLK0P/N or MGTREFCLK1P/N of this quad.

Quad 2

The second quad should be connected to SSD B (SSD2) as follows:

Direction	PCIe lane	FMC Pin	FMC name	Net name
MGT_RXP/N0	0	A14/A15	DP4_M2C_P/N	SSDB2FPGA_0_P/N
MGT_TXP/N0	0	A34/A35	DP4_C2M_P/N	FPGA2SSDB_0_P/N
MGT_RXP/N1	1	A18/A19	DP5_M2C_P/N	SSDB2FPGA_1_P/N
MGT_TXP/N1	1	A38/A39	DP5_C2M_P/N	FPGA2SSDB_1_P/N
MGT_RXP/N2	2	B16/B17	DP6_M2C_P/N	SSDB2FPGA_2_P/N
MGT_TXP/N2	2	B36/B37	DP6_C2M_P/N	FPGA2SSDB_2_P/N
MGT_RXP/N3	3	B12/B13	DP7_M2C_P/N	SSDB2FPGA_3_P/N
MGT_TXP/N3	3	B32/B33	DP7_C2M_P/N	FPGA2SSDB_3_P/N

The clock reference for this SSD (FMC pins GBTCLK1_M2C_P/N) should be connected to MGTREFCLK0P/N or MGTREFCLK1P/N of this quad.

Required I/O

The following I/O pins should be connected to the FPGA as they are required by the mezzanine card:

FMC Pin	FMC name	Net	Description
G6	LA00_P_CC	PERST_A	PCIe reset for SSD1 (active high)
G7	LA00_N_CC	PEDET_A	PCIe detect for SSD1
H10	LA04_P	PERST_B	PCIe reset for SSD2 (active high)
H11	LA04_N	PEDET_B	PCIe detect for SSD2
H13	LA07_P	DISABLE_SSD2_PWR	Disable switching regulator for SSD2 (0=Enable,1=Disable)

Example Designs

The example designs for the FPGA Drive FMC Gen4 are released open source under the MIT license and maintained on Github. We *strongly* encourage community contributions to the example designs.

FPGA Drive FMC example design

Description

This example design demonstrates use of one or two SSDs with the carrier boards listed below. The main IP in the design implements the PCIe root complex. The design can be used with a baremetal application that reports on the status of the PCIe links and performs enumeration of the detected SSDs. The design also can be used with a custom PetaLinux build that allows the SSDs to be accessed through standard Linux commands and a file system.

Links

- Git repo
- Documentation

Supported carrier boards

The Git repo contains an example design for each of the following carrier boards.

- AMD Xilinx KC705 Kintex-7 Development board
- AMD Xilinx VC707 Virtex-7 Development board
- AMD Xilinx VC709 Virtex-7 Development board
- AMD Xilinx ZC706 Zynq-7000 Development board
- Avnet PicoZed FMC Carrier Card V2 Zynq-7000 Development Board
- AMD Xilinx KCU105 Kintex UltraScale Development board
- AMD Xilinx ZCU104 Zynq UltraScale+ Development board
- AMD Xilinx ZCU106 Zynq UltraScale+ Development board
- AMD Xilinx ZCU111 Zynq UltraScale+ Development board
- Avnet UltraZed EV Carrier Zynq UltraScale+ Development board

Some of these boards have more than one FMC connector that can support FPGA Drive FMC Gen4, while some of them have specific limitations on the number of SSDs or PCIe lanes that they can support. For more information about these limitations, refer to the reference design documentation.

Supported SSDs

The reference design documentation provides a list of tested SSDs to help guide your selection of SSD for use with FPGA Drive FMC Gen4.

Programming Guide

This section provides the details of the programming requirements to operate the FPGA Drive FMC Gen4 hardware and customise functionality.

IBERT testing

The FPGA Drive FMC Gen4 comes with 2x M.2 loopback modules. These modules can be used to test the combined signal integrity of the carrier and mezzanine card, and can be useful when debugging issues on custom boards. To illustrate the use of the M.2 loopback modules with IBERT, we have put together the following videos.

Part 1: Hardware setup

How to attach the M.2 loopback modules and prepare your hardware for the IBERT loopback test.

https://www.youtube.com/watch?v=tGQ1nY0BSJ4

Part 2: Using IBERT in Vivado

Download the pre-built IBERT bitstream:

- KCU105 IBERT Prebuild bitstream (HPC)
- ZCU102 IBERT Prebuild bitstream (HPC0)
- ZCU106 IBERT Prebuild bitstream (HPC0)

Try this: disable the DFE (decision feedback equalizer) when doing a 2D eye scan – the gigabit traces on the FPGA Drive FMC have very low losses, so the performance is generally better without the DFE.

https://www.youtube.com/watch?v=xxw8I608ycw

Part 3: Generate your own IBERT

How to generate an IBERT bitstream for your own hardware if you don't find a pre-built bitstream listed above.

https://www.youtube.com/watch?v=0BuY2tYWP1k

EEPROM

The 2K EEPROM is intended to store information that identifies the mezzanine card and also specifies the power supplies required by the card. This information is typically read by the system power management on the carrier board when it is powered up. In typical user applications, it should not be necessary to read the data on the EEPROM, and we highly recommend against writing to the EEPROM. Nevertheless, if you wish to access the EEPROM, it can be read and written to at the I2C address 0x50.

A6	A5	A4	A3	A2	A1	A0	Hexadecimal
1	0	1	0	0	0	0	0x50

The FMC pins of the EEPROM's I2C bus are shown below, and it is up to the user to determine their corresponding connections to the FPGA/MPSoC on the carrier board being used.

I2C bus signal	FMC pin name	FMC pin number
SCL (clock)	SCL	C30
SDA (data)	SDA	C31

Be aware that on some carrier boards, the FMC I2C bus passes through an I2C MUX. On some boards it connects to FPGA pins whereas on others it connects to PS pins. If you wish to communicate with the EEPROM, it is necessary to check the schematic drawing of your carrier board to determine the structure of the I2C bus and to which pins it connects.

FMC EEPROM Tool

The Opsero FMC EEPROM Tool can be used to verify the EEPROM contents of Opsero FMC products using an FPGA or MPSoC board such as the ZCU102 or VCU118 board. The tool can also be used to reprogram the EEPROM in the case that it was mistakely erased or corrupted.

Only use this tool with Opsero FMC products. The use of this tool with FMCs from other manufacturers is strictly prohibited and may result in damage to the FMC or to the carrier board.

Supported boards

The tool currently supports the following FPGA/MPSoC boards. You must have at least one of these boards in order to use the tool.

- ZedBoard
- ZCU102 Rev1.0 and Rev1.1
- KC705
- KCU105
- VCU118
- ZCU104

Download

The tool can be downloaded at the link below:

Opsero FMC EEPROM Tool v1.3

The zip file contains a boot file (bitstream or BOOT.bin) for each of the supported boards.

Usage instructions

To run the tool, follow these steps:

5. Plug the FMC card you wish to reprogram into one of the FMC connectors of your FPGA/MPSoC board. The tool is designed to probe all of the FMC connectors on the FPGA/MPSoC board.

6. If you are using the ZedBoard, be sure to set the VADJ jumper setting to 1.8V. If you are using the KC705, be sure that your FMC card can support a VADJ of 2.5V, which is the default setting of that board.

7. Connect the UART of your FPGA/MPSoC board to a PC.

8. For Zynq and Zynq MP boards, a BOOT.bin file is provided. Copy this file to your board's SD card and configure it to boot from SD card. Then plug the SD card back into the board and power it up.

9. For FPGA boards, a bitstream is provided with an embedded ELF file. Power up your FPGA/MPSoC board and then download the bitstream to the FPGA board using the Vivado Hardware Manager tool.

10. Open a terminal program such as Putty and connect to the serial port of your FPGA/MPSoC board. If you see nothing in the terminal window, press ENTER to redisplay the menu.

11. Use the menu options to do the following:

    – **Program the EEPROM (p)**
    You will be asked to select the FMC product from a list, and also to enter the product's serial number. Note that entering incorrect information here can lead to your FMC card being damaged by a VADJ voltage that is greater than it's true rating. If you are not sure about the product to select here, please contact Opsero first.

Board Revision History

Rev A

- The FPGA Drive FMC Gen4 (OP063) is an upgrade of the original FPGA Drive FMC (OP047) product which is now discontinued. Details on the design improvements were described in this blog post.
- Date of first manufacture: 2021-12-02
- Commercially released

References

Board Files

Rev-A

- FPGA Drive FMC Gen4 Rev-A Schematics PDF
- FPGA Drive FMC Gen4 Rev-A Assembly Drawing PDF
- FPGA Drive FMC Gen4 Rev-A 3D STEP model

Part Datasheets

Use the links below to access the datasheets of the significant parts on the mezzanine card.

- Samtec, High pin count FMC connector, ASP-134488-01 datasheet
- Amphenol, PCIe M.2 connector, MDT420M02003 datasheet
- ON Semi, Digital FET N-Channel, FDV303N datasheet
- TI, 3-17V 2-3A Buck Converter, TPS62913RPUR datasheet
- MicroChip, 2x Output PCIe Clock Generator, DSC557-0334FI1 datasheet
- ST, 2K EEPROM, M24C02-FDW6TP datasheet

Revision History

Date	Version	Description
2023-05-09	1.0	Initial PDF release.

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