FAIRCHILD SEMICONDUCTOR®

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FSLV16211
24-Bit Bus Switch

Features

- 5Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Packaged in Fine-Pitch Ball Grid Array (FBGA) and Thin Shrink Small Outline Package (TSSOP)

Description

The FSLV16211 is a 24-bit, high-speed, low-voltage bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

This device's design allows this part to be used as a 12-bit or 24-bit bus switch. When $\overline{OE}1$ is LOW, Port 1A is connected to Port 1B. When $\overline{OE}2$ is LOW, Port 2A is connected to Port 2B.

Ordering Information

Part Number	Pb-Free	Operating Temperature Range	Package	Packing Method
FSLV16211GX	Yes	-40°C to 85°C	54-Ball, Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide	Tape and Reel
FSLV16211MTD	Yes	-40°C to 85°C	56-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC M0-153, 6.1mm Wide	Trays
FSLV16211MTDX	Yes	-40°C to 85°C	56-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC M0-153, 6.1mm Wide	Tape and Reel

Application Diagram

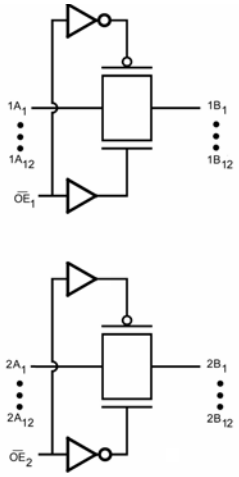


Figure 1. Logic Diagram

Connection Diagram

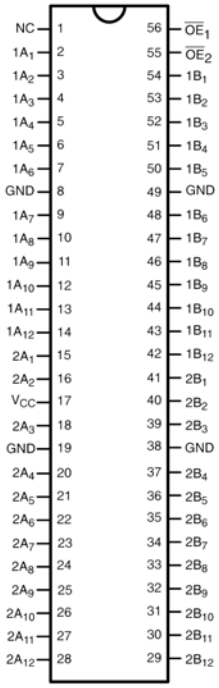


Figure 2. Pin Assignments for TSSOP (Top Through View)

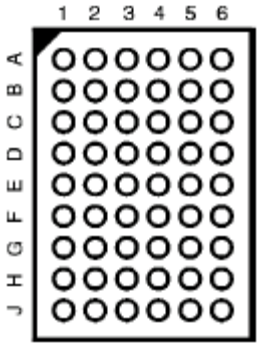


Figure 3. Pin Assignments for FBGA (Top Through View)

Pin Description

Pin Name	Description
$\overline{OE}_1$, $\overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	$1A_2$	$1A_1$	NC	OE_2	$1B_1$	$1B_2$
B	$1A_4$	$1A_3$	$1A_7$	OE_1	$1B_3$	$1B_4$
C	$1A_6$	$1A_5$	GND	$1B_7$	$1B_5$	$1B_6$
D	$1A_{10}$	$1A_9$	$1A_8$	$1B_8$	$1B_9$	$1B_{10}$
E	$1A_{12}$	$1A_{11}$	$2A_1$	$2B_1$	$1B_{11}$	$1B_{12}$
F	$2A_4$	$2A_3$	$2A_2$	$2B_2$	$2B_3$	$2B_4$
G	$2A_6$	$2A_5$	VCC	GND	$2B_5$	$2B_6$
H	$2A_8$	$2A_7$	$2A_9$	$2B_9$	$2B_7$	$2B_8$
I	$2A_{12}$	$2A_{11}$	$2A_{10}$	$2B_{10}$	$2B_{11}$	$2B_{12}$

Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A,1B	2A, 2B
Low	Low	1A=1B	2A=2B
Low	High	1A=1B	Z
High	Low	Z	2A=2B
High	High	Z	Z

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	4.6	V
V_S	DC Switch Voltage[1]	-0.5	4.6	V
V_{IN}	DC Input Voltage	-0.5	4.6	V
I_{IK}	DC Input Diode Current		-50	mA
I_{OUT}	DC Output Sink Current		128	mA
I_{CC}/I_{GNG}	DC V_{CC}/GND Current		+/-100	mA
T_{STG}	Storage Temperature Range	-65	150	°C

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.[2]

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Power Supply Operating		2.3	3.6	V
V_{IN}	Input Voltage		0	3.6	V
V_{OUT}	Output Voltage		0	3.6	V
t_r, t_f	Input Rise and Fall Time	Switch Control Input	0	4.0	ns/V
		Switch I/O	0	DC	ns/V
T_A	Free Air Operating Temperature		-40	85	°C

Note:

2. Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Not all conditions may appear on all switch types.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = -40°C to +85°C			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN} = -18mA	3.0			-1.2	V
V_{IH}	HIGH Level Control Input Voltage		2.3-2.7	1.7			V
			2.7-3.6	2.0			
V_{IL}	LOW Level Control Input Voltage		2.3-2.7			0.7	V
			2.7-3.6			0.8	
I_L	Input Leakage Current	Force V_I = 3.6V, I_{OUT} = 0.0A	2.3			10.0	µA
		Force V_I = 3.6V	0.0			10.0	
		$0 \leq V_{IN} \leq$ 3.6V	3.6			1.0	
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, I_{OUT} = 0A	3.6			10.0	µA
ΔI_{CC}	Increase in I_{CC} per Input	One Input at 3V Other Inputs at V_{CC} or GND	3.6			300.0	µA
I_{OZ}	Off-State Leakage	0.0 ≤ A, B ≤ 3.6V	3.6	-1.0		1.0	µA
R_{ON}	Switch On Resistance	I_{IN} = 64mA, V_I = 0.0V	3.0		5.0	7.0	Ω
		I_{IN} = 30mA, V_I = 0.0V	3.0		5.0	7.0	
		I_{IN} = 15mA, V_I = 2.4V	3.0		10.0	15.0	
		I_{IN} = 15mA, V_I = 3.0V	2.3			20.0	
		I_{IN} = 64mA, V_I = 0.0V	2.3		5.0	8.0	
		I_{IN} = 30mA, V_I = 0.0V	2.3		5.0	8.0	
		I_{IN} = 15mA, V_I = 1.7V	2.3		10.0	15.0	
		I_{IN} = 15mA, V_I = 2.0V	2.3			20.0	

AC Electrical Characteristics

Symbol	Parameter	T_A=-40°C to +85°C		T_A=40°C to +85°C		Units
		C_L=30pF, R_L=500Ω		C_L=50pF, R_L=500Ω		
		V_{CC} = 2.5V ± 0.20V		V_{CC}=3.3V ± 0.30V		
		Min.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay(3)		0.15		0.25	ns
t_{PHZ}, t_{PLZ}	Enable Time	0.5	4.7	1.0	7.0	ns
t_{PZH}, t_{PZL}	Disable Time	0.5	5.1	1.0	5.5	ns

Note:

3. This parameter is guaranteed by design, but is not production tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).

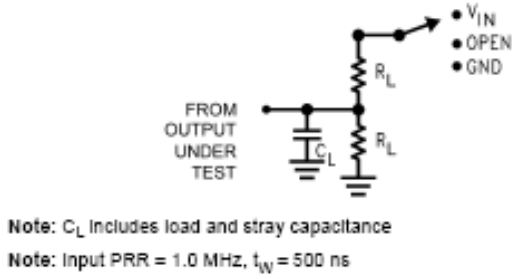
Capacitance

T_A = +25°C, f = 1MHz, unless otherwise noted.

Symbols	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Control Pin Input Capacitance	V_{CC} – 3.3V		4.5		pF
$C_{I/O}$	Input/Output Capacitance	V_{CC},$\overline{OE}$= 3.3V		18.0		pF

Capacitance is characterized, but not production tested.

AC Loading Waveforms



Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

TEST	SWITCH
t_{PD}	Open
t_{PLZ}/t_{PZL}	V_{IN}
t_{PHZ}/t_{PZH}	GND

Figure 4. AC Test Circuit

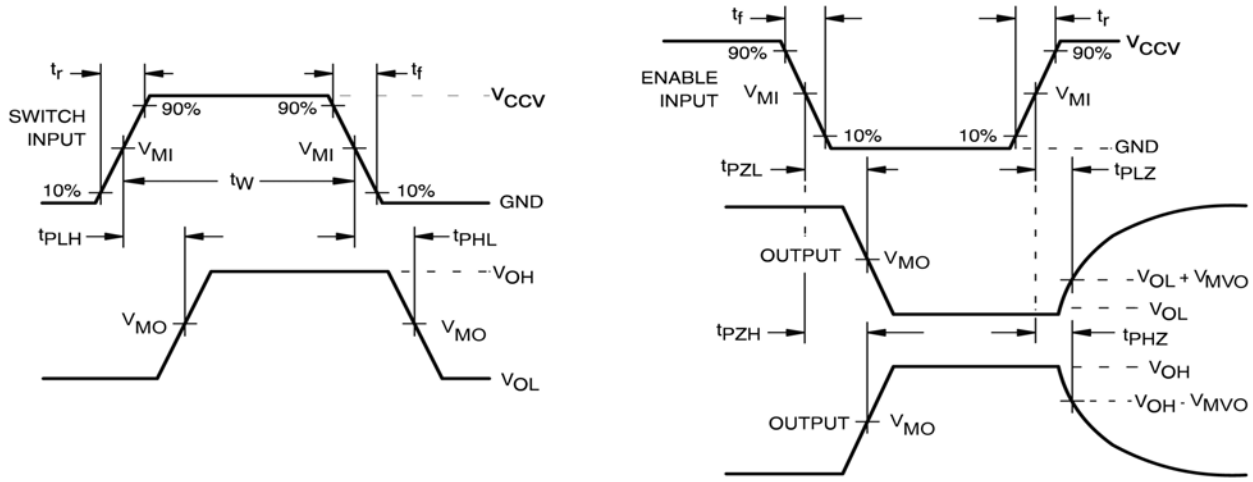
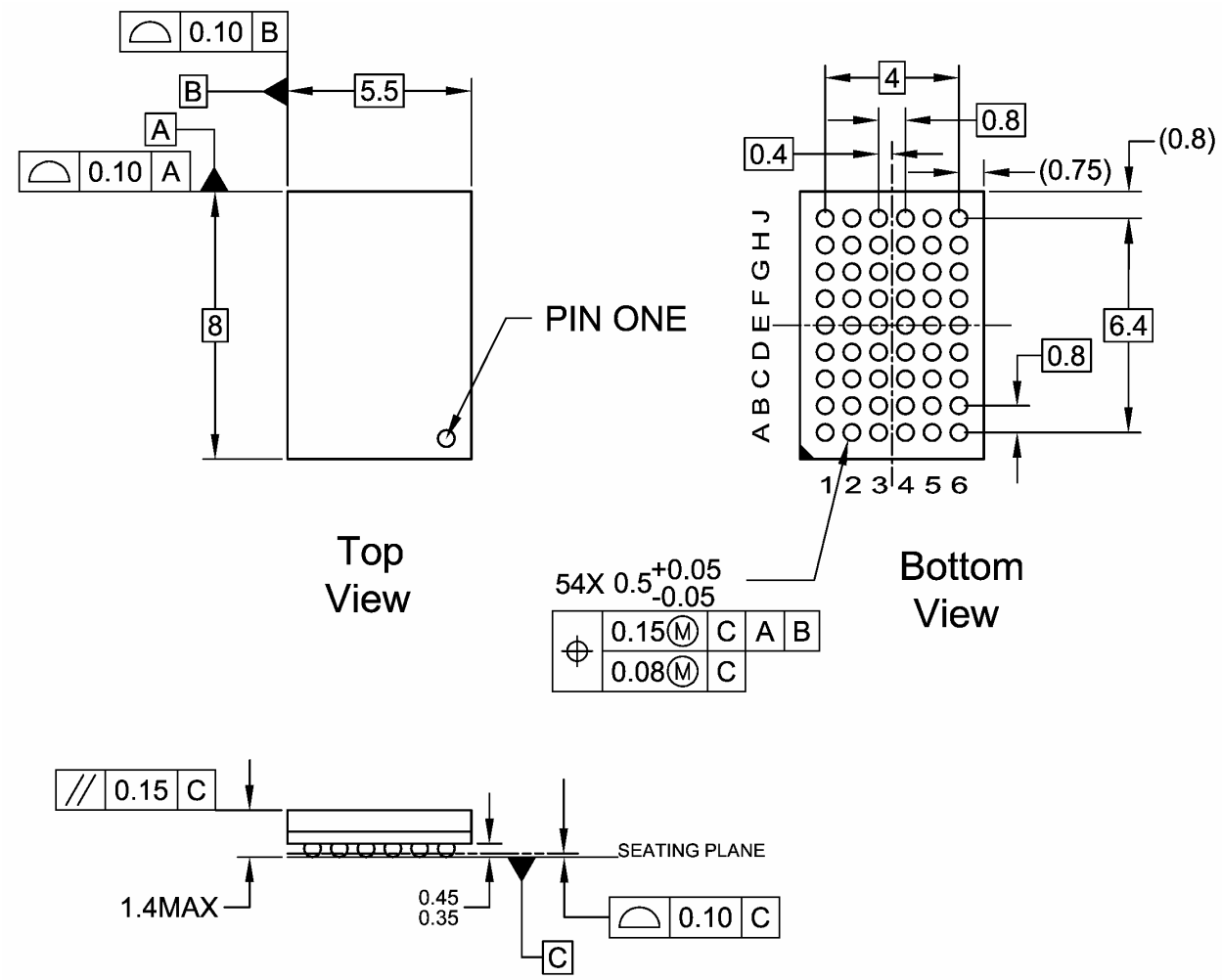


Figure 5. AC Waveforms

V_{CC}		
Symbol	**3.3V ± 0.3V**	**2.5V ± 0.2V**
V_{MI}	1.5V	$V_{CC}/2$
V_{MO}	1.5V	$V_{CC}/2$
V_{MVO}	0.3V	0.15V
V_{IN}	6.0V	2 x V_{CC}
V_{CCV}	3.0V	V_{CC}
t_r/t_f	2ns	2.5ns

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205

B. ALL DIMENSIONS IN MILLIMETERS

C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS

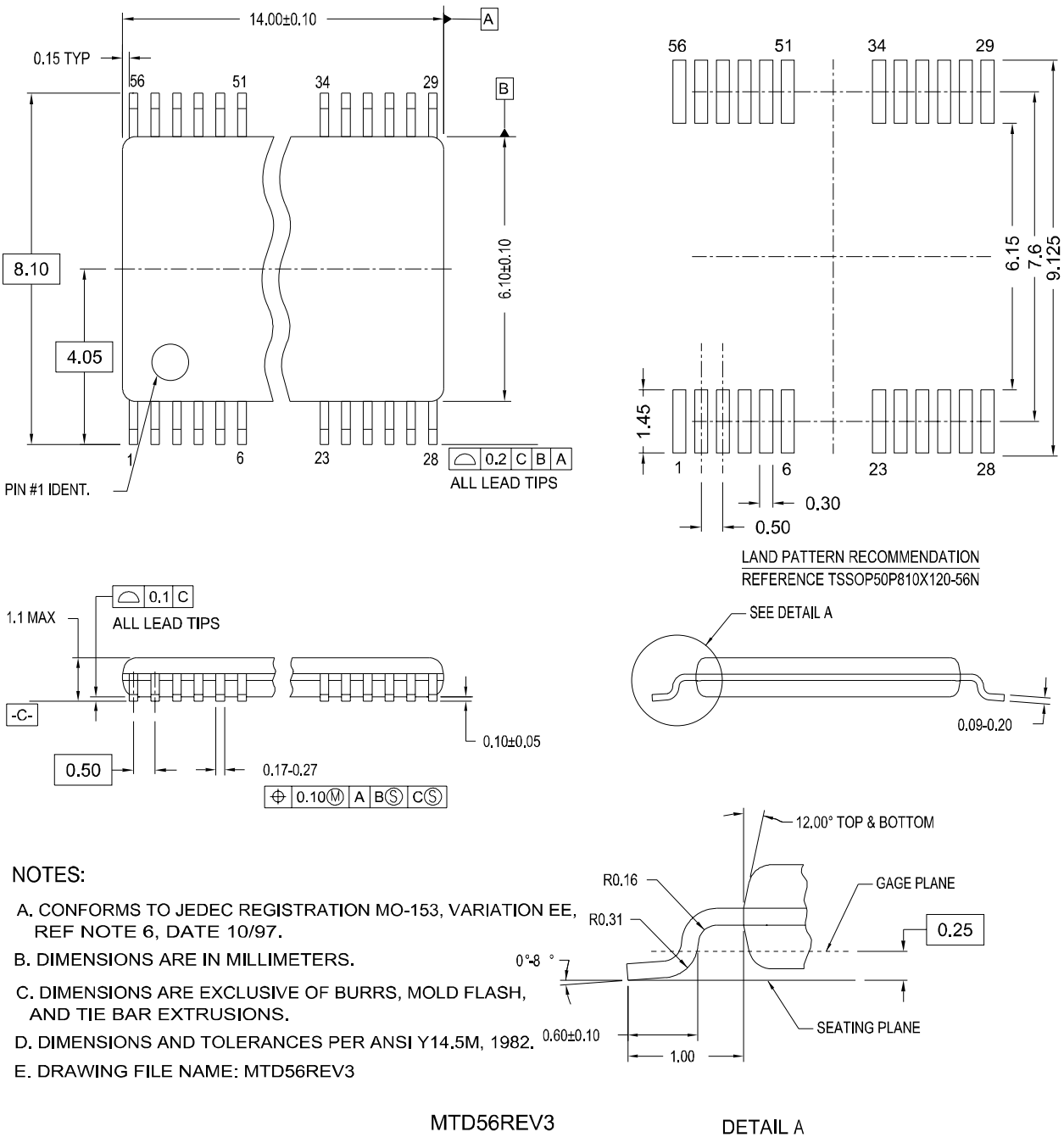
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

Figure 6. 54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

Physical Dimensions (Continued)

Dimensions are in millimeters (inches) unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION EE, REF NOTE 6, DATE 10/97.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

E. DRAWING FILE NAME: MTD56REV3

Figure 7. 56-Lead Thin-Shrink Small Outline Package (TSSOP), JEDEC MO153, 6.1mm Wide

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