STANDARD MICROSYSTEMS CORPORATION
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FDC37C65C+
PRELIMINARY

2.88MB Floppy Disk Controller

FEATURES

- Supports 1 Mbit/sec Data Rate
- Supports Vertical Recording Format
- Format Compatible with Intel 82077
- Pin-to-Pin Compatible with Industry Standard FDC37C65C and WD37C65C
- Licensed NEC 765B Core Provides the Correct Detection of All Overrun and Underrun Conditions
- Internal 16 Byte FIFO with Programmable Threshold
- Integrates Formatter/Controller, Data Separation, Write Precompensation, Data Rate Selection, Clock Generation, and Drive Interface Drivers and Receivers into One Chip
- IBM PC/AT Compatible Format (Single, Double and Extra Density)
- Provides Required Signal Qualification to DMA Channel (in PC/AT Mode)
- BIOS Compatible; Dual Speed Spindle Drive Support
- Enhanced Host Interface:
  - 100% AT Compatible
  - Capable of Driving 20 LS TTL Loads
  - Schmitt Trigger Inputs (Except Data Bus and XTAL)
- Compatible With 80X86 Family, PD8080/85/88, PD8086, and PD780 (Z-80®) Microprocessors
- Internal Address Mark Detection Circuitry
- Internal Power Up Reset Circuitry
- Provides Direct Interface to Floppy Disk Drives
- Provides the Disk Change and Disk Change Enable Inputs, Allowing Direct Connection of DCHG to the FDC37C65C+ with PLCC Package
- 48 mA Sink Drivers and Schmitt Trigger Line Receivers on Drive Interface
- 125, 250, 300, 500, & 1 Mbit/sec Data Rates
- Multisector and Multitrack Transfer Capability
- User Programmable Track Stepping Rate and Head Load/Unload Time
- Controls up to Four Floppy or Micro-Floppy Drives
- Data Transfer in DMA or Non-DMA Mode
- Parallel Seek Operations on up to Four Drives
- Integrates Improved Standard Microsystems FDC92C39 Digital Data Separator Algorithm
- Automatic Write Precompensation with Disable Option at 1 Mbit
- Power-Down Mode For Reduced Power Consumption
- On-Chip Clock Generation
- Available in Either 40-Pin DIP or 44-Pin PLCC
- XTAL Oscillator Circuits (PLCC)/TTL Clock Inputs (DIP) Allow for Use Of Non-Standard As Well As Standard Data Rates
- Low Power CMOS, +5 V Supply

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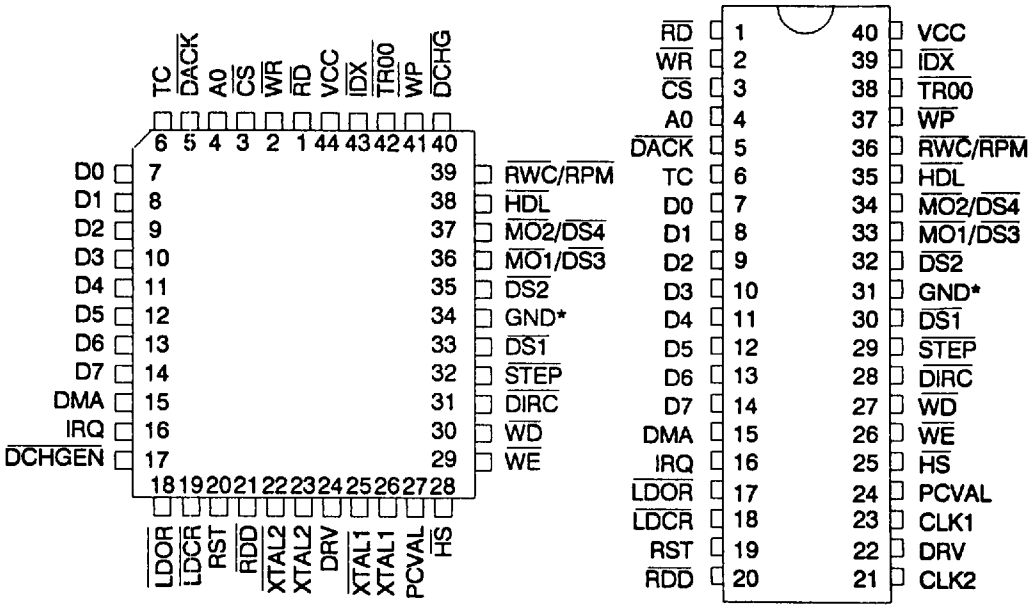
PIN CONFIGURATION



*Refer to Note in DC Electrical Characteristics

Package: 44-Pin PLCC or 40-Pin DIP

Ordering Information: FDC37C65C+LJ P for PLCC
FDC37C65C+ P for DIP

GENERAL DESCRIPTION

The FDC37C65C+ is a CMOS device which interfaces a host microprocessor to up to four floppy disk drives. It integrates the Formatter/Controller, Data Separator, Write *Precompensation* generator, Data Rate Selector, Clock Generator, and FIFO in one package. The FDC37C65C+ provides a complete microprocessor interface, a microsequencer, and a disk drive interface.

Toshiba vertical (perpendicular) recording is supported as well as conventional longitudinal format recording. This is required for the new 2.88MB floppy disk drives.

The microprocessor interface of the FDC37C65C+ supports a 12 MHz microprocessor bus without the use of wait states. For PC and PC/AT applications, the device provides qualification of interrupt and DMA requests.

The disk drive interface of the FDC37C65C+ directly connects to up to four drives. All drive-related outputs can sink 48 mA; all host related-outputs can sink 24 mA. All host- and drive-related inputs except for the data bus and crystal have internal Schmitt triggers.

The FDC37C65C+ uses two clock inputs which provide the necessary signals for internal timing. A 9600, 16/32 MHz oscillator handles the data rates of 1 Mbit, 500, 250, and 125 Kbits/sec. Internal crystal oscillator circuits may be used with the 44-pin PLCC package. The 40-pin DIP requires TTL clock inputs.

The FDC37C65C+ may be used in applications using two speed disk drives, such as AT compatible systems.

DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	DIP PIN NO.	NAME	SYMBOL	DESCRIPTION
			HOST PROCESSOR INTERFACE	
7-14	7-14	Data 0-7	D0-D7	Input/Output. The data bus connection used by the host microprocessor to transmit and receive data to and from the FDC37C65C+. These pins are in a high-impedance state when not in output mode.
1	1	$\overline{\text{Read}}$	$\overline{\text{RD}}$	Input. This active low signal is issued by the host microprocessor to indicate a read operation. A low level on this input when the FDC37C65C+ is selected enables data from the Buffer or Status Register onto the data bus for reading by the host.

DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	DIP PIN NO.	NAME	SYMBOL	DESCRIPTION
2	2	Write	$\overline{WR}$	Input. This active low signal is issued by the host microprocessor to indicate a write operation. A low level on this input when the FDC37C65C+ is selected enables data from the data bus to be written into the FDC37C65C+, latching the data on the rising edge.
3	3	Chip Select	$\overline{CS}$	Input. This active low signal issued by the host microprocessor allows data transfers to occur.
4	4	Address 0	A0	Input. This host processor signal determines whether data or status information will appear on the Data Bus. A low level selects the status level; a high level selects the data register.
15	15	Direct Memory Access Request	DMA	Output. This active high signal is a DMA request for byte transfers of data. This signal is cleared when the host responds with the $\overline{DACK}$ signal going low. This signal is normally driven in the Base Mode. When the FDC37C65C+ is in the Special or PC/AT mode, this pin is three-stated and is enabled by the DMAEN signal from the Digital Output Register.
5	5	DMA Acknowledge	$\overline{DACK}$	Input. A low level on this pin indicates a response by the host to a DMA request. It is used by the DMA controller to transfer data to or from the FDC37C65C+. Logical equivalent to $\overline{CS}$ and A0 = logic "1". In Special or PC/AT mode, this signal is qualified by DMAEN from the Digital Output Register.

DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	DIP PIN NO.	NAME	SYMBOL	DESCRIPTION
6	6	Terminal Count	TC	Input. This active high signal indicates to the FDC37C65C+ that data transfers are complete. In Base Mode, TC will be qualified by $\overline{DACK}$ only in DMA operations. In non-DMA (Programmed I/O) operations, $\overline{CS}$ and the $\overline{RD}$ and $\overline{WR}$ signals are used as a gating function. In Special or PC/AT mode, TC will always be qualified by $\overline{DACK}$ (whether in DMA or non-DMA operation), but will only be qualified by $\overline{DACK}$ if DMAEN from the Digital Output Register is a logic "1". If the FIFO is not enabled, all operations will terminate successfully with the use of TC qualified as described above. In non-DMA operations where TC is not used, the operations will terminate successfully but report termination errors on the completion of the command. If the FIFO is enabled, all DMA operations will terminate successfully.
16	16	Interrupt	IRQ	Output. This interrupt indicates the completion of command execution and in non-DMA operation also indicates data transfer requests. This signal is normally driven in the Base mode. When the FDC37C65C+ is in the Special or PC/AT mode, this pin is three-stated and is enabled by the DMAEN signal from the Digital Output Register.
18	17	$\overline{\text{Load Digital Output Register}}$	$\overline{LDOR}$	Input. Active low Digital Output Register load enable. When $\overline{LDOR}$ and $\overline{WR}$ are low, the Data Bus is enabled into the Digital Output Register, latching on the rising edge of $\overline{LDOR}$ and $\overline{WR}$. When $\overline{LDOR}$, $\overline{LDCR}$ and $\overline{WR}$ are low, the Format Control Register is selected.

DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	DIP PIN NO.	NAME	SYMBOL	DESCRIPTION
19	18	Load Data Rate Selection Register	LDCR	Input. This active low signal allows access to the Data Rate Selection Register and Format Control Register. When LDCR and WR are low, DB0, DB1 and DB3 of the Data Bus are enabled into this register, latching on the rising edge of LDOR or WR. When LDCR, RD, and DCHGEN are low, the DCHG input status is carried on bit D7 of the Data Bus, while bits D0-D6 remain in the high impedance state. When LDOR, LDCR and WR are low, the Format Control Register is selected.
20	19	Reset	RST	Input. This active high signal resets the FDC37C65C+. When RST occurs, the FDC37C65C+ defaults to Base Mode and the data rate is defaulted to 250K MFM (or 125K FM, code dependent, CLK1 = 16 MHz). When RST is active, the high current driver outputs to the disk drive are disabled.
		DRIVE INTERFACE		
21	20	Read Disk Data	RDD	Input. Raw serial bit stream from the disk drive. Each falling edge represents a flux transition of the encoded data.
29	26	Write Enable	WE	Output. This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
30	27	Write Data	WD	Output. This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media. This output is enabled only when Write Enable is low.
28	25	Head Select	HS	Output. This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed.

DESCRIPTION OF PIN FUNCTIONS

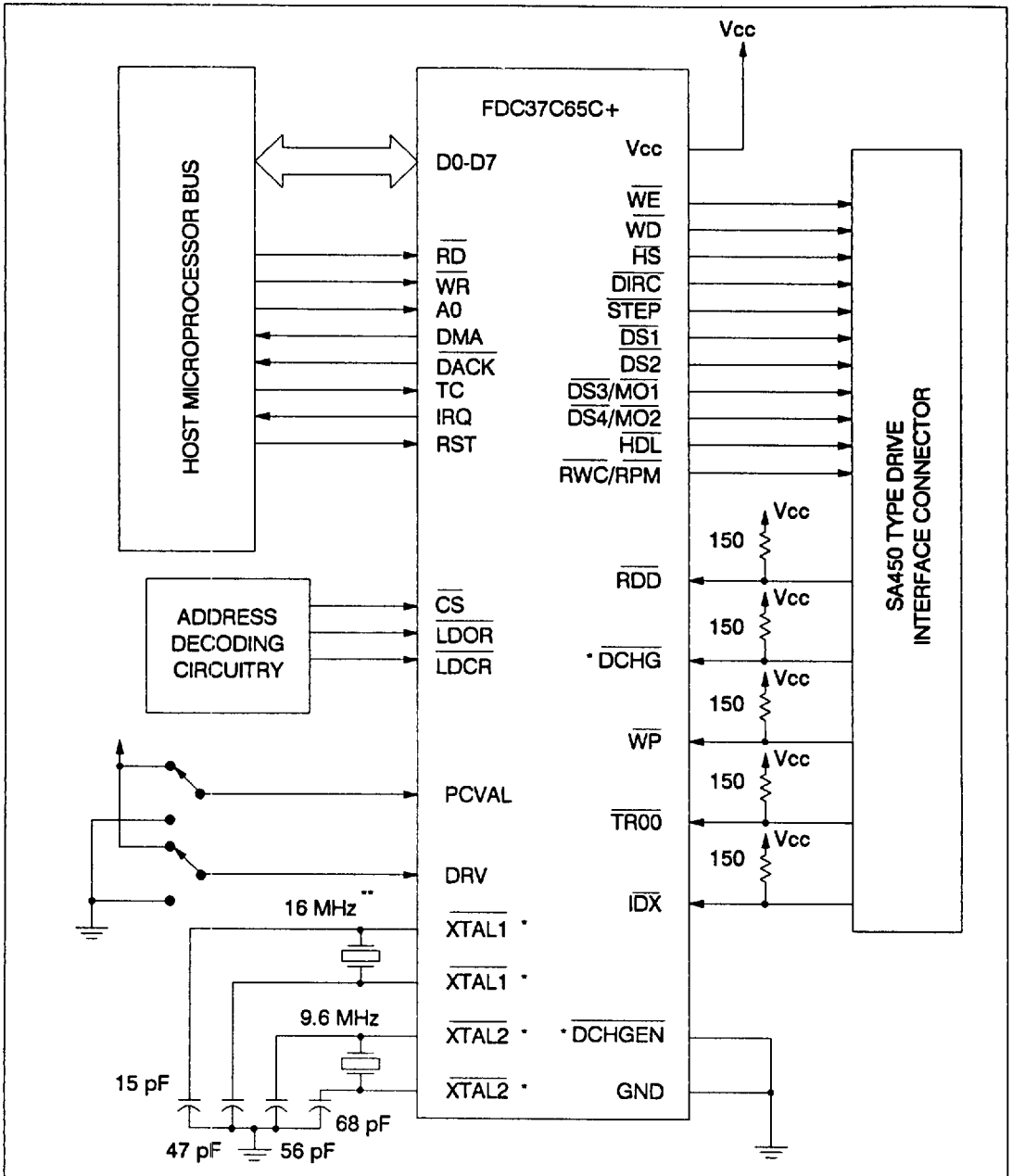
PLCC PIN NO.	DIP PIN NO.	NAME	SYMBOL	DESCRIPTION
31	28	$\overline{\text{Direction Control}}$	$\overline{\text{DIRC}}$	Output. This high current output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion.
32	29	$\overline{\text{Step Pulse}}$	$\overline{\text{STEP}}$	Output. This active low high current driver issues a low pulse for each track-to-track movement of the head.
40	N/A	$\overline{\text{Disk Change}}$	$\overline{\text{DCHG}}$	Input. This active low input senses from the disk drive that the drive door is open or that the diskette has possibly been changed since the last drive selection.
17	N/A	$\overline{\text{Disk Change Enable}}$	$\overline{\text{DCHGEN}}$	Input. This active low input enables the $\overline{\text{DCHG}}$ input status onto D7 during a read of the Digital Input Register. This signal is connected to an internal pull-up resistor.
33	30	$\overline{\text{Drive Select 1}}$	$\overline{\text{DS1}}$	Output. This is an active low output. When the FDC37C65C+ is in the PC/AT/EISA Mode, a logic "0" on DSEL and a logic "1" on MOEN1 from the Digital Output Register will cause $\overline{\text{DS1}}$ to enable the Drive 1 interface. When the FDC37C65C+ is in the Base Mode or the Special Mode, $\overline{\text{DS1}}$ is number 1 of the four decoded Unit Selects, as specified in the device command, and the Digital Output Register has no effect.
35	32	$\overline{\text{Drive Select 2}}$	$\overline{\text{DS2}}$	Output. This is an active low output. When the FDC37C65C+ is in the PC/AT Mode, a logic "1" on DSEL and a logic "1" on MOEN2 from the Digital Output Register will cause $\overline{\text{DS2}}$ to enable the Drive 2 interface. When the FDC37C65C+ is in the Base Mode or the Special Mode, this output is number 2 of the four decoded Unit Selects, as specified in the device command, and the Digital Output register has no effect.

DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	DIP PIN NO.	NAME	SYMBOL	DESCRIPTION
36	33	Motor On 1/Drive Select 3	MO1/DS3	Output. This is an active low output. When the FDC37C65C+ is in the PC/AT Mode, a logic "1" on MOEN1 from the Digital Output Register will cause this output to go low, thereby acting as the Motor-On Enable for Drive 1. When the FDC37C65C+ is in the Base Mode or the Special Mode, this output is number 3 of the four decoded Unit Selects, as specified in the device command, thereby acting as drive select 3, and the Digital Output Register has no effect.
37	34	Motor On 2/Drive Select 4	MO2/DS4	Output. This is an active low output. When the FDC37C65C+ is in the PC/AT Mode, a logic "1" on MOEN2 from the Digital Output Register will cause this output to go low, thereby acting as the Motor-On Enable for Drive 2. When the FDC37C65C+ is in the Base Mode or the Special Mode, this output is number 4 of the four decoded Unit Selects, as specified in the device command, thereby acting as drive select 4, and the Digital Output Register has no effect.
38	35	Head Loaded	HDL	Output. This active low high current driving signal causes the head to be loaded against the media in the selected drive.
39	36	Reduced Write Current/ Revolutions Per Minute	RWC/RPM	Output. This active low signal occurs when tracks greater than 43 are being accessed, and the inner track location has caused increased bit density. This signal, valid in the Base Mode and the Special Mode, indicates that write precompensation is necessary. In the PC/AT mode, this signal may be used to select a 300 RPM spindle rate on two speed drives when 250 Kbps MFM is selected.
41	37	Write Protected	WP	Input. This active low Schmitt Trigger input senses from the disk drive that a disk is write protected.
42	38	Track 00	TR00	Input. This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.

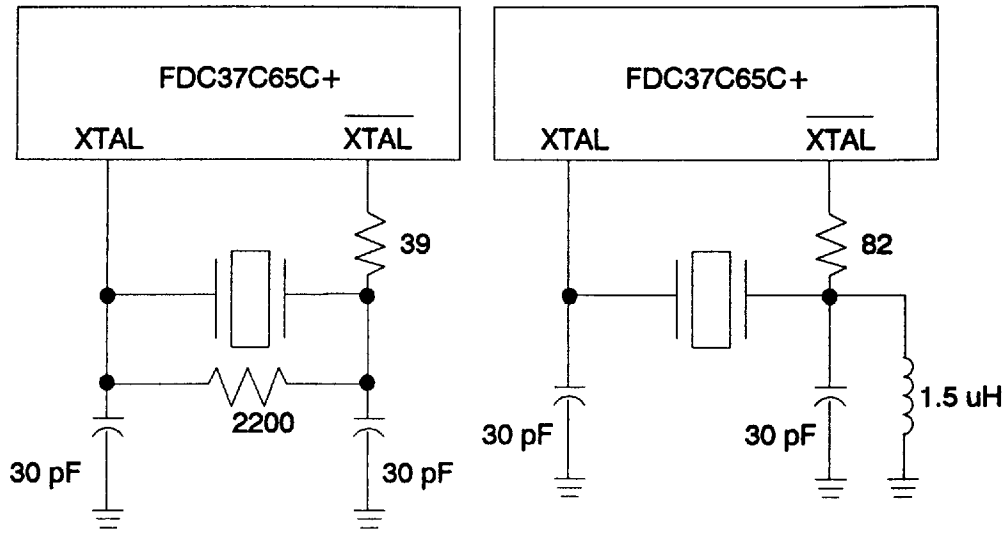
DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	DIP PIN NO.	NAME	SYMBOL	DESCRIPTION
43	39	$\overline{\text{Index}}$	$\overline{\text{IDX}}$	Input. This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
27	24	Precom-pensation Value	PCVAL	Input. The level on this pin determines the amount of write precompensation to be used on the inner tracks of the diskette. When precompensation is disabled, this pin has no effect. This input has an internal pull up resistor.
24	22	Drive Type	DRV	Input. This input is used to indicate the drive type being used. A logic "0" on this input indicates a two speed spindle motor, in which case the second clock input should be grounded. This signal is connected to an internal pull-up resistor.
MISCELLANEOUS				
N/A	23	CLOCK 1	CLK1	16 or 32 MHz TTL level clock input for all standard data rates. The frequency should be accurate to within 0.1% and may have a 40% to 60% duty cycle.
N/A	21	CLOCK 2	CLK2	TTL level clock input for non-standard data rates. The frequency is selected from the Data Rate Selection Register in Table 1.
25,26	N/A	$\overline{\text{Crystal 1}}$, Crystal 1	$\overline{\text{XTAL1}}$, XTAL1	An external 16 MHz or 32 MHz parallel resonant crystal should be connected to these pins for all standard data rates. If an external 16 MHz or 32 MHz TTL clock is used instead, it should be connected to XTAL1 and $\overline{\text{XTAL1}}$ should be left floating.
22,23	N/A	$\overline{\text{Crystal 2}}$, Crystal 2	$\overline{\text{XTAL2}}$, XTAL2	An external parallel resonant crystal should be connected to these pins for all non-standard data rates. If an external TTL clock is used instead, it should be connected to XTAL2 and $\overline{\text{XTAL2}}$ should be left floating.
44	40	Power	V_{CC}	+ 5 Volt supply pin.
34	31	Ground	GND	Ground pin. (Refer to note in DC Electrical Characteristics



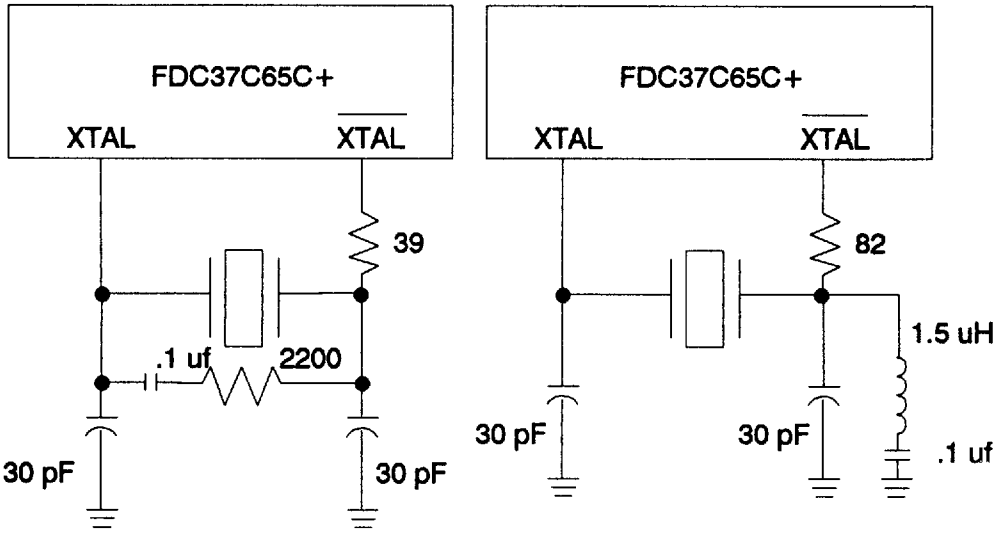
* These signals exist only for PLCC package.
** 32 MHz for 1 Mbit.

FIGURE 1 - TYPICAL SYSTEM BLOCK DIAGRAM



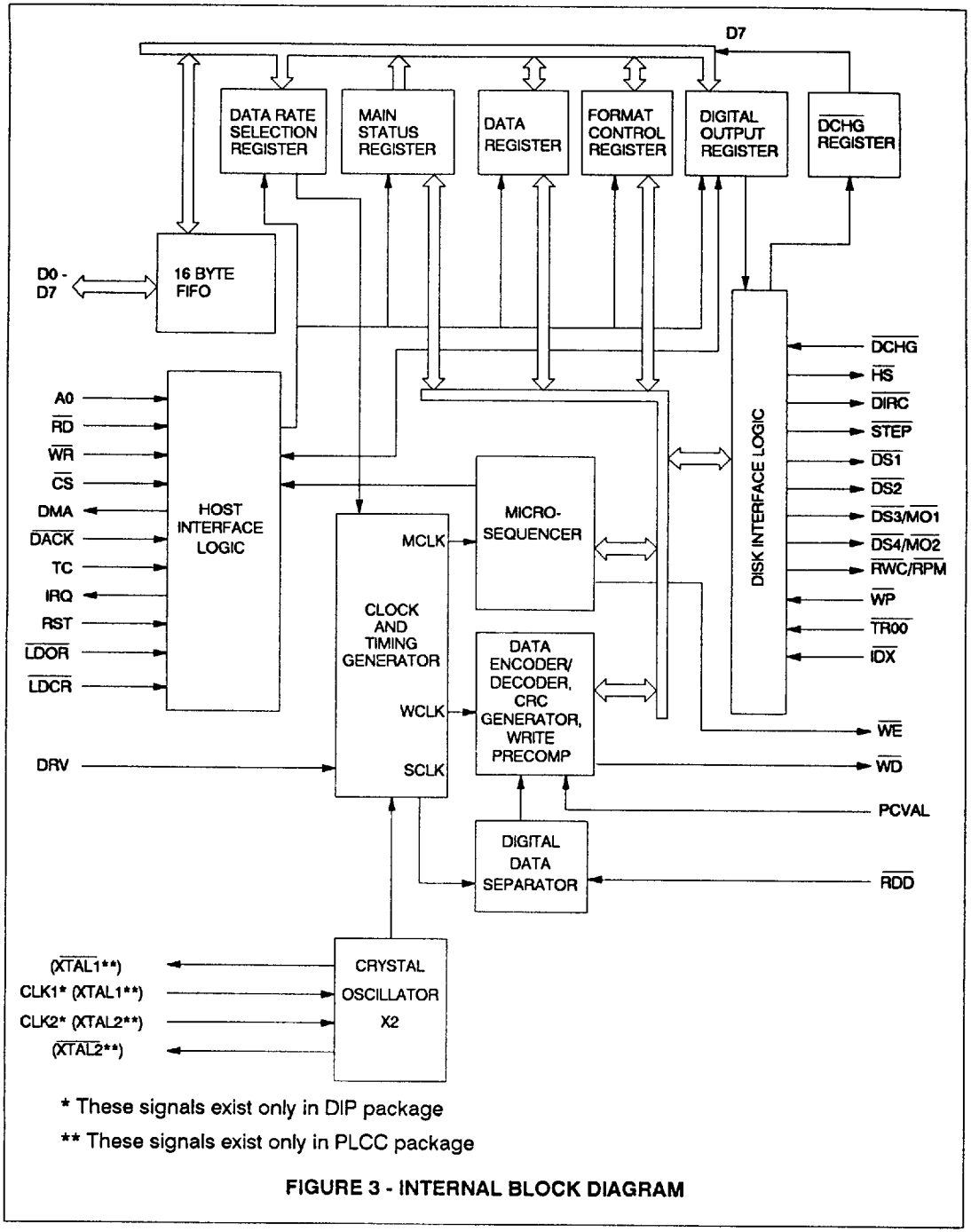
Crystal: 32 MHz, Parallel Resonant, Third Overtone
Source: Ecliptek Part No. EC 320-32 00 MHz or equivalent

FIGURE 2 - SUGGESTED OSCILLATOR CIRCUITS



Crystal: 32 MHz, Parallel Resonant, Third Overtone
Source: Ecliptek Part No. EC 320-32 00 MHz or equivalent

FIGURE 2A - SUGGESTED LOW POWER OSCILLATOR CIRCUITS



* These signals exist only in DIP package

** These signals exist only in PLCC package

FIGURE 3 - INTERNAL BLOCK DIAGRAM

SYSTEM DESCRIPTION

The system block diagram in Figure 1 illustrates a complete implementation of the FDC37C65C+ used in a floppy disk drive system. The FDC37C65C+ provides simple interfacing to both the microprocessor and the drive.

MICROPROCESSOR INTERFACE

The left half of Figure 1 illustrates a typical FDC37C65C+ interface to the microprocessor. It consists of an 8-bit data bus and a control bus. All signals are directly connected to the host, eliminating the need for external circuitry. All inputs to the FDC37C65C+ (except for the data bus) are Schmitt triggers and the outputs to the host are able to sink 24 mA. The FDC37C65C+ contains the following internal registers for interfacing to the host microprocessor: Data Rate Selection Register, Main Status Register, Data Register, Digital Output Register, and Perpendicular Format Register. The Data Rate Selection Register selects the data rate for internal clock generation and synchronization of disk data transfers. The Main Status Register contains information related to the status of the drives and provides handshaking functions for the microprocessor. The Data Register is used in data transfers with the drive during Read and Write operations, and holds the command blocks issued by the microprocessor and the results after the command is executed. The Digital Output Register provides the Motor On and Drive Select signals and the DMA Enable qualifier for the DMA and IRQ outputs. The Format Control Register provides FIFO operation control and selects longitudinal or vertical recording.

DRIVE INTERFACE

The right half of Figure 1 illustrates a typical FDC37C65C+ interface to up to four drives. All signals are directly connected to the drives, eliminating the need for external circuitry. All inputs to the FDC37C65C+ are Schmitt triggers and the outputs are open-drain, 48 mA drivers. The FDC37C65C+ contains the Standard Microsystems FDC92C39 algorithm, which provides Data Separation as well as Automatic Write Precompensation. The FDC37C65C+ also provides the $\overline{\text{DCHG}}$ and $\overline{\text{DCHGEN}}$ signals, which provide the option of connecting the $\overline{\text{DCHG}}$ signal directly to the FDC37C65C+ so that the $\overline{\text{DCHG}}$ status may be supplied to the host microprocessor via D7 of the data bus.

FUNCTIONAL DESCRIPTION

Refer to Figure 3 for Internal Block Diagram of the FDC37C65C+.

HOST INTERFACE LOGIC

NON-FIFO MODE

The internal registers are used chiefly in writing commands to, and reading status from, the FDC37C65C+. In the interfacing of the internal registers to the host, the user must keep in mind a few considerations. During the Command Phase of a command, the Main Status Register must be read before each byte of the command word is written into the data register to ensure that bits D6 and D7 are logic "0" and "1 ", respectively. During the Result Phase of a command, the Main Status Register must be read before each result byte from the data register is read to ensure that bits D6 and D7 are both logic "1 ". The user should ensure that 12 μs elapses before each access of the

Main Status Register by the CPU. To avoid waiting 12 μs before each access to the Main Status Register in a Command Phase, the user may save time by polling D6 and D7 of the Main Status Register for the appropriate bit settings. When the correct bit settings appear, the FDC37C65C+ is ready for commands. No access of the Main Status Register is necessary in the execution phase of a command. During the execution phase, each receipt of a data byte from the drive is indicated by an interrupt signal on the IRQ pin when the FDC37C65C+ is in the non-DMA mode. The generation of a Read or Write signal clears the interrupt and outputs the data onto the data bus. If the processor cannot respond to the interrupts quickly enough (every 13 μs for MFM and 27 μs for FM), then it may poll the Main Status Register and bit D7 functions as the interrupt signal. If a Write command is in process, then the Write signal performs the reset to the interrupt.

The timing parameters mentioned above will double for mini floppy data rates. After an interrupt in the non-DMA Mode, the Main Status Register must be examined to determine the cause, since it could be a data interrupt or a command termination interrupt, either normal or abnormal. In the DMA Mode, no interrupt signals occur during the Execution Phase. Instead. a DMA Request is generated and the DMA controller responds with a DMA Acknowledge and either a Read or a Write, which clears the DMA Request. After the completion of the Execution Phase or the EOT sector has been read or written, an interrupt will occur, signifying the beginning of the Result Phase. The reading of the first byte of data from the Data Register clears the interrupt. In PC/AT use, since non-DMA host transfers are not normally used, the FDC37C65C+ will successfully complete commands but will always give abnormal termination error status, since the TC signal is qualified by the DACK signal.

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while DACK is true and the $\overline{CS}$ signal is gated with $\overline{RD}$ and $\overline{WR}$ during programmed I/O operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA Mode is being used, the $\overline{DACK}$ signal should be pulled up to V_{CC}.

During the Result Phase of a command, all bytes from the Data Register must be read in order to successfully complete the command, and the FDC37C65C+ will not accept a new command until all bytes have been read. The bytes in the Command Phase and the Result Phase must be written and read in the exact order as seen in the Commands section of this document. No shortening of the phases is allowed. The last byte sent to the FDC37C65C+ in a Command Phase causes the Execution Phase to automatically begin and when the last data byte is read out in the Result Phase, the command is automatically ended, making the FDC37C65C+ ready for a new command.

INTERNAL REGISTERS

The FDC37C65C+ contains ten internal registers to facilitate the interfacing between the host microprocessor and the disk drive, as well as a FIFO. The ten registers consist of the Data Rate Selection Register, the Main Status Register, Status Registers 0-3, the Data Register, the Digital Output Register,the Digital Input Register, and the Format Control Register. Table 1 shows the bit combinations required to access the registers. Combinations other than the ones shown are illegal.

Table 1 - Register Accesses

DCHGEN	$\overline{CS}$	A0	$\overline{LDCR}$	$\overline{LDOR}$	$\overline{RD}$	$\overline{WR}$	FUNCTION	ADDR
X	0	0	1	1	1	0	Write Master Status Register[1,2]	3F4H
X	1	X	1	0	1	0	Write Digital Output Register	3F2H
X	0	0	1	1	0	1	Read Main Status Register	3F4H
X	0	1	1	1	0	1	Read Data Register	3F5H
X	0	1	1	1	1	0	Write Data Register	3F5H
0	1	X	0	1	0	1	Read Digital Input Register	3F7H
X	1	X	0	1	1	0	Write Data Rate Selection Register	3F7H
X	X	X	0	0	1	0	Write Format Control Register	User Defined
X	X	X	X	X	0	0	Illegal	

Status Registers 0-3 are available only in the result phase of a command and may be read only after the completion of the command.

[1] DB0 = 1
[2] $\overline{CS}$ = $\overline{WR}$ = 0 is allowed when A0 = 0, the RST pin is inactive, and bit 2 of the Digital Output Register = 1 (Software Reset disabled). This places the FDC37C65C+ into the Power Down Mode.

Data Rate Selection Register

The Data Rate Selection Register provides support logic that latches the DB0, DB1, and DB3 of the data bus upon receiving $\overline{LDCR}$ and $\overline{WR}$. These bits are used to select the desired data rate which, in turn, controls the internal clock generation. When the data rate is switched, the clock is de-glitched to allow for continuous operation. If the Data Rate Selection Register is not being used, the data rate is determined by the supplied clock or crystal. The frequency is 64 times the desired MFM data rate up to a maximum clock frequency of 32 MHz. Therefore, the maximum data rate that can be used without the use of the Data Rate Selection Register is 250 Kbits/s. Refer to Table 2 for manipulation of the Data Rate Selection Register. When bit D3 of the Data Selection Register is "1", and bit D5 of the Format Control Register is "1" (Enhanced Mode), an internal divider is enabled, allowing 500, 250, 125 Kbits/s operations with a 32 MHz clock.

Digital Input Register

When $\overline{LDCR}$ and $\overline{RD}$ are active together and Disk Change Enable ($\overline{DCHGEN}$) is low, DB7 is driven with the inverted value of the $\overline{DCHG}$ input. Bits DB6-DB0 remain tristated.

Table 2A - Data Rate Selection Register - 32 MHz*

DB3	DB1	DB0	DRV	ENCODING SCHEME	DATA RATE (KBITS/s)	RPM (in PC/AT/ EISA Mode)
X	0	0	X	MFM	500	1
X	0	0	X	FM	250	1
X	0	1	0	MFM	250	0
X	0	1	1	MFM	300	0
X	1	0	X	MFM	250	1
X	1	0	X	FM	125	1
X	1	1	X	FM	125	0

Table 2B - Data Rate Selection Register - 32 MHz**

DB3	DB1	DB0	DRV	ENCODING SCHEME	DATA RATE (BITS/S)	RPM (in PC/AT/ EISA Mode)
1	0	0	X	MFM	1M	1
1	0	0	X	FM	500k	1
1	0	1	0	MFM	500k	0
1	0	1	1	MFM (9.6 MHz XTAL)	300k	0
1	1	0	X	MFM, RST	500k	1
1	1	0	X	FM, RST	250k	1
1	1	1	X	FM	250k	0
0	0	0	X	MFM	500k	1
0	0	0	X	FM	250k	1
0	0	1	0	MFM	250k	0
0	0	1	1	MFM	300k	0
0	1	0	X	MFM, RST Default	250k	1
0	1	0	X	FM, RST Default	125k	1
0	1	1	X	FM	125k	0

*Bit DB5 of the Format Control Register must be set to "0".
**Bit DB5 of the Format Control Register must be set to "1", Enhanced Mode.

The FDC37C65C+ also supports 150 Kbit/s FM data transfer as shown in Table 2C. This data rate is selected by driving CLK1 or XTAL1 with 9.6 MHz.

Table 2C - Data Rate Selection Register - 150/300 Kbit/s Option

DB1	DB0	DRV	ENCODING SCHEME	DATA RATE (KBITS/S)	RPM (in PC/AT/ EISA Mode)
0	1	1	MFM	300	0
0	1	1	FM	150	0

The Write Precompensation may be disabled in the PC/AT/EISA mode by writing a logic high to bit 2 of the Control Register. Please note that a hardware reset will reset bit 2 to a logic low, re-enabling Write Precompensation.

Table 2D - PC/AT and EISA Mode Control Register Configuration

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION	CLOCK QUALIFIER
0	Data Rate	0	None
1	Data Rate	1	None
2	No Write Precomp	0	None
3	Data Rate	÷2	None
4-7	Reserved	None	None

Main Status Register

The Main Status Register is an 8-bit register that contains the status information of the FDC37C65C+, and may be accessed at any time. Only the Main Status Register may be accessed to facilitate the transfer of data between the microprocessor and the FDC37C65C+. That is, Status Registers 0-3 may be read only after the completion of a command and provide no assistance in the transfer of data between the microprocessor and the FDC37C65C+. Each time the Main Status Register is accessed, the microprocessor should wait 12 μs if 500 kbits/sec MFM is selected as the data rate, 6 μs if 1 Mbit/sec is selected, and 24 μs if 250 kbits/sec MFM is selected. Refer to Table 3 for the contents of the Main Status Register.

Table 3 - Main Status Register Read

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	FDD 0 Busy	D0B	A high level on this bit indicates that drive 0 is in the Seek Mode and that the FDC37C65C+ will not accept READ or WRITE commands.*
1	FDD 1 Busy	D1B	A high level on this bit indicates that drive 1 is in the Seek Mode and that the FDC37C65C+ will not accept READ or WRITE commands.
2	FDD 2 Busy	D2B	A high level on this bit indicates that drive 2 is in the Seek Mode and that the FDC37C65C+ will not accept READ or WRITE commands.
3	FDD 3 Busy	D3B	A high level on this bit indicates that drive 3 is in the Seek Mode and that the FDC37C65C+ will not accept READ or WRITE commands.
4	FDC Busy	CB	A high level on this bit indicates that a READ or WRITE command is in progress and that the FDC37C65C+ will not accept any other command.
5	Execution Mode	EXM	A high level on this bit indicates that the FDC37C65C+ is in the Execution Phase in Non-DMA Mode. When this bit goes low, the Execution Phase has ended and the Results Phase has begun. This bit operates only in the Non-DMA Mode.
6	Data	DIO	A high level on this bit indicates that the direction of data transfer is from the Data Register to the microprocessor. A low level on this bit indicates that the direction of data transfer is from the microprocessor to the Data Register.
7	Request	RQM	A high level on this bit indicates that the Data Register is ready to send or receive data to or from the microprocessor. Both the DIO and the RQM bits should be used to perform the "ready" and "direction" handshaking functions to the host.

*Note: A write to the Main Status Register ($\overline{CS}$ = $\overline{WR}$ = 0) when bit DB0 = 1, bit DB2 of the Digital Output Register = 1 and A0 = RST = 0, will place the FDC37C65C+ in the Power Down Mode.

Table 4 - Master Status Register Write

BIT NO.	SIGNAL NAME & FUNCTION	RESET CONDITION	CLOCK QUALIFIER
0	Power Down Mode (PDM)	0	None
1-7	Reserved	None	None

The Main Status Register of the FDC37C65C+ is a Read/Write Register; the write configuration is used for the Power Down mode only. This new Write Only Register is called the Master Status Register 1 (MSR1). Master Status Register 1 (MSR1): $\overline{CS}=0$, AO=0, Write Only.

Table 5 - Power Down Feature

BIT	SIGNAL NAME	FUNCTION
0	Power Down Mode	If logic = 1, causes FDC to enter in power down mode If logic = 0, normal operation

Status Registers 0-3

Status Registers 0-3 are each 8 bit registers that contain status information on the FDC37C65C+ and are available only in the Result Phase and may be read only after completing a command. The command that has been executed determines which of the Status Registers will be read. Refer to Tables 6-9 for the contents of Status Registers 0-3.

Table 6 - Status Register 0

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Unit Select 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.
1	Unit Select 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
2	Head Select	HS	This flag is used to indicate the state of the head at interrupt.
3	Not Ready	NR	This bit will always be a logic "0", since Drive Ready is always presumed to be true.
4	Equipment Check	EC	A high level on this bit indicates that the Track 0 signal has failed to occur after 255 step pulses (Recalibrate Command).
5	Seek End	SE	A high level on this bit indicates that the FDC37C65C+ has completed the seek command.
6,7	Interrupt Code	IC	The four combinations of these bits indicate four different situations: 7 6 0 0 Normal Termination of command was completed and properly executed. 0 1 Abnormal Termination (AT) of command. Execution of command was started but not successfully completed. 1 0 Invalid Command (IC) issue. Command which was issued was never started. 1 1 Abnormal Termination (AT) of command. During execution of command, the ready signal from drive changed state.

Table 7 - Status Register 1

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Missing Address Mark	MA	A high level on his bit indicates that the FDC37C65C+ cannot detect the Data Address Mark or the Deleted Data Address Mark. In this case, the MD bit of Status Register 2 is also set to a logic "1".
1	Not Writable	NW	A high level on this bit indicates that, during execution of the WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK Command, the FDC37C65C+ has detected a $\overline{WP}$ signal from the drive, indicating that the diskette is write protected.
2	No Data	ND	A high level on this bit indicates one of three conditions. Either 1) during the execution of the READ DATA, READ DELETED DATA, WRITE DATA or WRITE DELETED DATA Command, the FDC37C65C+ cannot find the sector specified in the Internal Data Register, or 2) during the execution of the READ ID Command, the FDC37C65C+ cannot read the ID field without an error, or 3) during the execution of the READ A CYLINDER Command, the starting sector cannot be found.
3	(not used)		This bit is not used and is always at a logic "0".
4	Overrun)	OR	A high level on this bit indicates that the FDC37C65C+ has not been serviced by the microprocessor during data transfers within a certain time interval.
5	Data Error	DE	A high level on this bit indicates that the FDC37C65C+ has detected a Cyclic Redundancy Check Error in either the ID field or the data field.
6	(not used)		This bit is not used and is always at a logic "0".
7	End of Cylinder	EN	A high level on this bit indicates that the FDC37C65C+ has tried to access a sector beyond the final sector of a cylinder.

Table 8 - Status Register 2

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Missing Address Mark in Data Field	MD	A high level on this bit indicates that the FDC37C65C+, upon reading data from the drive, cannot find a Data Address Mark, or Deleted Data Address Mark.
1	Bad Cylinder	BC	A high level on this bit indicates that the contents of the cylinder on the medium is different from that stored in the Internal Data Register and the contents of the cylinder is FFH. This bit is related to the ND (No Data) bit of Status Register 1.
2	Scan Not Satisfied	SN	A high level on this bit indicates that, during the execution of a SCAN Command, the FDC37C65C+ cannot find a sector on the cylinder which meets the specified condition.
3	Scan Equal Hit	SH	A high level on this bit indicates that, during the execution of a SCAN command, the condition of "equal" has been satisfied.
4	Wrong Cylinder	WC	A high level on this bit indicates that the contents of the cylinder on the medium is different from that stored in the Internal Data Register. This bit is related to the ND (No Data) bit of Status Register 1.
5	Data Error	DE	A high level on this bit indicates that the FDC37C65C+ has detected a Cyclic Redundancy Check Error in the data field.
6	Control Mark	CM	A high level on this bit indicates that, during the execution of the READ DATA or SCAN Command, the FDC37C65C+ has encountered a sector which contains a Deleted Data Address Mark.
7	(not used)		This bit is not used and is always at a logic "0".

Table 9 - Status Register 3

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Unit Select 0	US0	This bit is used to indicate the status of the Unit Select 0 signal to the drive.
1	Unit Select 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the drive.
2	Head Address	HD	This bit is used to indicate the status of the Side Select signal to the drive.
3*			This bit is always a logic 1.
4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal to the drive.
5	Ready	RY	This bit is always a logic "1".
6	$\overline{\text{Write Protected}}$	$\overline{\text{WP}}$	This bit is used to indicate the status of the $\overline{\text{WRITE PROTECTED}}$ signal from the drive.
7	Fault	FT	This bit is always a logic "0".

*NOTE: Different from NEC765 and WD37C65

Data Register

The Data Register is an 8-bit register which stores data, commands, parameters, and drive status information. Data is read from or written to the Data Register in order to program or obtain results of a command that has been issued.

Digital Output Register

The Digital Output Register provides for selection of the disk drive and control of the disk drive spindle motors. These selections are typically implemented with the standard latched port found in floppy disk subsystems. The Digital Output Register provides support logic that latches the data bus upon receiving the $\overline{\text{LDOR}}$ and $\overline{\text{WR}}$ signals. Refer to Table 10 for the contents of the Digital Output Register.

FIFO

All disk data transfers and command parameter information pass through the 16 byte FIFO. The FIFO has a programmable threshold (see Format Control Register) for fine-tuning system performance. The FIFO defaults to transparent operation after a reset to ensure FDC37C65C compatibility.

The FIFO is transparent at the beginning of a command. The FIFO is cleared as the FDC37C65C+ begins command execution to avoid the transfer of invalid data.

FIFO Use During Verify Mode Operation

When the BIOS or firmware performs a VERIFY SECTOR operation, the DMA is placed into Verify Transfer Mode. In this mode, the DMA

does not read any data from the floppy controller. This mode of operation requires the use of special hardware and software to allow this to work when a FIFO is used. This hardware is included in the FDC37C65C+. To enable this hardware, the BIOS or firmware must set bit D6 of the FORMAT CONTROL register during a verify sector operation and ensure that it is cleared at all other times. The DMA must be in SINGLE TRANSFER MODE during the verify operation (it must be in SINGLE TRANSFER MODE at all times). This will ensure that there is one $\overline{DACK}$ for each byte.

Table 10 - Digital Output Register

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Drive Select	DSEL	A low level on this bit, when MOEN 1 is a logic "1", activates a $\overline{DS1}$ ($\overline{Drive\ Select\ 1}$ output pin). A high level on this bit, when MOEN2 is a logic "1" activates $\overline{DS2}$ ($\overline{Drive\ Select\ 2}$ output pin). This bit only activates $\overline{DS1}$ or $\overline{DS2}$ when the FDC37C65C+ is in PC/AT/EISA Mode.
1	$\overline{Drive\ Select\ Enable}$	$\overline{DSELEN}$	A low level on this bit enables $\overline{DS1}$ and $\overline{DS2}$ to become active.
2	$\overline{Soft\ Reset}$	$\overline{SRST}$	A low level on this bit provides for soft reset of the FDC37C65C+.
3	DMA Enable	DMAEN	This bit, active in Special Mode and PC/AT/EISA Mode, qualifies the DMA and IRQ outputs and the $\overline{DACK}$ input.
4	Motor 1 On Enable	MOEN1	The MO1 signal is the inverted output of this signal, which is active only in the PC/AT/EISA Mode.
5	Motor 2 On Enable	MOEN2	The MO2 signal is the inverted output of this signal, which is active only in the PC/AT/EISA Mode.
6	(not used)		This bit is not used.
7	Mode Select	MSEL	During a software reset, a low level on this bit selects PC/AT/EISA Mode while a high level selects Special Mode.

Format Control Register

The Format Control Register is used to control the FIFO operating mode and select the vertical or horizontal recording modes. All bits are reset to logic "0" by a hardware reset. This is equivalent to a FIFO threshold of 1, FIFO disabled (transparent), and horizontal (longitudinal) recording enabled. In addition, the enhanced features of the "plus" version of the device are disabled, and the device will operate fully as a FDC37C65C.

The Format Control Register allows the FIFO to be fine-tuned for optimal system operation. Maximum compatibility with older systems may be achieved by disabling the FIFO. When FIFO operation is selected, the maximum time to service the disk may be calculated as:

$$Delay = Thresh \times \frac{1}{Data\ Rate} \times 8 - 1.5\mu s$$

When the FIFO is disabled (transparent), the delay is calculated with a threshold value of 1.

Table 11 - Format Control Register

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0-3	FIFO Threshold	FTHR	Bits 0 - 3 set the FIFO threshold to a value from 0 to 15. Bit 3 is the MSB and bit 0 is the LSB.
4	FIFO Enable	FEN	When bit 4 is set to a logic 1, the FIFO is enabled. When bit 4 is set to zero, the FIFO is transparent.
5	Enhanced Operation	ENO	When bit 5 is set to a logic 1, the FDC37C65C+ enhanced features are enabled. When bit 5 is set to a logic 0, the FDC37C65C+ will operate as a FDC37C65C. This bit also enables bit 3 in the Data Rate Register.
6	Verify	VER	When this bit is set, DACK is required for each byte transferred.
7	Vertical Mode	VEN	When bit 7 is set to a logic 1, Vertical (Perpendicular) recording operation is enabled. When bit 7 is set to a logic 0, conventional longitudinal recording operation is enabled.

MODES OF OPERATION

The FDC37C65C+ may operate under three different modes. They are the Base, Special, and PC/AT/EISA Modes. Table 12 illustrates the features of each mode of operation. The Data Rate Selection Register is used in any of the three modes without a change in its functionality. Figure 4 illustrates the block diagram of all the possible entries within the three operation modes.

Base Mode

After a hardware reset, Base Mode may be entered by a microprocessor access to the FDC37C65C+. The recommended access is a read of the Main Status Register. When a hardware reset occurs, the FDC37C65C+ is held in a soft reset, with the DMA and IRQ outputs tri-stated. When the Base Mode is entered, the DMA and IRQ signals resume their normal driving conditions. The Drive Select ($\overline{DS1}$ - $\overline{DS4}$) outputs, which provide for a 1 out of 4 decoding of the Unit Select bits of the command structure, may be used in the Base Mode. Please note that the Digital Output Register may not be used during Base Mode. There is, consequently, no qualifying by DMAEN and no Soft Reset. The Reduced Write Current (RWC) output, which indicates the necessity of write precompensation, may be used in the Base Mode.

PC/AT/EISA Mode

When the FDC37C65C+ is being used in a PC/AT/EISA or compatible system environment, the user will have to be in the PC/AT Mode.

In the PC/AT/EISA Mode, the Drive Select ($\overline{DS1}$-$\overline{DS4}$) outputs are replaced with the DSEL, MOEN1 , and MOEN2 signals from the Digital Output Register. The DMAEN signal from the Digital Output Register may be used as a qualifier for the DMA and IRQ outputs, and the

$\overline{SRST}$ signal may be used to do a software driven reset. The Reduced Write Current ($\overline{RWC}$) output now performs the function of Revolutions Per Minute ($\overline{RPM}$). Users with two speed drives may reduce spindle speed from a nominal 360 RPM to 300 RPM when this signal is active low. Similarly, this signal may be used to reduce write current when a slower data rate is selected for a given drive. In order to enter the PC/AT/EISA Mode from the Base Mode, the user will perform a write to the Digital Output Register (an $\overline{LDOR}$ and a $\overline{WR}$). The data written may be anything except an 80H, because a logic "1" in Bit 7 of the Digital Output Register is used to select Special Mode.

In order to enter the PC/AT Mode from the Special Mode, the user will write 00H to the Digital Output Register. That is,

- Bit 0: X (Don't care)
- Bit 1: X (Don't care)
- Bit 2: 0 (A low level on $\overline{SRST}$ causes a soft reset)
- Bit 3: X (Don't care)
- Bit 4: 0 (Disable Motor On Enable 1)
- Bit 5: 0 (Disable Motor On Enable 2)
- Bit 6: X (Don't care)
- Bit 7: 0 (A low level on MSEL selects PC/AT/EISA Mode)

To complete the entry into the PC/AT/EISA Mode from the Special Mode, the user will then read the Data Rate Selection Register address (an $\overline{LDCR}$ and an $\overline{RD}$).

Special Mode

In the Special Mode, the Drive Select (DS1 - DS4) outputs, which provide for a 1 out of 4 decoding of the Unit Select bits of the command structure, may be used. The DMAEN signal from the Digital Output Register may be used as a qualifier for the DMA and IRQ outputs and the $\overline{DACK}$ input. The SRST bit may be used to do a software driven reset. The Reduced Write Current ($\overline{RWC}$) output, which indicates the necessity of write precompensation, may also be used in the Special Mode.

In order to enter the Special Mode, the user will write 80H into the Digital Output Register (an $\overline{LDOR}$ and a $\overline{WR}$) because a logic "1" in Bit 7 of the Digital Output Register selects Special Mode. That is,

- Bit 0: X (Don't care)
- Bit 1: X (Don't care)
- Bit 2: 0 (A low level on $\overline{SRST}$ causes a soft reset)
- Bit 3: X (Don't care)
- Bit 4: 0 (Disable Motor On Enable 1)
- Bit 5: 0 (Disable Motor On Enable 2)
- Bit 6: X (Don't care)
- Bit 7: 1 (A high level on MSEL selects Special Mode)

To complete the entry into the Special Mode, the user will then read the Data Rate Selection Register address (an $\overline{LDCR}$ and $\overline{RD}$).

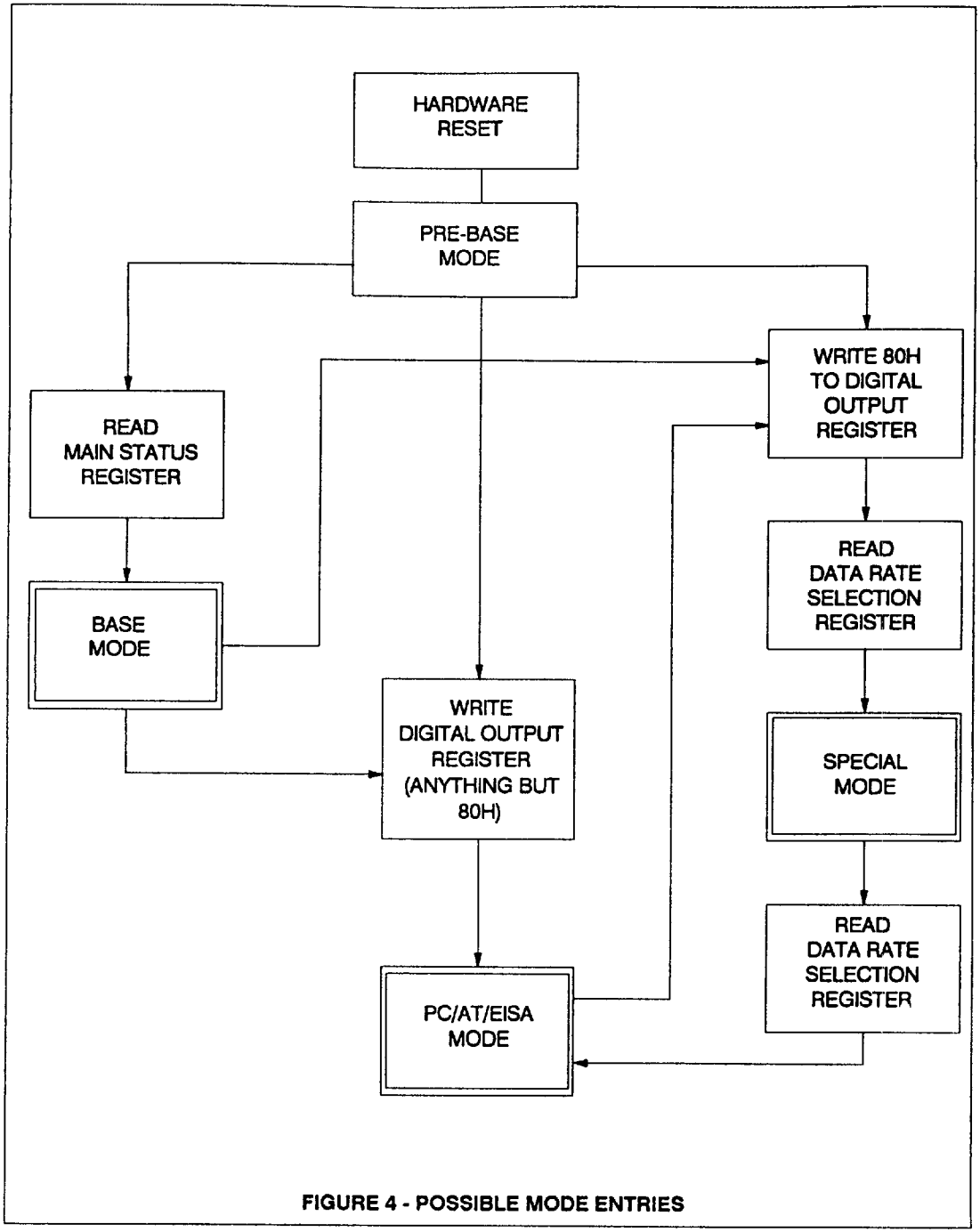


FIGURE 4 - POSSIBLE MODE ENTRIES

Table 12 - Modes of Operation

FEATURES	BASE MODE	PC/AT/EISA MODE	SPECIAL MODE
Functions of DSEL1-4	DSEL1-4	DSEL1-2, MOEN1-2	DSEL1-4
Software Reset supported	No	Yes	Yes
DMA pin supported by DMAEN bit	No	Yes	Yes
IRQ pin qualified by DMAEN bit	No	Yes	Yes
Functions of $\overline{RPM}/\overline{RWC}$	$\overline{RWC}$	$\overline{RPM}$	$\overline{RWC}$

Power Down Mode

The FDC37C65C+ may be placed into the Power down Mode by writing a 1 to bit 0 of the Main Status Register, when hardware and software interrupts are inactive. The FDC37C65C+ will return to normal operation when RST is made active, resetting the FDC37C65C+. In the Power Down Mode, the controller core is halted, stopping the oscillators, shutting down all Schmitt trigger reference voltages, three-stating all 48 mA drivers, and shutting down the low V_{CC} detect circuit. This will reduce I_{CC} to less than 100 μA.

POLLING ROUTINE

Following either a hard or soft reset, the FDC37C65C+ automatically begins polling the drives for a change in the Ready lines. The polling is done continuously between commands and between step pulses in the SEEK command. The purpose of the polling routine is to detect when the drives return to a Ready status after being reset or after a command is completed. The polling sequence is Drive 1, 2, 3, 4, and each drive is polled every 1.024 ms, except during the READ/WRITE commands. For mini-floppies, the polling rate is 2.048 ms. In Special or PC/AT Modes, if DMAEN is not valid by 1 ms after reset becomes inactive, then IRQ may already be set and pending when enabled onto the bus. When the FDC37C65C+ is in the PC/AT Mode, the user will not see the polling at the Drive Select signals. Refer to Figure 5 for the general timing of the Drive Select Polling.

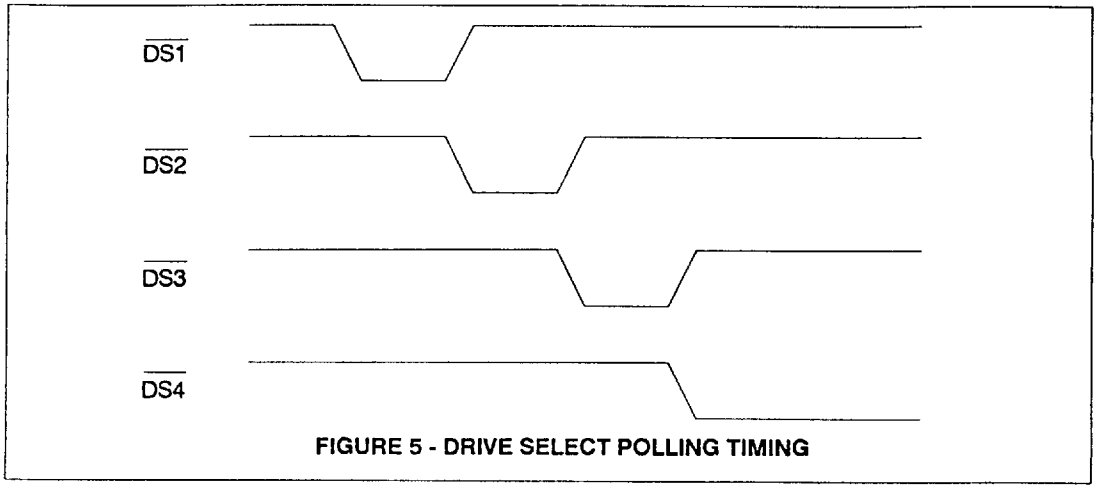


FIGURE 5 - DRIVE SELECT POLLING TIMING

RESET LOGIC

A hardware reset is performed by applying a logic "1" to the RST pin of the FDC37C65C+. When a hardware reset occurs, the device will remain in the reset condition for the duration of the pulse. Once the pulse is removed, the FDC37C65C+ will default to pre-Base Mode with a data rate of 250 kbits/s MFM (or 125 kbits/s FM, code dependent) when a 16 MHz input clock is used. The FDC37C65C+ will default to 500 kbits/s MFM when a 32 MHz input clock is used. A software reset is performed by applying a logic "0" to bit 2 of the Digital Output Register. When a software reset occurs, the FDC37C65C+ is reset the same as it is during a hardware reset, with the exception that the mode and the data rate are not affected. During a reset, the high current driver outputs to the drives are disabled. Neither a hard reset nor a soft reset will affect the values of the internal timers, that is, Head Unload Time, Head Load Time, and Step Rate Time (described in the COMMANDS section of this document). If the on chip crystal oscillators are used instead of the TTL clock inputs, a longer duration of the pulse on the RST pin during a hardware reset is required to stabilize the internal timing. The FDC37C65C+ contains internal circuitry to automatically reset the device during initial power-up. The device also contains power fail protection circuitry in the disk interface which allows it to reset itself in the event of power failure.

DATA SEPARATOR AND WRITE PRECOMPENSATION

The Data Separator portion of the FDC37C65C+ is based on the Standard Microsystems FDC92C39. It performs the complete data separation function of separating the data and clock pulses from the FM and MFM encoded data. In addition, it contains the Automatic Write Precompensation Logic necessary when writing to the inner and outer tracks of the drive. The encoded Write Data signal is synchronized to the input clock and is clocked through an internal shift register, but is delayed upon being output. When a logic "0" is applied to the PCVAL pin and a track inside of track 43 is accessed, data will be precompensated by ±187 ns. For MFM encoding, when a logic "1" is applied to the PCVAL Pin, data will be precompensated by ±125 ns, regardless of track number and data rate. For frequencies other than 16 MHz on the CLK1 pin, the precompensation value will be three clock cycles for PCVAL="0", or two clock cycles for PCVAL="1". When CLK2 is used for

nonstandard data rates, the precompensation value is always two clock cycles, thus disabling the function of PCVAL. Note that FM encoding is not precompensated. Precompensation may be disabled by writing a logic high to bit D2 of the Data Rate Selection Register.

Table 13 - Precompensation Values

DATA RATES	PRECOMPENSATION VALUES			
	PCVAL = 0 DRS BIT 3 = 0	PCVAL = 1 DRS BIT 3 = 0	PCVAL = 0 DRS BIT 3 = 1	PCVAL = 1 DRS BIT 3 = 1
1 Mbps			± 93.5 ns	± 62.5 ns
500k	± 187 ns	± 125 ns	± 93.5 ns	± 62.5 ns
300k	± 187 ns	± 187.5 ns	± 187.5 ns	± 187.5 ns
250k	± 187 ns	± 125 ns	± 93.5 ns	± 62.5 ns
125k	± 187 ns	± 125 ns		

COMMAND SEQUENCE

The FDC37C65C+ is capable of performing 18 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC37C65C+ and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC37C65C+ receives all information required to perform a particular operation from the processor.

Execution Phase : The FDC37C65C+ performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information is made available to the processor.

Table 14 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of the Main Status Register (A_0 = 0) or the Data Register (A_0 = 1).
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 255 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7 - D_0	Data Bus	8-bit Data bus; D_7 is the most significant bit, and D_0 is the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT	End of Track	EOT is the final Sector number on a Cylinder. During Read or Write operation the FDC37C65C+ will stop data transfer after a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands, this value determines the number of bytes that VCO's will stay low after two CRC bytes. During Format command GPL determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in the ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	HLT stands for the head load time in the FDC37C65C+ (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0, the FDC37C65C+ will automatically start searching for sector 1 on side 1.
N	Number	N stands for the number of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of head.

Table 14 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R is the Sector number which will be read or written.
R/W	Read/Write	R/W is the Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT is the Stepping Rate for the FDC37C65C+. The stepping rate applies to all drives. The stepping rate is programmable from 1 to 16 ms in 1 ms increments. F_H = 1 ms, E_H = 2 ms, etc.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0-ST3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive (0 or 1).

INSTRUCTION SET

Table 15 lists the required parameters and the results associated with each command that the FDC37C65C+ is capable of performing. Refer to Table 14 for explanations of the various symbols used.

TABLE 15 - INSTRUCTION SET [1] [2] [3]

READ DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

[1] Symbols used in this table are described in the beginning of this section

[2] A_0 should equal binary 1 for all operations.

[3] X = Don't care, usually made to equal binary 0.

READ DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main system and FDD.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main system and FDD.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ A TRACK									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ ID									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information read during Execution Phase from Floppy Disk
	R	H								
	R	R								
	R	N								

FORMAT A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire track
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	(undefined)								In this case, the ID information has no meaning
	R	(undefined)								
	R	(undefined)								
	R	(undefined)								

SCAN EQUAL									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

SCAN LOW OR EQUAL										
PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

SCAN HIGH OR EQUAL									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

RECALIBRATE									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track 0.

SENSE INTERRUPT STATUS

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	STO								FDC status information at the end of seek-operation.
	R	PCN								

SPECIFY

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

SENSE DRIVE STATUS

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R	ST3								Status information about FDD

SEEK

PHASE	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	NCN								
Execution										Head positioned over proper cylinder on diskette

INVALID CODES									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	——— Invalid Codes ———								Invalid Command Codes (NoOp - FDC goes into Standby State)
Result	R	——— ST0 ———								ST0 = 80_H

SOFTWARE RESET									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND Execution	W	0	0	1	1	0	1	1	0	Command Codes

RETURN VERSION									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	X	X	X	1	0	0	0	0	Command Codes
Result	R	1	0	1	0	0	0	0	0	

FUNCTIONAL DESCRIPTION OF COMMANDS

Read Data

A set of nine (9) byte words are required to place the FDC37C65C+ into the Read Data Mode. After the Read Data command has been issued, the FDC37C65C+ loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC37C65C+ outputs data (from the data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation". The Read Data Command may be terminated by the receipt of a Terminal count signal. TC should be issued at the same time that the $\overline{\text{DACK}}$ for the last byte of data is sent. Upon receipt of this signal, the FDC37C65C+ stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then, at the end of the sector, terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC37C65C+ depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 16 shows the Transfer Capacity.

Table 16 - Transfer Capacity

MULTI-TRACK MT	MFM/FM MF	BYTES/ SECTOR N	MAXIMUM TRANSFER CAPACITY (Bytes/Sector) X (Number of Sectors)	FINAL SECTOR READ FROM DISKETTE
0	0	00	(128) x (26) = 3,328	26 at Side 0
0	1	01	(256) x (26) = 6,656	or 26 at Side 1
1	0	00	(128) x (52) = 6,656	26 at Side 1
1	1	01	(256) x (52) = 13,312	
0	0	01	(256) x (15) = 3,840	15 at Side 0
0	1	02	(512) x (15) = 7,680	or 15 at Side 1
1	0	01	(256) x (30) = 7,680	15 at Side 1
1	1	02	(512) x (30) = 15,360	
0	0	02	(512) x (8) = 4,096	8 at Side 0
0	1	03	(1024) x (8) = 8,192	or 8 at Side 1
1	0	02	(512) x (16) = 8,192	8 at Side 1
1	1	03	(1024) x (16) = 16,384	

The "multi-track" function (MT) allows the FDC37C65C+ to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector L, Side 0 and completing at Sector L, Side 1 (Sector L is the last sector on the side). Please note that this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, the DTL defines the data length which the FDC37C65C+ must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC37C65C+ reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexadecimal.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC37C65C+ detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC37C65C+ sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively. After reading the ID and Data Fields in each sector, the FDC37C65C+ checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC37C65C+ sets the DC (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC37C65C+ also sets the DD (Data Error in Data field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.

If the FDC37C65C+ reads a Deleted Data Address Mark from the diskette, and the SK bit (bit D5 in the first Command Word is not set (SK = 0) then the FDC37C65C+ sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC37C65C+ skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC37C65C+ and the processor, via the data bus the FDC37C65C+ must be serviced within the time calculated using the equation shown in the section "Format Control Register", or the FDC37C65C+ sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 17 shows the value for C, H, R, and N, when the processor terminates the Command.

Table 17 - ID Information in Processor - Terminated Command

MT	HD	FINAL SECTOR TRANSFERRED TO PROCESSOR	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

NOTES: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes are required to set the FDC37C65C+ into the Write Data mode. After the Write Data command has been issued, the FDC37C65C+ loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the specify command), and begins reading ID Fields. When all four bytes loaded during the Command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC37C65C+ takes data from the processor byte-by-byte via the data bus, and outputs it to the drive.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written. The FDC37C65C+ continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC37C65C+, it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, then the remainder of the data field is filled with 00 (zeros).

The FDC37C65C+ reads the ID field of each sector and checks the CRC bytes. If the FDC37C65C+ detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this, the FDC37C65C+ sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. Status register 0 also has bit 7 and 6 set to 0 and 1 respectively.

Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC37C65C+ detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, the FDC37C65C+ skips the sector with the Data Address Mark and reads the next sector.

Read a Track

This command is similar to the READ DATA Command except that this is a continuous READ operation where the entire data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC37C65C+ starts reading all data fields on the track, as continuous blocks of data. If the FDC37C65C+ finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC37C65C+ compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC37C65C+ does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.

Read ID

The READ ID Command is used to give the present position of the recording head. The FDC37C65C+ stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette before the INDEX HOLE is encountered for the second time, the MA (Missing Address Mark) flag in Status Register 1 is set to a "1" (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a "1" (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to "0" and "1" respectively. During this command there is no data transfer between FDC37C65C+ and the CPU except during the result phase.

Format a Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette. Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; four data requests per sector are

made by the FDC37C65C+ for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the FDC37C65C+ for each sector on the track. If the FDC37C65C+ is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register are incremented by one after each sector is formatted. The R register therefore contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC37C65C+ encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the drive at the end of a write operation, then the FDC37C65C+ sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also, the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 18 shows the relationship between N, SC, GPL for various sector sizes. (See Table 19 for recommended IBM PC and PC/AT compatible programming parameters.)

Table 18

FORMAT	SECTOR SIZE	N	SC	GPL[1]	GPL[2][3]
8" Standard Floppy					
FM Mode	128 Bytes/Sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode [4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF

FORMAT	SECTOR SIZE	N	SC	GPL[1]	GPL[2][3]
5¼" Minifloppy					
FM Mode	128 Bytes/Sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode [4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	09	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Micro Floppydisk®					
FM Mode	128 Bytes/Sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode	256	1	0F	0E	36
	512	2	09	1B	54
	1024[5]	3	05	35	74

NOTES:
(1) Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
(2) Suggested values of GPL in format command.
(3) All values except sector size and hexadecimal.
(4) In MFM mode FDC37C65C + cannot perform a Read/Write/Format operation with 128 bytes/sector. (N = 00)
(5) 1 Mbit/s vertical mode.

Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC37C65C + compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of:

$$D_{FDD} = D_{PROCESSOR}, D_{FDD} \leq D_{PROCESSOR}, \text{ or}$$

$$D_{FDD} \geq D_{PROCESSOR}$$

The hexadecimal byte of FF either from memory or from the drive can be used as a mask byte because it always meets the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur:

1. The conditions for scan are met (equal, low, or high), or,
2. The last sector on the track is reached (EOT), or
3. The terminal count signal is received.

If the conditions for scan are met, then the FDC37C65C+ sets the SH (Scan Hit) flag of Status Register 2 to a "1" (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC37C65C+ sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC37C65C+ to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 19 shows the status of bits SH and SN under various conditions of SCAN.

Table 19

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 (SN)	BIT 3 (SH)	
Scan Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	1	0	$D_{FDD} \neq D_{PROCESSOR}$
Scan Low or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} < D_{PROCESSOR}$
	1	0	$D_{FDD} > D_{PROCESSOR}$
Scan High or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} > D_{PROCESSOR}$
	1	0	$D_{FDD} < D_{PROCESSOR}$

If the FDC37C65C+ encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC37C65C+ skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC37C65C+ sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read, or the MT (Multi-Track) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21, the following will

happen: Sectors 21, 23 and 25 will be read, then the next sector (26) will be skipped, and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command, data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC37C65C+ ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The read/write head within the drive is moved from cylinder to cylinder under control of the Seek Command. FDC37C65C+ has four independent Present Cylinder Registers for each drive. They are clear only after the Recalibrate command. The FDC37C65C+ compares the PCN (Present Cylinder Number), which is the current head position, with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to drive set to a 1 (high),and Step Pulses are issued (Step In).

PCN > NCN: Direction signal to drive set to a 0 (low), and Step Pulses are issued (Step Out).

The rate at which Step Pulses are issued is controlled by the SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued, NCN is compared against PCN; when NCN = PCN, the SE (Seek End) flag in Status Register 0 is set to a 1 (high), and the command is terminated. At this point the FDC37C65C+ interrupt goes high. Bits DB0 - DB3 in the Main Status Register are set during the seek operation and are cleared by the Sense Interrupt Status Command.

During the Command Phase of the Seek operation, the FDC37C65C+ is in the FDC37C65C+ BUSY state, but during the Execution Phase it is in the NON-BUSY state. While the FDC37C65C+ is in the NON BUSY state, another seek Command may be issued, and in this manner parallel Seek Operations may be performed on up to 4 Drives at once. No other command can be issued for as long as the FDC37C65C+ is in process of sending Step Pulses to any drive.

If a drive is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between the first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the drive to the Track 0 position. The FDC37C65C+ clears the contents of the PCN counter, and checks the status of the Track 0 signal from the drive. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 255 Step Pulses have been issued, the FDC37C65C+ sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1's

(highs), and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

The ability to overlap RECALIBRATE Commands to multiple drives and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command.

Sense Interrupt Status

An Interrupt signal will be generated by the FDC37C65C+ for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of drive changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in the NON-DMA Mode, DB5 in the Main Status Register is high. Upon entering the Result Phase this bit is cleared.

Reasons 1 and 4 do not require a Sense Interrupt Status command. The interrupt is cleared by reading or writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register, 0 identifies the cause of the interrupt. See Table 20.

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Issuing the Sense Interrupt Status Command without an interrupt pending is treated as an invalid command.

Table 20

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms, ... 0F = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between the Head Load signal going high and the Read/Write operation starting. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms,... 7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK1 or XTAL1). Times indicated above are for a 16 MHz clock; if the clock is reduced to 8 MHz then the time intervals are increased by a factor of two. If the clock is increased to 32 MHz then all time intervals are decreased by a factor of two.

The choice of DMA or non-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1), the non-DMA mode is selected, and when ND = 0, the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the drives. Status Register 3 contains the Drive Status information stored internally in the FDC37C65C+ registers.

Return Version

The Return Version command identifies the type of chip in use. A value of A0H is returned as the result byte. No interrupts are generated.

Invalid

If an invalid command is sent to the FDC37C65C+ (a command not defined above), then the FDC37C65C+ will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC37C65C+ during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the FDC37C65C+ is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0, it will find an 80 hex indicating an invalid command was received. A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC37C65C+ will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC37C65C+ in a standby or no operation state.

Recording Format

When bit D7 of the Format Control Register is reset to "0", the FDC37C65C+ will default to the standard single density or double density formats as shown below. The FDC37C65C+ will implement the Toshiba Vertical Recording Format when bit D7 of the Format Control Register is set. The vertical recording format will have a gap 2 length of 41 bytes for 1

megabit operation, and a gap 2 length of 22 bytes for 500 kbits/s operation. At 1 Mbps, A FORMAT command will therefore format 41 bytes of gap 2; a READ command for 1 Mbps will skip over 42 bytes before searching for the sync field. The WRITE DATA command will skip 3 bytes after the CRC and will then write 38 bytes of 4E before writing 12 bytes of 00.

At 500 kbps, A FORMAT command will therefore format 22 bytes of gap 2; a READ command will skip over 23 bytes before searching for the sync field. The WRITE DATA command will skip 3 bytes after the CRC and will then write 19 bytes of 4E before writing 12 bytes of 00.

FLOPPY DISK FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		C	H	S	N	C	GAP2	SYNC	DATA AM		DATA	C	GAP3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE	Y L	D	E C	O	R C	22x 4E	12x 00	3x A1	FB F8		R C		

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a	SYNC	IAM	GAP1	SYNC	IDAM	C	H	S	N	C	GAP2	SYNC	DATA AM	DATA	C	GAP3	GAP 4b
40x FF	6x 00	FC	26x FF	6x 00	FE	Y L	D	E C	O	R C	11x FF	6x 00	FB or F8		R C		

TOSHIBA VERTICAL RECORDING FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		C	H	S	N	C	GAP2	SYNC	DATA AM		DATA	C	GAP3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE	Y L	D	E C	O	R C	41x 4E	12x 00	3x A1	FB F8		R C		

Table 21 - Comparison: FDC37C65C & FDC37C65C+

FDC37C65C	FDC37C65C+
Max Data Rate: 1 Mbps	Max Data Rate: 1 Mbps
Max Clock: 32 MHz	Max Clock: 32 MHz
Power Down Mode	Power Down Mode
Recalibrate (Restore) Command will issue up to 77 pulses	Recalibrate Command will issue up to 255 step pulses
Longitudinal Recording only	Vertical or Longitudinal recording
No FIFO	FIFO included
Return Version = 90H	Return Version = A0H
	Requires Verify bit

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -55° to +150°C
Lead Temperature Range (soldering, 10 seconds) . . . . . +325°C
Positive Voltage on any pin, with respect to Ground . . . . . V_{cc} +0.3V
Negative Voltage on any pin, with respect to Ground . . . . . -0.3V
Maximum V_{cc} . . . . . +7V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C - 70°C, V_{cc} = +5.0 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Low Input Voltage 1 (D0-D7, XTAL1, XTAL2)	V_{IL1}			0.8	V	TTL Levels
High Input Voltage 1 (D0-D7, XTAL1, XTAL2)	V_{IH1}	2.0			V	
Low Input Voltage 2 (Low to High Threshold) (All inputs except D0-D7, XTAL1, XTAL2)	V_{IL2}	0.8			V	Schmitt Trigger
High Input Voltage 2 (High to Low Threshold) (All inputs except D0-D7, XTAL1, XTAL2)	V_{IH2}			2.0	V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}	0.45			V	
Low Output Voltage 1 (D0-D7, IRQ, DMA)	V_{OL1}			0.4	V	I_{OL} = 24.0 mA
High Output Voltage 1 (D0-D7, IRQ, DMA)	V_{OH1}	2.4			V	I_{OH} = -5.0 mA
Low Output Voltage 2 (All outputs except D0-D7, IRQ, DMA)	V_{OL2}			0.4	V	I_{OL} = 48 mA**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Input Leakage Current 1 (All inputs except PCVAL and DRV)	I_{L1}			±10.0	μA	V_{IN} = 0-5V
Low Input Pull-Up Current (PCVAL and DRV)	I_{PU}	10.0		60	μA	V_{IN} = 0V
High Input Leakage Current 2 (PCVAL and DRV)	I_{L2}	0.0		-10.0	μA	V_{IN} = 5V
V_{CC} Supply Current 1	I_{CC1}			45	mA	100μA Source Loads
V_{CC} Supply Current 2	I_{CC2}			95	mA	5 mA Source Loads
Power Down Mode V_{CC} Supply Current	I_{CCPD}			100	μA	V_{IN} = GND or V_{CC}; I_O = 0*
Power Qualified Reset Threshold	V_{POR}	2.8		4.35	V	

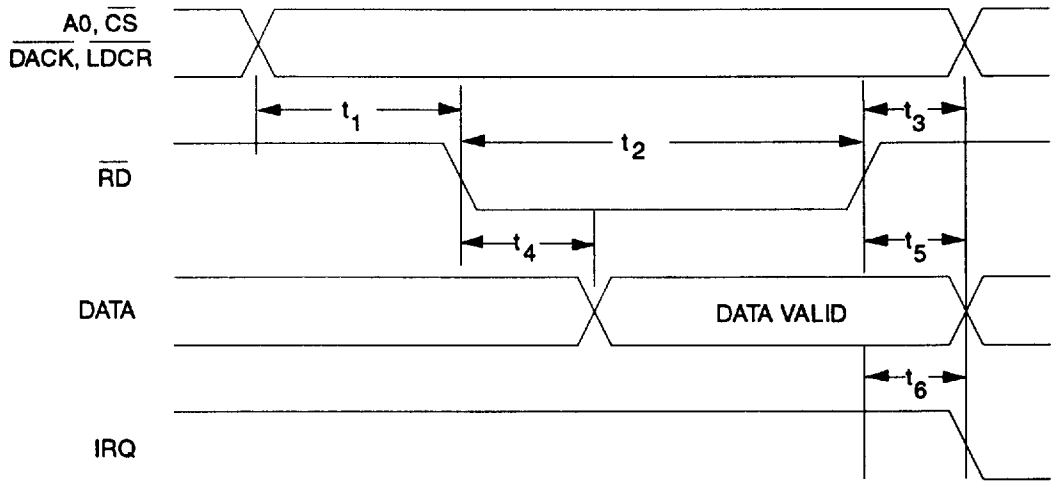
*NOTE: Low power oscillator circuits must be used (see Page 11, Figure 2A).

**NOTE: Grounding Requirements:
Due to the large number of high current bus drivers, care must be exercised in the layout of the chip ground and ground trace. It is perferable that a full ground plane and decoupling capacitors be used. Where this is not possible, a local ground plane with the ground trace from this chip to the power connector should be as wide as possible and proper decoupling capacitors should be placed as close to the chip as possible.

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 5V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

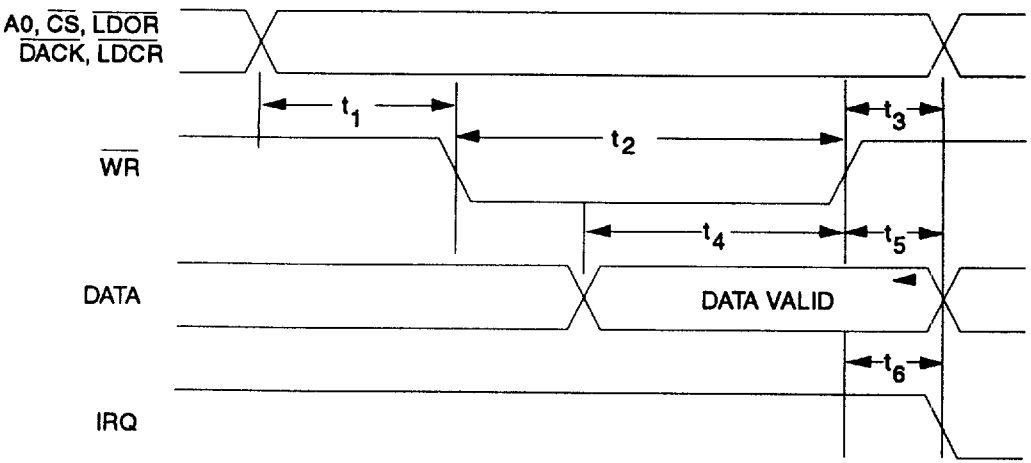
TIMING DIAGRAMS



	Parameter	min	typ	max	units
t_1	A0,CS,DACK,LDCR Set Up to RD Low	0			ns
t_2	RD Width	90			ns
t_3	A0,CS,DACK,LDCR Hold from RD High	0			ns
t_4	Data Access Time from RD Low			90	ns
t_5	Data to Float Delay from RD High			65	ns
t_6	IRQ Reset Delay from RD High			X + (150ns)*	

*X specifies one MCLK period. It is dependent upon selected data rate (see Table 13).

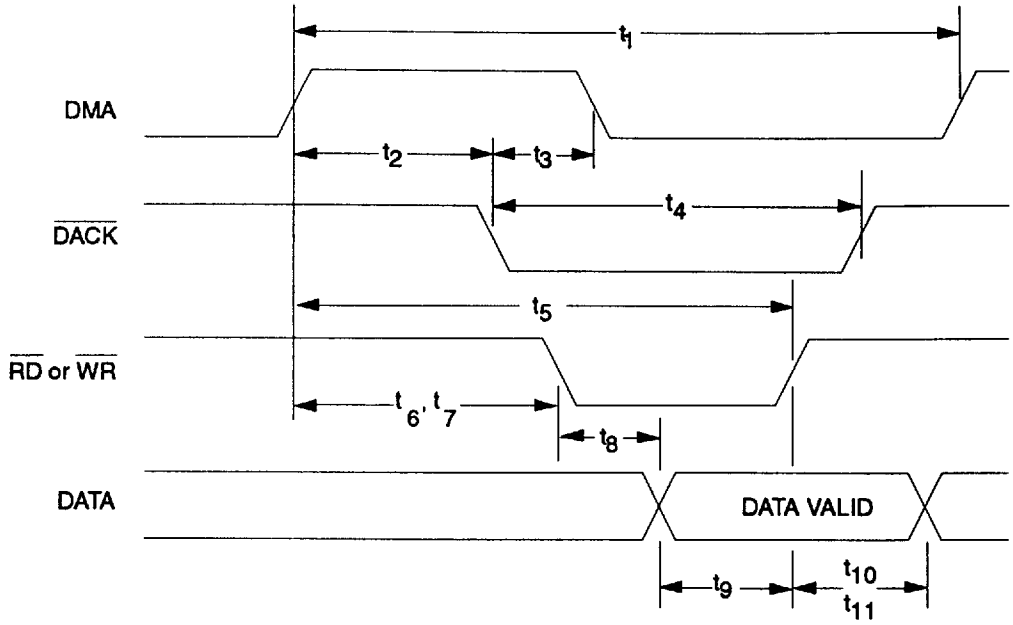
FIGURE 6 - MICROPROCESSOR READ TIMING



	Parameter	min	typ	max	units
t_1	A0,CS,DACK,LDCR,LDOR Set Up time to WR Low	0			ns
t_2	WR Width	60			ns
t_3	A0,CS,DACK,LDCR,LDOR Hold from WR High	0			ns
t_4	Data Set Up Time to WR High	80			ns
t_5	Data Hold Time from WR High	0			ns
t_6	IRQ Reset Delay from WR High			X + (150ns)*	

*X specifies one MCLK period. It is dependent upon selected data rate (see Table 13).

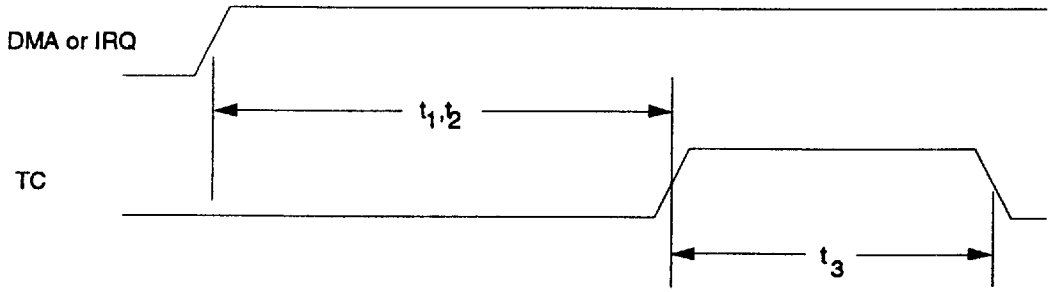
FIGURE 7 - MICROPROCESSOR WRITE TIMING



	Parameter	min	typ	max	units
t_1	DMA Cycle Time	52			X*
t_2	$\overline{DACK}$ Delay Time from DMA High	0			ns
t_3	DMA Reset Delay from $\overline{DACK}$ Low			140	ns
t_4	$\overline{DACK}$ Width	90			ns
t_5	$\overline{RD}$ or $\overline{WR}$ Response from DMA High			48	X*
t_6	$\overline{RD}$ Delay from DMA High	0			ns
t_7	$\overline{WR}$ Delay from DMA High	0			ns
t_8	Data Access Time from $\overline{RD}$ Low			90	ns
t_9	Data Set Up Time to $\overline{WR}$ High	80			ns
t_{10}	Data to Float Delay from $\overline{RD}$ High	10		65	ns
t_{11}	Data Hold Time from $\overline{WR}$ High	0			ns

*X specifies one MCLK period. It is dependent upon selected data rate (see Table 13).

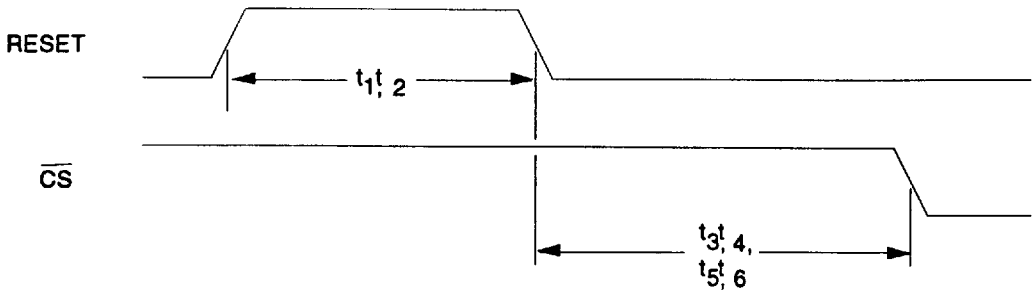
FIGURE 8 - DMA TIMING



	Parameter	min	typ	max	units
t_1	TC Delay from Last DMA or IRQ,$\overline{RD}$	0		192	X*
t_2	TC Delay from Last DMA or IRQ,$\overline{WR}$	0		384	X*
t_3	TC Width	60			ns

*X specifies one MCLK period. It is dependent upon selected data rate (see Table 13).

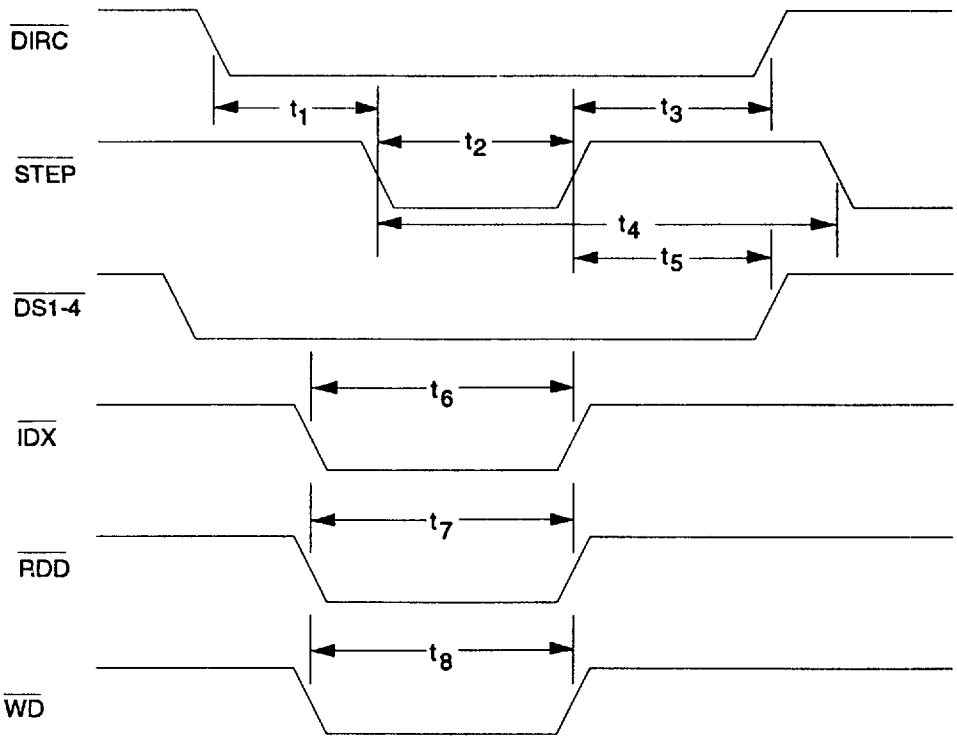
FIGURE 9 - TERMINAL COUNT TIMING



	Parameter	min	typ	max	units
t_1	RESET Width - TTL Driven CLK1	250			ns
t_2	RESET Width - Software Reset	5			X*
t_3	Chip Access Delay from RESET Low - TTL	32			X*
t_4	Chip Access Delay from Software RESET Low	40			X*
t_5	Chip Access Delay from RESET Low - XTAL1 at 16 MHz	500			uS
t_6	XTAL2 Access Delay after Reset 9.6 MHz	1000			uS

*X specifies one MCLK period. It is dependent upon selected data rate (see Table 13).

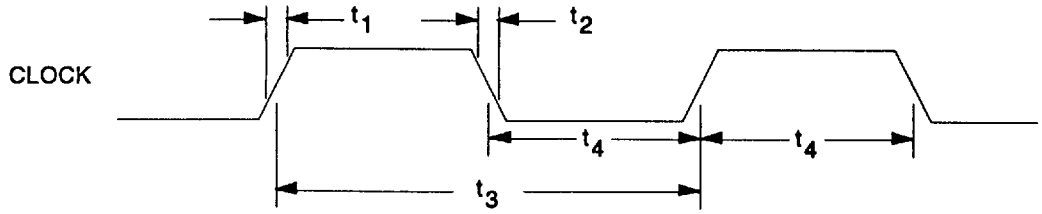
FIGURE 10 - RESET TIMING



	Parameter	min	typ	max	units
t_1	$\overline{DIRC}$ Set Up to $\overline{STEP}$ Low	4			X*
t_2	$\overline{STEP}$ Active time Low	24			X*
t_3	$\overline{DIRC}$ Hold Time After $\overline{STEP}$	96			X*
t_4	$\overline{STEP}$ Cycle Time	132			X*
t_5	$\overline{DS1\text{-}4}$ Hold Time from $\overline{STEP}$ Low	20			X*
t_6	$\overline{IDX}$ Pulse Width	2			X*
t_7	$\overline{RDD}$ Active Time Low	40			ns
t_8	$\overline{WD}$ Write Data Width Low		.5		Y*

*X specifies one MCLK period. It is dependent upon selected data rate (see Table 13).
*Y specifies one WCLK period. It is dependent upon selected data rate (see Table 13).

FIGURE 11 - DISK DRIVE TIMING



	Parameter	min	typ	max	units
t_1	Clock Rise Time (V_{IN} = 0.8 to 2.0)			2	ns
t_2	Clock Fall Time (V_{IN}= 2.0 to 0.8)			2	ns
t_3	Clock Period	31.0			ns
t_4	Clock Active (High or Low)	13.5			ns

FIGURE 12 - CLOCK TIMING

Table 22 - Programming Values for Floppy Disk Controllers (IBM PC and PC/AT Compatible Systems)

PARAMETER	HEX VALUES TO BE PROGRAMMED				
	2.88 MB 3.5"	1.44 MB 3.5"	720 KB 3.5"	1.2 MB 5.25"	360 KB 5.25"
Bytes/Sector	02	02	02	02	02
Sectors/Track	24	12	09	0F	09
Gap Length (Read/Write)	1B	1B	2A	1B	2A
Gap Length (Format)	54	6C	50	54	50
Head Settle Time (ms)	15	15	15	15	15
Motor Start Up (1/8 sec)	08	08	08	08	08
Cylinders	80	80	80	80	40
Tracks	160	160	160	160	80
Tracks/Inch	135	135	135	96	48
Heads	02	02	02	02	02
RPM	300	300	300	360	300
Transfer (KB/s)	1M	500	250	500	250

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