2048MB DDR2 DIMM

2GB DDR2 DIMM based on 128MX8 , 8Banks, 1.8V

Features

.Performance range (Bandwidth: 5.3 GB/sec)

Part No.	Max Freq. (Clock)	Speed Grade
78.A1G9O.XX4	333MHz(3ns@CL5)	667 Mbps

- JEDEC standard 1.8V ± 0.1V Power Supply
- VDDQ = 1.8V ± 0.1V
- Internal Bank:8 Bank
- Posted CAS
- Programmable CAS Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1 , 2 , 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4 , 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Refresh and Self Refresh
  Average Refesh Period 7.8us
- Serial presence detect with EEPROM
- Compliance with RoHS
- Compliance with CE
- DDR2 SDRAM Package: 60ball FBGA - 128Mx8

Pin Description

Pin Name	Description	Pin Name	Description
A0-A13	DDR2 SDRAM address bus	CK0, CK1, CK2	DDR2 SDRAM clocks (positive line of differential pair)
BA0, BA1	DDR2 SDRAM bank select	$\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	DDR2 SDRAM clocks (negative line of differential pair)
$\overline{RAS}$	DDR2 SDRAM row address strobe	SCL	I^2C serial bus clock for EEPROM
$\overline{CAS}$	DDR2 SDRAM column address strobe	SDA	I^2C serial bus data line for EEPROM
$\overline{WE}$	DDR2 SDRAM wirte enable	SA0-SA2	I^2C serial address select for EEPROM
$\overline{S0}$, $\overline{S1}$	DIMM Rank Select Lines	V_{DD}*	DDR2 SDRAM core power supply
CKE0,CKE1	DDR2 SDRAM clock enable lines	V_{DDQ}*	DDR2 SDRAM I/O Driver power supply
ODT0, ODT1	On-die termination control lines	V_{REF}	DDR2 SDRAM I/O reference supply
DQ0 - DQ63	DIMM memory data bus	V_{SS}	Power supply return (ground)
CB0 - CB7	DIMM ECC check bits	V_{DD}SPD	Serial EEPROM positive power supply
DQS0 - DQS8	DDR2 SDRAM data strobes	NC	Spare Pins(no connect)
DM(0-8)	DDR2 SDRAM data masks	RESET	Not used on UDIMM
$\overline{DQS0}$-$\overline{DQS8}$	DDR2 SDRAM differential data strobes	TEST	Used by memory bus analysis tools (unused on memory DIMMs)

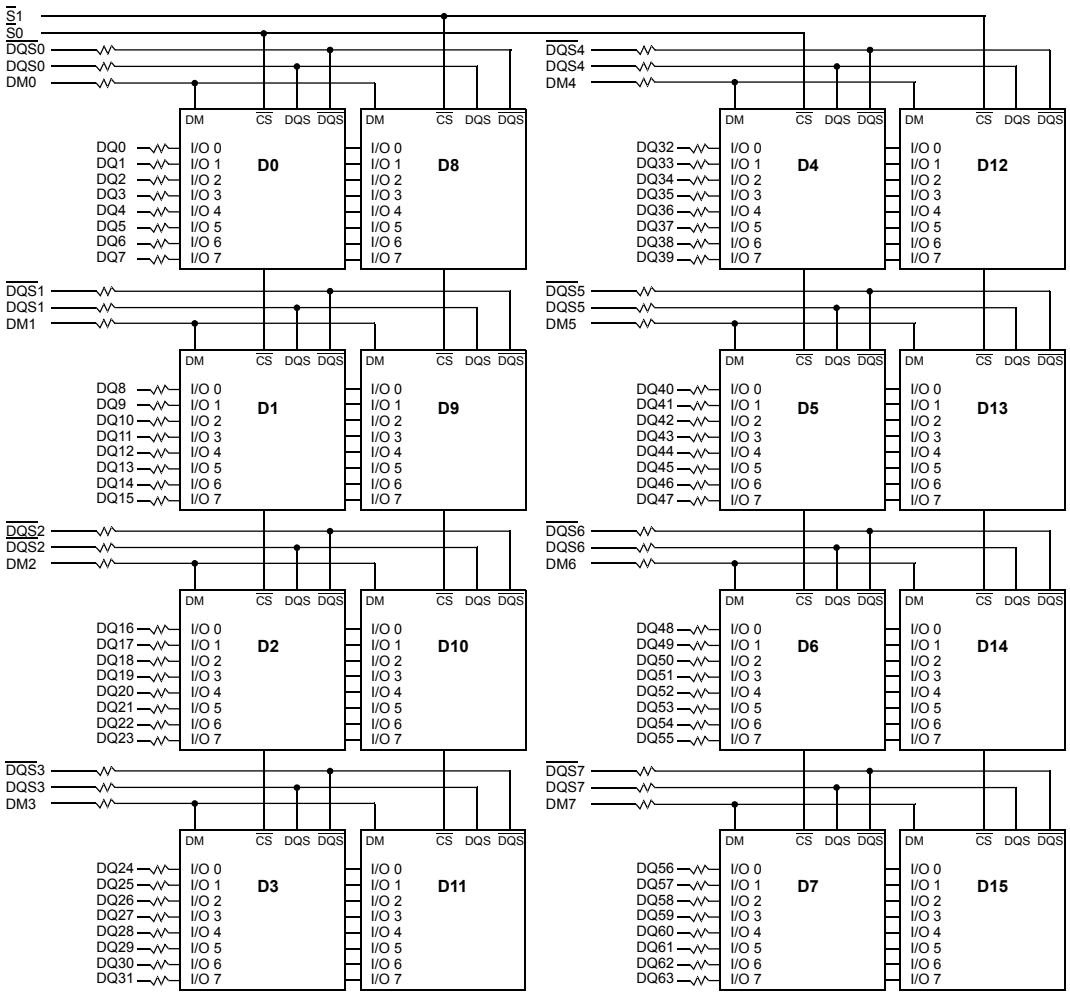
*The VDD and VDDQ pins are tied to the single power-plane on PCB.

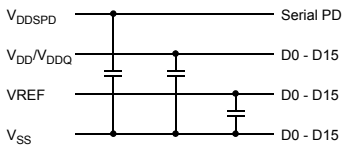
Pin Description

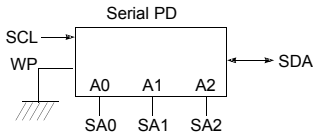
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	121	V_{SS}	31	DQ19	151	V_{SS}	61	A4	181	V_{DDQ}	91	V_{SS}	211	DM5
2	V_{SS}	122	DQ4	32	V_{SS}	152	DQ28	62	V_{DDQ}	182	A3	92	$\overline{DQS}5$	212	NC
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V_{SS}
4	DQ1	124	V_{SS}	34	DQ25	154	V_{SS}	64	V_{DD}	184	V_{DD}	94	V_{SS}	214	DQ46
5	V_{SS}	125	DM0	35	V_{SS}	155	DM3	KEY				95	DQ42	215	DQ47
6	$\overline{DQS}0$	126	NC	36	$\overline{DQS}3$	156	NC	65	V_{SS}	185	CK0	96	DQ43	216	V_{SS}
7	DQS0	127	V_{SS}	37	DQS3	157	V_{SS}	66	V_{SS}	186	$\overline{CK}0$	97	V_{SS}	217	DQ52
8	V_{SS}	128	DQ6	38	V_{SS}	158	DQ30	67	V_{DD}	187	V_{DD}	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	NC	188	A0	99	DQ49	219	V_{SS}
10	DQ3	130	V_{SS}	40	DQ27	160	V_{SS}	69	V_{DD}	189	V_{DD}	100	V_{SS}	220	CK2
11	V_{SS}	131	DQ12	41	V_{SS}	161	NC	70	A10/AP	190	BA1	101	SA2	221	$\overline{CK}2$
12	DQ8	132	DQ13	42	NC	162	NC	71	BA0	191	V_{DDQ}	102	NC, TEST[2]	222	V_{SS}
13	DQ9	133	V_{SS}	43	NC	163	V_{SS}	72	V_{DDQ}	192	$\overline{RAS}$	103	V_{SS}	223	DM6
14	V_{SS}	134	DM1	44	V_{SS}	164	NC	73	$\overline{WE}$	193	$\overline{S}0$	104	$\overline{DQS}6$	224	NC
15	$\overline{DQS}1$	135	NC	45	NC	165	NC	74	$\overline{CAS}$	194	V_{DDQ}	105	DQS6	225	V_{SS}
16	DQS1	136	V_{SS}	46	NC	166	V_{SS}	75	V_{DDQ}	195	ODT0	106	V_{SS}	226	DQ54
17	V_{SS}	137	CK1	47	V_{SS}	167	NC	76	$\overline{S}1$	196	NC/A13	107	DQ50	227	DQ55
18	NC	138	$\overline{CK}1$	48	NC	168	NC	77	ODT1	197	V_{DD}	108	DQ51	228	V_{SS}
19	NC	139	V_{SS}	49	NC	169	V_{SS}	78	V_{DDQ}	198	V_{SS}	109	V_{SS}	229	DQ60
20	V_{SS}	140	DQ14	50	V_{SS}	170	V_{DDQ}	79	V_{SS}	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V_{DDQ}	171	CKE1	80	DQ32	200	DQ37	111	DQ57	231	V_{SS}
22	DQ11	142	V_{SS}	52	CKE0	172	V_{DD}	81	DQ33	201	V_{SS}	112	V_{SS}	232	DM7
23	V_{SS}	143	DQ20	53	V_{DD}	173	NC	82	V_{SS}	202	DM4	113	$\overline{DQS}7$	233	NC
24	DQ16	144	DQ21	54	NC	174	NC	83	$\overline{DQS}4$	203	NC	114	DQS7	234	V_{SS}
25	DQ17	145	V_{SS}	55	NC	175	V_{DDQ}	84	DQS4	204	V_{SS}	115	V_{SS}	235	DQ62
26	V_{SS}	146	DM2	56	V_{DDQ}	176	A12	85	V_{SS}	205	DQ38	116	DQ58	236	DQ63
27	$\overline{DQS}2$	147	NC	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V_{SS}
28	DQS2	148	V_{SS}	58	A7	178	V_{DD}	87	DQ35	207	V_{SS}	118	V_{SS}	238	VDDSPD
29	V_{SS}	149	DQ22	59	V_{DD}	179	A8	88	V_{SS}	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V_{SS}				

NC = No Connect, RFU = Reserved for Future Use
1. Pin173 Pin174 are reserved for 2Gb/4Gb comp. base Unbuffered DIMM.
2. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

Function Block Diagram







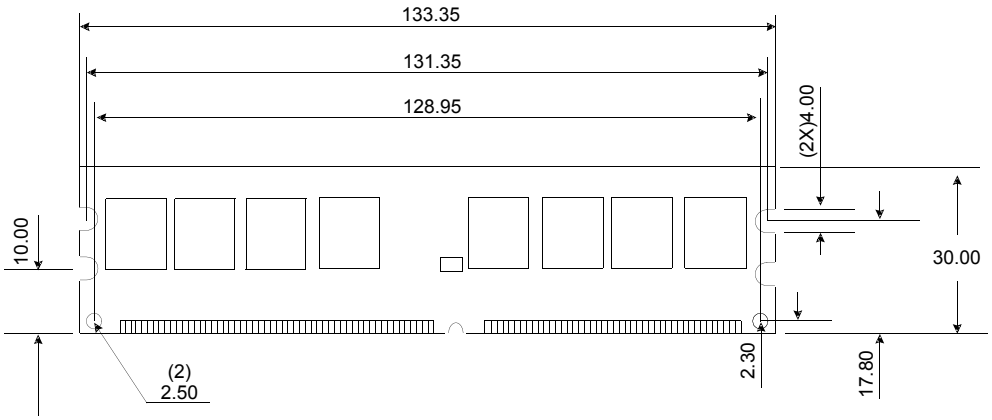
BA0 - BA1	BA0-BA1 : DDR2 SDRAMs D0 - D15
A0 - A13	A0-A13 : DDR2 SDRAMs D0 - D15
CKE0	CKE : DDR2 SDRAMs D0 - D7
CKE1	CKE : DDR2 SDRAMs D8 - D15
$\overline{RAS}$	$\overline{RAS}$: DDR2 SDRAMs D0 - D15
$\overline{CAS}$	$\overline{CAS}$: DDR2 SDRAMs D0 - D15
$\overline{WE}$	$\overline{WE}$: DDR2 SDRAMs D0 - D15
ODT0	ODT : DDR2 SDRAMs D0 - D7
ODT1	ODT : DDR2 SDRAMs D8 - D15

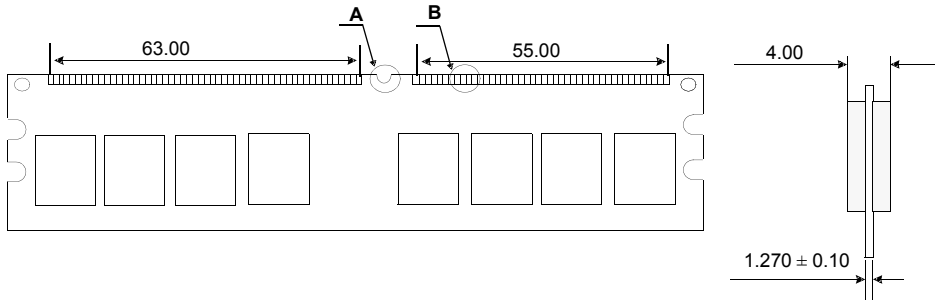
* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/$\overline{CK0}$	4 DDR2 SDRAMs
*CK1/$\overline{CK1}$	6 DDR2 SDRAMs
*CK2/$\overline{CK2}$	6 DDR2 SDRAMs

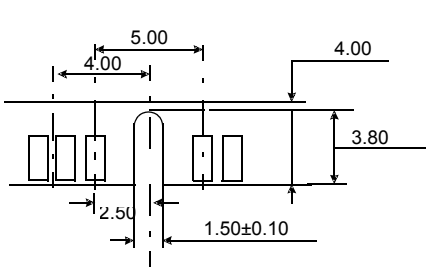
*Wire per Clock Loading Table/Wiring Diagrams

Notes :
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 3 Ohms ± 5%.

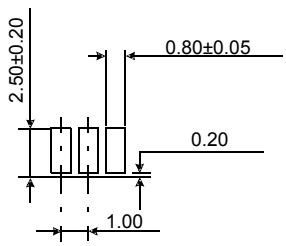
PACKAGE DIMENSIONS



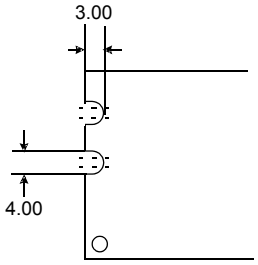




Detail A



Detail B



The used device is 128M x8 DDR2,FBGA.