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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR μ PA2770GR

SWITCHING DUAL P-CHANNEL POWER MOS FET

DESCRIPTION

The $\mu PA2770GR$ is Dual P-Channel MOS Field Effect Transistors designed for Motor Drive application.

FEATURES

· Low on-state resistance

R_{DS(on)1} = 26 mΩ MAX. (V_{GS} = -10 V, I_D = -3.5 A) R_{DS(on)2} = 35 mΩ MAX. (V_{GS} = -4.5 V, I_D = -3.5 A)

- Low input capacitance
 C_{iss} = 2200 pF TYP.
- · Built-in gate protection diode
- Small and surface mount package (Power SOP8)

ABSOLUTE MAXIMUM RATINGS

$(T_A = 25^{\circ}C \text{ All terminals are connected.})$

PARAMETER	SYMBOL	RATINGS	UNIT
Drain to Source Voltage (V _{GS} = 0 V)	VDSS	-40	V
Gate to Source Voltage (V _{DS} = 0 V)	Vgss	∓20	V
Drain Current (DC)	I _{D(DC)}	∓7	Α
Drain Current (pulse) Note 1	I _{D(pulse)}	∓28	Α
Total Power Dissipation (1 unit) Note 2	Рт	1.7	W
Total Power Dissipation (2 units) Note 2	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current Note 3	las	-7	Α
Single Avalanche Energy Note 3	Eas	4.9	mJ

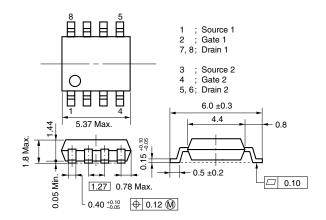
- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 2. Mounted on ceramic substrate of 2000 mm² x 1.6 mm
 - 3. Starting Tch = 25°C, VdD = -20 V x Vdss, Rg = 25 Ω , L = 100 μ H, Vgs = -20 V \rightarrow 0 V

ORDERING INFORMATION

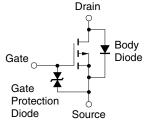
PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
μ PA2770GR-E1-AY ^{Note}				
μ PA2770GR-E2-AY ^{Note}	Pure Sn	Tape 2500 p/reel	Power SOP8	

Note Pb-free (This product does not contain Pb in the external electrode.)

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT (1/2 circuit)



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

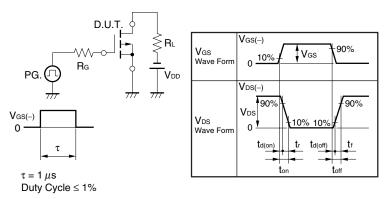
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	Ipss	V _{DS} = -40 V, V _{GS} = 0 V			-10	μΑ
Gate Leakage Current	Igss	V _{GS} = ∓20 V, V _{DS} = 0 V			∓10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance Note	y fs	V _{DS} = -10 V, I _D = -3.5 A	5	11		S
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = -10 V, I _D = -3.5 A		21	26	mΩ
Drain to Source On-state Resistance Note	R _{DS(on)2}	V _{GS} = -4.5 V, I _D = -3.5 A		24	35	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V		2200		pF
Output Capacitance	Coss	V _{GS} = 0 V		350		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		260		pF
Turn-on Delay Time	t _{d(on)}	$V_{DD} = -20 \text{ V}, I_D = -3.5 \text{ A}$		11		ns
Rise Time	tr	V _{GS} = -10 V		27		ns
Turn-off Delay Time	t _{d(off)}	$R_G = 10 \Omega$		160		ns
Fall Time	t _f			88		ns
Total Gate Charge	QG	I _D = -7 A		45		nC
Gate to Source Charge	Qgs	V _{DD} = -32 V		5.2		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = -10 V		12		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 7 A, V _{GS} = 0 V		0.84	1.5	V
Reverse Recovery Time	trr	I _F = -7 A, V _{GS} = 0 V		54		ns
Reverse Recovery Charge	Qrr	di/dt = -50 A/μs		25		nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$PG. \square \geqslant 50 \Omega$ $V_{GS} = -20 \rightarrow 0 \text{ V} \square \square$ V_{DD} V_{DD} V_{DD} $Starting T_{ch}$

TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T. & \\ \hline \\ I_G = -2 \text{ mA} \\ \hline \\ PG. & \\ \hline \\ \end{array} \begin{array}{c} R_L \\ \hline \\ V_{DD} \end{array}$$



dT - Percentage of Rated Power - %

20

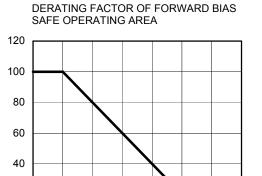
0

0

25

50

TYPICAL CHARACTERISTICS (TA = 25°C)



T_A - Ambient Temperature - °C

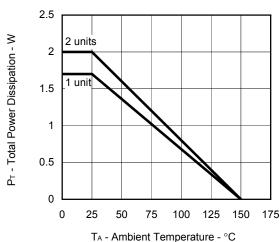
100 125

150

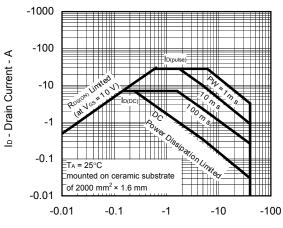
175

75

TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

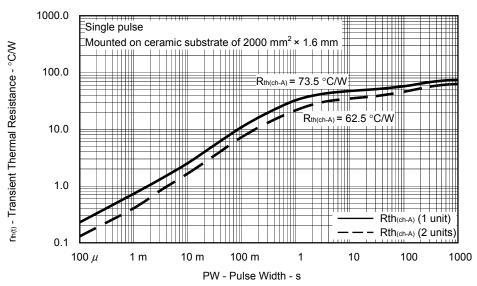


FORWARD BIAS SAFE OPERATING AREA



V_{DS} - Drain to Source Voltage - V

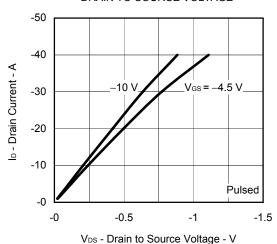
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



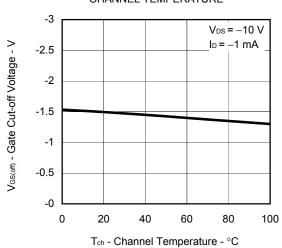
3



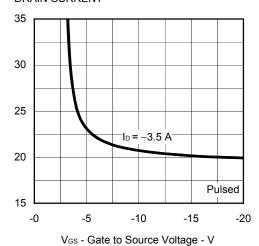
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



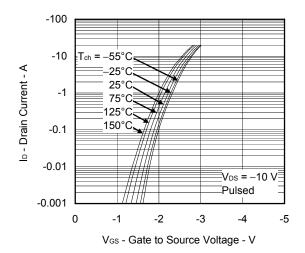
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



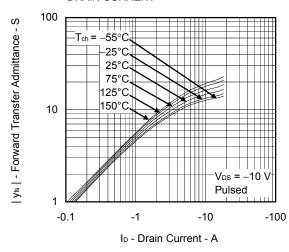
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



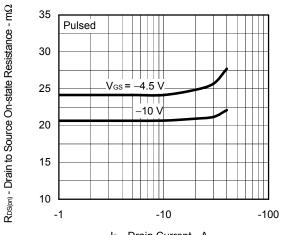
FORWARD TRANSFER CHARACTERISTICS



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

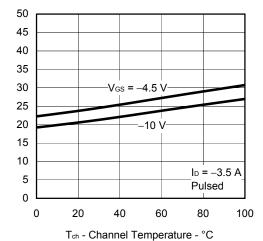


R_{DS(o1)} - Drain to Source On-state Resistance - mΩ

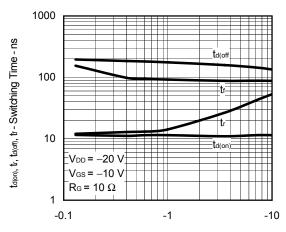


RDS(m) - Drain to Source On-state Resistance - m\Omega

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

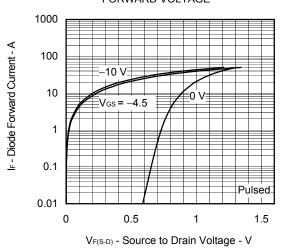


SWITCHING CHARACTERISTICS

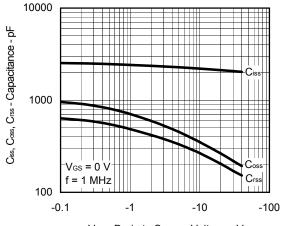


ID - Drain Current - A

SOURCE TO DRAIN DIODE FORWARD VOLTAGE

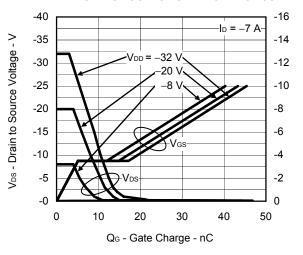


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

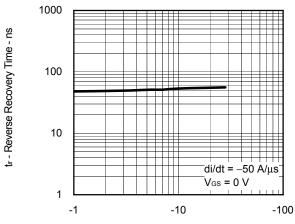


V_{DS} - Drain to Source Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



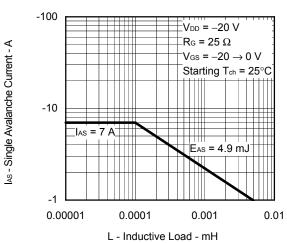
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



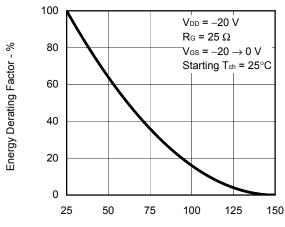
IF - Diode Forward Current - A

Ves - Gate to Source Voltage - V

SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



Starting T_{ch} - Starting Channel Temperature - $^{\circ}\text{C}$



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