FAIRCHILD SEMICONDUCTOR®

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FAN53600 / FAN53610
3 MHz, 600 mA / 1A Synchronous Buck Regulator

Features

- 600 mA or 1 A Output Current Capability
- 26 µA Typical Quiescent Current
- 3 MHz Fixed-Frequency Operation
- Best-in-Class Load Transient Response
- Best-in-Class Efficiency
- 2.3 V to 5.5 V Input Voltage Range
- 2.5 V to 3.3 V Fixed Output Voltage
- Low Ripple Light-Load PFM Mode
- Forced PWM and External Clock Synchronization
- Internal Soft-Start
- Input Under-Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- Optional Output Discharge
- 6-Bump WLCSP, 0.4 mm Pitch

Applications

- 3G, 4G, WiFi®, WiMAX™, and WiBro® Data Cards
- Tablets
- DSC, DVC
- Netbooks®, Ultra-Mobile PCs

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Description

The FAN53600/10 is a 3 MHz step-down switching voltage regulator, available in 600 mA or 1 A options, that delivers a fixed output from an input voltage supply of 2.5 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53600/10 is capable of delivering a peak efficiency of 92%, while maintaining efficiency over 80% at load currents as low as 1 mA.

The regulator operates at a nominal fixed frequency of 3 MHz, which reduces the value of the external components to as low as 1 µH for the output inductor and 4.7 µF for the output capacitor. In addition, the Pulse-Width Modulation (PWM) modulator can be synchronized to an external frequency source.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate the device in Power-Save Mode with a typical quiescent current of 26 µA. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed-frequency control, operating at 3 MHz. In Shutdown Mode, the supply current drops below 1 µA, reducing power consumption. For applications that require minimum ripple or fixed frequency, PFM Mode can be disabled using the MODE pin.

The FAN53600/10 is available in 6-bump, 0.4 mm pitch, Wafer-Level Chip-Scale Package (WLCSP).

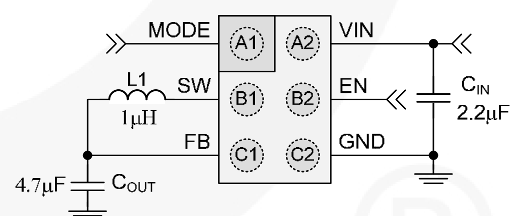

Figure 1. Typical Application

Ordering Information

Part Number	Output Voltage(1)	Max. Output Current	Active Discharge(2)	Package	Temperature Range	Packing
FAN53610AUC29X	2.9 V	1 A	Yes	WLCSP-6, 0.4 mm Pitch	–40 to +85°C	Tape and Reel
FAN53610AUC30X	3.0 V	1A	Yes			
FAN53600AUC33X	3.3 V	600 mA	Yes			

Notes:
1. Other voltage options available on request. Contact a Fairchild representative.
2. All voltage and output current options are available with or without active discharge. Contact a Fairchild representative.

Pin Configurations

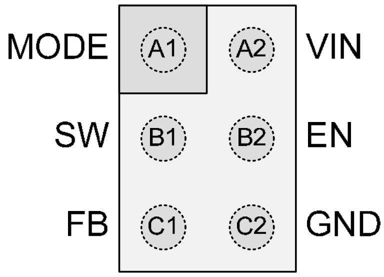

Figure 2. Bumps Facing Down

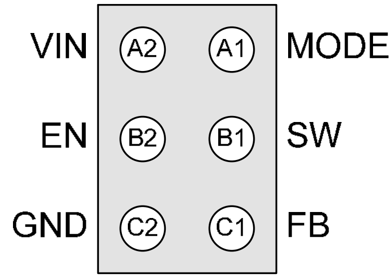

Figure 3. Bumps Facing Up

Pin Definitions

Pin #	Name	Description
A1	MODE	**MODE**. Logic 1 on this pin forces the IC to stay in PWM Mode. Logic 0 allows the IC to automatically switch to PFM Mode during light loads. The regulator also synchronizes its switching frequency to two times the frequency provided on this pin. Do not leave this pin floating.
B1	SW	**Switching Node**. Connect to output inductor.
C1	FB	**Feedback**. Connect to output voltage.
C2	GND	**Ground**. Power and IC ground. All signals are referenced to this pin.
B2	EN	**Enable**. The device is in Shutdown Mode when voltage to this pin is <0.4 V and enabled when >1.2 V. Do not leave this pin floating.
A2	VIN	**Input Voltage**. Connect to input power source.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Input Voltage		–0.3	7.0	V
V_{SW}	Voltage on SW Pin		–0.3	V_{IN} + 0.3(3)	V
V_{CTRL}	EN and MODE Pin Voltage		–0.3	V_{IN} + 0.3(3)	V
	Other Pins		–0.3	V_{IN} + 0.3(3)	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	3.5		kV
		Charged Device Model per JESD22-C101	1.5		
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:
3. Lesser of 7 V or V_{IN}+0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range		2.3		5.5	V
I_{OUT}	Output Current	FAN53600	0		600	mA
		FAN53610	0		1	A
L	Inductor			1		μH
C_{IN}	Input Capacitor			2.2		μF
C_{OUT}	Output Capacitor V_{OUT}<2.7 V		1.6	4.7	12.0	μF
	V_{OUT} ≥2.7 V			10		
T_A	Operating Ambient Temperature		–40		+85	°C
T_J	Operating Junction Temperature		–40		+125	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with two-layer 1s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	150	°C/W

Electrical Characteristics

Minimum and maximum values are at $V_{IN} = V_{EN}$ = 2.3 V to 5.5 V, V_{MODE} = 0 V (AUTO Mode), and T_A = -40°C to +85°C; circuit of Figure 1, unless otherwise noted. Typical values are at T_A = 25°C, $V_{IN} = V_{EN}$ = 3.6 V, V_{OUT}=2.9 V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supplies						
I_Q	Quiescent Current	No Load, Not Switching		26		µA
		PWM Mode		3		mA
$I_{(SD)}$	Shutdown Supply Current	V_{IN} = 3.6 V, EN = GND		0.25	1.00	µA
V_{UVLO}	Under-Voltage Lockout Threshold	Rising V_{IN}		2.15	2.27	V
V_{UVHYST}	Under-Voltage Lockout Hysteresis			200		mV
Logic Inputs: EN and MODE Pins						
V_{IH}	Enable HIGH-Level Input Voltage		1.2			V
V_{IL}	Enable LOW-Level Input Voltage				0.4	V
V_{LHYST}	Logic Input Hysteresis Voltage			100		mV
I_{IN}	Enable Input Leakage Current	Pin to V_{IN} or GND		0.01	1.00	µA
Switching and Synchronization						
f_{SW}	Switching Frequency(4)	V_{IN} = 3.6 V, T_A = 25°C	2.7	3.0	3.3	MHz
f_{SYNC}	MODE Synchronization Range(4)	Square Wave at MODE Input	1.3	1.5	1.7	MHz
Regulation						
V_O	Output Voltage Accuracy, 2.500 V to 2.900 V	I_{LOAD} = 0 to 400 mA, $V_{IN} \geq V_{OUT}$ + 150 mV	-5		+3	%
		I_{LOAD} = 0 to 600 mA, $V_{IN} \geq V_{OUT}$ + 300 mV	-3		+3	%
		I_{LOAD} = 0 to 1000 mA, V_{IN} =3.6V	-4		+3	%
	Output Voltage Accuracy, 2.900 V to 3.300 V	I_{LOAD} = 0 to 600 mA, $V_{IN} \geq V_{OUT}$ + 300 mV	-3		+3	%
		I_{LOAD} = 0 to 1000 mA, V_{IN} =5.0 V	-4		+3	%
t_{SS}	Soft-Start	From EN Rising Edge		180	300	µs
Output Driver						
$R_{DS(on)}$	PMOS On Resistance	$V_{IN} = V_{GS}$ = 3.6 V		175		mΩ
	NMOS On Resistance	$V_{IN} = V_{GS}$ = 3.6 V		165		mΩ
$I_{LIM(OL)}$	PMOS Peak Current Limit	Open-Loop for FAN53600	900	1100	1250	mA
		Open-Loop for FAN53610	1500	1750	2000	mA
R_{DIS}	Output Discharge Resistance	EN = GND		230		Ω
T_{TSD}	Thermal Shutdown	CCM Only		150		°C
T_{HYS}	Thermal Shutdown Hysteresis			15		°C

Notes:

4. Limited by the effect of t_{OFF} minimum *(see Operation Description section)*.
5. The Electrical Characteristics table reflects open-loop data.

Typical Performance Characteristics

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6$ V, $V_{MODE} = 0$ V (AUTO Mode), and $T_A = 25°C$.

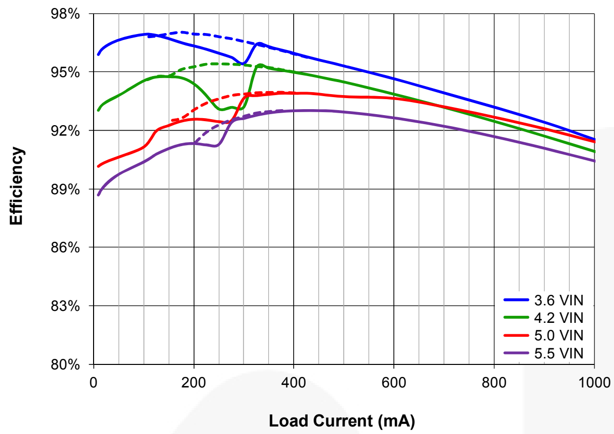

Figure 4. Efficiency vs. Load Current and Input Voltage, V_{OUT}=3.3 V, Dotted for Decreasing Load

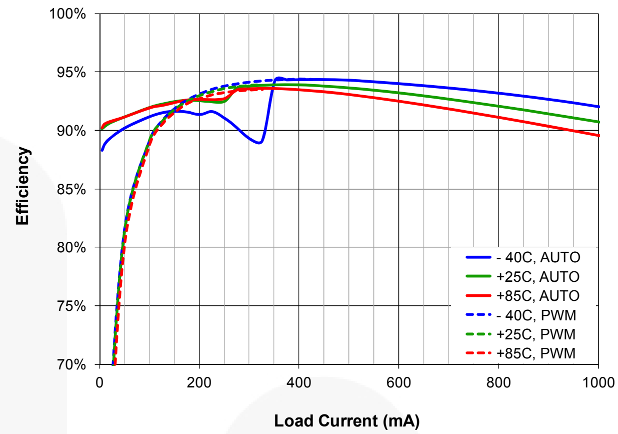

Figure 5. Efficiency vs. Load Current and Temperature V_{IN}=5 V, V_{OUT}=3.3 V, Dotted for FPWM

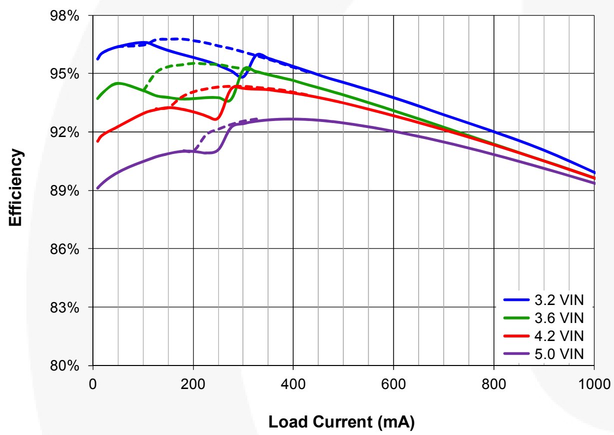

Figure 6. Efficiency vs. Load Current and Input Voltage, V_{OUT}=2.9 V, Dotted for Decreasing Load

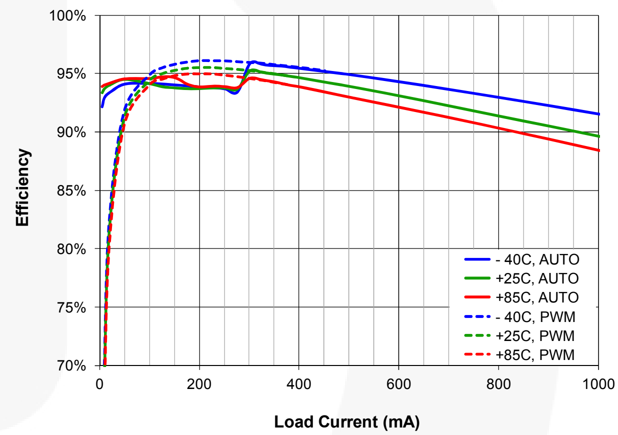

Figure 7. Efficiency vs. Load Current and Temperature, V_{OUT}=2.9 V, Dotted for FPWM

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6$ V, $V_{MODE} = 0$ V (AUTO Mode), and $T_A = 25°C$.

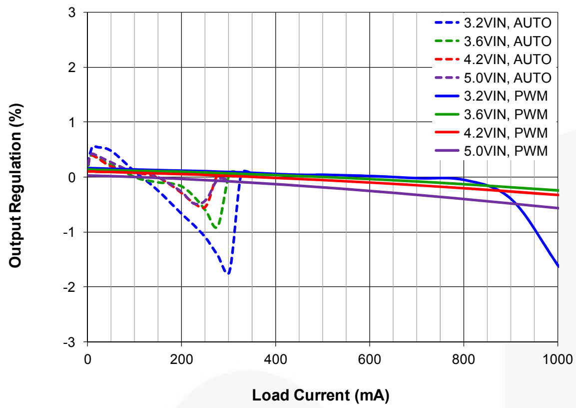

Figure 8. ΔV$_{OUT}$ (%) vs. Load Current and Input Voltage, V_{OUT}=2.9 V, Normalized to 3.6 V_{IN}, 500 mA Load, FPWM, Dotted for Auto Mode

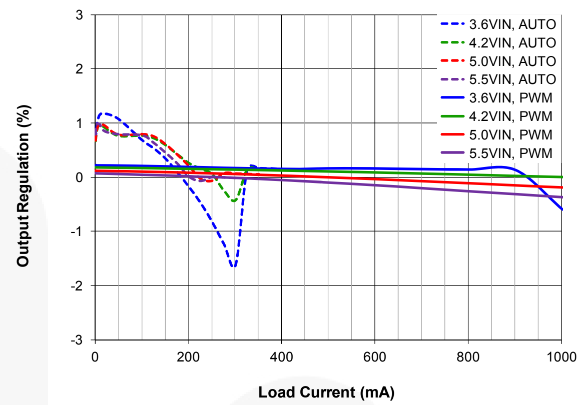

Figure 9. ΔV$_{OUT}$ (%) vs. Load Current and Input Voltage, V_{OUT}=3.3 V, Normalized to 3.6 V_{IN}, 500 mA Load, FPWM, Dotted for Auto Mode

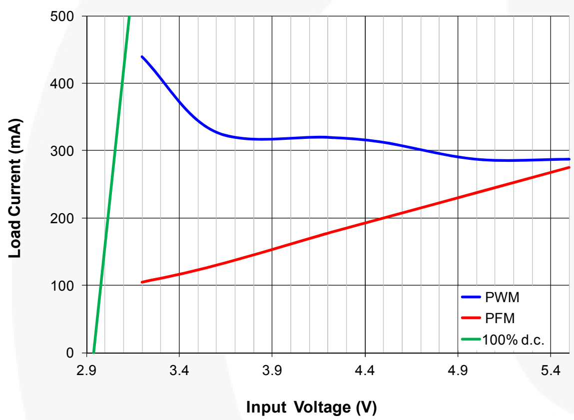

Figure 10. PFM / PWM /100% Duty Cycle Boundary vs. Input Voltage, V_{OUT}=2.9 V

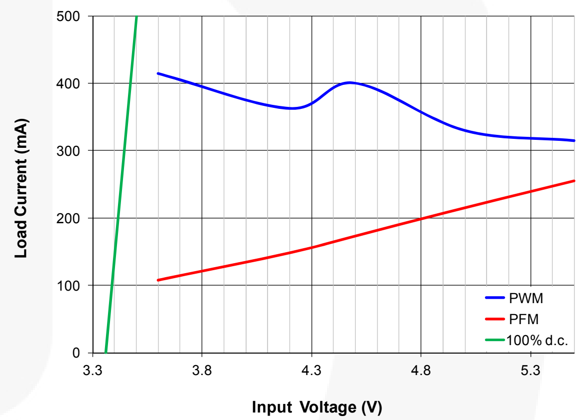

Figure 11. PFM / PWM /100% Duty Cycle Boundary vs. Input Voltage, V_{OUT}=3.3 V

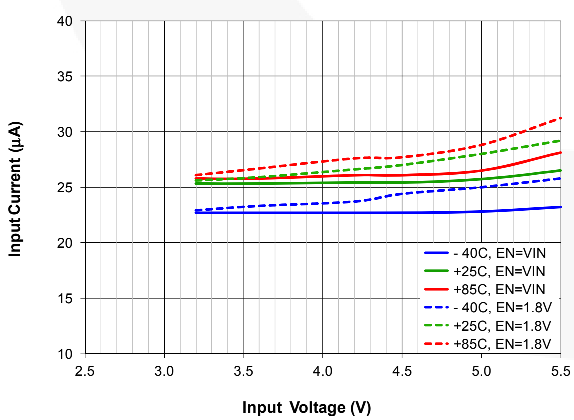

Figure 12. Quiescent Current vs. Input Voltage and Temperature, V_{OUT}=2.9 V, EN=V_{IN} Solid, Dotted for EN=1.8 V

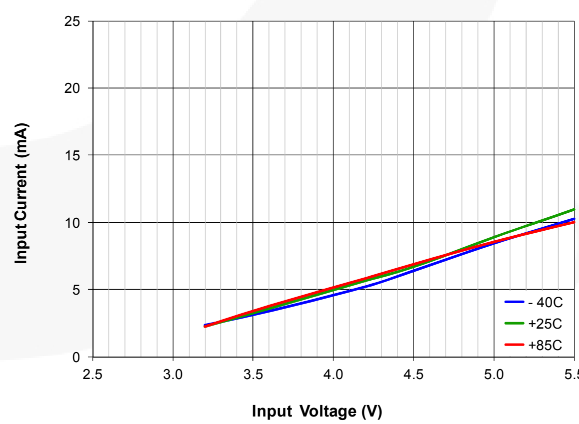

Figure 13. Quiescent Current vs. Input Voltage and Temperature, V_{OUT}=2.9 V, Mode=EN=V_{IN} (FPWM)

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6$ V, $V_{MODE} = 0$ V (AUTO Mode), and $T_A = 25°C$.

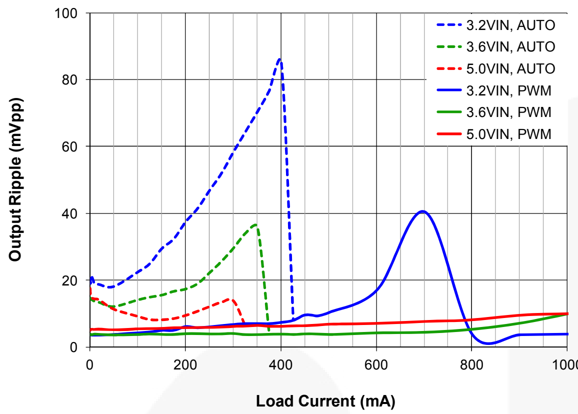

Figure 14. Output Ripple vs. Load Current and Input Voltage, V_{OUT}=2.9 V, FPWM, Dotted for Auto Mode

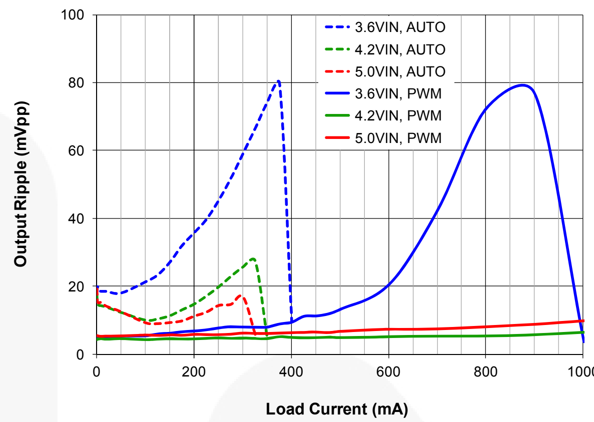

Figure 15. Output Ripple vs. Load Current and Input Voltage, V_{OUT}=3.3 V, FPWM, Dotted for Auto Mode

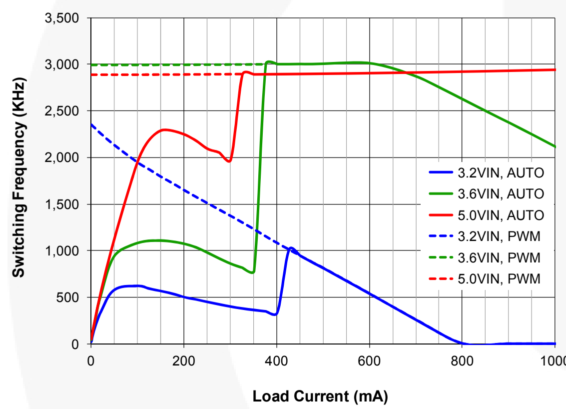

Figure 16. Frequency vs. Load Current and Input Voltage, V_{OUT}=2.9 V, Auto Mode, Dotted for FPWM

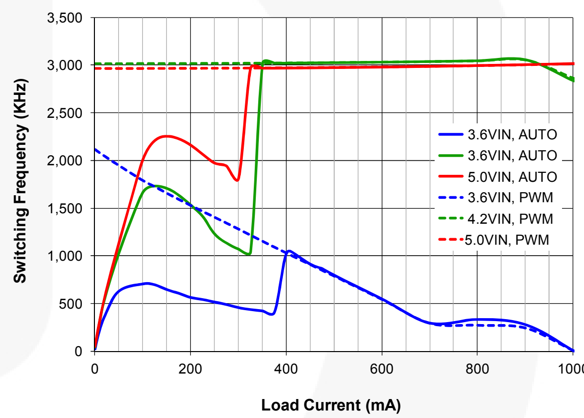

Figure 17. Frequency vs. Load Current and Input Voltage, V_{OUT}=3.3 V, Auto Mode, Dotted for FPWM

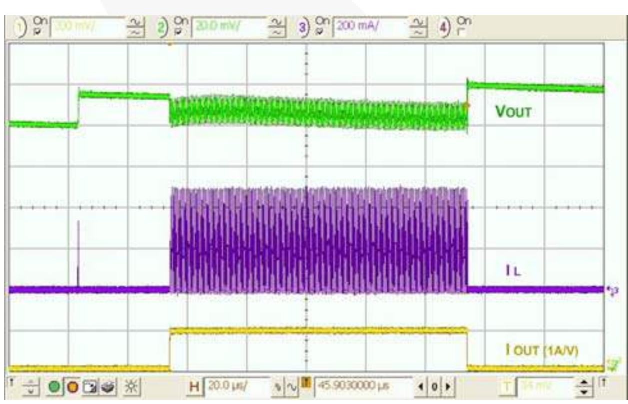

Figure 18. Load Transient, V_{IN}=5 V, V_{OUT}=3.3 V, 10-200-10 mA, 100 ns Edge

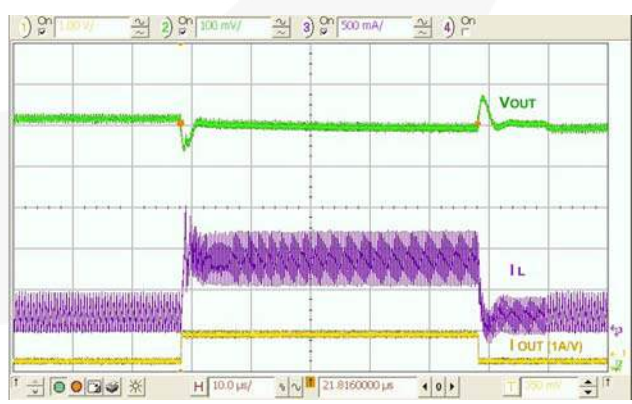

Figure 19. Load Transient, V_{IN}=5 V, V_{OUT}=3.3 V, 200-800-200 mA, 100 ns Edge

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6$ V, $V_{MODE} = 0$ V (AUTO Mode), and $T_A = 25°C$.

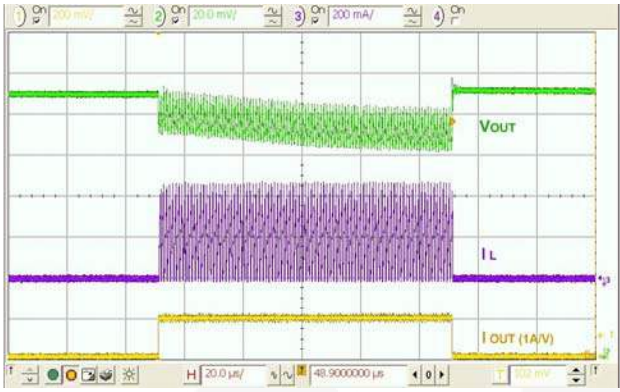

Figure 20. Load Transient, V_{IN}=5 V, V_{OUT}=2.9 V, 10-200-10 mA, 100 ns Edge

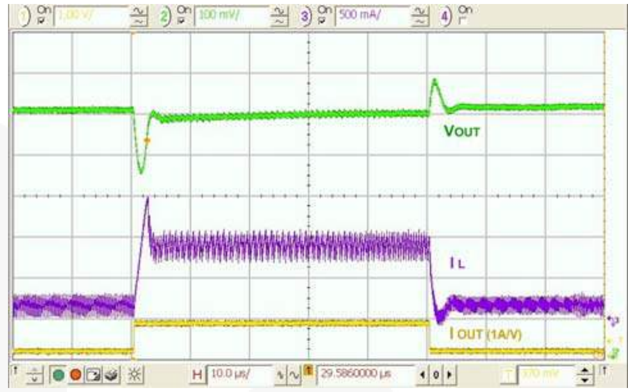

Figure 21. Load Transient, V_{IN}=5 V, V_{OUT}=2.9 V, 200-800-200 mA, 100 ns Edge

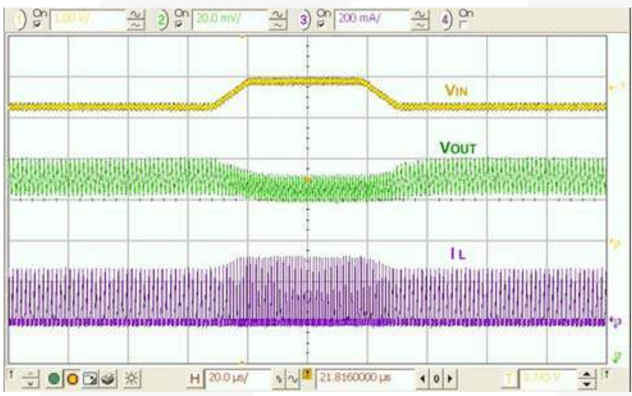

Figure 22. Line Transient, 3.3-3.9-3.3 V_{IN}, 10 µs Edge, V_{OUT}=2.9 V, 58 mA Load

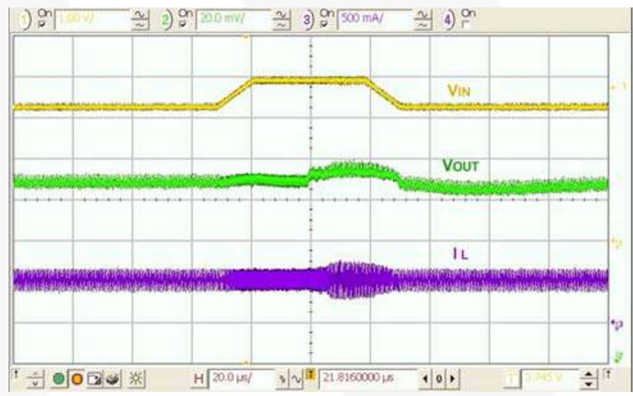

Figure 23. Line Transient, 3.3-3.9-3.3 V_{IN}, 10 µs Edge, V_{OUT}=2.9 V, 600 mA Load

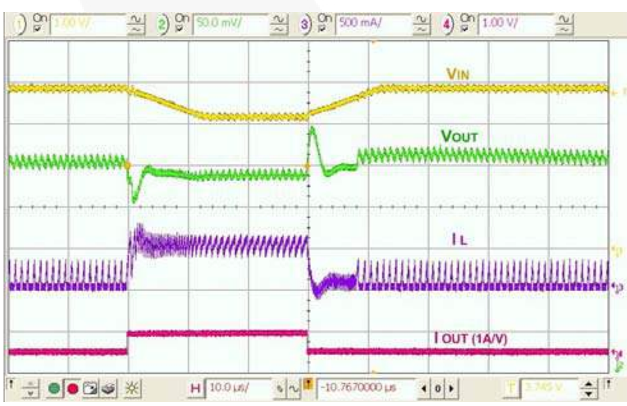

Figure 24. Combined Line / Load Transient, V_{OUT}=2.9 V, 3.9-3.3-3.9 V_{IN}, 10 µs Edge, 58-500-58 mA Load, 100 ns Edge

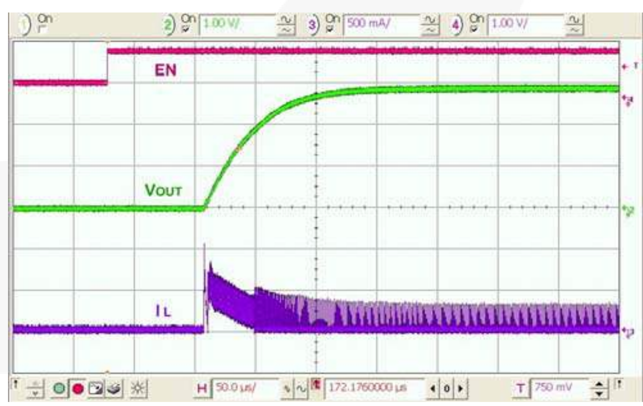

Figure 25. Startup, V_{OUT}=2.9 V, 50 Ω Load

Typical Performance Characteristics (Continued)

Unless otherwise noted, V_{IN} = V_{EN} = 3.6 V, V_{MODE} = 0 V (AUTO Mode), and T_A = 25°C.

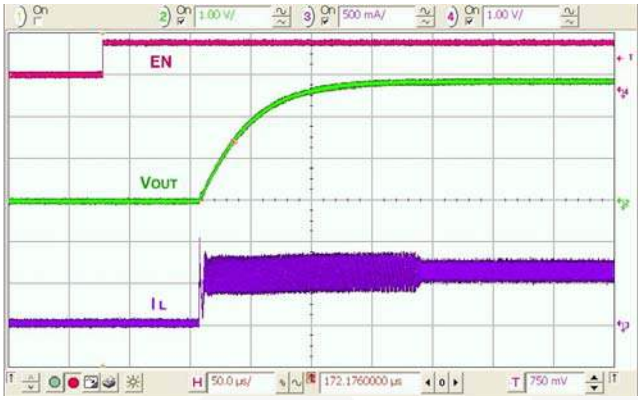

Figure 26. Startup, V_{OUT}=2.9 V, 4.7 Ω Load

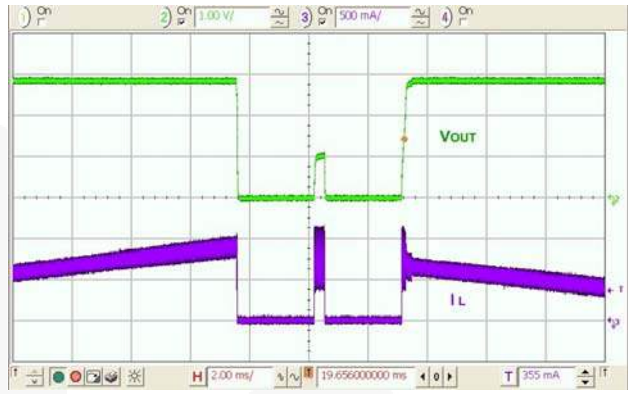

Figure 27. Over-Current, Load Increasing Past Current Limit, V_{OUT}=2.9 V, FAN53600

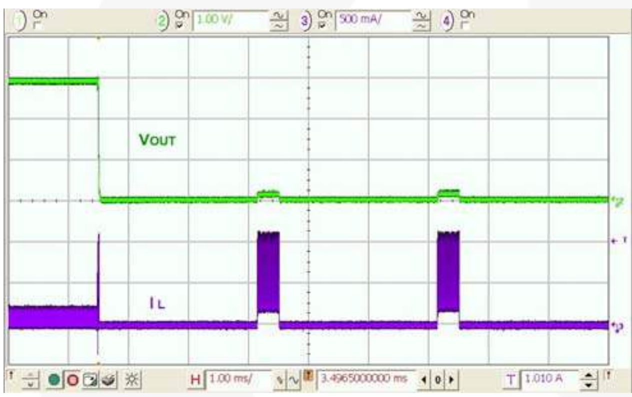

Figure 28. 250 mΩ Fault, Rapid Fault, V_{OUT}=2.9 V, FAN53600

Operation Description

The FAN53600/10 is a 3 MHz, step-down switching voltage regulator, available in 600 mA or 1 A options, that delivers a fixed output from an input voltage supply of 2.3 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53600/10 is capable of delivering a peak efficiency of 92%, while maintaining efficiency over 80% at load currents as low as 1 mA.

The regulator operates at a nominal fixed frequency of 3 MHz, which reduces the value of the external components to as low as 1 µH for the output inductor and 4.7 µF for the output capacitor. In addition, the PWM modulator can be synchronized to an external frequency source.

Control Scheme

The FAN53600/10 uses a proprietary, non-linear, fixed-frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN53600/10 operates in Discontinuous Current (DCM), single-pulse, PFM Mode; which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is seamless, with a glitch of less than 18 mV at V_{OUT} during the transition between DCM and CCM modes.

Combined with exceptional transient response characteristics, the very low quiescent current of the controller (26 µA) maintains high efficiency, even at very light loads, while preserving fast transient response for applications requiring tight output regulation.

100% Duty Cycle Operation

When V_{IN} approaches V_{OUT}, the regulator increases its duty cycle until 100% duty cycle is reached. As the duty cycle approaches 100%, the switching frequency declines due to the minimum off-time ($t_{OFF(MIN)}$) of about 50 ns imposed by the control circuit. When 100% duty cycle is reached, V_{OUT} follows V_{IN} with a drop-out voltage ($V_{DROPOUT}$) determined by the total resistance between V_{IN} and V_{OUT} as calculated by:

$$V_{DROPOUT} = I_{LOAD} \bullet \left(PMOS\ R_{DS(ON)} + DCR_L \right) \quad (1)$$

Enable and Soft-Start

When EN is LOW, all circuits are off and the IC draws ~50 nA of current. When EN is HIGH and V_{IN} is above its UVLO threshold, the regulator begins a soft-start cycle. The output ramp during soft-start is a fixed slew rate of 50 mV/µs from 0 to 1 V_{OUT}, then 12.5 mV/µs until the output reaches its setpoint. Regardless of the state of the MODE pin, PFM Mode is enabled to prevent current from being discharged from C_{OUT} if soft-start begins when C_{OUT} is charged.

All voltage options can be ordered with a feature that actively discharges FB to ground through a 230 Ω path when EN is LOW. Raising EN above its threshold voltage activates the part and starts the soft-start cycle. During soft-start, the internal reference is ramped using an exponential RC shape to prevent overshoot of the output voltage. Current limiting minimizes inrush during soft-start.

The IC may fail to start if heavy load is applied during startup and/or if excessive C_{OUT} is used. This is due to the current-limit fault response, which protects the IC in the event of an over-current condition present during soft-start.

The current required to charge C_{OUT} during soft-start, commonly referred to as "displacement current," is given as:

$$I_{DISP} = C_{OUT} \bullet \frac{dV}{dt} \quad (2)$$

where the $\frac{dV}{dt}$ term refers to the soft-start slew rate above.

To prevent shutdown during soft-start, the following condition must be met:

$$I_{DISP} + I_{LOAD} < I_{MAX(DC)} \quad (3)$$

where $I_{MAX(DC)}$ is the maximum load current the IC is guaranteed to support.

Startup into Large C_{OUT}

Multiple soft-start cycles are required for no-load startup if C_{OUT} is greater than 15 µF. Large C_{OUT} requires light initial load to ensure the FAN53600/10 starts appropriately. The IC shuts down for 1.3 ms when I_{DISP} exceeds I_{LIMIT} for more than 210 µs of current limit. The IC then begins a new soft-start cycle. Since C_{OUT} retains its charge when the IC is off, the IC reaches regulation after multiple soft-start attempts.

MODE Pin

Logic 1 on this pin forces the IC to stay in PWM Mode. Logic 0 allows the IC to automatically switch to PFM during light loads. If the MODE pin is toggled, with a frequency between 1.3 MHz and 1.7 MHz, the converter synchronizes its switching frequency to two times the frequency on the MODE pin (f_{MODE}).

The MODE pin is internally buffered with a Schmitt trigger, which allows the MODE pin to be driven with slow rise and fall times. An asymmetric duty cycle for frequency synchronization is also permitted as long as the minimum time below $V_{IL(MAX)}$ or above $V_{IH(MAX)}$ is 100 ns.

Current Limit, Fault Shutdown, and Restart

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high-side switch. Upon reaching this point, the high-side switch turns off, preventing high currents from causing damage. The regulator continues to limit the current cycle by cycle. After 16 cycles of current limit, the regulator triggers an over-current fault, causing the regulator to shut down for about 1.3 ms before attempting a restart.

If the fault was caused by short circuit, the soft-start circuit attempts to restart and produces an over-current fault after about 250 µs, which results in a duty cycle of less than 0%, limiting power dissipation.

The closed-loop peak-current limit, $I_{LIM(PK)}$, is not the same as the open-loop tested current limit, $I_{LIM(OL)}$, in the Electrical Characteristics table. This is primarily due to the effect of propagation delays of the IC current-limit comparator.

Under-Voltage Lockout (UVLO)

When EN is HIGH, the under-voltage lockout keeps the part from operating until the input supply voltage rises high enough to properly operate. This ensures no misbehavior of the regulator during startup or shutdown.

Thermal Shutdown (TSD)

When the die temperature increases, due to a high load condition and/or a high ambient temperature, the output switching is disabled until the temperature on the die has fallen sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 15°C hysteresis.

Minimum Off-Time and Switching Frequency

$t_{OFF(MIN)}$ is 50 ns. This imposes constraints on the maximum $\frac{V_{OUT}}{V_{IN}}$ that the FAN53600/10 can provide, or the maximum output voltage it can provide at low V_{IN} while maintaining a fixed switching frequency in PWM Mode.

When V_{IN} is LOW, fixed switching frequency is maintained as long as:

$$\frac{V_{OUT}}{V_{IN}} \le 1 - t_{OFF(MIN)} \bullet f_{SW} \approx 0.85 .$$

The switching frequency drops when the regulator cannot provide sufficient duty cycle at 3 MHz to maintain regulation. This occurs when V_{OUT} >0.85 V_{IN} at high load currents. The calculation for switching frequency is given by:

$$f_{SW} = \min\left(\frac{1}{t_{SW(MAX)}}, 3MHz\right) \tag{4}$$

where:

$$t_{SW(MAX)} = 50ns \bullet \left(1 + \frac{V_{OUT} + I_{OUT} \bullet R_{OFF}}{V_{IN} - I_{OUT} \bullet R_{ON} - V_{OUT}}\right) \tag{5}$$

where:

$$R_{OFF} = R_{DSON\_N} + DCR_L$$

$$R_{ON} = R_{DSON\_P} + DCR_L .$$

Applications Information

Selecting the Inductor

The output inductor must meet both the required inductance and the energy handling capability of the application. The inductor value affects average current limit, the PWM-to-PFM transition point, output voltage ripple, and efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \bullet \left(\frac{V_{IN} - V_{OUT}}{L \bullet f_{SW}} \right) \quad (6)$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current, given by:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad (7)$$

The transition between PFM and PWM operation is determined by the point at which the inductor valley current crosses zero. The regulator DC current when the inductor current crosses zero, I_{DCM}, is:

$$I_{DCM} = \frac{\Delta I}{2} \quad (8)$$

The FAN53600/10 is optimized for operation with L = 1 µH, but is stable with inductances up to 2.2 µH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$.

Efficiency is affected by inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases DCR; but since ΔI increases, the RMS current increases, as do the core and skin effect losses:

$$I_{RMS} = \sqrt{I_{OUT(DC)}{}^2 + \frac{\Delta I^2}{12}} \quad (9)$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs, as well as the inductor DCR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current and higher DCR.

Table 1 shows the effects of inductance higher or lower than the recommended 1 µH on regulator performance.

Output Capacitor

Table 2 suggests 0402 capacitors. 0603 capacitors may further improve performance in that the effective capacitance is higher. This improves transient response and output ripple.

Increasing C_{OUT} has no effect on loop stability and can therefore be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is:

$$\Delta V_{OUT} = \Delta I_L \left[\frac{f_{SW} \cdot C_{OUT} \cdot ESR^2}{2 \cdot D \cdot (1 - D)} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \right] \quad (10)$$

Input Capacitor

The 2.2 µF ceramic input capacitor should be placed as close as possible between the VIN pin and GND to minimize parasitic inductance. If a long wire is used to bring power to the IC, additional "bulk" capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective capacitance value decreases as V_{IN} increases due to DC bias effects.

Table 1. Effects of Changes in Inductor Value (470 nH Recommended Value) on Regulator Performance

Inductor Value	$I_{MAX(LOAD)}$	ΔV_{OUT}	Transient Response
Increase	Increase	Decrease	Degraded
Decrease	Decrease	Increase	Improved

Table 2. Recommended Passive Components and Variation Due to DC Bias

Component	Description	Vendor	Min.	Typ.	Comment
L1	1 µH, 2012, 190 mΩ, 0.8 A	Murata LQM21PN1R0MC0		1 µH	Not recommended for 1 A load
	1 µH, 1.4 A, 85 mΩ, 2016	**Murata LQM2MPN1R0M**		1 µH	Utilized to generate graphs, Figure 4 — Figure 28
C_{IN}	2.2 µF, 6.3 V, X5R, 0402	Murata or Equivalent GRM155R60J225ME15 GRM188R60J225KE19D	1.0 µF	2.2 µF	Decrease primarily due to DC bias (V_{IN}) and elevated temperature
C_{OUT}	4.7 µF, X5R 0603	Murata or Equivalent GRM188R60G106ME47D	1.6 µF	4.7 µF	Decrease primarily due to DC bias (V_{OUT}) and elevated temperature

PCB Layout Guidelines

There are only three external components: the inductor and the input and output capacitors. For any buck switcher IC, including the FAN53600/10, it is important to place a low-ESR input capacitor very close to the IC, as shown in Figure 29. The input capacitor ensures good input decoupling, which helps reduce noise at the output terminals and ensures that the control sections of the IC do not behave erratically due to excessive noise. This reduces switching cycle jitter and ensures good overall performance. It is important to place the common GND of C_{IN} and C_{OUT} as close as possible to the C2 terminal. There is some flexibility in moving the inductor further away from the IC; in that case, V_{OUT} should be considered at the C_{OUT} terminal.

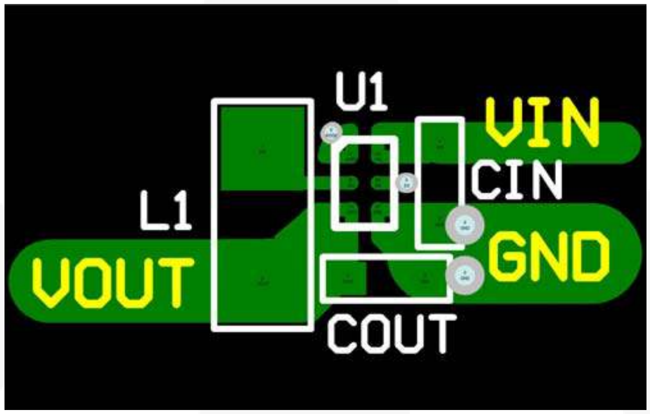

Figure 29. 3 MHz PCB Layout Guidance

Physical Dimensions

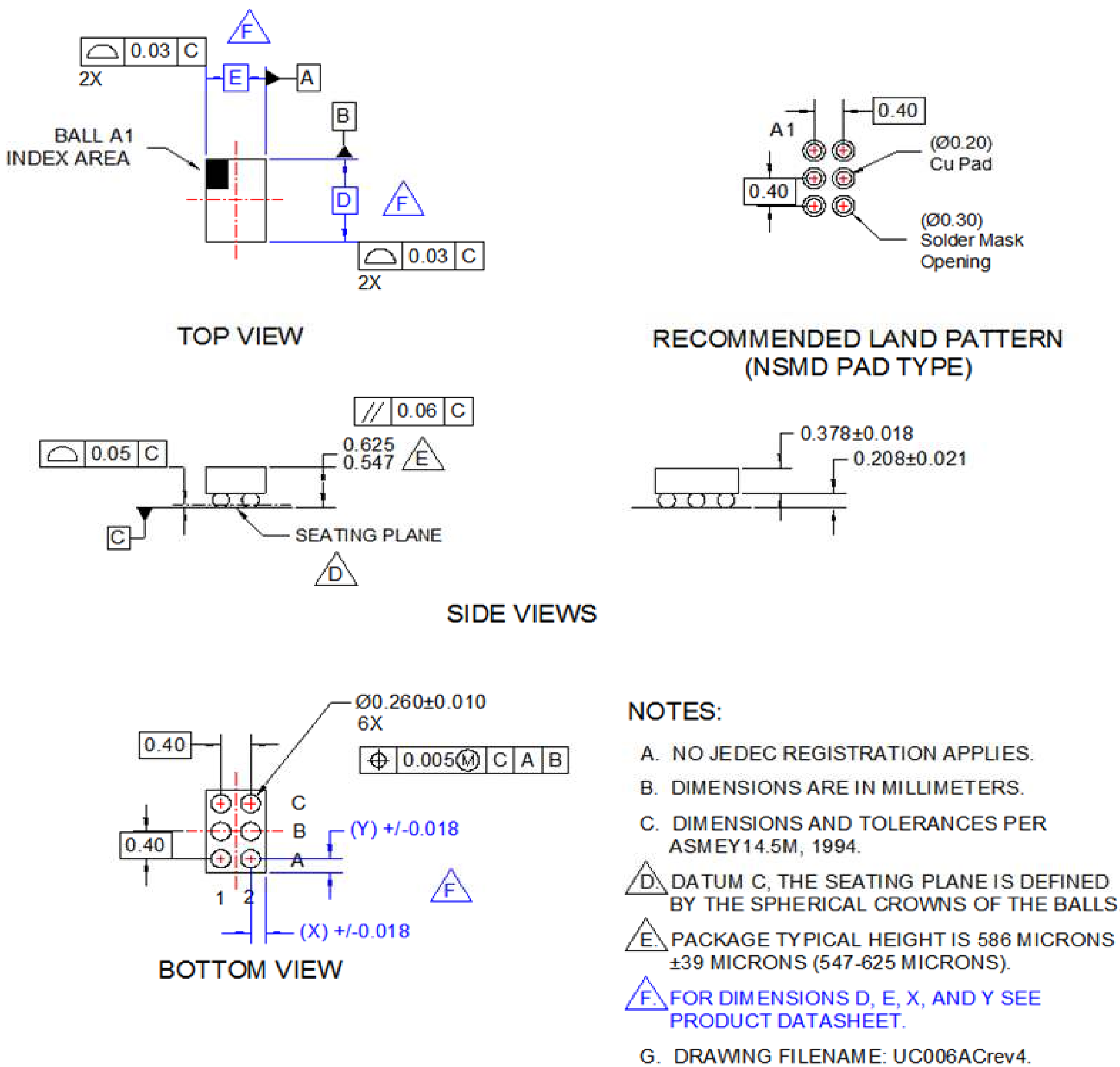

Figure 30. 6-Bump WLCSP, 0.4 mm Pitch

Product-Specific Dimensions

Product	D	E	X	Y
FAN53610AUC29X	1.160 ±0.030	0.860 ±0.030	0.230	0.180
FAN53610AUC30X	1.160 ±0.030	0.860 ±0.030	0.230	0.180
FAN53610UC33X	1.160 ±0.030	0.860 ±0.030	0.230	0.180

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