

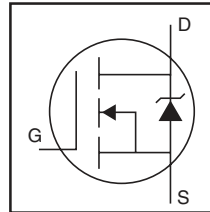
# IRFR3806PbF IRFU3806PbF

## Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

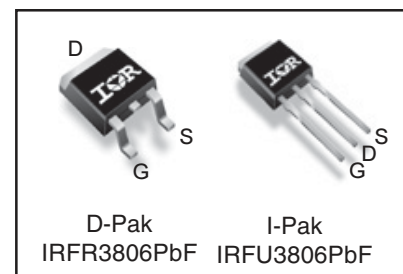
## Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability



HEXFET® Power MOSFET

$V_{DSS}$	<b>60V</b>
$R_{DS(on)}$ <b>typ.</b> <b>max.</b>	<b>12.6mΩ</b>
	<b>15.8mΩ</b>
$I_D$	<b>43A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

## Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	43	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	31	
$I_{DM}$	Pulsed Drain Current ①	170	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	71	W
	Linear Derating Factor	0.47	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
dv/dt	Peak Diode Recovery ③	24	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		

## Avalanche Characteristics

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	73	mJ
$I_{AR}$	Avalanche Current ①	25	A
$E_{AR}$	Repetitive Avalanche Energy ④	7.1	mJ

## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	2.12	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑦⑨	—	62	

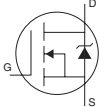
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.075	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5mA①
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	12.6	15.8	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 25A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	41	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 25A
Q <sub>g</sub>	Total Gate Charge	—	22	30	nC	I <sub>D</sub> = 25A
Q <sub>gs</sub>	Gate-to-Source Charge	—	5.0	—		V <sub>DS</sub> = 30V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	6.3	—		V <sub>GS</sub> = 10V ④
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	28.3	—		I <sub>D</sub> = 25A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V
R <sub>G(int)</sub>	Internal Gate Resistance	—	0.79	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	6.3	—	ns	V <sub>DD</sub> = 39V
t <sub>r</sub>	Rise Time	—	40	—		I <sub>D</sub> = 25A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	49	—		R <sub>G</sub> = 20Ω
t <sub>f</sub>	Fall Time	—	47	—		V <sub>GS</sub> = 10V ④
C <sub>iss</sub>	Input Capacitance	—	1150	—		V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	130	—		V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	67	—	pF	f = 1.0MHz
C <sub>oss</sub> eff. (ER)	Effective Output Capacitance (Energy Related)⑥	—	190	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 60V ⑥
C <sub>oss</sub> eff. (TR)	Effective Output Capacitance (Time Related)⑤	—	230	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 60V ⑤

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	43	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	170		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 25A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	22	33	ns	T <sub>J</sub> = 25°C V <sub>R</sub> = 51V, T <sub>J</sub> = 125°C I <sub>F</sub> = 25A
Q <sub>rr</sub>	Reverse Recovery Charge	—	17	26	nC	T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C di/dt = 100A/μs ④
I <sub>RRM</sub>	Reverse Recovery Current	—	1.4	—	A	T <sub>J</sub> = 25°C
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.23mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 25A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ I<sub>SD</sub> ≤ 25A, di/dt ≤ 1580A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

- ⑤ C<sub>oss</sub> eff. (TR) is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ C<sub>oss</sub> eff. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.

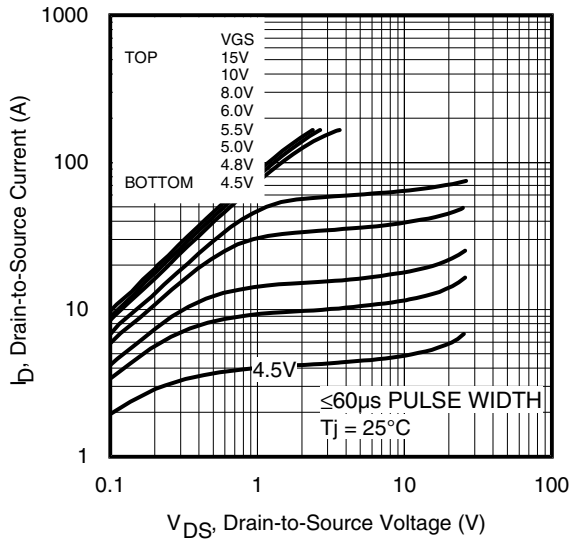


Fig 1. Typical Output Characteristics

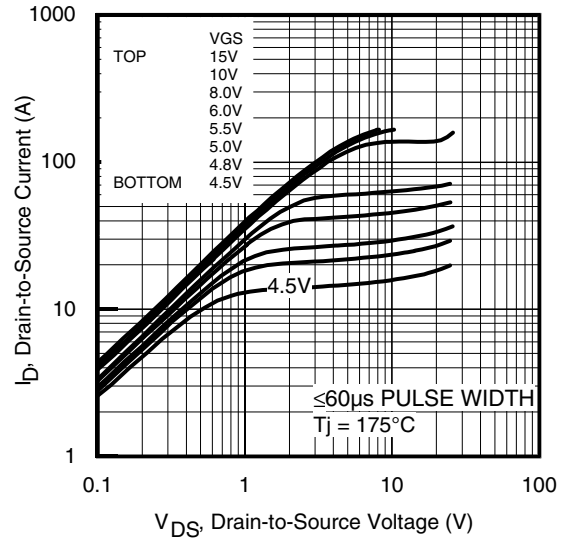


Fig 2. Typical Output Characteristics

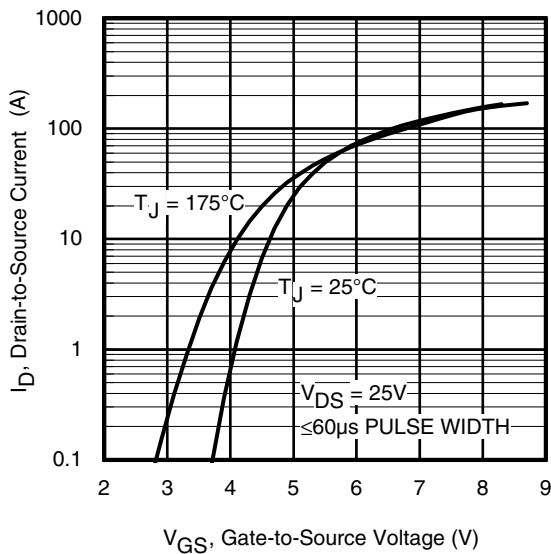


Fig 3. Typical Transfer Characteristics

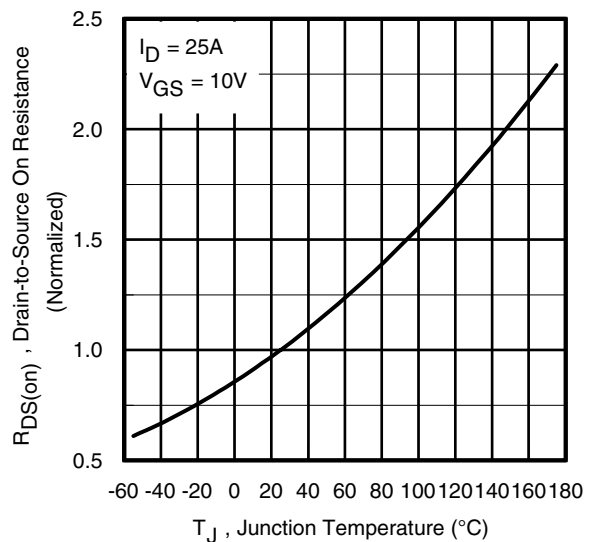


Fig 4. Normalized On-Resistance vs. Temperature

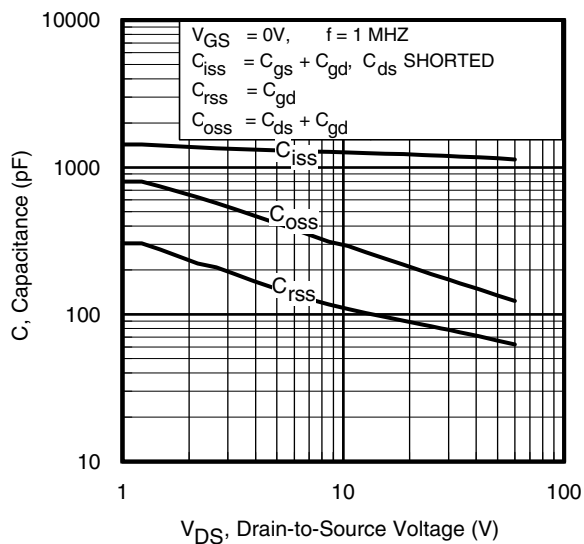


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

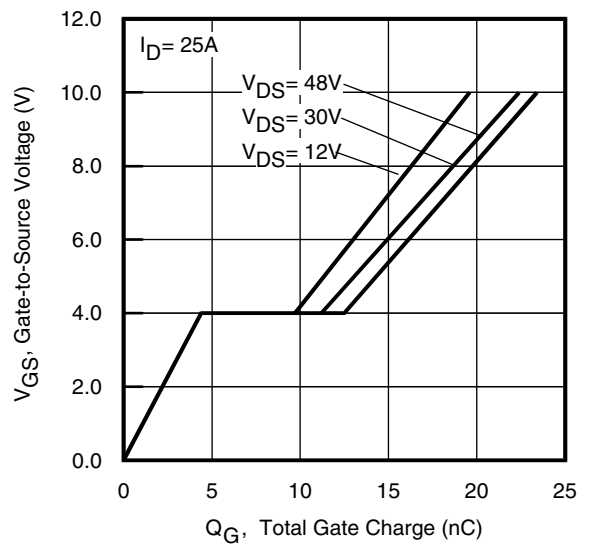


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

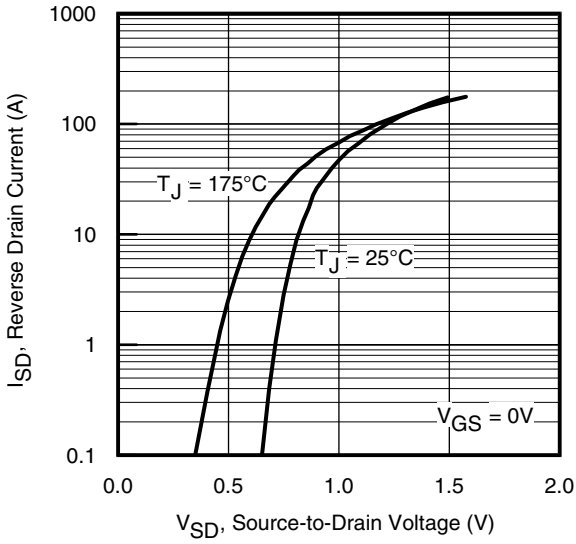


Fig 7. Typical Source-Drain Diode Forward Voltage

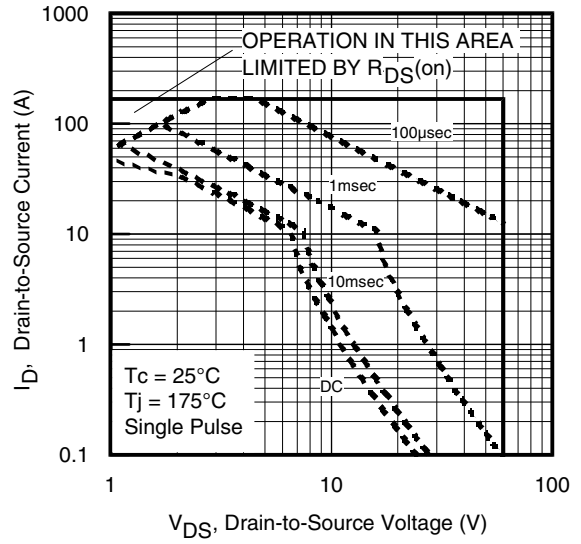


Fig 8. Maximum Safe Operating Area

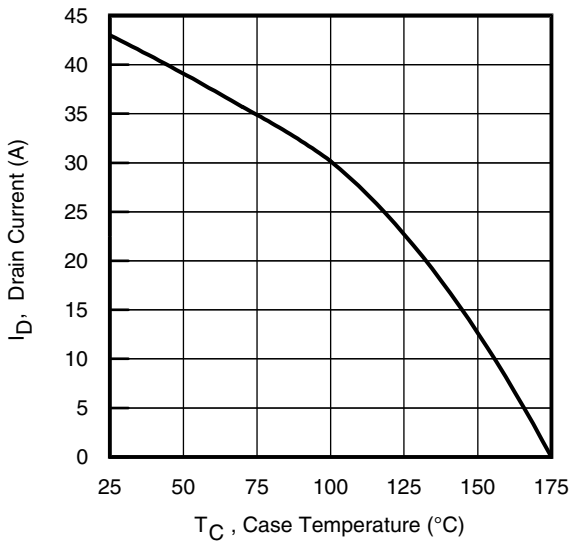


Fig 9. Maximum Drain Current vs. Case Temperature

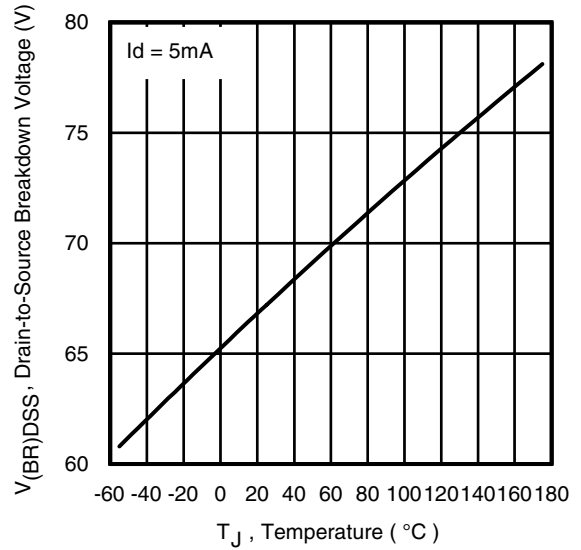


Fig 10. Drain-to-Source Breakdown Voltage

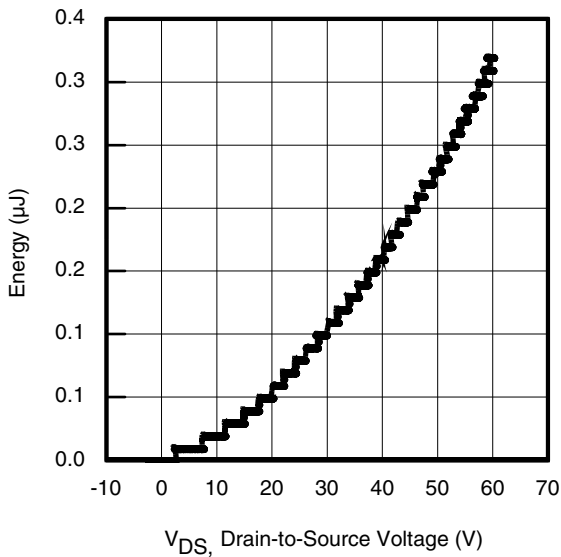


Fig 11. Typical C<sub>OSS</sub> Stored Energy

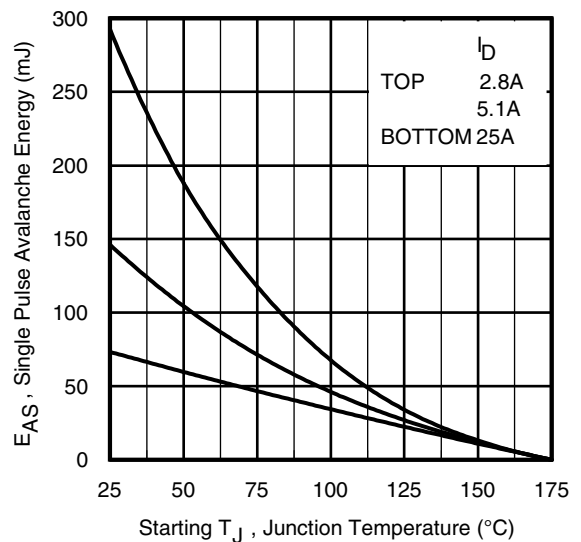


Fig 12. Maximum Avalanche Energy vs. Drain Current

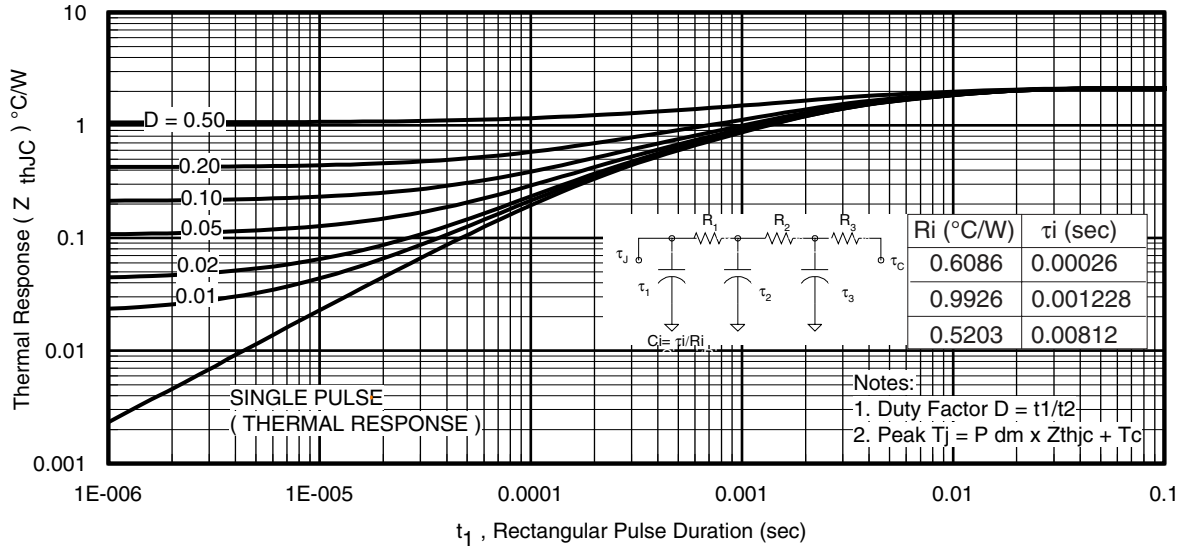


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

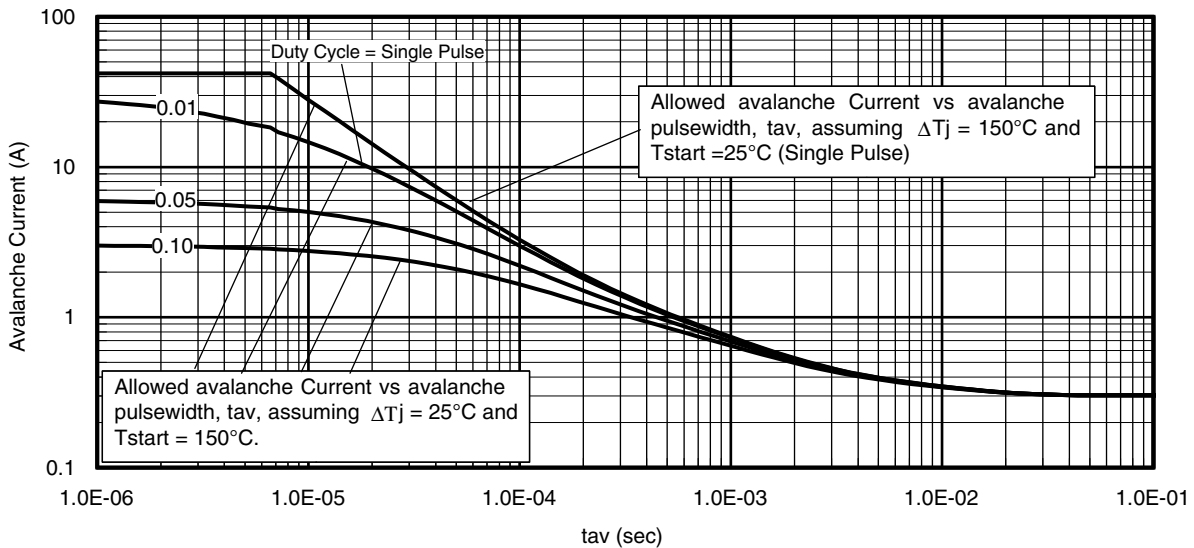
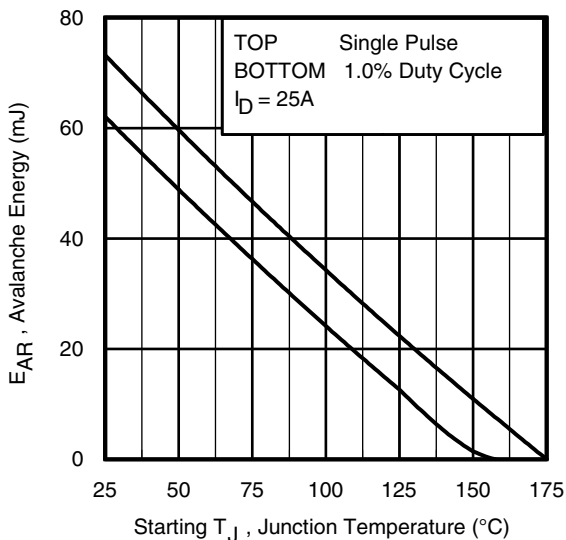


Fig 14. Typical Avalanche Current vs. Pulsewidth



**Notes on Repetitive Avalanche Curves, Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

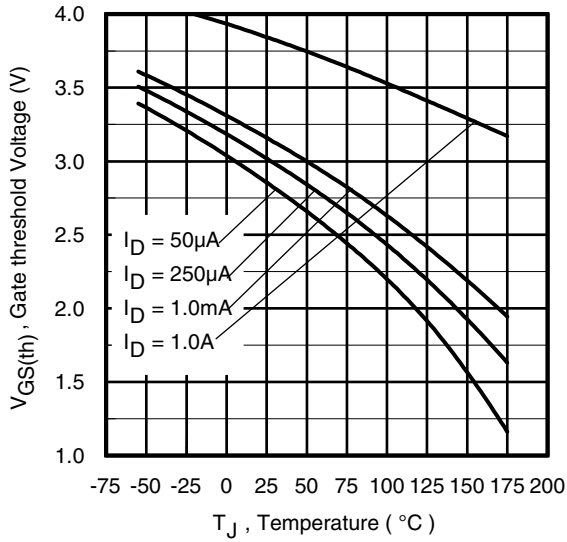


Fig 16. Threshold Voltage vs. Temperature

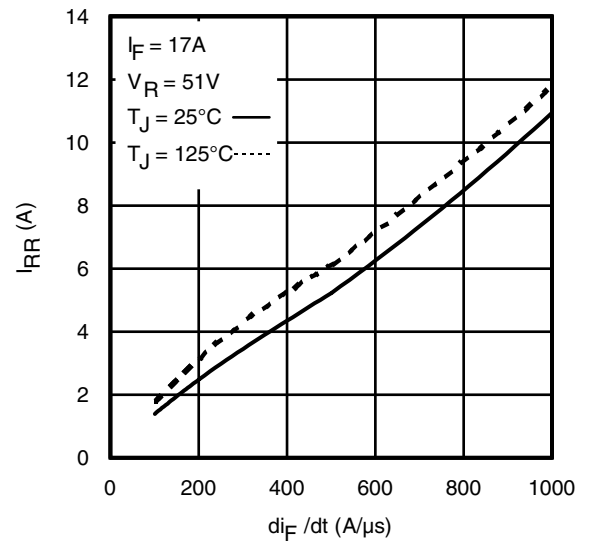


Fig. 17 - Typical Recovery Current vs.  $di/dt$

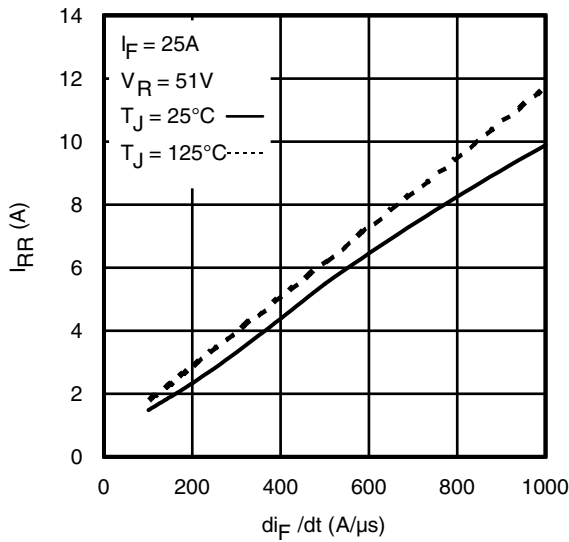


Fig. 18 - Typical Recovery Current vs.  $di/dt$

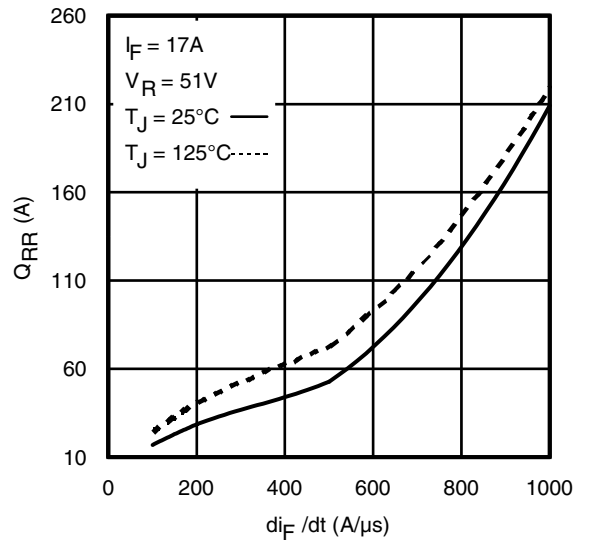


Fig. 19 - Typical Stored Charge vs.  $di/dt$

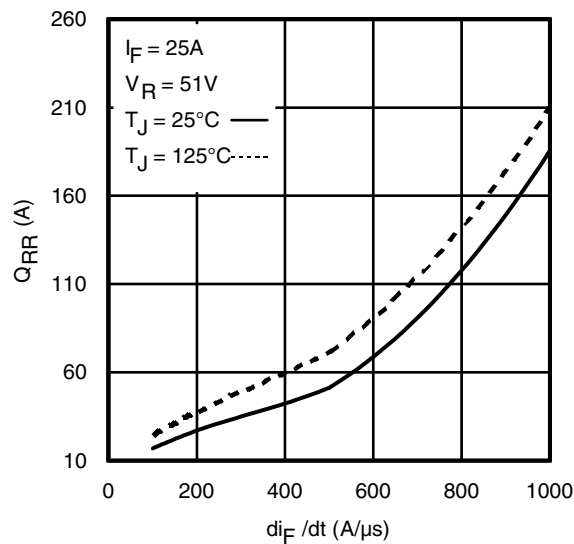
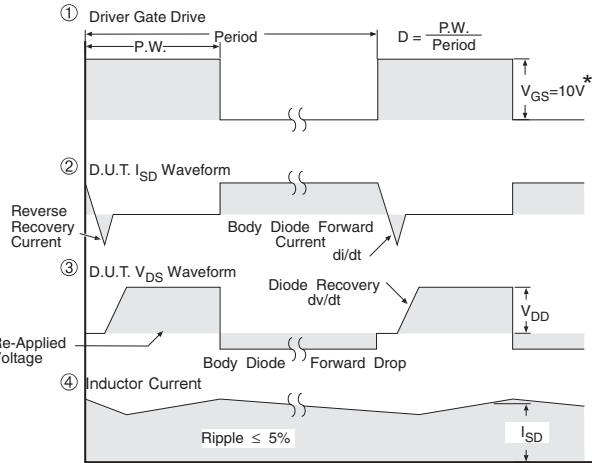
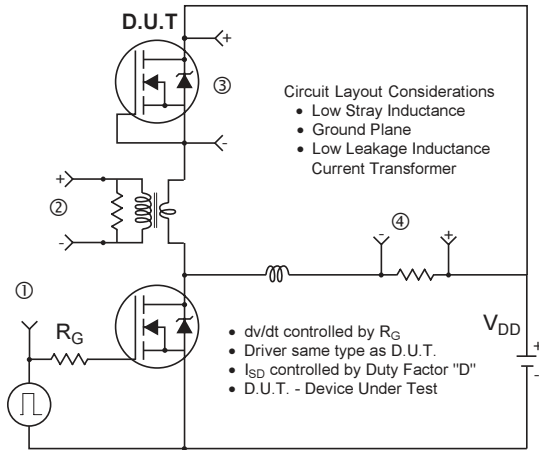
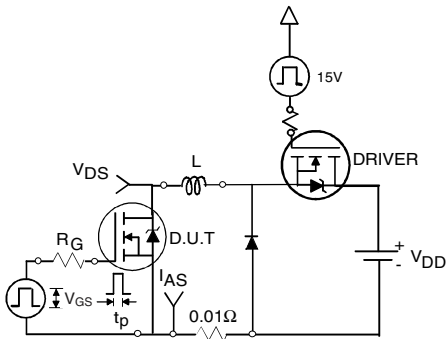


Fig. 20 - Typical Stored Charge vs.  $di/dt$

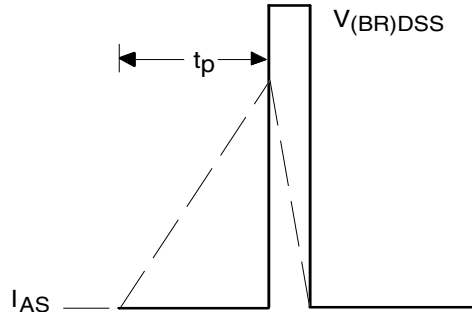


\*  $V_{GS} = 5V$  for Logic Level Devices

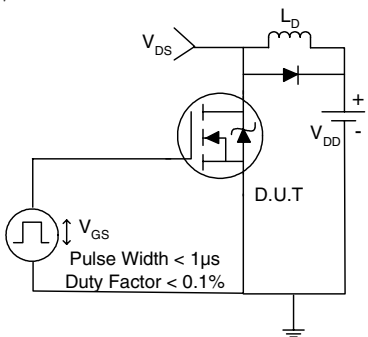
**Fig 20. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



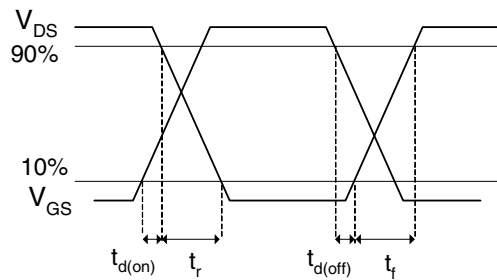
**Fig 21a. Unclamped Inductive Test Circuit**



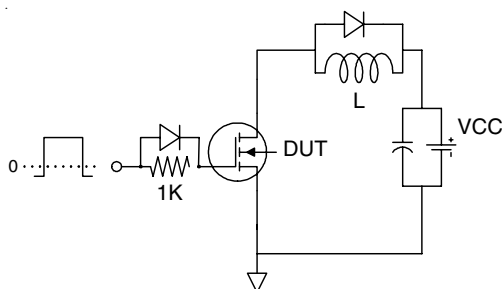
**Fig 21b. Unclamped Inductive Waveforms**



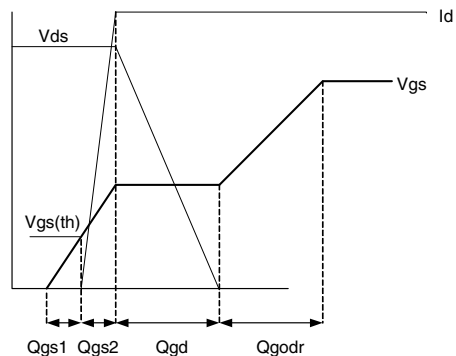
**Fig 22a. Switching Time Test Circuit**



**Fig 22b. Switching Time Waveforms**



**Fig 23a. Gate Charge Test Circuit**

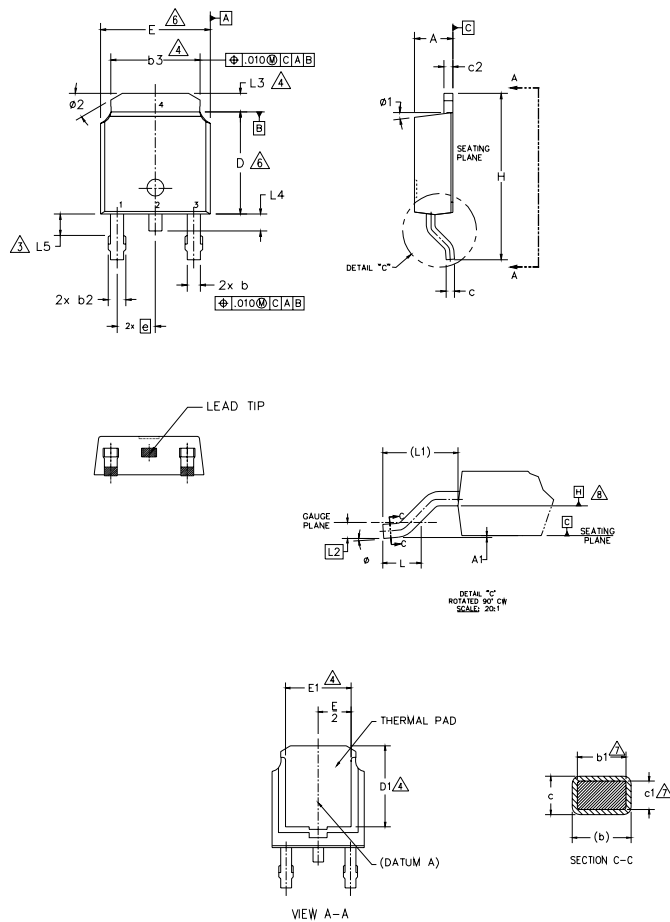


**Fig 23b. Gate Charge Waveform**

# IRFR/U3806PbF

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- △ LEAD DIMENSION UNCONTROLLED IN L5.
- △ DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- △ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- △ DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- △ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	7
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	4
b1	0.65	0.79	.025	.031	
b2	0.76	1.14	.030	.045	7
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	6
c1	0.41	0.56	.016	.022	
c2	0.46	0.89	.018	.035	4
D	5.97	6.22	.235	.245	
D1	5.21	-	.205	-	6
E	6.35	6.73	.250	.265	
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	LEAD ASSIGNMENTS
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		HEXFET
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	IGBT & CoPAK
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
φ	0"	10"	0"	10"	
φ1	0"	15"	0"	15"	1.- GATE 2.- DRAIN 3.- SOURCE 4.- DRAIN
φ2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

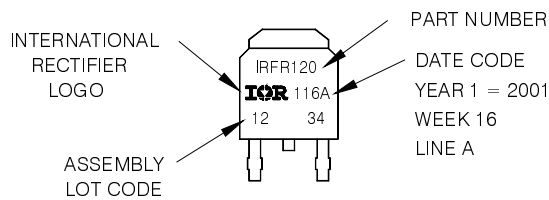
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 2001  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"

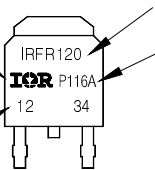
"P̄" in assembly line position indicates  
"Lead-Free" qualification to the consumer-level



OR

INTERNATIONAL  
RECTIFIER  
LOGO

ASSEMBLY  
LOT CODE



PART NUMBER

DATE CODE  
P = DESIGNATES LEAD-FREE  
PRODUCT (OPTIONAL)

P̄ = DESIGNATES LEAD-FREE  
PRODUCT QUALIFIED TO THE  
CONSUMER LEVEL (OPTIONAL)

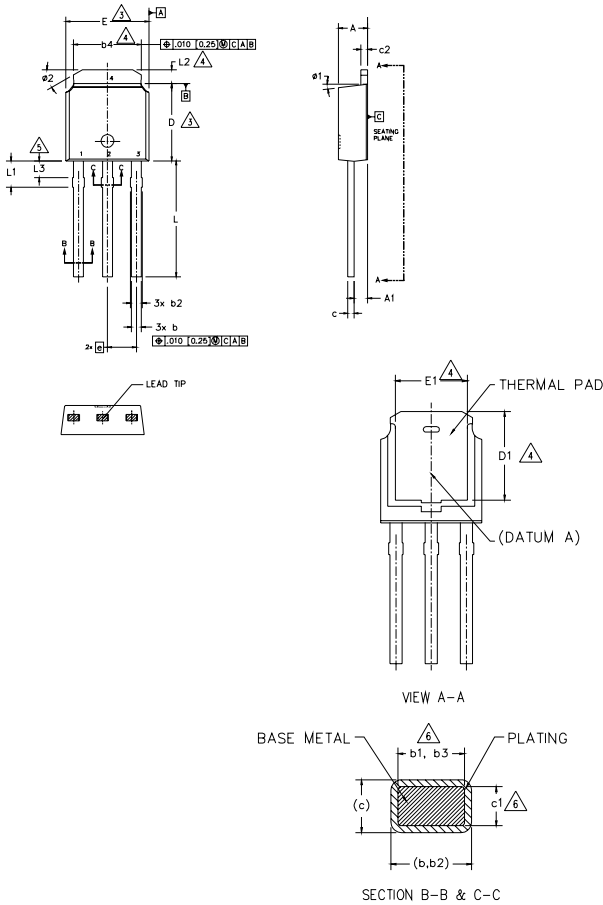
YEAR 1 = 2001  
WEEK 16  
A = ASSEMBLY SITE CODE

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



# I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- △ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- △ THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- △ LEAD DIMENSION UNCONTROLLED IN L3.
- △ DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
- 8.- CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	1.14	1.52	.045	.060	5
Ø1	0"	15"	0"	15"	
Ø2	25"	35"	25"	35"	

LEAD ASSIGNMENTS

HEXFET

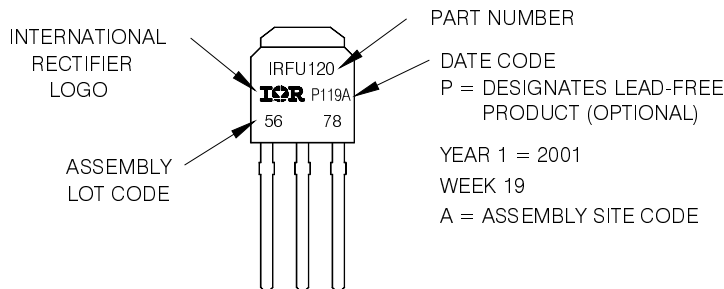
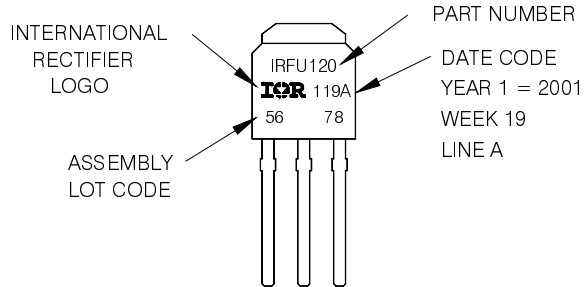
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 2001  
IN THE ASSEMBLY LINE 'A'

Note: "P" in assembly line position  
indicates Lead-Free"

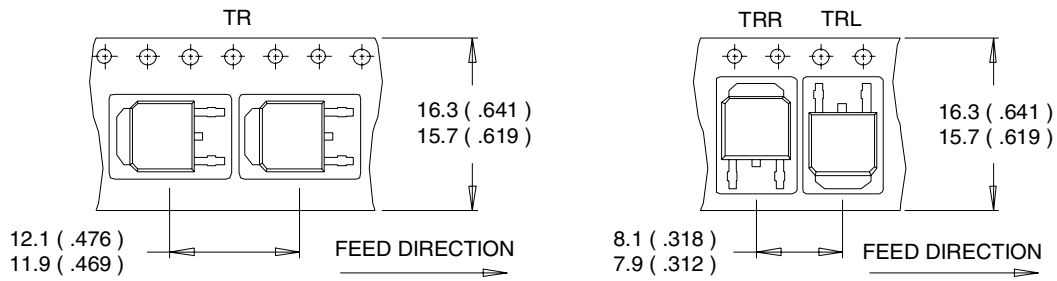
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

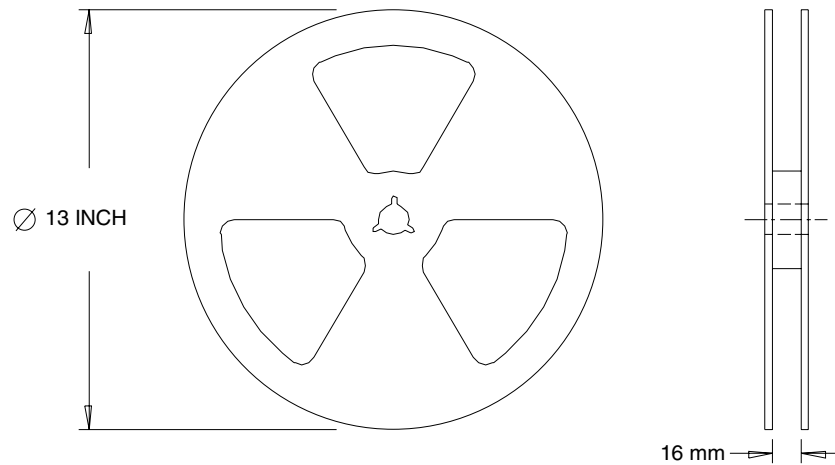
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

**Note:** For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.

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