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S6E2DF Series

32-bit ARM® Cortex®-M4F FM4 Microcontroller

Devices in the S6E2DF Series are highly integrated 32-bit microcontrollers with high performance and competitive cost. This series is based on the ARM Cortex-M4F Processor with on-chip Flash memory and SRAM. The series has peripheral functions such as graphics engine, display controller, motor control timers, ADCs, and Communication Interfaces (USB, UART, CSIO, I²C, LIN). The products that are described in this data sheet are TYPE4-M4 category products. See the FM4 Family Peripheral Manual Main Part (002-04856).

Features

32-bit ARM Cortex-M4F Core

- Processor version: r0p1
- Up to 160 MHz frequency operation
- Built-in FPU
- Supports DSP instructions
- Memory Protection Unit (MPU): improves the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit system timer (Sys Tick): System timer for OS task management

On-Chip Memories

- Flash memory

This series has on-chip flash memory with these features:

  - 384 Kbytes
  - Built-in Flash Accelerator System with 16 Kbytes trace buffer memory
  - Security function for code protection
  - Notes:
    - The read access to flash memory can be achieved without wait-cycle up to operation frequency of 72 MHz.
    - Even at the operation frequency more than 72 MHz, an equivalent access to flash memory can be obtained by Flash Accelerator System.

- SRAM

This is composed of two independent SRAMs (SRAM0 and SRAM2). SRAM0 is connected to I-code bus and D-code bus of Cortex-M4F core. SRAM2 is connected to the system bus of Cortex-M4F core.

  - SRAM0: 32 Kbytes
  - SRAM2: 4 Kbytes

- VRAM

This series is equipped with a SRAM for GDC.

  - Max 512 Kbytes

- VFLASH

S6E2DF5GJA is equipped with a Flash for GDC.

  - 2 Mbytes

External Bus Interface

- Supports SRAM, NOR, NAND Flash and SDRAM devices
- Up to two chip selects CS0 and CS8 (CS8 is only for SDRAM)
- 8-/16-bit data width
- Up to 25-bit address bit
- Maximum area size : Up to 256 Mbytes
- Supports address/data multiplexing
- Supports external RDY function
- Supports the scramble function
  - Possible to set the validity/invalidity of the scramble function for the external areas 0x6000_0000 to 0x7FFF_FFFF in 4 Mbytes units.
  - Possible to set two kinds of the scramble key.
  - Note: It is necessary to prepare the dedicated software library to use the scramble function.

USB Interface (One channel)

A USB interface is composed of device and host.

- USB device
  - USB2.0 Full-Speed supported
  - Max 6 EndPoint supported
    - EndPoint 0 is for control transfer
    - EndPoint 1, 2 can be selected for bulk-transfer, interrupt-transfer or isochronous-transfer
    - EndPoint 3 to 5 can select bulk-transfer or interrupt-transfer
  - EndPoint 1 to 5 comprise the double buffer
  - The size of each endpoint is as follows.
    - Endpoint 0, 2 to 5: 64 bytes
    - EndPoint 1: 256 bytes
- USB host
  - USB2.0 Full-Speed / Low-Speed supported
  - Bulk-transfer, interrupt-transfer and isochronous-transfer support
  - USB device connected/disconnected automatically detect
  - In/out token handshake packet automatically accepted
  - Max 256-byte packet-length supported
  - Wake-up function supported

Multi-function Serial Interface (Max eight channels)

- 64 bytes with FIFO (the FIFO step numbers vary depending on the settings of the communication mode or bit length.)
- Operation mode is selectable from the following for each channel.
  - UART
  - CSIO
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch.6 and ch.7 only)
  - Supports High-speed SPI (ch.6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/Slave mode supported
  - LIN break field generation (can change to 13 to 16-bit length)
  - LIN break delimiter generation (can change to 1 to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I^2C
  - Standard mode (Max 100 kbps) / Fast mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.4=ch.A) supported

DMA Controller (Eight channels)

The DMA controller has an independent bus for the CPU, so the CPU and the DMA controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or requested from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System Data Transfer Controller) (128 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can directly access the memory/peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

A/D Converter (Max 24 channels)

- 12-bit A/D Converter
  - Successive Approximation type
  - Built-in 2 units
  - Conversion time: 1.0 µs @ 3.3 V
  - Priority conversion available (priority at two levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: four steps)

Base Timer (Max eight channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set to which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port relocate function
- Up to 98 general-purpose I/O ports @ 120-pin package
- Some I/O pins are 5V tolerant.
  See "4. Pin Descriptions" and "5. I/O Circuit Type" for the corresponding pins.

Multi-Function Timer (One unit)

The multi-function timer is composed of the following blocks.

Minimum resolution : 6.25 ns

- 16-bit free-run timer × 3ch.
- Input capture × 4ch.
- Output compare × 6ch.
- A/D activation compare × 6ch.
- Waveform generator × 3ch.
- 16-bit PPG timer × 3ch.

The following functions can be used to achieve motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D converter activate function
- DTIF (motor emergency stop) interrupt function

Real-Time Clock (RTC)

The real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC) (One channel)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The dual timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The watch counter is used for wake up from the low-power consumption mode. It is possible to select the main clock, sub clock, built-in High-speed CR clock or built-in Low-speed CR clock as the clock source.

Interval timer: up to 64 s (Max) @ Sub Clock: 32.768 kHz

External Interrupt Controller Unit

- External interrupt input pin: Max 16 pins
- Include one non-maskable interrupt (NMI)

Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a hardware watchdog and a software watchdog.

The hardware watchdog timer is clocked by low-speed internal CR oscillator. Therefore, the hardware watchdog is active in any power saving mode except RTC mode and stop mode.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

PRGCRC (Programmable Cyclic Redundancy Check) Accelerator

The CRC accelerator helps verify data transmission or storage integrity.

CCITT CRC16, IEEE-802.3 CRC32 and a generating polynominal are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7
- Generating polynominal

SD Card Interface

It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

I^2S Interface (TX x two channels, RX x two channels)

- Support three transfer protocols
  - I^2S
  - Left Justified
  - DSP mode
- Master/Slave Mode selectable
- RX only, TX only or TX and RX simultaneous operation selectable
- Word length is programmable from 7 bits to 32 bits
- RX/TX FIFO integrated (RX: 66 words x 32 bits, TX: 66 words x 32 bits)
- DMA, interrupts, or polling based data transfer supported

GDC Unit

- Controller for external graphics display
- Accelerator for 2D block image transfer (blit) operations
- Embedded SRAM video memory
- High-Speed Quad SPI (Serial Peripheral Interface for external memory extensions)
- SDRAM interface for external memory extensions
- HBI (Hyper Bus Interface) interface for external memory extensions
- Maximum core system clock frequency : 160 MHz

Clock and Reset

- Clocks

Five clock sources (two external oscillators, two internal CR oscillator, and Main PLL) that are dynamically selectable.

  - Main clock: 4 MHz to 20 MHz
  - Sub Clock : 32.768 kHz
  - High-speed internal CR Clock: 4 MHz
  - Low-speed internal CR Clock: 100 kHz
  - Main PLL Clock

- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timers reset
  - Low voltage detector reset
  - Clock supervisor reset

Clock Super Visor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Six low-power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby Stop (selectable from with/without RAM retention)

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32 kHz oscillation circuit
- Power-on circuit
- Back up register : 32 bytes
- Port circuit

Debug

- Serial Wire Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

- Two Power Supplies
  - Power supply:

    VCC= 2.7 V to 3.6 V (when USB or GDC unit is not used)

    = 3.0 V to 3.6 V (when USB or GDC unit is used)
  - Power supply for VBAT:

    VBAT = 1.65 V to 3.6 V

Table of Contents

1. Product Lineup

Memory Size

Product Name		S6E2DF5G0A S6E2DF5J0A	S6E2DF5GJA
On-chip Flash memory		384 Kbytes	
On-chip SRAM	SRAM	36 Kbytes	
	SRAM0	32 Kbytes	
	SRAM2	4 Kbytes	
VRAM for GDC		512 Kbytes	
VFLASH for GDC		-	2 Mbytes

Function

Product Name			S6E2DF5G0A	S6E2DF5J0A	S6E2DF5GJA
Pin count			120/161	176	120
CPU			Cortex-M4F, MPU, NVIC 128ch.		
	Freq.		160 MHz		
Power supply voltage range			2.7 V to 3.6 V		
USB2.0 (Device/Host)			1ch.		
DMAC			8ch.		
DSTC			128ch.		
GDC unit	Graphics・Display controller		1 unit		
	High-Speed Quad SPI		1ch.		(VFLASH only)
	Hyper Bus Interface		1 unit		-
	SDRAM-IF		-	1ch.	-
External Bus Interface			Addr:25-bit (Max), Data: 8-/16-bit, CS:2 (Max) SRAM, NOR Flash, NAND Flash, SDRAM		
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			8ch. (Max)		
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)		
MF Timer	A/D activation compare	6ch.	1 unit		
	Input capture	4ch.			
	Free-run timer	3ch.			
	Output compare	6ch.			
	Waveform generator	3ch.			
	PPG	3ch.			
SD Card Interface			1 unit		
I^{2}S			2 units		
QPRC			1ch.		
Dual Timer			1 unit		
Real-Time Clock			1 unit		
Watch Counter			1 unit		
CRC Accelerator			Yes(Fixed, Programmable)		
Watchdog Timer			1ch. (SW) + 1ch. (HW)		
External Interrupts			16 pins (Max)+ NMI × 1		
I/O ports			98 pins (Max)	154 pins (Max)	90 pins (Max)
12-bit A/D converter			24ch. (2 units)		
CSV (Clock Super Visor)			Yes		
LVD (Low-Voltage Detector)			2ch.		
Built-in CR		High-speed	4 MHz		
		Low-speed	100 kHz		
Debug Function			SWJ-DP/ETM		
Unique ID			Yes		

Notes:
- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See 12.4.3 Built-in CR Oscillation Characteristics for the accuracy of the built-in CR.*

2. Packages

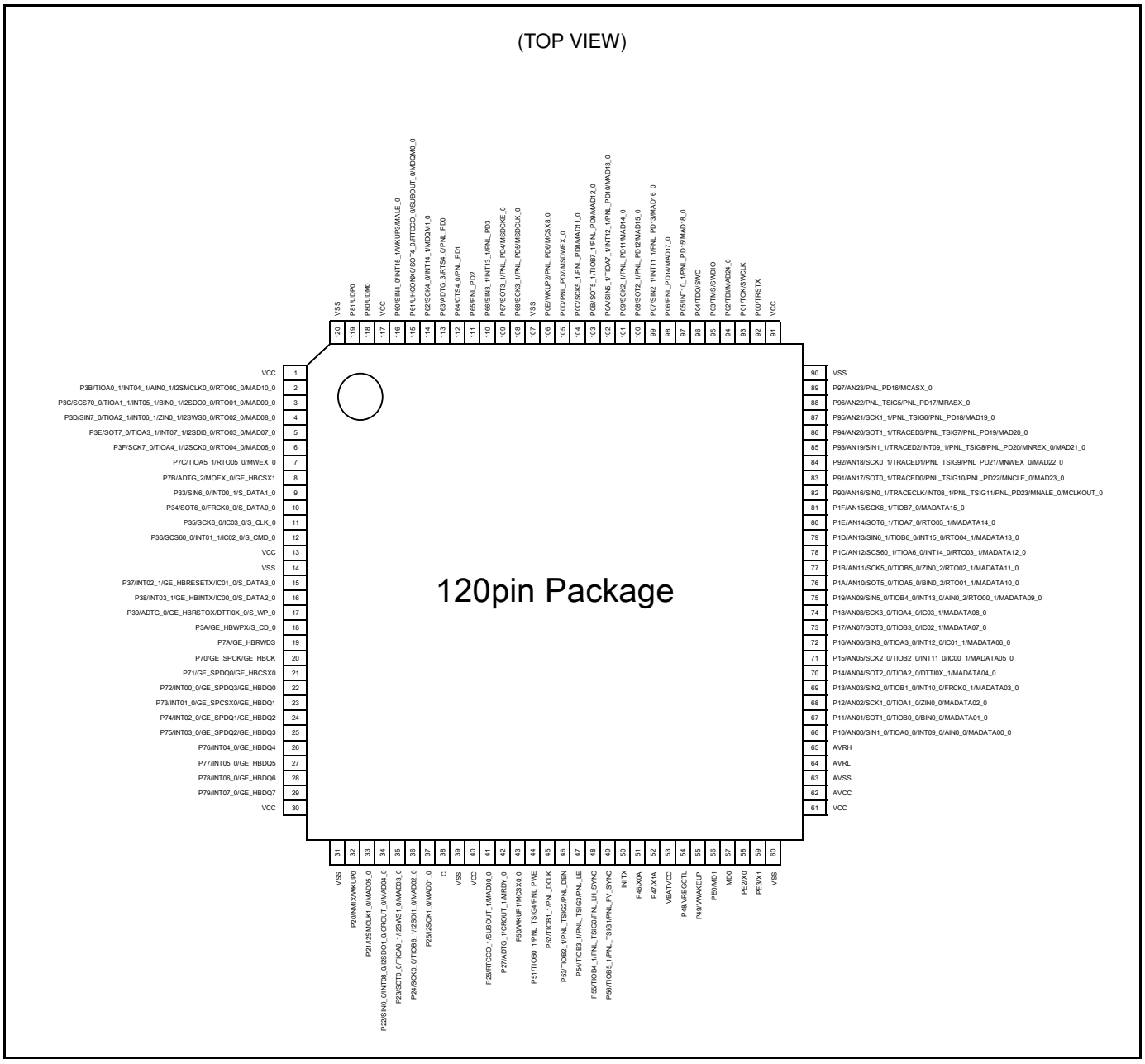
Package \ Product Name	S6E2DF5G0A	S6E2DF5J0A	S6E2DF5GJA
LQFP: LQM120 (0.5 mm pitch)	❍	-	❍
LQFP: LQP176 (0.5 mm pitch)	-	❍	-
FBGA: FDJ161 (0.5 mm pitch)	❍	-	-
Ex-LQFP(TEQFP): LEM120 (0.5 mm pitch)	❍		

❍: Supported

Note:
- *See 14. Package Dimensions for detailed information on each package.*

3. Pin Assignment

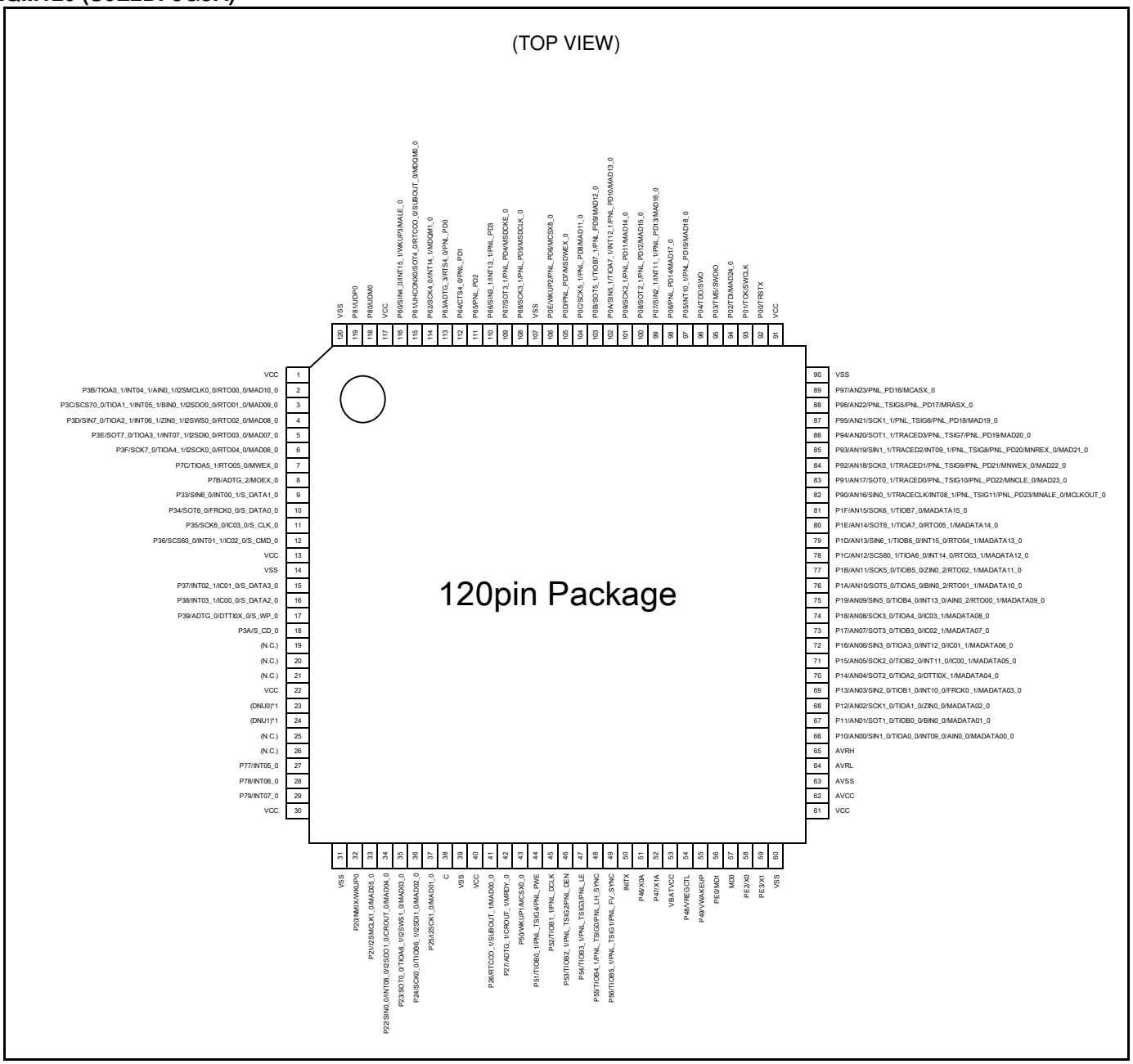
LQM120 / LEM120



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*
  Use the extended port function register (EPFR) to select the pin.

LQM120 (S6E2DF5GJA)



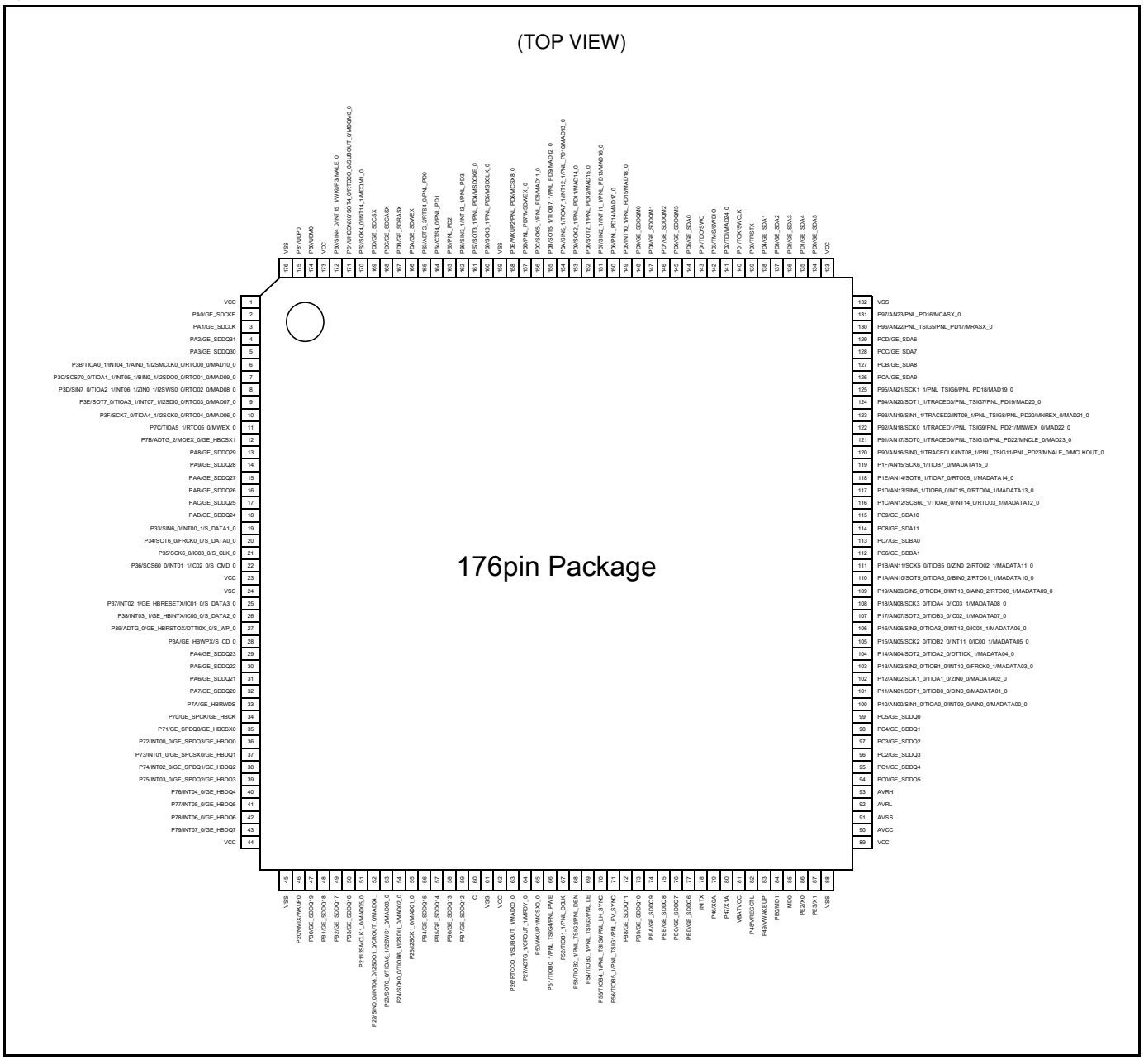
*1: The DNU0 / 1 (23 pin / 24 pin), please pull up and short-circuit on the board.
For more information, please refer to the 7.Handling Devices.

(N.C.): Do not connect anything.

Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*
  Use the extended port function register (EPFR) to select the pin.

LQP176



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*
  Use the extended port function register (EPFR) to select the pin.

FDJ161

(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSS	UDP0	UDM0	VCC	VSS	P66	VSS	P0C	P09	VSS	TCK	VCC	VSS
B	VSS	P60	P61	P62	P64	P67	P0E	P0B	P08	TDO	TMS	TRSTX	VSS
C	VCC	P3C	P3B	P63	P65	P68	P0D	P0A	P07	P05	TDI	P96	P97
D	P3F	P3E	P3D	P7C	VSS	VSS	VSS	VSS	P06	P92	P93	P94	P95
E	P35	P34	P33	P7B	VSS	VSS	VSS	VSS	VSS	P1E	P1F	P90	P91
F	P39	P38	P37	P36	VSS	VSS			VSS	P1A	P1B	P1C	P1D
G	VCC	P7A	P3A	VSS	VSS				VSS	P16	P17	P18	P19
H	VSS	P72	P73	VSS	VSS				VSS	P12	P13	P14	P15
J	P70	P74	P75	VSS	VSS	VSS	VSS	VSS	VSS	VSS	P11	AVRH	AVRL
K	P71	P76	P77	VSS	P24	VSS	P50	P52	P54	VSS	P10	AVSS	AVCC
L	VCC	P78	P79	P22	P25	VSS	P51	P53	P55	P56	P48	P49	VCC
M	VSS	P20	P21	P23	P26	VSS	VSS	INITX	VBAT	VSS	MD0	MD1	VSS
N	VSS	C	VSS	VCC	P27	VSS	X0A	VSS	X1A	VSS	X0	X1	VSS

Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.*
  Use the extended port function register (EPFR) to select the pin.

4. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
1	1	1	C1	VCC	—	—
2	—	—	—	PA0	K	I
				GE_SDCKE		
3	—	—	—	PA1	K	I
				GE_SDCLK		
4	—	—	—	PA2	L	I
				GE_SDDQ31		
5	—	—	—	PA3	L	I
				GE_SDDQ30		
6	2	2	C3	P3B	G	K
				TIOA0_1		
				INT04_1		
				AIN0_1		
				I2SMCLK0_0		
				RTO00_0 (PPG00_0)		
				MAD10_0		
7	3	3	C2	P3C	G	K
				SCS70_0		
				TIOA1_1		
				INT05_1		
				BIN0_1		
				I2SDO0_0		
				RTO01_0 (PPG00_0)		
				MAD09_0		
8	4	4	D3	P3D	G	K
				SIN7_0		
				TIOA2_1		
				INT06_1		
				ZIN0_1		
				I2SWS0_0		
				RTO02_0 (PPG02_0)		
				MAD08_0		

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
9	5	5	D2	P3E SOT7_0 (SDA7_0) TIOA3_1 INT07_1 I2SDI0_0 RTO03_0 (PPG02_0) MAD07_0	G	K
10	6	6	D1	P3F SCK7_0 (SCL7_0) TIOA4_1 I2SCK0_0 RTO04_0 (PPG04_0) MAD06_0	G	I
11	7	7	D4	P7C TIOA5_1 RTO05_0 (PPG04_0) MWEX_0	G	I
12	8	–	E4	P7B ADTG_2 GE_HBCSX1 MOEX_0	K	I
–	–	8	–	P7B ADTG_2 MOEX_0	K	I
13	–	–	–	PA8 GE_SDDQ29	L	I
14	–	–	–	PA9 GE_SDDQ28	L	I
15	–	–	–	PAA GE_SDDQ27	L	I
16	–	–	–	PAB GE_SDDQ26	L	I
17	–	–	–	PAC GE_SDDQ25	L	I
18	–	–	–	PAD GE_SDDQ24	L	I

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
19	9	9	E3	P33 SIN6_0 INT00_1 S_DATA1_0	D	K
20	10	10	E2	P34 SOT6_0 (SDA6_0) FRCK0_0 S_DATA0_0	D	I
21	11	11	E1	P35 SCK6_0 (SCL6_0) IC03_0 S_CLK_0	D	I
22	12	12	F4	P36 SCS60_0 INT01_1 IC02_0 S_CMD_0	D	K
23	13	13	G1	VCC	—	—
24	14	14	H1	VSS	—	—
25	15	—	F3	P37 GE_HBRESETX INT02_1 IC01_0 S_DATA3_0	D	K
—	—	15	—	P37 INT02_1 IC01_0 S_DATA3_0	D	K
26	16	—	F2	P38 GE_HBINTX INT03_1 IC00_0 S_DATA2_0	D	K
—	—	16	—	P38 INT03_1 IC00_0 S_DATA2_0	D	K

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
27	17	—	F1	P39 ADTG_0 GE_HBRSTOX DTTI0X_0 S_WP_0	E	I
—	—	17	—	P39 ADTG_0 DTTI0X_0 S_WP_0	E	I
28	18	—	G3	P3A GE_HBWPX S_CD_0	E	I
—	—	18	—	P3A S_CD_0	E	I
29	—	—	—	PA4 GE_SDDQ23	L	I
30	—	—	—	PA5 GE_SDDQ22	L	I
31	—	—	—	PA6 GE_SDDQ21	L	I
32	—	—	—	PA7 GE_SDDQ20	L	I
33	19	—	G2	P7A GE_HBRWDS	K	I
—	—	19	—	(N.C.)	—	—
34	20	—	J1	P70 GE_SPCK GE_HBCK	K	I
—	—	20	—	(N.C.)	—	—
35	21	—	K1	P71 GE_SPDQ0 GE_HBCSX0	K	I
—	—	21	—	(N.C.)	—	—
36	22	—	H2	P72 GE_SPDQ3 GE_HBDQ0 INT00_0	K	K
—	—	22	—	VCC	—	—
37	23	—	H3	P73 GE_SPCSX0 GE_HBDQ1 INT01_0	K	K
—	—	23	—	(DNU0)	—	—

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
38	24	—	J2	P74 GE_SPDQ1 GE_HBDQ2 INT02_0	K	K
—	—	24	—	(DNU1)	—	—
39	25	—	J3	P75 GE_SPDQ2 GE_HBDQ3 INT03_0	K	K
—	—	25	—	(N.C.)	—	—
40	26	—	K2	P76 GE_HBDQ4 INT04_0	K	K
—	—	26	—	(N.C.)	—	—
41	27	—	K3	P77 GE_HBDQ5 INT05_0	K	K
—	—	27	—	P77 INT05_0	K	K
42	28	—	L2	P78 GE_HBDQ6 INT06_0	K	K
—	—	28	—	P78 INT06_0	K	K
43	29	—	L3	P79 GE_HBDQ7 INT07_0	K	K
—	—	29	—	P79 INT07_0	K	K
44	30	30	L1	VCC	—	—
45	31	31	M1	VSS	—	—
46	32	32	M2	P20 NMIX WKUP0	I	F
47	—	—	—	PB0 GE_SDDQ19	L	I
48	—	—	—	PB1 GE_SDDQ18	L	I
49	—	—	—	PB2 GE_SDDQ17	L	I
50	—	—	—	PB3 GE_SDDQ16	L	I

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
51	33	33	M3	P21 I2SMCLK1_0 MAD05_0	E	I
52	34	34	L4	P22 CROUT_0 SIN0_0 INT08_0 I2SDO1_0 MAD04_0	E	K
53	35	35	M4	P23 SOT0_0 (SDA0_0) TIOA6_1 I2SWS1_0 MAD03_0	E	I
54	36	36	K5	P24 SCK0_0 (SCL0_0) TIOB6_1 I2SDI1_0 MAD02_0	E	I
55	37	37	L5	P25 I2SCK1_0 MAD01_0	E	I
56	—	—	—	PB4 GE_SDDQ15	L	I
57	—	—	—	PB5 GE_SDDQ14	L	I
58	—	—	—	PB6 GE_SDDQ13	L	I
59	—	—	—	PB7 GE_SDDQ12	L	I
60	38	38	N2	C	—	—
61	39	39	N3	VSS	—	—
62	40	40	N4	VCC	—	—
63	41	41	M5	P26 RTCCO_1 SUBOUT_1 MAD00_0	E	I
64	42	42	N5	P27 ADTG_1 CROUT_1 MRDY_0	E	I

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
65	43	43	K7	P50 WKUP1 MCSX0_0	D	P
66	44	44	L7	P51 TIOB0_1 PNL_PWE PNL_TSIG4	E	I
67	45	45	K8	P52 TIOB1_1 PNL_DCLK	D	I
68	46	46	L8	P53 TIOB2_1 PNL_DEN PNL_TSIG2	E	I
69	47	47	K9	P54 TIOB3_1 PNL_LE PNL_TSIG3	E	I
70	48	48	L9	P55 TIOB4_1 PNL_LH_SYNC PNL_TSIG0	E	I
71	49	49	L10	P56 TIOB5_1 PNL_FV_SYNC PNL_TSIG1	E	I
72	–	–	–	PB8 GE_SDDQ11	L	I
73	–	–	–	PB9 GE_SDDQ10	L	I
74	–	–	–	PBA GE_SDDQ9	L	I
75	–	–	–	PBB GE_SDDQ8	L	I
76	–	–	–	PBC GE_SDDQ7	L	I
77	–	–	–	PBD GE_SDDQ6	L	I
78	50	50	M8	INITX	B	C
79	51	51	N7	P46 X0A	P	S
80	52	52	N9	P47 X1A	Q	T

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
81	53	53	M9	VBAT	—	—
82	54	54	L11	P48 VREGCTL	O	U
83	55	55	L12	P49 VWAKEUP	O	U
84	56	56	M12	PE0 MD1	C	E
85	57	57	M11	MD0	J	D
86	58	58	N11	PE2 X0	A	A
87	59	59	N12	PE3 X1	A	B
88	60	60	M13	VSS	—	—
89	61	61	L13	VCC	—	—
90	62	62	K13	AVCC	—	—
91	63	63	K12	AVSS	—	—
92	64	64	J13	AVRL	—	—
93	65	65	J12	AVRH	—	—
94	—	—	—	PC0 GE_SDDQ5	L	I
95	—	—	—	PC1 GE_SDDQ4	L	I
96	—	—	—	PC2 GE_SDDQ3	L	I
97	—	—	—	PC3 GE_SDDQ2	L	I
98	—	—	—	PC4 GE_SDDQ1	L	I
99	—	—	—	PC5 GE_SDDQ0	L	I
100	66	66	K11	P10 AN00 SIN1_0 TIOA0_0 INT09_0 AIN0_0 MADATA00_0	F	M

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
101	67	67	J11	P11 AN01 SOT1_0 (SDA1_0) TIOB0_0 BIN0_0 MADATA01_0	F	L
102	68	68	H10	P12 AN02 SCK1_0 (SCL1_0) TIOA1_0 ZIN0_0 MADATA02_0	F	L
103	69	69	H11	P13 AN03 SIN2_0 TIOB1_0 INT10_0 FRCK0_1 MADATA03_0	F	M
104	70	70	H12	P14 AN04 SOT2_0 (SDA2_0) TIOA2_0 DTTI0X_1 MADATA04_0	F	L
105	71	71	H13	P15 AN05 SCK2_0 (SCL2_0) TIOB2_0 INT11_0 IC00_1 MADATA05_0	F	M
106	72	72	G10	P16 AN06 SIN3_0 TIOA3_0 INT12_0 IC01_1 MADATA06_0	F	M

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
107	73	73	G11	P17 AN07 SOT3_0 (SDA3_0) TIOB3_0 IC02_1 MADATA07_0	F	L
108	74	74	G12	P18 AN08 SCK3_0 (SCL3_0) TIOA4_0 IC03_1 MADATA08_0	F	L
109	75	75	G13	P19 AN09 SIN5_0 TIOB4_0 INT13_0 AIN0_2 RTO00_1 (PPG00_1) MADATA09_0	F	M
110	76	76	F10	P1A AN10 SOT5_0 (SDA5_0) TIOA5_0 BIN0_2 RTO01_1 (PPG00_1) MADATA10_0	F	L
111	77	77	F11	P1B AN11 SCK5_0 (SCL5_0) TIOB5_0 ZIN0_2 RTO02_1 (PPG02_1) MADATA11_0	F	L
112	–	–	–	PC6 GE_SDBA1	K	I

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
113	—	—	—	PC7	K	I
				GE_SDBA0		
114	—	—	—	PC8	K	I
				GE_SDA11		
115	—	—	—	PC9	K	I
				GE_SDA10		
116	78	78	F12	P1C	F	M
				AN12		
				SCS60_1		
				TIOA6_0		
				INT14_0		
				RTO03_1 (PPG02_1)		
				MADATA12_0		
117	79	79	F13	P1D	F	M
				AN13		
				SIN6_1		
				TIOB6_0		
				INT15_0		
				RTO04_1 (PPG04_1)		
				MADATA13_0		
118	80	80	E10	P1E	F	L
				AN14		
				SOT6_1 (SDA6_1)		
				TIOA7_0		
				RTO05_1 (PPG04_1)		
				MADATA14_0		
119	81	81	E11	P1F	F	L
				AN15		
				SCK6_1 (SCL6_1)		
				TIOB7_0		
				MADATA15_0		

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
120	82	82	E12	P90 AN16 SIN0_1 INT08_1 PNL_PD23 PNL_TSIG11 MCLKOUT_0 MNALE_0 TRACECLK	F	O
121	83	83	E13	P91 AN17 SOT0_1 (SDA0_1) PNL_PD22 PNL_TSIG10 MAD23_0 MNCLE_0 TRACED0	F	N
122	84	84	D10	P92 AN18 SCK0_1 (SCL0_1) PNL_PD21 PNL_TSIG9 MAD22_0 MNWEX_0 TRACED1	F	N
123	85	85	D11	P93 AN19 SIN1_1 INT09_1 PNL_PD20 PNL_TSIG8 MAD21_0 MNREX_0 TRACED2	F	O
124	86	86	D12	P94 AN20 SOT1_1 (SDA1_1) PNL_PD19 PNL_TSIG7 MAD20_0 TRACED3	F	N

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
125	87	87	D13	P95 AN21 SCK1_1 (SCL1_1) PNL_PD18 PNL_TSIG6 MAD19_0	F	L
126	—	—	—	PCA GE_SDA9	K	I
127	—	—	—	PCB GE_SDA8	K	I
128	—	—	—	PCC GE_SDA7	K	I
129	—	—	—	PCD GE_SDA6	K	I
130	88	88	C12	P96 AN22 PNL_PD17 PNL_TSIG5 MRASX_0	F	L
131	89	89	C13	P97 AN23 PNL_PD16 MCASX_0	F	L
132	90	90	B13	VSS	—	—
133	91	91	A12	VCC	—	—
134	—	—	—	PD0 GE_SDA5	K	I
135	—	—	—	PD1 GE_SDA4	K	I
136	—	—	—	PD2 GE_SDA3	K	I
137	—	—	—	PD3 GE_SDA2	K	I
138	—	—	—	PD4 GE_SDA1	K	I
139	92	92	B12	P00 TRSTX	E	G
140	93	93	A11	P01 TCK SWCLK	E	G

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
141	94	94	C11	P02 TDI MAD24_0	E	H
142	95	95	B11	P03 TMS SWDIO	E	G
143	96	96	B10	P04 TDO SWO	E	G
144	–	–	–	PD5 GE_SDA0	K	I
145	–	–	–	PD6 GE_SDDQM3	K	I
146	–	–	–	PD7 GE_SDDQM2	K	I
147	–	–	–	PD8 GE_SDDQM1	K	I
148	–	–	–	PD9 GE_SDDQM0	K	I
149	97	97	C10	P05 INT10_1 PNL_PD15 MAD18_0	E	K
150	98	98	D9	P06 PNL_PD14 MAD17_0	E	I
151	99	99	C9	P07 SIN2_1 INT11_1 PNL_PD13 MAD16_0	E	K
152	100	100	B9	P08 SOT2_1 (SDA2_1) PNL_PD12 MAD15_0	E	I
153	101	101	A9	P09 SCK2_1 (SCL2_1) PNL_PD11 MAD14_0	E	I

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
154	102	102	C8	P0A SIN5_1 TIOA7_1 INT12_1 PNL_PD10 MAD13_0	E	K
155	103	103	B8	P0B SOT5_1 (SDA5_1) TIOB7_1 PNL_PD9 MAD12_0	E	I
156	104	104	A8	P0C SCK5_1 (SCL5_1) PNL_PD8 MAD11_0	E	I
157	105	105	C7	P0D PNL_PD7 MSDWEX_0	D	I
158	106	106	B7	P0E WKUP2 PNL_PD6 MCSX8_0	D	P
159	107	107	A7	VSS	—	—
160	108	108	C6	P68 SCK3_1 (SCL3_1) PNL_PD5 MSDCLK_0	D	I
161	109	109	B6	P67 SOT3_1 (SDA3_1) PNL_PD4 MSDCKE_0	D	I
162	110	110	A6	P66 SIN3_1 INT13_1 PNL_PD3	E	K
163	111	111	C5	P65 PNL_PD2	E	I
164	112	112	B5	P64 CTS4_0 PNL_PD1	E	I

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
165	113	113	C4	P63 ADTG_3 RTS4_0 PNL_PD0	E	I
166	—	—	—	PDA GE_SDWEX	K	I
167	—	—	—	PDB GE_SDRASX	K	I
168	—	—	—	PDC GE_SDCASX	K	I
169	—	—	—	PDD GE_SDCSX	K	I
170	114	114	B4	P62 SCK4_0 (SCL4_0) INT14_1 MDQM1_0	N	K
171	115	115	B3	P61 UHCONX0 RTCCO_0 SUBOUT_0 SOT4_0 (SDA4_0) MDQM0_0	N	I
172	116	116	B2	P60 WKUP3 SIN4_0 INT15_1 MALE_0	I	Q
173	117	117	A4	VCC	—	—
174	118	118	A3	P80 UDM0	H	R
175	119	119	A2	P81 UDP0	H	R
176	120	120	B1	VSS	—	—

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161			
–	–	–	A1, A5, A10, A13, D5, D6, D7, D8, E5, E6, E7, E8, E9, F5, F6, F9, G4, G5, G9, H4, H5, H9, J4, J5, J6, J7, J8, J9, J10, K4, K6, K10, L6, M6, M7, M10, N1, N6, N8, N10, N13	VSS	–	–

Signal Description

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
ADC	ADTG_0	A/D converter external trigger input pin	27	17	17	F1
	ADTG_1		64	42	42	N5
	ADTG_2		12	8	8	E4
	ADTG_3		165	113	113	C4
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	100	66	66	K11
	AN01		101	67	67	J11
	AN02		102	68	68	H10
	AN03		103	69	69	H11
	AN04		104	70	70	H12
	AN05		105	71	71	H13
	AN06		106	72	72	G10
	AN07		107	73	73	G11
	AN08		108	74	74	G12
	AN09		109	75	75	G13
	AN10		110	76	76	F10
	AN11		111	77	77	F11
	AN12		116	78	78	F12
	AN13		117	79	79	F13
	AN14		118	80	80	E10
	AN15		119	81	81	E11
	AN16		120	82	82	E12
	AN17		121	83	83	E13
	AN18		122	84	84	D10
	AN19		123	85	85	D11
	AN20		124	86	86	D12
	AN21		125	87	87	D13
	AN22		130	88	88	C12
	AN23		131	89	89	C13
Base Timer 0	TIOA0_0	Base Timer ch.0 TIOA Pin	100	66	66	K11
	TIOA0_1		6	2	2	C3
	TIOB0_0	Base Timer ch.0 TIOB Pin	101	67	67	J11
	TIOB0_1		66	44	44	L7
Base Timer 1	TIOA1_0	Base Timer ch.1 TIOA Pin	102	68	68	H10
	TIOA1_1		7	3	3	C2
	TIOB1_0	Base Timer ch.1 TIOB Pin	103	69	69	H11
	TIOB1_1		67	45	45	K8

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
Base Timer 2	TIOA2_0	Base Timer ch.2 TIOA Pin	104	70	70	H12
	TIOA2_1		8	4	4	D3
	TIOB2_0	Base Timer ch.2 TIOB Pin	105	71	71	H13
	TIOB2_1		68	46	46	L8
Base Timer 3	TIOA3_0	Base Timer ch.3 TIOA Pin	106	72	72	G10
	TIOA3_1		9	5	5	D2
	TIOB3_0	Base Timer ch.3 TIOB Pin	107	73	73	G11
	TIOB3_1		69	47	47	K9
Base Timer 4	TIOA4_0	Base Timer ch.4 TIOA Pin	108	74	74	G12
	TIOA4_1		10	6	6	D1
	TIOB4_0	Base Timer ch.4 TIOB Pin	109	75	75	G13
	TIOB4_1		70	48	48	L9
Base Timer 5	TIOA5_0	Base Timer ch.5 TIOA Pin	110	76	76	F10
	TIOA5_1		11	7	7	D4
	TIOB5_0	Base Timer ch.5 TIOB Pin	111	77	77	F11
	TIOB5_1		71	49	49	L10
Base Timer 6	TIOA6_0	Base Timer ch.6 TIOA Pin	116	78	78	F12
	TIOA6_1		53	35	35	M4
	TIOB6_0	Base Timer ch.6 TIOB Pin	117	79	79	F13
	TIOB6_1		54	36	36	K5
Base Timer 7	TIOA7_0	Base Timer ch.7 TIOA Pin	118	80	80	E10
	TIOA7_1		154	102	102	C8
	TIOB7_0	Base Timer ch.7 TIOB Pin	119	81	81	E11
	TIOB7_1		155	103	103	B8
Debugger	SWCLK	Serial wire debug interface clock input pin	140	93	93	A11
	SWDIO	Serial wire debug interface data input / output pin	142	95	95	B11
	SWO	Serial wire viewer output pin	143	96	96	B10
	TCK	JTAG test clock input pin	140	93	93	A11
	TDI	JTAG test data input pin	141	94	94	C11
	TDO	JTAG debug data output pin	143	96	96	B10
	TMS	JTAG test mode state output pin	142	95	95	B11
	TRACECLK	Trace CLK output pin of ETM	120	82	82	E12
	TRACED0	Trace data output pin of ETM	121	83	83	E13
	TRACED1		122	84	84	D10
	TRACED2		123	85	85	D11
	TRACED3		124	86	86	D12
	TRSTX	JTAG test reset Input pin	139	92	92	B12

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
External Bus	MAD00_0	External bus interface address bus	63	41	41	M5
	MAD01_0		55	37	37	L5
	MAD02_0		54	36	36	K5
	MAD03_0		53	35	35	M4
	MAD04_0		52	34	34	L4
	MAD05_0		51	33	33	M3
	MAD06_0		10	6	6	D1
	MAD07_0		9	5	5	D2
	MAD08_0		8	4	4	D3
	MAD09_0		7	3	3	C2
	MAD10_0		6	2	2	C3
	MAD11_0		156	104	104	A8
	MAD12_0		155	103	103	B8
	MAD13_0		154	102	102	C8
	MAD14_0		153	101	101	A9
	MAD15_0		152	100	100	B9
	MAD16_0		151	99	99	C9
	MAD17_0		150	98	98	D9
	MAD18_0		149	97	97	C10
	MAD19_0		125	87	87	D13
	MAD20_0		124	86	86	D12
	MAD21_0		123	85	85	D11
	MAD22_0		122	84	84	D10
	MAD23_0		121	83	83	E13
	MAD24_0		141	94	94	C11
	MCSX0_0	External bus interface chip select output pin	65	43	43	K7
	MCSX8_0		158	106	106	B7
	MADATA00_0	External bus interface data bus	100	66	66	K11
	MADATA01_0		101	67	67	J11
	MADATA02_0		102	68	68	H10
	MADATA03_0		103	69	69	H11
	MADATA04_0		104	70	70	H12
	MADATA05_0		105	71	71	H13
	MADATA06_0		106	72	72	G10
	MADATA07_0		107	73	73	G11
	MADATA08_0		108	74	74	G12
	MADATA09_0		109	75	75	G13
	MADATA10_0		110	76	76	F10
	MADATA11_0		111	77	77	F11
	MADATA12_0		116	78	78	F12
	MADATA13_0		117	79	79	F13
	MADATA14_0		118	80	80	E10
	MADATA15_0		119	81	81	E11

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
External Bus	MDQM0_0	External bus interface byte mask signal output pin	171	115	115	B3
	MDQM1_0		170	114	114	B4
	MALE_0	External bus interface Address Latch enable output signal for multiplex	172	116	116	B2
	MRDY_0	External bus interface external RDY input signal	64	42	42	N5
	MCLKOUT_0	External bus interface external clock output pin	120	82	82	E12
	MNALE_0	External bus interface ALE signal to control NAND Flash output pin	120	82	82	E12
	MNCLE_0	External bus interface CLE signal to control NAND Flash output pin	121	83	83	E13
	MNREX_0	External bus interface read enable signal to control NAND Flash output pin	123	85	85	D11
	MNWEX_0	External bus interface write enable signal to control NAND Flash output pin	122	84	84	D10
	MOEX_0	External bus interface read enable signal for SRAM	12	8	8	E4
	MWEX_0	External bus interface write enable signal for SRAM	11	7	7	D4
	MSDCLK_0	SDRAM interface SDRAM clock output pin	160	108	108	C6
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	161	109	109	B6
	MRASX_0	SDRAM interface SDRAM row active strobe pin	130	88	88	C12
	MCASX_0	SDRAM interface SDRAM column active strobe pin	131	89	89	C13
	MSDWEX_0	SDRAM interface SDRAM write enable pin	157	105	105	C7
External Interrupt	INT00_0	External interrupt request 00 input pin	36	22	-	H2
	INT00_1		19	9	9	E3
	INT01_0	External interrupt request 01 input pin	37	23	-	H3
	INT01_1		22	12	12	F4
	INT02_0	External interrupt request 02 input pin	38	24	-	J2
	INT02_1		25	15	15	F3
	INT03_0	External interrupt request 03 input pin	39	25	-	J3
	INT03_1		26	16	16	F2
	INT04_0	External interrupt request 04 input pin	40	26	-	K2
	INT04_1		6	2	2	C3
	INT05_0	External interrupt request 05 input pin	41	27	27	K3
	INT05_1		7	3	3	C2
	INT06_0	External interrupt request 06 input pin	42	28	28	L2
	INT06_1		8	4	4	D3
	INT07_0	External interrupt request 07 input pin	43	29	29	L3
	INT07_1		9	5	5	D2
	INT08_0	External interrupt request 08 input pin	52	34	34	L4
	INT08_1		120	82	82	E12
	INT09_0	External interrupt request 09 input pin	100	66	66	K11
	INT09_1		123	85	85	D11

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
External Interrupt	INT10_0	External interrupt request 10 input pin	103	69	69	H11
	INT10_1		149	97	97	C10
	INT11_0	External interrupt request 11 input pin	105	71	71	H13
	INT11_1		151	99	99	C9
	INT12_0	External interrupt request 12 input pin	106	72	72	G10
	INT12_1		154	102	102	C8
	INT13_0	External interrupt request 13 input pin	109	75	75	G13
	INT13_1		162	110	110	A6
	INT14_0	External interrupt request 14 input pin	116	78	78	F12
	INT14_1		170	114	114	B4
	INT15_0	External interrupt request 15 input pin	117	79	79	F13
	INT15_1		172	116	116	B2
	NMIX	Non-Maskable Interrupt input pin	46	32	32	M2
GPIO	P00	General-purpose I/O port 0	139	92	92	B12
	P01		140	93	93	A11
	P02		141	94	94	C11
	P03		142	95	95	B11
	P04		143	96	96	B10
	P05		149	97	97	C10
	P06		150	98	98	D9
	P07		151	99	99	C9
	P08		152	100	100	B9
	P09		153	101	101	A9
	P0A		154	102	102	C8
	P0B		155	103	103	B8
	P0C		156	104	104	A8
	P0D		157	105	105	C7
	P0E		158	106	106	B7
	P10	General-purpose I/O port 1	100	66	66	K11
	P11		101	67	67	J11
	P12		102	68	68	H10
	P13		103	69	69	H11
	P14		104	70	70	H12
	P15		105	71	71	H13
	P16		106	72	72	G10
	P17		107	73	73	G11
	P18		108	74	74	G12
	P19		109	75	75	G13
	P1A		110	76	76	F10
	P1B		111	77	77	F11
	P1C		116	78	78	F12
	P1D		117	79	79	F13
	P1E		118	80	80	E10
	P1F		119	81	81	E11

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
GPIO	P20	General-purpose I/O port 2	46	32	32	M2
	P21		51	33	33	M3
	P22		52	34	34	L4
	P23		53	35	35	M4
	P24		54	36	36	K5
	P25		55	37	37	L5
	P26		63	41	41	M5
	P27		64	42	42	N5
	P33	General-purpose I/O port 3	19	9	9	E3
	P34		20	10	10	E2
	P35		21	11	11	E1
	P36		22	12	12	F4
	P37		25	15	15	F3
	P38		26	16	16	F2
	P39		27	17	17	F1
	P3A		28	18	18	G3
	P3B		6	2	2	C3
	P3C		7	3	3	C2
	P3D		8	4	4	D3
	P3E		9	5	5	D2
	P3F		10	6	6	D1
	P46	General-purpose I/O port 4	79	51	51	N7
	P47		80	52	52	N9
	P48		82	54	54	L11
	P49		83	55	55	L12
	P50	General-purpose I/O port 5	65	43	43	K7
	P51		66	44	44	L7
	P52		67	45	45	K8
	P53		68	46	46	L8
	P54		69	47	47	K9
	P55		70	48	48	L9
	P56		71	49	49	L10
	P60	General-purpose I/O port 6	172	116	116	B2
	P61		171	115	115	B3
	P62		170	114	114	B4
	P63		165	113	113	C4
	P64		164	112	112	B5
	P65		163	111	111	C5
	P66		162	110	110	A6
	P67		161	109	109	B6
	P68		160	108	108	C6

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
GPIO	P70	General-purpose I/O port 7	34	20	—	J1
	P71		35	21	—	K1
	P72		36	22	—	H2
	P73		37	23	—	H3
	P74		38	24	—	J2
	P75		39	25	—	J3
	P76		40	26	—	K2
	P77		41	27	27	K3
	P78		42	28	28	L2
	P79		43	29	29	L3
	P7A		33	19	—	G2
	P7B		12	8	8	E4
	P7C		11	7	7	D4
	P80	General-purpose I/O port 8	174	118	118	A3
	P81		175	119	119	A2
	P90	General-purpose I/O port 9	120	82	82	E12
	P91		121	83	83	E13
	P92		122	84	84	D10
	P93		123	85	85	D11
	P94		124	86	86	D12
	P95		125	87	87	D13
	P96		130	88	88	C12
	P97		131	89	89	C13
	PA0	General-purpose I/O port A	2	—	—	—
	PA1		3	—	—	—
	PA2		4	—	—	—
	PA3		5	—	—	—
	PA4		29	—	—	—
	PA5		30	—	—	—
	PA6		31	—	—	—
	PA7		32	—	—	—
	PA8		13	—	—	—
	PA9		14	—	—	—
	PAA		15	—	—	—
	PAB		16	—	—	—
	PAC		17	—	—	—
	PAD		18	—	—	—

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
GPIO	PB0	General-purpose I/O port B	47	—	—	—
	PB1		48	—	—	—
	PB2		49	—	—	—
	PB3		50	—	—	—
	PB4		56	—	—	—
	PB5		57	—	—	—
	PB6		58	—	—	—
	PB7		59	—	—	—
	PB8		72	—	—	—
	PB9		73	—	—	—
	PBA		74	—	—	—
	PBB		75	—	—	—
	PBC		76	—	—	—
	PBD		77	—	—	—
	PC0	General-purpose I/O port C	94	—	—	—
	PC1		95	—	—	—
	PC2		96	—	—	—
	PC3		97	—	—	—
	PC4		98	—	—	—
	PC5		99	—	—	—
	PC6		112	—	—	—
	PC7		113	—	—	—
	PC8		114	—	—	—
	PC9		115	—	—	—
	PCA		126	—	—	—
	PCB		127	—	—	—
	PCC		128	—	—	—
	PCD		129	—	—	—
	PD0	General-purpose I/O port D	134	—	—	—
	PD1		135	—	—	—
	PD2		136	—	—	—
	PD3		137	—	—	—
	PD4		138	—	—	—
	PD5		144	—	—	—
	PD6		145	—	—	—
	PD7		146	—	—	—
	PD8		147	—	—	—
	PD9		148	—	—	—
	PDA		166	—	—	—
	PDB		167	—	—	—
	PDC		168	—	—	—
	PDD		169	—	—	—

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
GPIO	PE0	General-purpose I/O port E	84	56	56	M12
	PE2		86	58	58	N11
	PE3		87	59	59	N12
Multi-function serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	52	34	34	L4
	SIN0_1		120	82	82	E12
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I²C (operation mode 4).	53	35	35	M4
	SOT0_1 (SDA0_1)		121	83	83	E13
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I²C (operation mode 4)	54	36	36	K5
	SCK0_1 (SCL0_1)		122	84	84	D10
Multi-function serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	100	66	66	K11
	SIN1_1		123	85	85	D11
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN(operation modes 0 to 3) and as SDA1 when it is used in an I²C (operation mode 4).	101	67	67	J11
	SOT1_1 (SDA1_1)		124	86	86	D12
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I²C (operation mode 4).	102	68	68	H10
	SCK1_1 (SCL1_1)		125	87	87	D13
Multi-function serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	103	69	69	H11
	SIN2_1		151	99	99	C9
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation mode 0 to 3) and as SDA2 when it is used in an I²C (operation mode 4).	104	70	70	H12
	SOT2_1 (SDA2_1)		152	100	100	B9
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.2 clock I/O Pin. This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I²C (operation mode 4).	105	71	71	H13
	SCK2_1 (SCL2_1)		153	101	101	A9
Multi-function serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	106	72	72	G10
	SIN3_1		162	110	110	A6
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I²C (operation mode 4).	107	73	73	G11
	SOT3_1 (SDA3_1)		161	109	109	B6
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation mode 2) and as SCL3 when it is used in an I²C (operation mode 4).	108	74	74	G12
	SCK3_1 (SCL3_1)		160	108	108	C6

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
Multi-function serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	172	116	116	B2
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	171	115	115	B3
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I^2C (operation mode 4).	170	114	114	B4
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	164	112	112	B5
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	165	113	113	C4
Multi-function serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	109	75	75	G13
	SIN5_1		154	102	102	C8
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I^2C (operation mode 4).	110	76	76	F10
	SOT5_1 (SDA5_1)		155	103	103	B8
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I^2C (operation mode 4).	111	77	77	F11
	SCK5_1 (SCL5_1)		156	104	104	A8
Multi-function serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	19	9	9	E3
	SIN6_1		117	79	79	F13
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	20	10	10	E2
	SOT6_1 (SDA6_1)		118	80	80	E10
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I^2C (operation mode 4).	21	11	11	E1
	SCK6_1 (SCL6_1)		119	81	81	E11
	SCS60_0	Multi-function serial interface ch.6 chip select 0 input/output pin	22	12	12	F4
	SCS60_1		116	78	78	F12

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
Multi-function serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	8	4	4	D3
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	9	5	5	D2
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I^2C (operation mode 4).	10	6	6	D1
	SCS70_0	Multi-function serial interface ch.7 chip select 0 input/output pin	7	3	3	C2
Multi-function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of Multi-function timer 0.	27	17	17	F1
	DTTI0X_1		104	70	70	H12
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	20	10	10	E2
	FRCK0_1		103	69	69	H11
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	26	16	16	F2
	IC00_1		105	71	71	H13
	IC01_0		25	15	15	F3
	IC01_1		106	72	72	G10
	IC02_0		22	12	12	F4
	IC02_1		107	73	73	G11
	IC03_0		21	11	11	E1
	IC03_1		108	74	74	G12
	RTO00_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	6	2	2	C3
	RTO00_1 (PPG00_1)		109	75	75	G13
	RTO01_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	7	3	3	C2
	RTO01_1 (PPG00_1)		110	76	76	F10
	RTO02_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	8	4	4	D3
	RTO02_1 (PPG02_1)		111	77	77	F11
	RTO03_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	9	5	5	D2
	RTO03_1 (PPG02_1)		116	78	78	F12

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
Multi-function Timer 0	RTO04_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	10	6	6	D1
	RTO04_1 (PPG04_1)		117	79	79	F13
	RTO05_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	11	7	7	D4
	RTO05_1 (PPG04_1)		118	80	80	E10
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	100	66	66	K11
	AIN0_1		6	2	2	C3
	AIN0_2		109	75	75	G13
	BIN0_0	QPRC ch.0 BIN input pin	101	67	67	J11
	BIN0_1		7	3	3	C2
	BIN0_2		110	76	76	F10
	ZIN0_0	QPRC ch.0 ZIN input pin	102	68	68	H10
	ZIN0_1		8	4	4	D3
	ZIN0_2		111	77	77	F11
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	171	115	115	B3
	RTCCO_1		63	41	41	M5
	SUBOUT_0	Sub clock output pin	171	115	115	B3
	SUBOUT_1		63	41	41	M5
USB0	UDM0	USB ch.0 device/host D – pin	174	118	118	A3
	UDP0	USB ch.0 device/host D + pin	175	119	119	A2
	UHCONX0	USB ch.0 external pull-up control pin	171	115	115	B3
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	46	32	32	M2
	WKUP1	Deep standby mode return signal input pin 1	65	43	43	K7
	WKUP2	Deep standby mode return signal input pin 2	158	106	106	B7
	WKUP3	Deep standby mode return signal input pin 3	172	116	116	B2
VBAT	VREGCTL	On-board regulator control pin	82	54	54	L11
	VWAKEUP	The return signal input pin from a hibernation state	83	55	55	L12
SD memory card interface	S_CLK_0	SD memory card clock output pin	21	11	11	E1
	S_CMD_0	SD memory card command output	22	12	12	F4
	S_DATA1_0	SD memory card data bus	19	9	9	E3
	S_DATA0_0		20	10	10	E2
	S_DATA3_0		25	15	15	F3
	S_DATA2_0		26	16	16	F2
	S_CD_0	SD memory card detection pin	28	18	18	G3
	S_WP_0	SD memory card write protection	27	17	17	F1

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
I²S 0	I2SMCLK0_0	I²S ch.0 external clock pin	6	2	2	C3
	I2SDO0_0	I²S ch.0 serial transition data output pin	7	3	3	C2
	I2SWS0_0	I²S ch.0 frame synchronization signal pin	8	4	4	D3
	I2SDI0_0	I²S ch.0 serial received data input pin	9	5	5	D2
	I2SCK0_0	I²S ch.0 bit clock pin	10	6	6	D1
I²S 1	I2SMCLK1_0	I²S ch.1 external clock pin	51	33	33	M3
	I2SDO1_0	I²S ch.1 serial transition data output pin	52	34	34	L4
	I2SWS1_0	I²S ch.1 frame synchronization signal pin	53	35	35	M4
	I2SDI1_0	I²S ch.1 serial received data input pin	54	36	36	K5
	I2SCK1_0	I²S ch.1 bit clock pin	55	37	37	L5
GDC High-Speed Quad SPI	GE_SPCK	SPI clock output pin	34	20	-	J1
	GE_SPDQ0	SPI data input / output pin	35	21	-	K1
	GE_SPDQ1		38	24	-	J2
	GE_SPDQ2		39	25	-	J3
	GE_SPDQ3		36	22	-	H2
	GE_SPCSX0	SPI chip select output pin	37	23	-	H3
GDC HyperBus I/F	GE_HBCK	HBI clock output pin	34	20	-	J1
	GE_HBDQ0	HBI data input / output pin	36	22	-	H2
	GE_HBDQ1		37	23	-	H3
	GE_HBDQ2		38	24	-	J2
	GE_HBDQ3		39	25	-	J3
	GE_HBDQ4		40	26	-	K2
	GE_HBDQ5		41	27	-	K3
	GE_HBDQ6		42	28	-	L2
	GE_HBDQ7		43	29	-	L3
	GE_HBCSX0	HBI chip select output pin	35	21	-	K1
	GE_HBCSX1		12	8	-	E4
	GE_HBRWDS	HBI RWDS input / output pin	33	19	-	G2
	GE_HBRESETX	HBI hardware reset output pin	25	15	-	F3
	GE_HBINTX	HBI interrupt input pin	26	16	-	F2
	GE_HBRSTOX	HBI reset input pin	27	17	-	F1
	GE_HBWPX	HBI write protect output pin	28	18	-	G3

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
GDC Panel	PNL_DCLK	GDC clock output pin	67	45	45	K8
	PNL_DEN	GDC data enable output pin (blanking signal)	68	46	46	L8
	PNL_PWE	GDC power enable control output pin	66	44	44	L7
	PNL_LE	GDC line end output pin	69	47	47	K9
	PNL_LH_SYNC	GDC horizontal synchronization output pin	70	48	48	L9
	PNL_FV_SYNC	GDC vertical synchronization output pin	71	49	49	L10
	PNL_PD0	GDC panel data output pin	165	113	113	C4
	PNL_PD1		164	112	112	B5
	PNL_PD2		163	111	111	C5
	PNL_PD3		162	110	110	A6
	PNL_PD4		161	109	109	B6
	PNL_PD5		160	108	108	C6
	PNL_PD6		158	106	106	B7
	PNL_PD7		157	105	105	C7
	PNL_PD8		156	104	104	A8
	PNL_PD9		155	103	103	B8
	PNL_PD10		154	102	102	C8
	PNL_PD11		153	101	101	A9
	PNL_PD12		152	100	100	B9
	PNL_PD13		151	99	99	C9
	PNL_PD14		150	98	98	D9
	PNL_PD15		149	97	97	C10
	PNL_PD16		131	89	89	C13
	PNL_PD17		130	88	88	C12
	PNL_PD18		125	87	87	D13
	PNL_PD19		124	86	86	D12
	PNL_PD20		123	85	85	D11
	PNL_PD21		122	84	84	D10
	PNL_PD22		121	83	83	E13
	PNL_PD23		120	82	82	E12
	PNL_TSIG0	GDC timing generator for panel control PNL_TSIG signals are customized synchronization signals for direct interfacing to the column and row drivers of most panel types. For more information, refer to Peripheral Manual (GDC Core part).	70	48	48	L9
	PNL_TSIG1		71	49	49	L10
	PNL_TSIG2		68	46	46	L8
	PNL_TSIG3		69	47	47	K9
	PNL_TSIG4		66	44	44	L7
	PNL_TSIG5		130	88	88	C12
	PNL_TSIG6		125	87	87	D13
	PNL_TSIG7		124	86	86	D12
	PNL_TSIG8		123	85	85	D11
	PNL_TSIG9		122	84	84	D10
	PNL_TSIG10		121	83	83	E13
	PNL_TSIG11		120	82	82	E12

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
GDC SDRAM-IF (176 pin only)	GE_SDA0	SDRAM-IF address output pin	144	-	-	-
	GE_SDA1		138	-	-	-
	GE_SDA2		137	-	-	-
	GE_SDA3		136	-	-	-
	GE_SDA4		135	-	-	-
	GE_SDA5		134	-	-	-
	GE_SDA6		129	-	-	-
	GE_SDA7		128	-	-	-
	GE_SDA8		127	-	-	-
	GE_SDA9		126	-	-	-
	GE_SDA10		115	-	-	-
	GE_SDA11		114	-	-	-
	GE_SDBA0	SDRAM-IF bank address output pin	113	-	-	-
	GE_SDBA1		112	-	-	-
	GE_SDCASX	SDRAM-IF column active output pin	168	-	-	-
	GE_SDRASX	SDRAM-IF row active output pin	167	-	-	-
	GE_SDWEX	SDRAM-IF write enable output pin	166	-	-	-
	GE_SDCKE	SDRAM-IF clock enable output pin	2	-	-	-
	GE_SDCLK	SDRAM-IF clock output pin	3	-	-	-
	GE_SDCSX	SDRAM-IF chip select output pin	169	-	-	-
	GE_SDDQ0	SDRAM-IF data input / output pin	99	-	-	-
	GE_SDDQ1		98	-	-	-
	GE_SDDQ2		97	-	-	-
	GE_SDDQ3		96	-	-	-
	GE_SDDQ4		95	-	-	-
	GE_SDDQ5		94	-	-	-
	GE_SDDQ6		77	-	-	-
	GE_SDDQ7		76	-	-	-
	GE_SDDQ8		75	-	-	-
	GE_SDDQ9		74	-	-	-
	GE_SDDQ10		73	-	-	-
	GE_SDDQ11		72	-	-	-
	GE_SDDQ12		59	-	-	-
	GE_SDDQ13		58	-	-	-
	GE_SDDQ14		57	-	-	-
	GE_SDDQ15		56	-	-	-
	GE_SDDQ16		50	-	-	-
	GE_SDDQ17		49	-	-	-
	GE_SDDQ18		48	-	-	-
	GE_SDDQ19		47	-	-	-
	GE_SDDQ20		32	-	-	-
	GE_SDDQ21		31	-	-	-
	GE_SDDQ22		30	-	-	-
	GE_SDDQ23		29	-	-	-

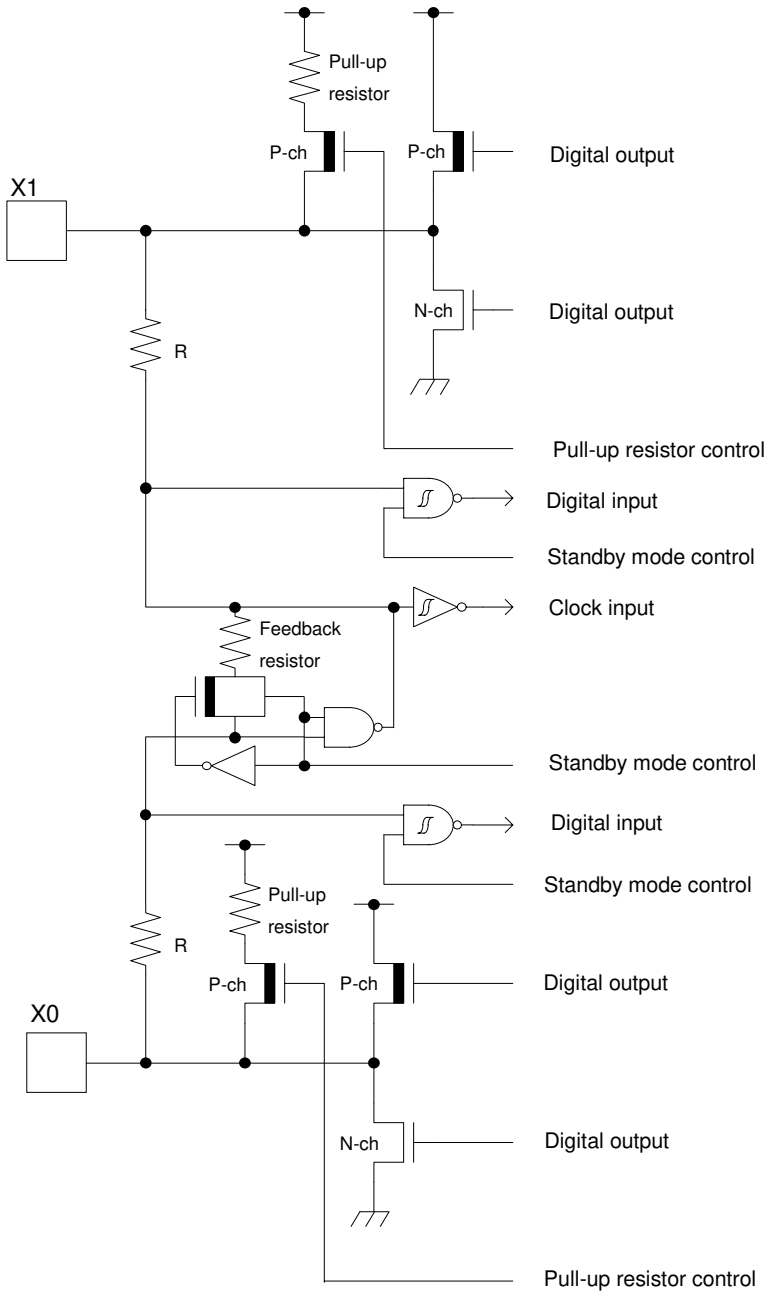
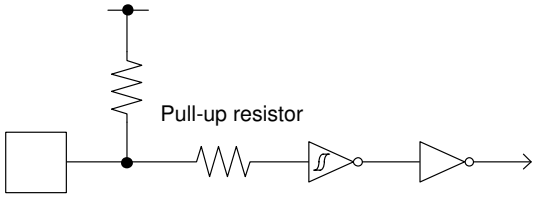
Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
GDC SDRAM-IF (176 pin only)	GE_SDDQ24	SDRAM-IF data input / output pin	18	-	-	-
	GE_SDDQ25		17	-	-	-
	GE_SDDQ26		16	-	-	-
	GE_SDDQ27		15	-	-	-
	GE_SDDQ28		14	-	-	-
	GE_SDDQ29		13	-	-	-
	GE_SDDQ30		5	-	-	-
	GE_SDDQ31		4	-	-	-
	GE_SDDQM0	SDRAM-IF input / output mask pin	148	-	-	-
	GE_SDDQM1		147	-	-	-
	GE_SDDQM2		146	-	-	-
	GE_SDDQM3		145	-	-	-
Reset	INITX	External Reset Input pin. A reset is valid when INITX = L.	78	50	50	M8
Mode	MD1	Mode 1 pin. During serial programming to Flash memory, MD1 = L must be input.	84	56	56	M12
	MD0	Mode 0 pin. During normal operation, MD0 = L must be input. During serial programming to Flash memory, MD0 = H must be input.	85	57	57	M11
Power	VCC	Power supply Pin	1	1	1	C1
			23	13	13	G1
			44	30	30	L1
			62	40	40	N4
			89	61	61	L13
			133	91	91	A12
			173	117	117	A4
GND	VSS	GND Pin	24	14	14	H1
			45	31	31	M1
			61	39	39	N3
			88	60	60	M13
			132	90	90	B13
			159	107	107	A7
			176	120	120	B1
Clock	X0	Main clock (oscillation) input pin	86	58	58	N11
	X0A	Sub clock (oscillation) input pin	79	51	51	N7
	X1	Main clock (oscillation) I/O pin	87	59	59	N12
	X1A	Sub clock (oscillation) I/O pin	80	52	52	N9
	CROUT_0	Built-in High-speed CR-osc clock output port	52	34	34	L4
	CROUT_1		64	42	42	N5
Analog Power	AVCC	A/D converter analog power supply pin	90	62	62	K13
	AVRL	A/D converter analog reference voltage input pin	92	64	64	J13
	AVRH	A/D converter analog reference voltage input pin	93	65	65	J12

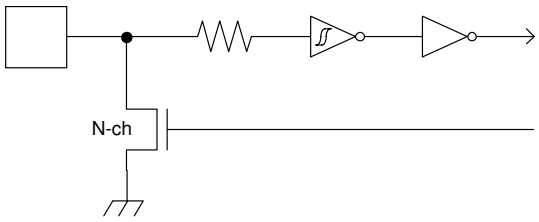
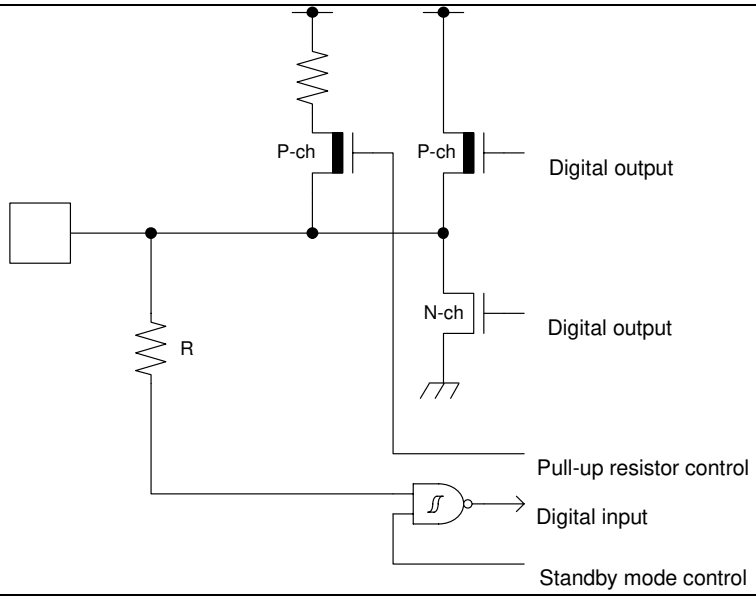
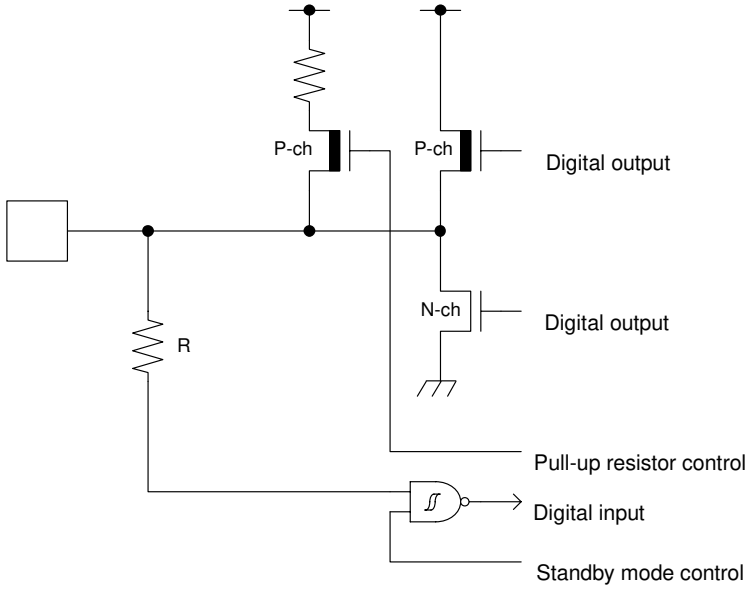
Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2DF5GJA)	FBGA161
VBAT Power	VBAT	VBAT power supply pin. Backup power supply (battery etc.) and system power supply.	81	53	53	M9
Analog GND	AVSS	A/D converter GND pin	91	63	63	K12
C Pin	C	Power supply stabilization capacity pin	60	38	38	N2

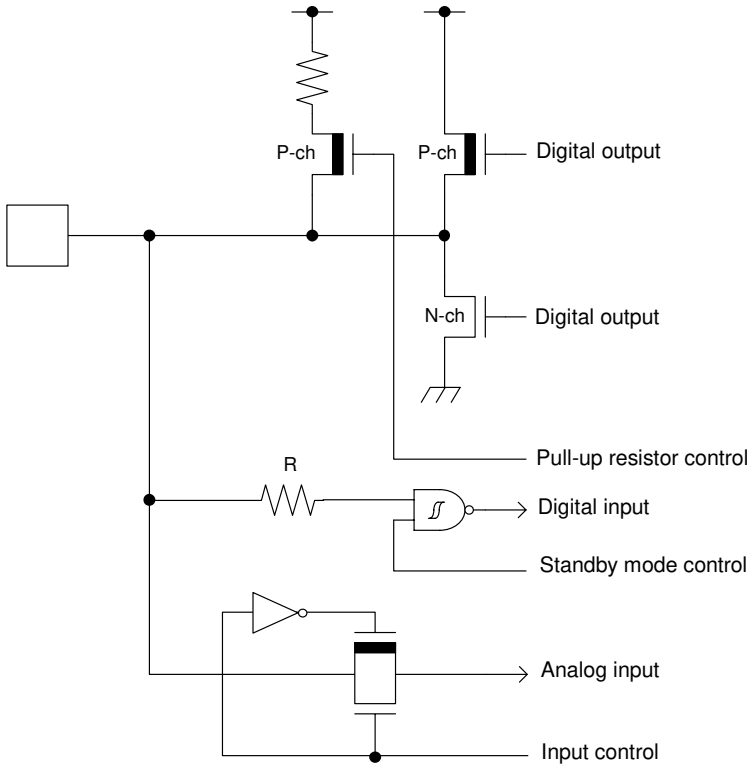
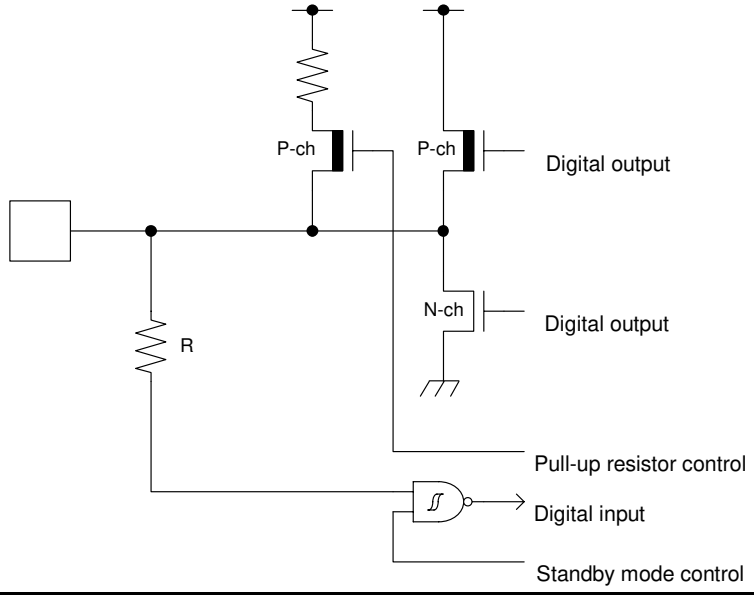
Note:

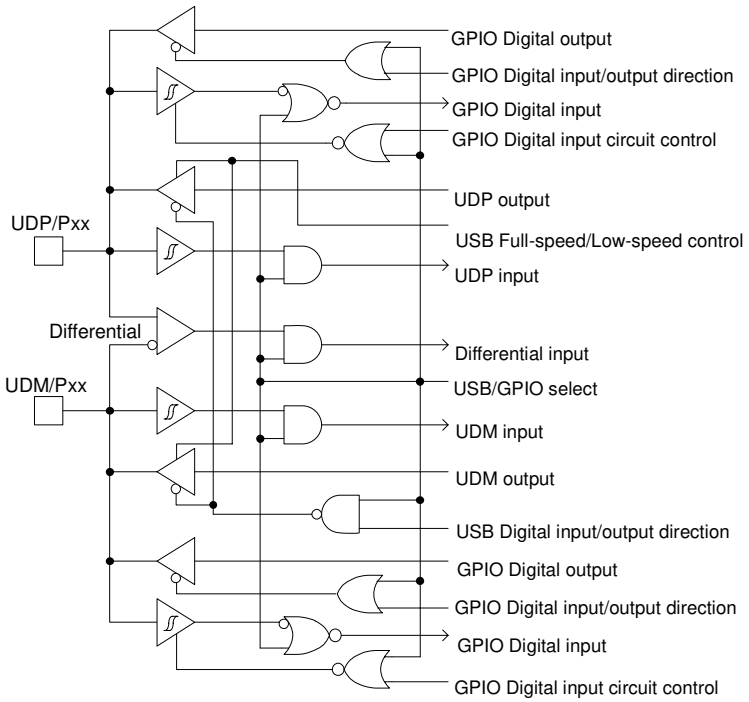
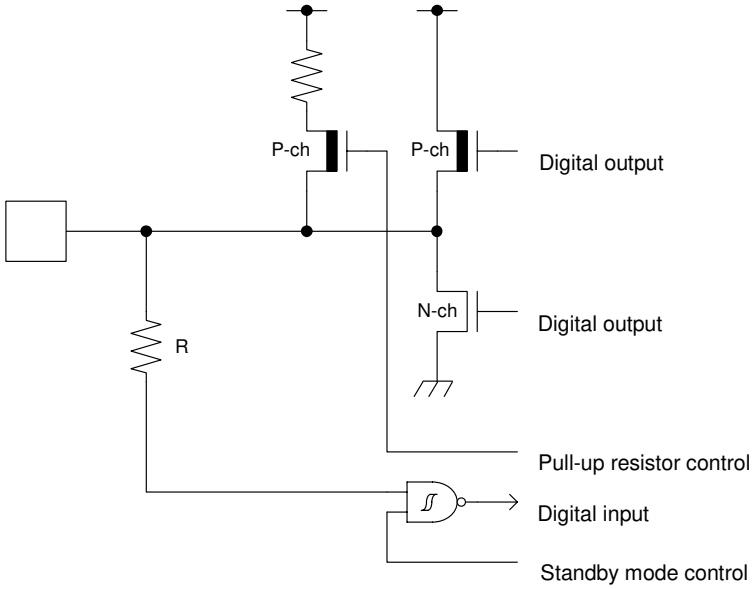
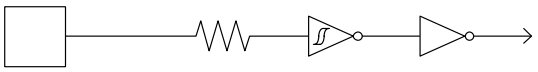
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

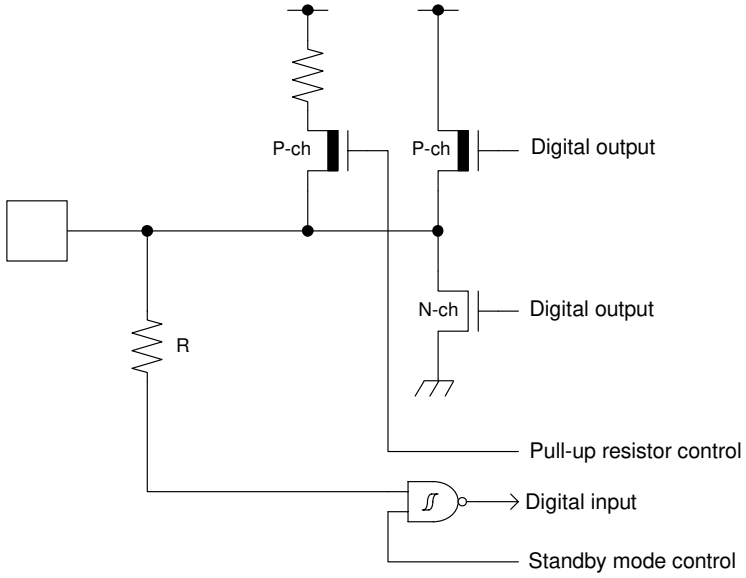
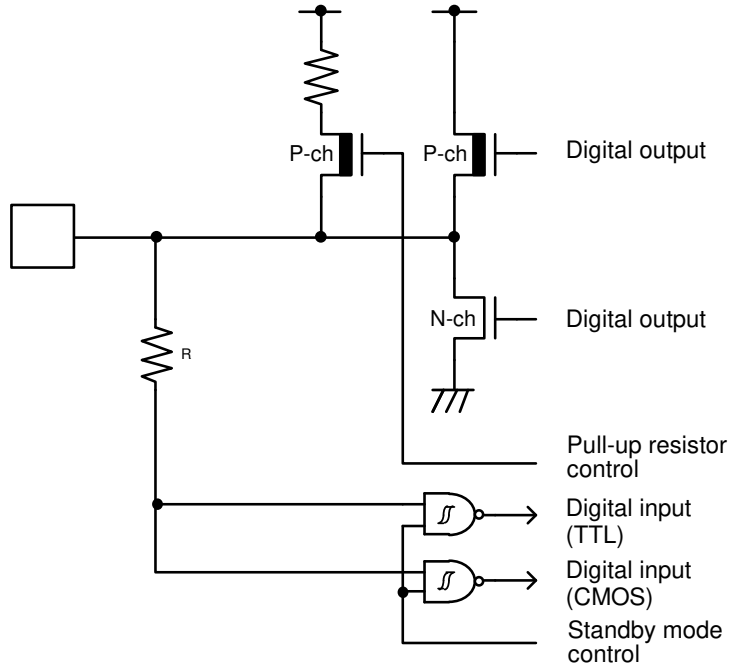
5. I/O Circuit Type

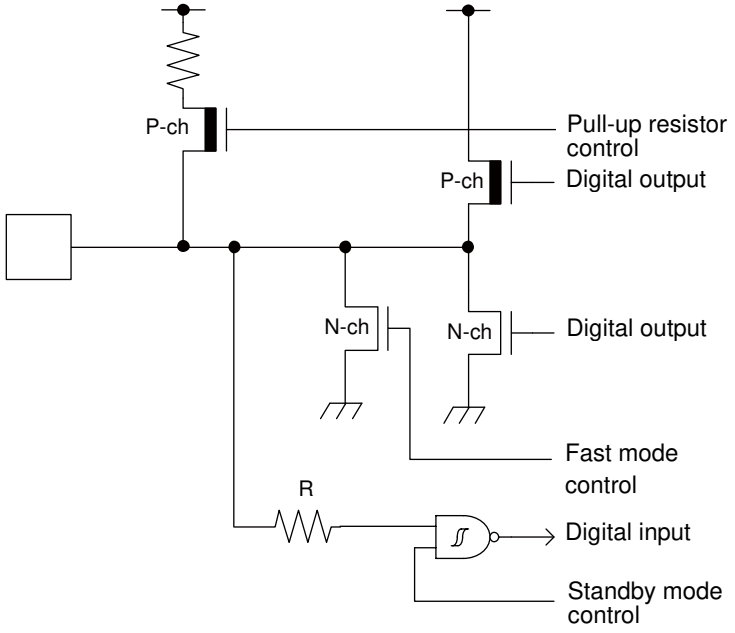
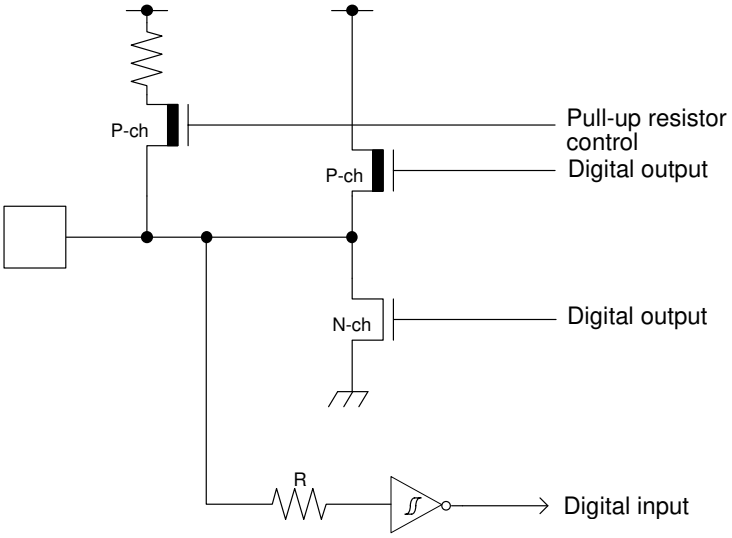
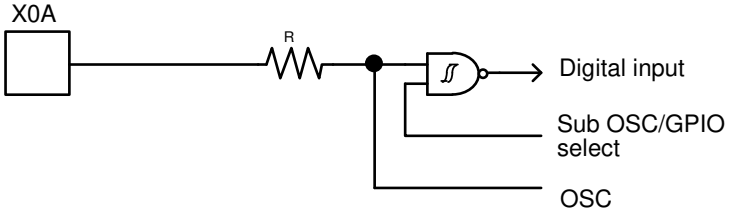
Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. ・Oscillation feedback resistor : Approximately 1 MΩ ・With Standby mode control When the GPIO is selected. ・CMOS level output. ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -2 mA, I_{OL} = 2 mA
B		・CMOS level hysteresis input ・Pull-up resistor : Approximately 80 kΩ

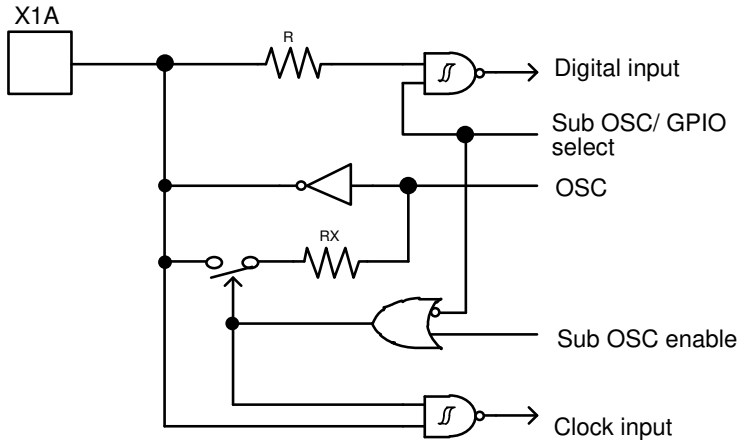
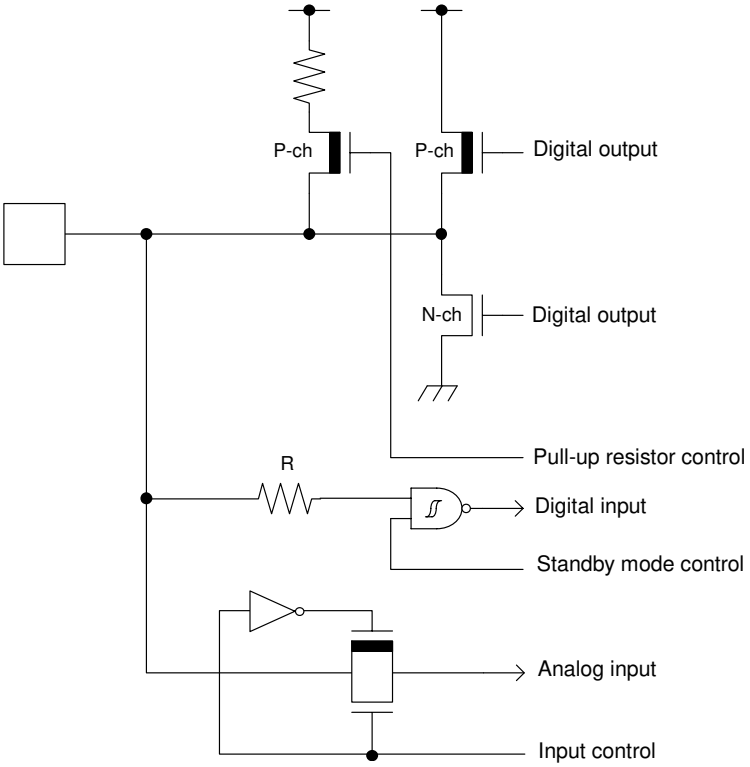
Type	Circuit	Remarks
C		・Open drain output ・CMOS level hysteresis input
D		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
E		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -2 mA, I_{OL} = 2 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Type	Circuit	Remarks
F		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -2 mA, I_{OL} = 2 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
G		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -8 mA, I_{OL} = 8 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Type	Circuit	Remarks
H		It is possible to select the USB I/O / GPIO function. When the USB I/O is selected. ・Full-speed, Low-speed control When the GPIO is selected. ・CMOS level output ・CMOS level hysteresis input ・With standby mode control ・I_{OH} = -20.5 mA, I_{OL} = 18.5 mA
I		・CMOS level output ・CMOS level hysteresis input ・5 V tolerant ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -2 mA, I_{OL} = 2 mA ・Available to control of PZR registers.
J		・CMOS level hysteresis input

Type	Circuit	Remarks
K		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -11 mA, I_{OL} = 11 mA
L		・CMOS level output ・CMOS level hysteresis input ・TTL level hysteresis input :SDRAM-IF Data Input only ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33 kΩ ・I_{OH} = -11 mA, I_{OL} = 11 mA

Type	Circuit	Remarks
N		・CMOS level output ・CMOS level hysteresis input ・5 V tolerant ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -3 mA, I_{OL} = 3 mA (GPIO) ・I_{OL} = 20 mA (Fast Mode Plus) ・Available to control of PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
O		・CMOS level output ・CMOS level hysteresis input ・5 V tolerant ・With pull-up resistor control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -2 mA, I_{OL} = 2 mA ・Available to control of PZR registers. ・Please refer to the "VBAT domain" setting of the IO in the “Peripheral Manual main part (002-04856)".
P		・CMOS level hysteresis input ・Please refer to the "VBAT domain" setting of the IO in the “Peripheral Manual main part (002-04856)".

Type	Circuit	Remarks
Q		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. ・Oscillation feedback resistor : Approximately 12 MΩ When the GPIO is selected. ・CMOS level hysteresis input ・Please refer to the "VBAT domain" setting of the IO in the “Peripheral Manual main part (002-04856)".
R		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each POWER pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS, between AVCC and AVSS and between AVRH and AVRL near this device.

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1 V/µs at a momentary fluctuation such as switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption.
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

■Surface mount type

Size:	More than 3.2 mm × 1.5 mm
Load capacitance:	Approximately 6 pF to 7 pF When the Standard setting (CCS/CCB=11001110)
Load capacitance:	Approximately 4 pF to 7 pF When the low power setting (CCS/CCB=00000100)

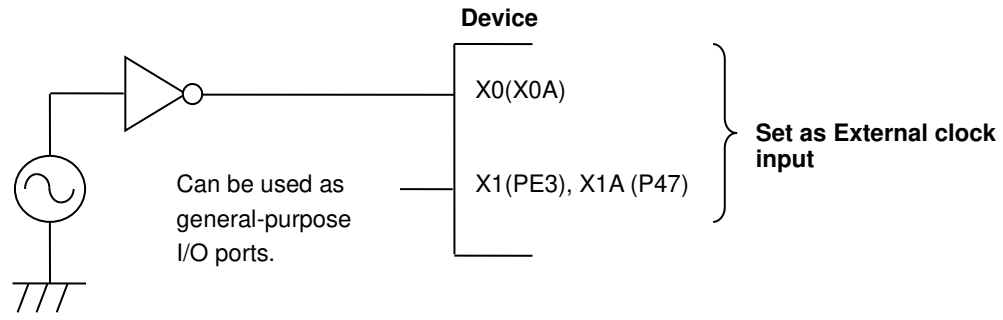
■Lead type

Load capacitance:	Approximately 6 pF to 7 pF When the Standard setting (CCS/CCB=11001110)
Load capacitance:	Approximately 4 pF to 7 pF When the low power setting (CCS/CCB=00000100)

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

● Example of Using an External Clock

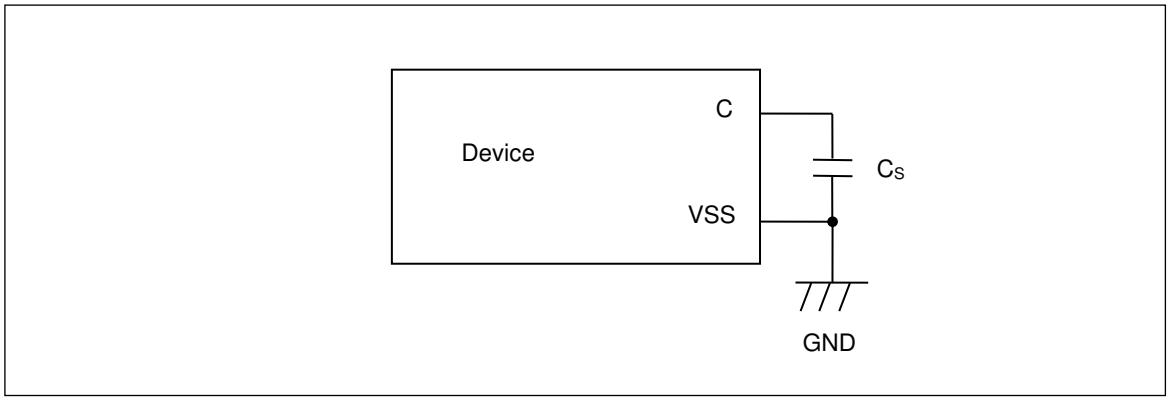


Handling when Using Multi-Function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled.
However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on Power-on

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

VBAT only Power-on is possible when VBAT and VCC turns Power-on and Hibernation control is setting and then turns Power-off.

About Hibernation control, see Chapter 7-3: VBAT Domain(B) in FM4 Family Peripheral Manual Main Part (002-04856).

Turning on : VBAT → VCC→ AVCC → AVRH
Turning off : AVRH → AVCC → VCC→ VBAT

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5V tolerant I/O.

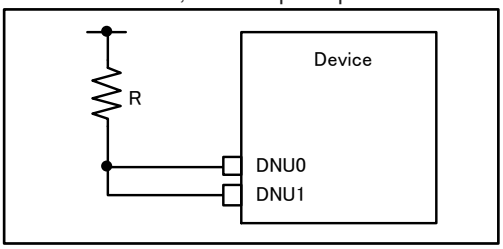
Pin Doubled as Debug Function

Please use as output only regarding the pin doubled as TDO/TMS/TDI/TCK/TRSTX, SWO/SWDIO/SWCLK.
Don't use as input.

S6E2DF5GJA

The following must correspond to S6E2DF5GJA.

1. Terminal DNU0 / 1 is short-circuited, and the pull-up of about 10kΩ is done.



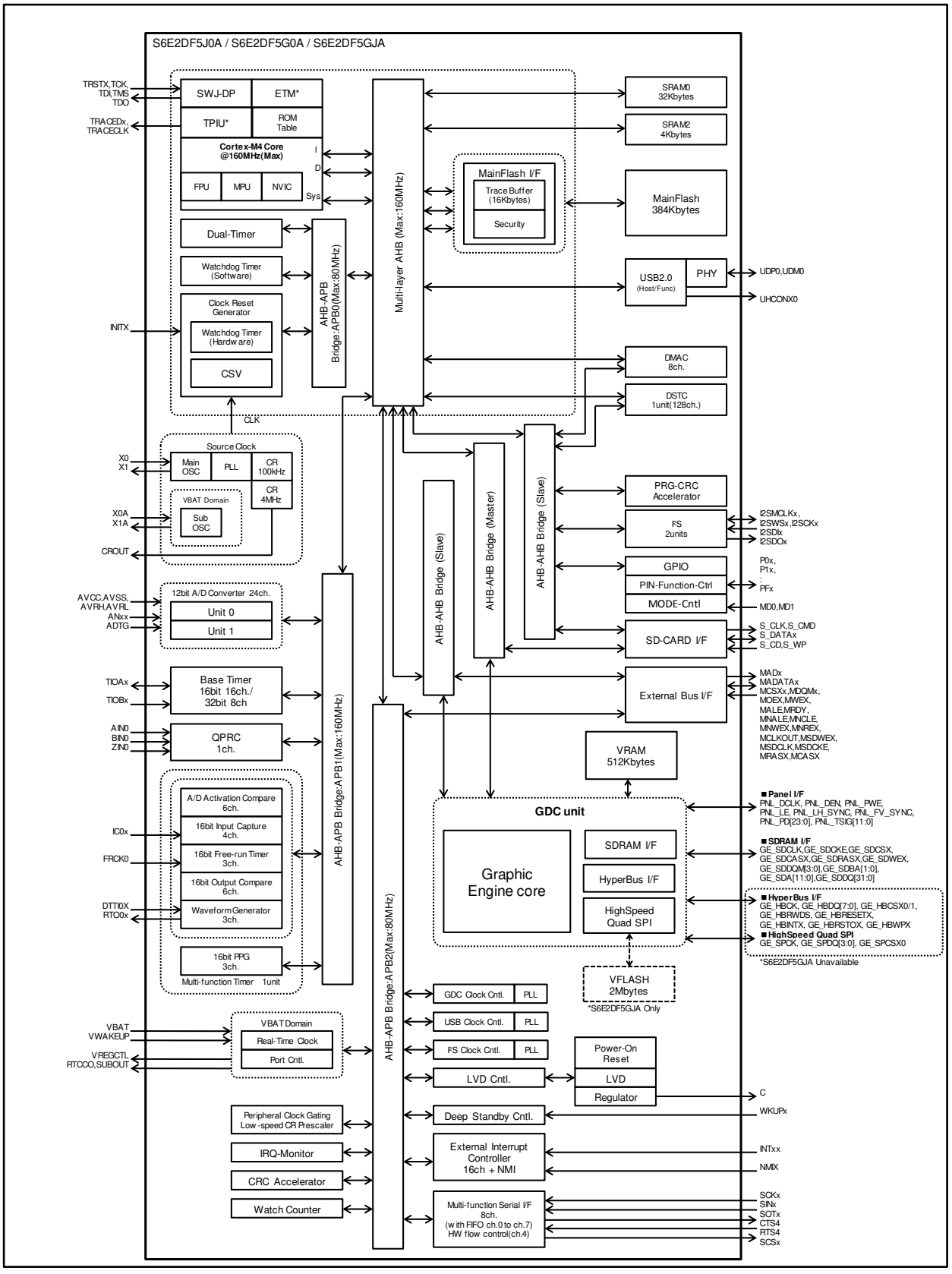
2. Please do not connect the open end NC terminal.
3. Please have the following port settings.

PFR7: bit6=0, bit10=0
PDOR7: bit6=0, bit10=0
DDR7: bit6=1, bit10=1

See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.

4. Please connect a bypass capacitor as close as possible to GND on the board and VCC in pin number 22.

8. Block Diagram

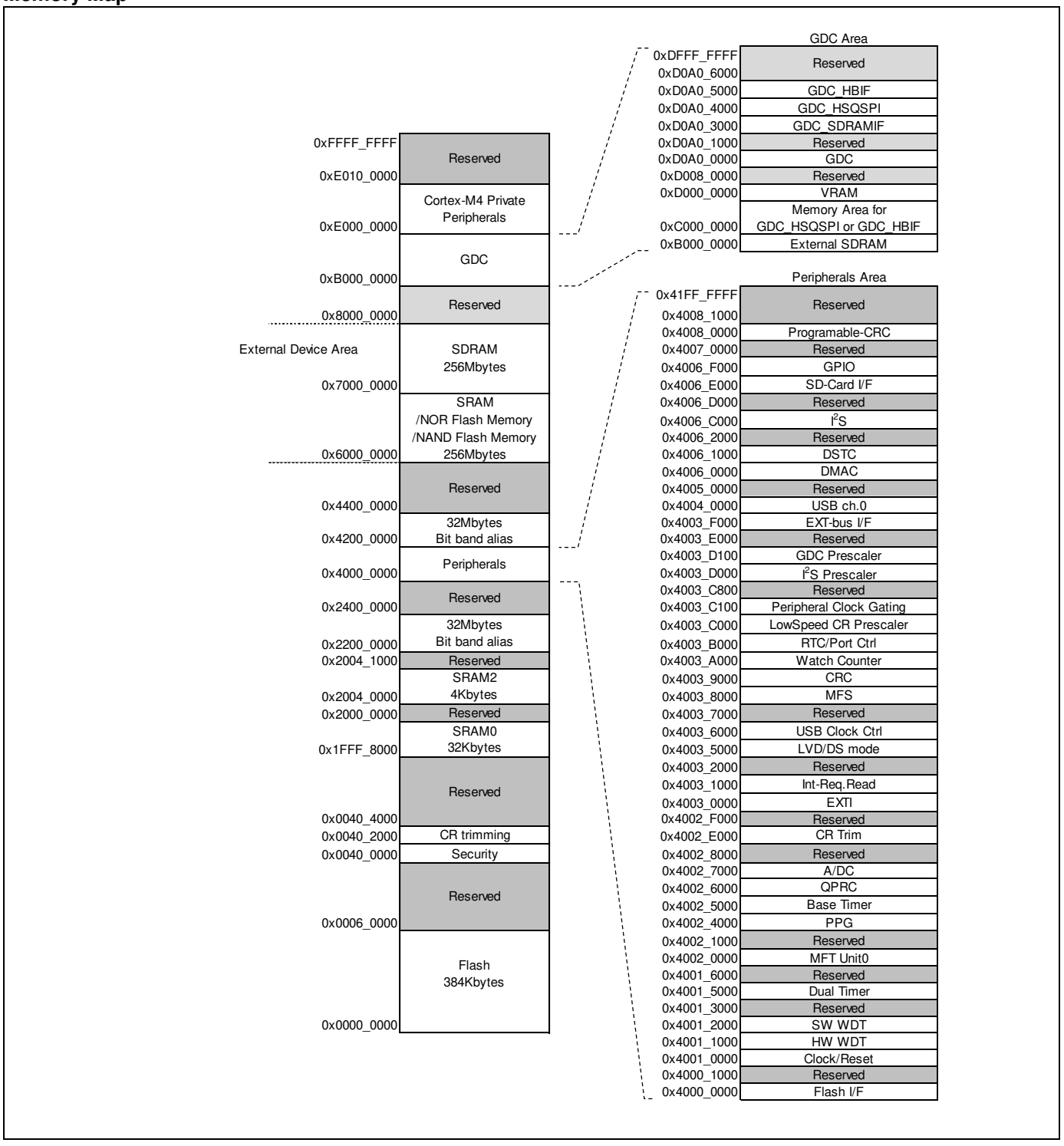


9. Memory Size

See Memory size in 1. Product Lineup to confirm the memory size.

10. Memory Map

Memory Map



Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low Voltage Detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		RTC/PortCtrl
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_CFFF		Reserved
0x4003_D000	0x4003_D0FF		I^2S Prescaler
0x4003_D100	0x4003_DFFF		GDC Prescaler
0x4003_E000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4004_FFFF	AHB	USB ch.0
0x4005_0000	0x4005_FFFF		Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_BFFF		Reserved
0x4006_C000	0x4006_CFFF		I^2S
0x4006_D000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD-Card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4007_0000	0x4007_FFFF		Reserved
0x4008_0000	0x4008_0FFF		Programmable-CRC
0x4008_1000	0x41FF_FFFF		Reserved
0xB000_0000	0xDFFF_FFFF	AHB	GDC unit

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0

  This is the period when the INITX pin is the L level.

- INITX=1

  This is the period when the INITX pin is the H level.

- SPL=0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL=1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation.

List of Pin Status

Pin status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ or Input enable	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state/ When oscillation stops*1,Hi-Z / Internal input fixed at 0					
C	INITX input pin	Pull-up / input enabled	Pull-up / input enabled	Pull-up / input enabled	Pull-up / input enabled	Pull-up / input enabled	Pull-up / input enabled	Pull-up / input enabled	Pull-up / input enabled	Pull-up / input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / input enabled	GPIO selected	Hi-Z / input enabled	GPIO selected
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled			Hi-Z / Internal input fixed at 0			GPIO selected
	GPIO selected									
G	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
H	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
I	Resource selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									

Pin status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
K	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									

Pin status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									
N	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
O	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External interrupt enabled selected						Maintain previous state			
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									
P	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	GPIO selected									

Pin status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	WKUP input enabled
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Hi-Z at trans-mission/ Internal input fixed at 0 at reception	Hi-Z at trans-mission/ Internal input fixed at 0 at reception	Hi-Z / input enabled	Hi-Z / input enabled	Hi-Z / input enabled	Hi-Z / input enabled

*1: Oscillation is stopped at Sub timer mode, low-speed CR timer mode, RTC mode, Stop mode, Deep standby RTC mode, and Deep standby Stop mode.

List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	Power-on Reset*1	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State	VBAT RTC Mode State	Return from VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Sable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Internal input fixed at 0	Internal input fixed at 0	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Setting prohibition	-
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Internal input fixed at 0	Internal input fixed at 0	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z/ Internal input fixed at 0 or input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state / When oscillation stops, Hi-Z*2	Maintain previous state / When oscillation stops, Hi-Z*2	Maintain previous state / When oscillation stops, Hi-Z*2	Maintain previous state / When oscillation stops, Hi-Z*2	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected / GPIO selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state

*1: When VBAT and VCC power on.

*2: When the SOSCNTL bit in the WTOSCCNT register is 0, Sub crystal oscillator output pin is maintain previous state. When the SOSCNTL bit in the WTOSCCNT register is 1, Oscillation is stopped at Stop mode and Deep standby Stop mode

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Power supply voltage (VBAT) *1 ,*3	V_{BAT}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog power supply voltage *1 ,*4	AV_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog reference voltage *1 ,*4	AVRH	V_{SS} - 0.5	V_{SS} + 4.6	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 4.6 V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6 V)	V	
L level maximum output current *5	I_{OL}	-	10	mA	2 mA type
			20	mA	4 mA type
			20	mA	8 mA type
			20	mA	11 mA type
			22.4	mA	I^2C Fm+
L level average output current *6	I_{OLAV}	-	2	mA	2 mA type
			4	mA	4 mA type
			8	mA	8 mA type
			11	mA	11 mA type
			20	mA	I^2C Fm+
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current *7	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current *5	I_{OH}	-	- 10	mA	2 mA type
			-20	mA	4 mA type
			- 20	mA	8 mA type
			- 20	mA	11 mA type
H level average output current *6	I_{OHAV}	-	- 2	mA	2 mA type
			-4	mA	4 mA type
			- 8	mA	8 mA type
			- 11	mA	11 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current *7	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	200	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: V_{BAT} must not drop below V_{SS} - 0.5 V.

*4: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

12.2 Recommended Operating Conditions

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	3.0	3.6	V	*1
				2.7 *5	3.6		*2
Power supply voltage (VBAT)		V_{BAT}	-	1.65	3.6	V	
Analog power supply voltage		AV_{CC}	-	2.7	3.6	V	$AV_{CC} = V_{CC}$
Analog reference voltage		AVRH	-	*4	AV_{CC}	V	
		AVRL	-	AVss	AVss	V	
Smoothing capacitor		C_S	-	1	10	µF	for built-in regulator *6
Operating temperature	Junction temperature	T_J	-	-40	+ 125	°C	
	Ambient temperature	T_A	-	-40	*3	°C	

*1: When using the GDC part .

When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0).

*2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80).

*3: The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (T_J).
The calculation formula of the ambient temperature (T_A) is shown below.

$$T_A(Max) = T_J(Max) - Pd(Max) \times \theta_{JA}$$

Pd: Power dissipation (W)
θ_{JA}: Package thermal resistance (°C/W)

$$Pd\ (Max) = V_{CC} \times I_{CC}\ (Max) + \Sigma\ (I_{OL} \times V_{OL}) + \Sigma\ ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

*4: The minimum value of Analog reference voltage depends on the value of compare clock cycle (t_{CCK}). See 14.5 12-bit A/D Converter for the details.

*5: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

*6: See "C pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table 12-1 Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θ_{JA} (°C/W)	Maximum Permissible Power (mW)	
			T_A= +85°C	T_A= +105°C
LQFP: LQM120 (0.5 mm pitch)	4 layers	38	1053	526
LQFP: LQM120 *1 (0.5 mm pitch)	4 layers	39	1026	513
LQFP: LQP176 (0.5 mm pitch)	4 layers	35	1143	571
FBGA: FDJ161 (0.5 mm pitch)	4 layers	35	1143	571
Ex-LQFP: LEM120 (0.5 mm pitch)	4 layers	18*2	2222	1111

*1: When S6E2DF5GJA product.
*2: This is a case where the connection process was carried out back exposed die pad foundation. Please connect directly to GND back exposed die pad.

Notes:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

I_{CC} is a current consumed in device.
It can be analyzed as follows.

$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$

$I_{CC}(INT)$: Current consumed in internal logic and memory, etc. through regulator
$\Sigma I_{CC}(IO)$: Sum of current (I/O switching current) consumed in output pin

For I_{CC} (INT), it can be anticipated by "(1) Current Rating" in "3. DC Characteristics" (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For Icc (IO), it depends on system used by customers.
The calculation formula is shown below.

$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times fsw$

C_{INT}: Pin internal load capacitance
C_{EXT}: External load capacitance of output pin
f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	2 mA type	1.93 pF
		4 mA type	3.45 pF
		8 mA type	3.42 pF

Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself.

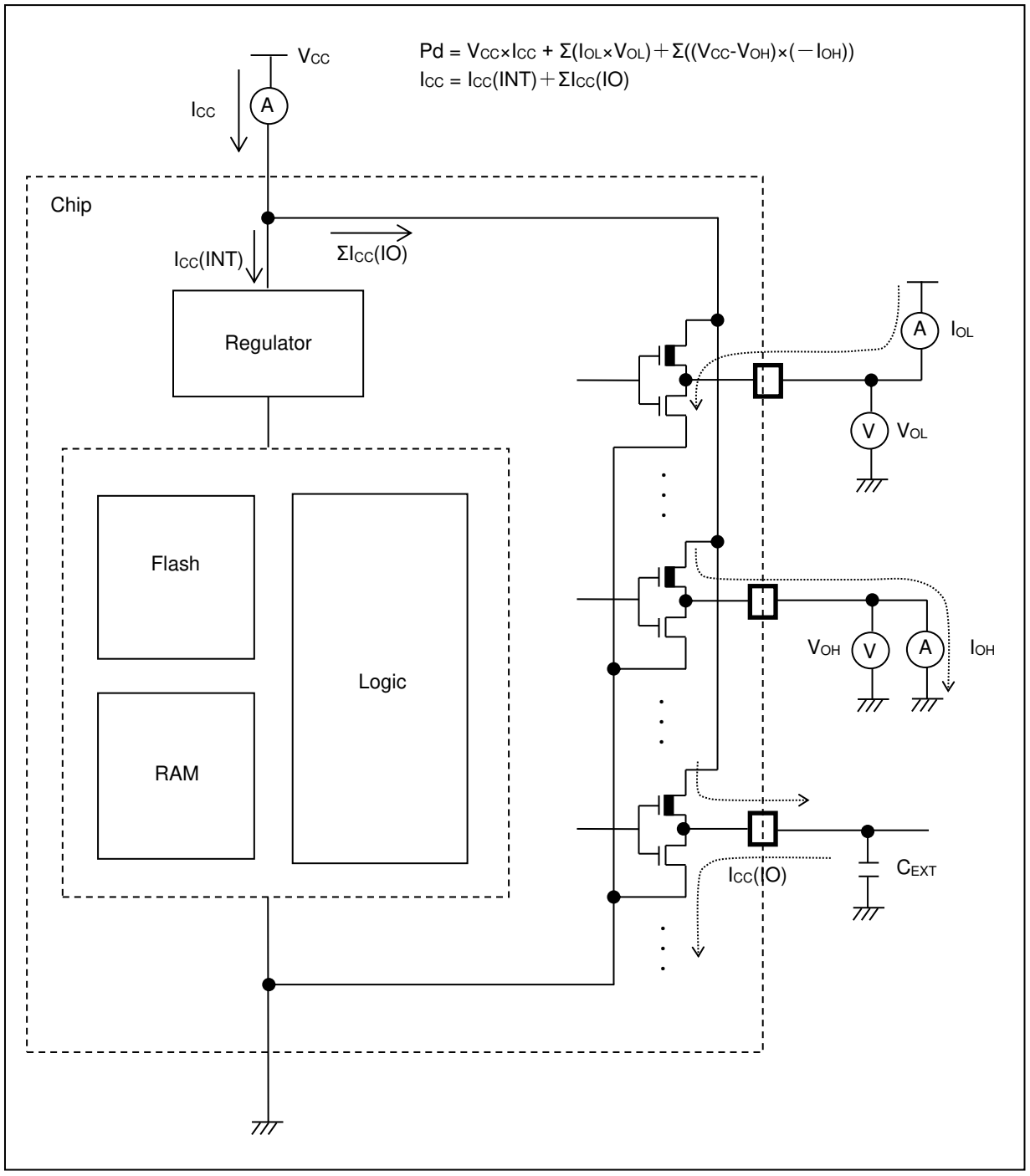
(1) Measure current value I_{CC} (Typ) at normal temperature (+25°C).
(2) Add maximum leak current value I_{CC} (leak_max) at operating on a value in (1).

$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$

Parameter	Symbol	Conditions	Current Value
Maximum leak current at operating	I_{CC}(leak_max)	T_J = +125 °C	66.8 mA
		T_J = +105 °C	33.7 mA
		T_J = +85 °C	22.8 mA

Note:
- *VFLASH of current is not included*

Current Explanation Diagram



12.3 DC Characteristics

12.3.1 Current Rating

Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7 (PLL)	*5	160 MHz	182	279	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
					144 MHz	176	270	mA	
					120 MHz	167	256	mA	
					100 MHz	159	244	mA	
					80 MHz	151	233	mA	
					60 MHz	143	221	mA	
					40 MHz	136	210	mA	
					20 MHz	128	199	mA	
					8 MHz	123	191	mA	
					4 MHz	122	190	mA	
			Normal operation , *6,*7 (PLL)	*5	160 MHz	43	117	mA	*3 When all peripheral clocks are OFF
					144 MHz	39	112	mA	
					120 MHz	34	106	mA	
					100 MHz	29	100	mA	
					80 MHz	24	95	mA	
					60 MHz	20	90	mA	
					40 MHz	15	84	mA	
					20 MHz	10	78	mA	
					8 MHz	7	74	mA	
					4 MHz	6	73	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*6: Data access is nothing to main flash memory and VFLASH memory

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Disabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7,*8 (PLL)	*5	160 MHz	185	285	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
					144 MHz	179	276	mA	
					120 MHz	169	261	mA	
					100 MHz	161	250	mA	
					80 MHz	154	239	mA	
					60 MHz	146	227	mA	
					40 MHz	138	215	mA	
					20 MHz	130	204	mA	
					8 MHz	125	196	mA	
					4 MHz	124	195	mA	
			Normal operation *6,*7,*8 (PLL)	*5	160 MHz	45	122	mA	*3 When all peripheral clocks are OFF
					144 MHz	41	117	mA	
					120 MHz	36	111	mA	
					100 MHz	31	105	mA	
					80 MHz	26	99	mA	
					60 MHz	22	94	mA	
					40 MHz	17	89	mA	
					20 MHz	12	83	mA	
					8 MHz	10	80	mA	
					4 MHz	9	79	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK2=HCLK/2, PCLK1=HCLK

*5: When not operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

*6: With data access to a main flash memory.

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*8: Data access is nothing to VFLASH memory

Table 12-4 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation , *6,*7,*8 (PLL)	*5	72 MHz	168	251	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
					60 MHz	161	242	mA	
					48 MHz	154	233	mA	
					36 MHz	147	224	mA	
					24 MHz	140	214	mA	
					12 MHz	133	205	mA	
					8 MHz	131	202	mA	
					4 MHz	128	199	mA	
				*5	72 MHz	41	114	mA	*3 When all peripheral clocks are OFF
					60 MHz	36	108	mA	
					48 MHz	32	104	mA	
					36 MHz	27	98	mA	
					24 MHz	23	94	mA	
					12 MHz	18	88	mA	
					8 MHz	17	87	mA	
					4 MHz	15	85	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

*5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FSYNDN.SD = 000)

*6: With data access to a main flash memory.

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*8: Data access is nothing to VFLASH memory

Table 12-5 Typical and Maximum Current Consumption in Normal Operation (other than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation, *6,*8 (built-in High-speed CR)	*5	4 MHz	110	181	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
						4.1	74	mA	*3 When all peripheral clocks are OFF
			Normal operation , *6,*7,*8 (Sub oscillation)	*5	32 kHz	0.7	76.65	mA	*3 When all peripheral clocks are ON
						0.69	71.65	mA	*3 When all peripheral clocks are OFF
			Normal operation , *6,*8 (built-in Low-speed CR)	*5	100 kHz	0.74	88.65	mA	*3 When all peripheral clocks are ON
						0.73	74.65	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FSYNDN.SD = 000)

*6: With data access to a main flash memory.

*7: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

*8: Data access is nothing to VFLASH memory

Table 12-6 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4 (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep *5,*6 operation (PLL)	160 MHz	103	181	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
				144 MHz	98	175	mA	
				120 MHz	91	168	mA	
				100 MHz	86	162	mA	
				80 MHz	80	155	mA	
				60 MHz	74	149	mA	
				40 MHz	69	143	mA	
				20 MHz	63	137	mA	
				8 MHz	59	132	mA	
				4 MHz	58	131	mA	
			Sleep *5,*6 operation (PLL)	160 MHz	24	91	mA	*3 When all peripheral clocks are OFF
				144 MHz	22	89	mA	
				120 MHz	19	86	mA	
				100 MHz	16	83	mA	
				80 MHz	14	81	mA	
				60 MHz	11	78	mA	
				40 MHz	9	76	mA	
				20 MHz	6	73	mA	
				8 MHz	5	72	mA	
				4 MHz	4	71	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*6: Data access is nothing to VFLASH memory

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency*4 (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep *5,*6 operation (PLL)	72 MHz	84	160	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
				60 MHz	80	155	mA	
				48 MHz	75	150	mA	
				36 MHz	71	145	mA	
				24 MHz	67	141	mA	
				12 MHz	63	137	mA	
				8 MHz	61	134	mA	
				4 MHz	60	133	mA	
				72 MHz	15	82	mA	*3 When all peripheral clocks are OFF
				60 MHz	13	80	mA	
				48 MHz	12	79	mA	
				36 MHz	10	77	mA	
				24 MHz	8	75	mA	
				12 MHz	7	74	mA	
				8 MHz	6	73	mA	
				4 MHz	5	72	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*6: Data access is nothing to VFLASH memory

Table 12-8 Typical and Maximum Current Consumption in Sleep Operation (other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4 (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep *6 operation (built-in High-speed CR)	4 MHz	56	126	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
					2	72	mA	*3 When all peripheral clocks are OFF
			Sleep *5,*6 operation (Sub oscillation)	32 kHz	0.52	69.65	mA	*3 When all peripheral clocks are ON
					0.51	69.65	mA	*3 When all peripheral clocks are OFF
			Sleep *6 operation (built-in Low-speed CR)	100 kHz	0.54	70.65	mA	*3 When all peripheral clocks are ON
					0.52	69.65	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

*6: Data access is nothing to VFLASH memory

Table 12-9 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	Stop mode	-	0.41	2.07	mA	*3, *4 T_A=+25°C
					-	21.35	mA	*3, *4 T_A=+85°C
					-	30.57	mA	*3, *4 T_A=+105°C
	I_{CCT}		Timer mode (built-in High-speed CR)	4 MHz	1.14	2.8	mA	*3, *4 T_A=+25°C
					-	22.08	mA	*3, *4 T_A=+85°C
					-	31.3	mA	*3, *4 T_A=+105°C
			Timer mode *5 (Sub oscillation)	32 kHz	0.43	2.09	mA	*3, *4 T_A=+25°C
					-	21.37	mA	*3, *4 T_A=+85°C
					-	30.59	mA	*3, *4 T_A=+105°C
			Timer mode (built-in Low-speed CR)	100 kHz	0.43	2.09	mA	*3, *4 T_A=+25°C
					-	21.37	mA	*3, *4 T_A=+85°C
					-	30.59	mA	*3, *4 T_A=+105°C
	I_{CCR}		RTC mode (Sub oscillation)	32 kHz	0.41	2.07	mA	*3, *4 T_A=+25°C
					-	21.35	mA	*3, *4 T_A=+85°C
					-	30.57	mA	*3, *4 T_A=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=3.6 V

*3: When all ports are fixed.

*4: When LVD is OFF

*5: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

Table 12-10 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode and VBAT

Parameter	Symbol	Pin Name	Conditions	Frequency (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCHD}	VCC	Deep Standby Stop mode (When RAM is OFF)	-	108	173	µA	*3, *4 T_A=+25°C
					-	1774	µA	*3, *4 T_A=+85°C
					-	2208	µA	*3, *4 T_A=+105°C
			Deep Standby Stop mode (When RAM is ON)	-	112	177	µA	*3, *4 T_A=+25°C
					-	1778	µA	*3, *4 T_A=+85°C
					-	2212	µA	*3, *4 T_A=+105°C
	I_{CCRD}		Deep Standby RTC mode (When RAM is OFF)	32 kHz	109	174	µA	*3, *4 T_A=+25°C
					-	1771	µA	*3, *4 T_A=+85°C
					-	2205	µA	*3, *4 T_A=+105°C
			Deep Standby RTC mode (When RAM is ON)		113	178	µA	*3, *4 T_A=+25°C
					-	1775	µA	*3, *4 T_A=+85°C
					-	2209	µA	*3, *4 T_A=+105°C
	I_{CCVBAT}	VBAT	RTC stop *8	-	0.009	0.032	µA	*3, *4, *5 T_A=+25°C
					-	0.994	µA	*3, *4, *5 T_A=+85°C
					-	1.491	µA	*3, *4, *5 T_A=+105°C
			RTC *6, *8 operation		1.0	1.636	µA	*3, *4 T_A=+25°C
					-	2.828	µA	*3, *4 T_A=+85°C
					-	4.242	µA	*3, *4 T_A=+105°C
			RTC *7, *8 operation		0.7	1.153	µA	*3, *4 T_A=+25°C
					-	2.277	µA	*3, *4 T_A=+85°C
					-	3.416	µA	*3, *4 T_A=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=3.6 V

*3: When all ports are fixed.

*4: When LVD is OFF

*5: When sub oscillation is OFF

*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit) When the Standard setting (CCS/CCB=11001110)

*7: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit) When the low power setting (CCS/CCB=00000100)

*8: In the case of setting RTC after VCC power on

Table 12-11 Typical and Maximum Current Consumption in Low-voltage Detection Circuit, Main Flash Memory Write/erase, VFLASH Memory

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	-	4	7	µA	For occurrence of interrupt
Main flash memory write/erase current	$I_{CCFLASH}$		At Write/Erase	-	13.4	15.8	mA	
VFLASH memory Standby current	$I_{CCVFLASH}$		At Standby	-	15	35	µA	
VFLASH memory Read current			At Read	-	9	14	mA	40MHz
					13	20		80MHz
VFLASH memory write/erase current			At Write/Erase	-	20	25	mA	

Peripheral Current Dissipation

Clock system	Peripheral		Unit	Frequency (MHz)			Unit	Remarks
				40	80	160		
HCLK	GPIO		All ports	0.30	0.60	1.19	mA	T_A=+25°C, V_{CC}=3.3 V
	DMAC		-	0.99	1.95	3.82		
	DSTC		-	0.41	0.83	1.61		
	External bus I/F		-	0.18	0.35	0.70		
	SD card I/F		-	0.52	1.02	2.03		
	USB		1ch.	0.47	0.93	1.85		
	I^2S		1 unit	0.36	0.71	1.42		
	Programmable CRC		-	0.04	0.09	0.18		
PCLK1	Base timer		4ch.	0.20	0.39	0.76	mA	T_A=+25°C, V_{CC}=3.3 V
	Multi-functional timer/PPG		1unit/4ch.	0.61	1.21	2.40		
	Quadrature position/Revolution counter		1ch.	0.04	0.09	0.18		
	A/DC		1 unit	0.25	0.50	1.00		
PCLK2	Multi-function serial		1ch.	0.44	0.88	-	mA	T_A=+25°C, V_{CC}=3.3 V
GECLK	GDC unit	GDC	1 unit	31	57	109	mA	T_A=+25°C, V_{CC}=3.3 V
		High-Speed Quad SPI	1ch.	1.1	2.3	-		
		HyperBus I/F	1 unit	0.6	1.2	-		
		SDRAM-IF	1ch.	2.3	4.6	-		

12.3.2 Pin Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
		5 V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
		TTL Schmitt input pin	-	2.0	-	V_{CC}+0.3	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		5 V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
		TTL Schmitt input pin	-	V_{SS} - 0.3	-	0.8	V	
H level output voltage	V_{OH}	2 mA type	I_{OH} = - 2 mA	V_{CC} - 0.5	-	V_{CC}	V	
		4 mA type	I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
		8 mA type	I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
		11 mA type	I_{OH} = - 11 mA	V_{CC} - 0.5	-	V_{CC}	V	High-speed IO
		The pin doubled as USB I/O	I_{OH} = - 13.0 mA	V_{CC} - 0.4	-	V_{CC}	V	
		The pin doubled as I^2C Fm+	I_{OH} = - 3 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO
L level output voltage	V_{OL}	2 mA type	I_{OL} = 2 mA	V_{SS}	-	0.4	V	
		4 mA type	I_{OL} = 4 mA	V_{SS}	-	0.4	V	
		8 mA type	I_{OL} = 8 mA	V_{SS}	-	0.4	V	
		11 mA type	I_{OL} = 11 mA	V_{SS}	-	0.4	V	
		The pin doubled as USB I/O	I_{OL} = 10.5 mA	V_{SS}	-	0.4	V	
		The pin doubled as I^2C Fm+	I_{OL} = 3 mA	V_{SS}	-	0.4	V	At GPIO
			I_{OL} = 20 mA					At I^2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	-	30	80	200	kΩ	
			-	15	33	70		High-speed IO
Input capacitance	C_{IN}	Other than VCC, VBAT, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

12.4 AC Characteristics

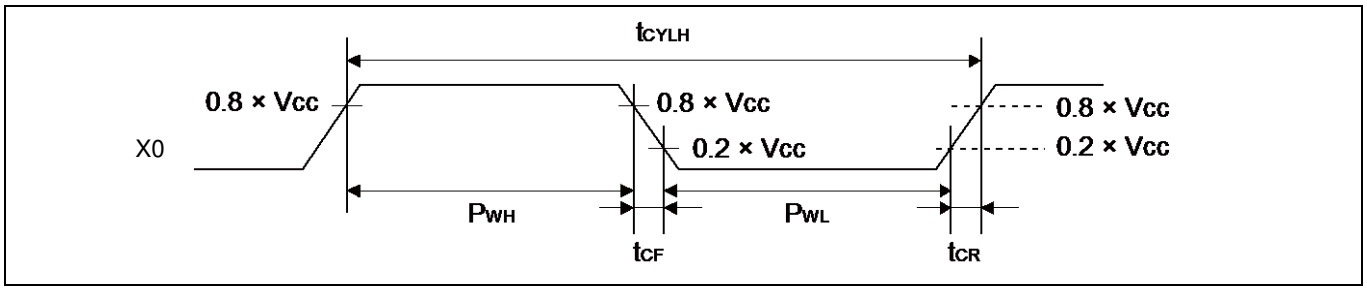
12.4.1 Main Clock Input Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	-	4	20	MHz	When crystal oscillator is connected
			-	4	20	MHz	When using external clock
Input clock cycle	t_{CYLH}		-	50	250	ns	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	f_{CM}	-	-	-	160	MHz	Master clock
	f_{CC}	-	-	-	160	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	80	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	160	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	80	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	5	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	10	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	5	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	10	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main part (002-04856).

*2: For about each APB bus which each peripheral is connected to, see Block Diagram in this data sheet.

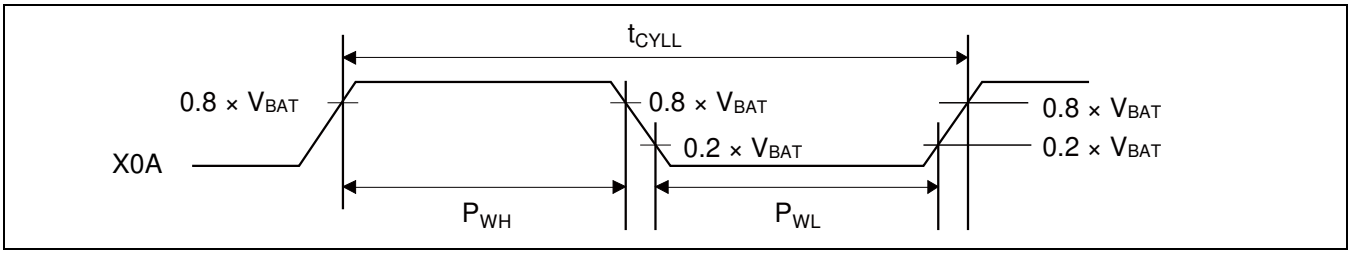


12.4.2 Sub Clock Input Characteristics

(V_{BAT} = 1.65V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected *
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock

*: For more information about crystal oscillator, see Sub crystal oscillator in 9. Handling Devices.



12.4.3 Built-in CR Oscillation Characteristics

Built-in High-speed CR

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_J = - 20 °C to + 105 °C	3.92	4	4.08	MHz	When trimming *1
		T_J = - 40 °C to + 125 °C	3.88	4	4.12		
		T_J = - 40 °C to + 125 °C	2.9	4	5		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency/temperature trimming.

*2: This is the time to stabilize the frequency of High-speed CR clock after setting trimming value. This period is able to use High-speed CR clock as source clock.

Built-in Low-speed CR

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (In the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	200	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1 : Clock in FM4 Family Peripheral Manual Main part (002-04856).

12.4.5 Operating Conditions of USB/I²S/GDC PLL (In the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	USB/GDC
				384	MHz	I²S
USB clock frequency *2	f_{CLKPLL}	-	-	50	MHz	After the M frequency division
I²S clock frequency *3	f_{CLKPLL}	-	-	12.288	MHz	After the M frequency division
GDC clock frequency *4	f_{CLKPLL}	-	-	160	MHz	After divided by GDC part

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about USB clock, see Chapter 2-2: USB Clock Generation in FM4 Family Peripheral Manual Communication Macro part (002-04856).

*3: For more information about I²S clock, see Chapter 7-1: I²S Clock Generation in FM4 Family Peripheral Manual Communication Macro part (002-04856).

*4: For more information about GDC clock, see FM4 Family Peripheral Manual GDC part (002-04917).

12.4.6 Operating Conditions of Main PLL (In the Case of Using Built-in High-Speed CR Clock for Input Clock of Main PLL)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	50	-	95	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	190	-	400	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	160	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main part (002-04856).

Note:

- *The High-speed CR clock (CLKHC) should be set with frequency/temperature trimming to act as the source clock of the Main PLL.*

12.4.7 Reset Input Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.8 Power-on Reset Timing

(V_{SS} = 0V)

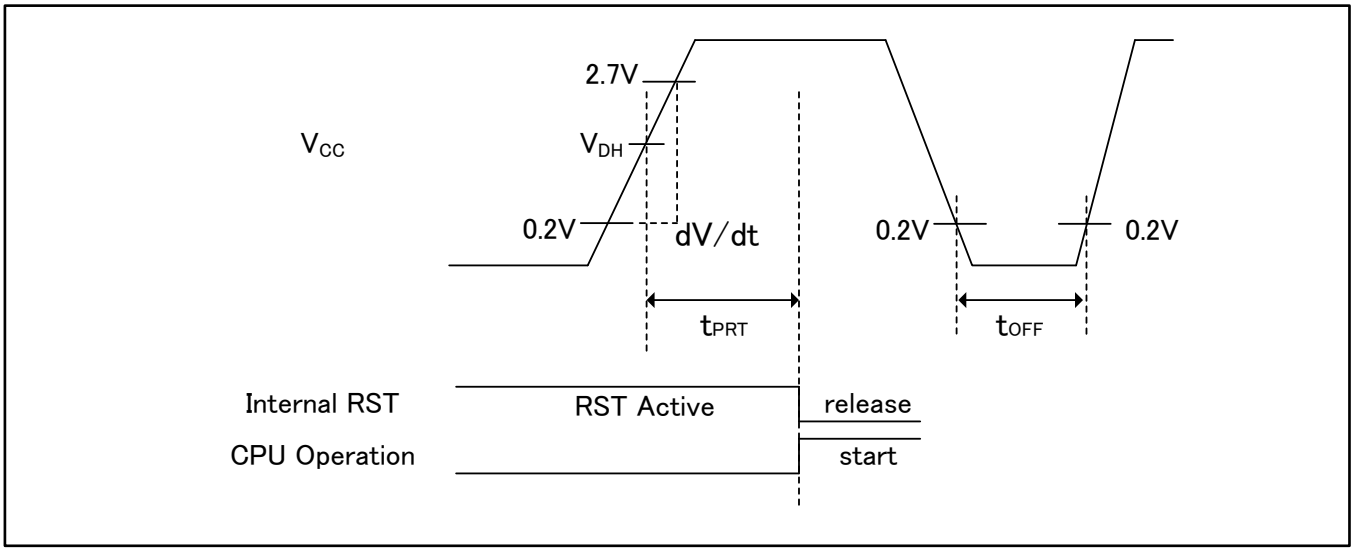
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	V_{CC}	-	1	-	-	ms	*1
Power ramp rate	dV/dt		VCC: 0.2V to 2.70V	0.6	-	1000	mV/µs	*2
Time until releasing Power-on reset	t_{PRT}		-	0.33	-	0.60	ms	

*1: V_{CC} must be held below 0.2V for a minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (tOFF>1ms).

Note:

- *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 7.*



Glossary

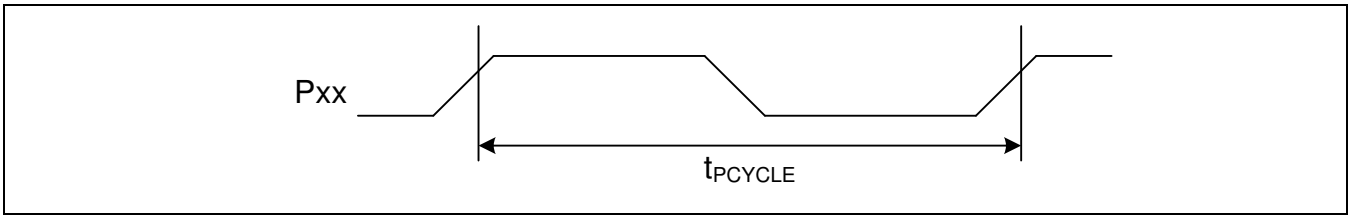
□ VDH: detection voltage of Low Voltage detection reset. See “12.7.Low-Voltage Detection Characteristics”.

12.4.9 GPIO Output Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	t_{PCYCLE}	Pxx*	-	-	32	MHz	

*: GPIO is a target.



12.4.10 External Bus Timing

External Bus Clock Output Characteristics

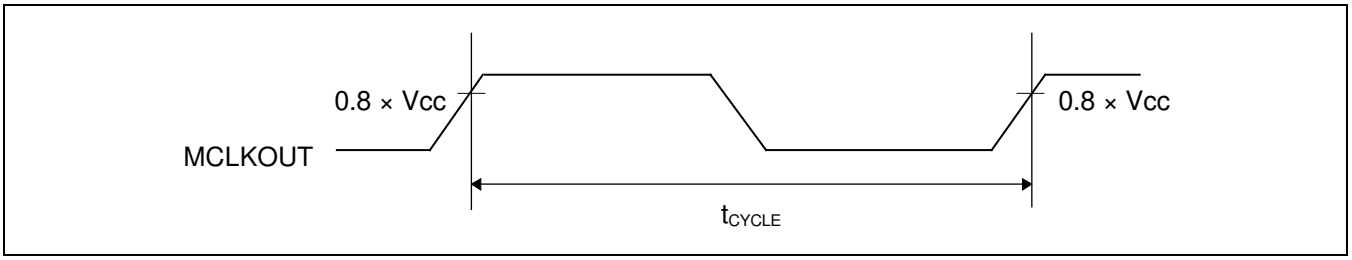
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	t_{CYCLE}	MCLKOUT*1		-	50*2	MHz	

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.

For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main part (002-04856).

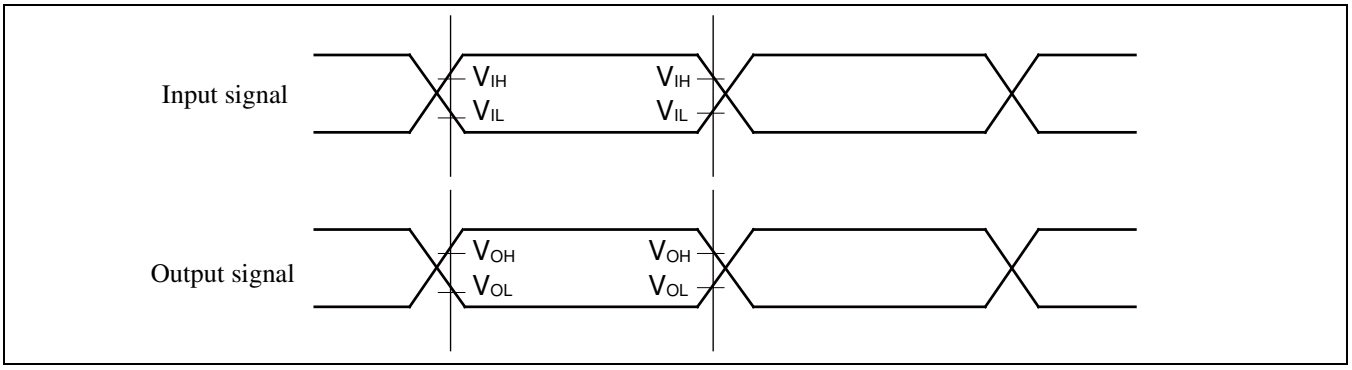
*2: Generate MCLKOUT at setting more than 4 divisions when the AHB bus clock exceeds 100 MHz.



External Bus Signal Input/output Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



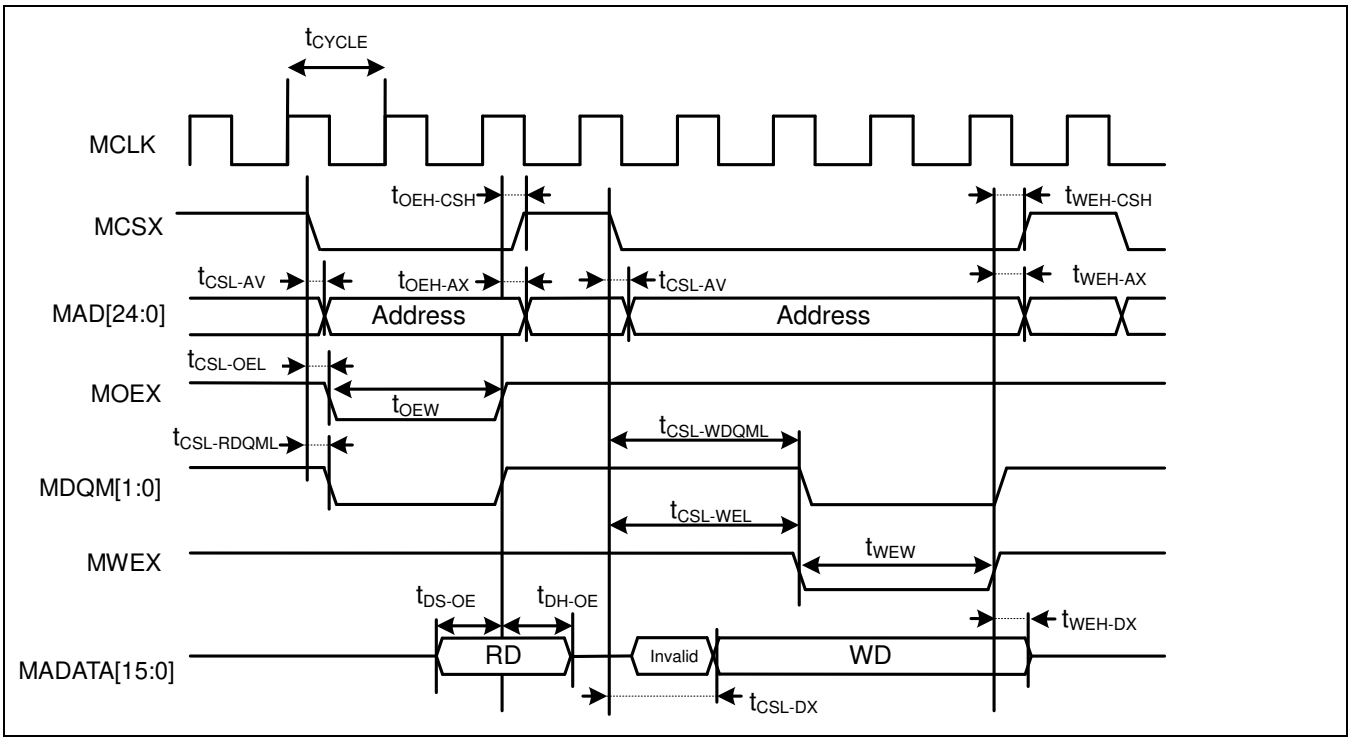
Separate Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MOEX Mininum pulse width	t_{OEW}	MOEX	-	MCLK×n-3	-	ns	
MCSX↓→Address output delay time	t_{CSL-AV}	MCSX, MAD[24:0]	-	-9	+9	ns	
MOEX↑→Address hold time	t_{OEH-AX}	MOEX, MAD[24:0]	-	0	MCLK×m+9	ns	
MCSX↓→ MOEX↓delay time	$t_{CSL-OEL}$	MOEX, MCSX	-	MCLK×m-9	MCLK×m+9	ns	
MOEX↑→ MCSX↑time	$t_{OEH-CSH}$		-	0	MCLK×m+9	ns	
MCSX↓→ MDQM↓delay time	$t_{CSL-RDQML}$	MCSX, MDQM[1:0]	-	MCLK×m-9	MCLK×m+9	ns	
Data setup→ MOEX↑time	t_{DS-OE}	MOEX, MADATA[15:0]	-	20	-	ns	
MOEX↑→ Data hold time	t_{DH-OE}	MOEX, MADATA[15:0]	-	0	-	ns	
MWEX Mininum pulse width	t_{WEW}	MWEX	-	MCLK×n-3	-	ns	
MWEX↑→Address output delay time	t_{WEH-AX}	MWEX, MAD[24:0]	-	0	MCLK×m+9	ns	
MCSX↓→ MWEX↓delay time	$t_{CSL-WEL}$	MWEX, MCSX	-	MCLK×n-9	MCLK×n+9	ns	
MWEX↑→ MCSX↑delay time	$t_{WEH-CSH}$		-	0	MCLK×m+9	ns	
MCSX↓→ MDQM↓delay time	$t_{CSL-WDQML}$	MCSX, MDQM[1:0]	-	MCLK×n-9	MCLK×n+9	ns	
MCSX↓→ Data output time	t_{CSL-DX}	MCSX, MADATA[15:0]	-	MCLK-9	MCLK+9	ns	
MWEX↑→ Data hold time	t_{WEH-DX}	MWEX, MADATA[15:0]	-	0	MCLK×m+9	ns	

Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*


tCYCLE
MCLK
MCSX
tOEH-CSH
tWEH-CSH
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
MAD[24:0]
Address
Address
tCSL-OEL
MOEX
tOEW
tCSL-RDQML
tCSL-WDQML
MDQM[1:0]
tCSL-WEL
tWEW
MWEX
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
MADATA[15:0]
tCSL-DX

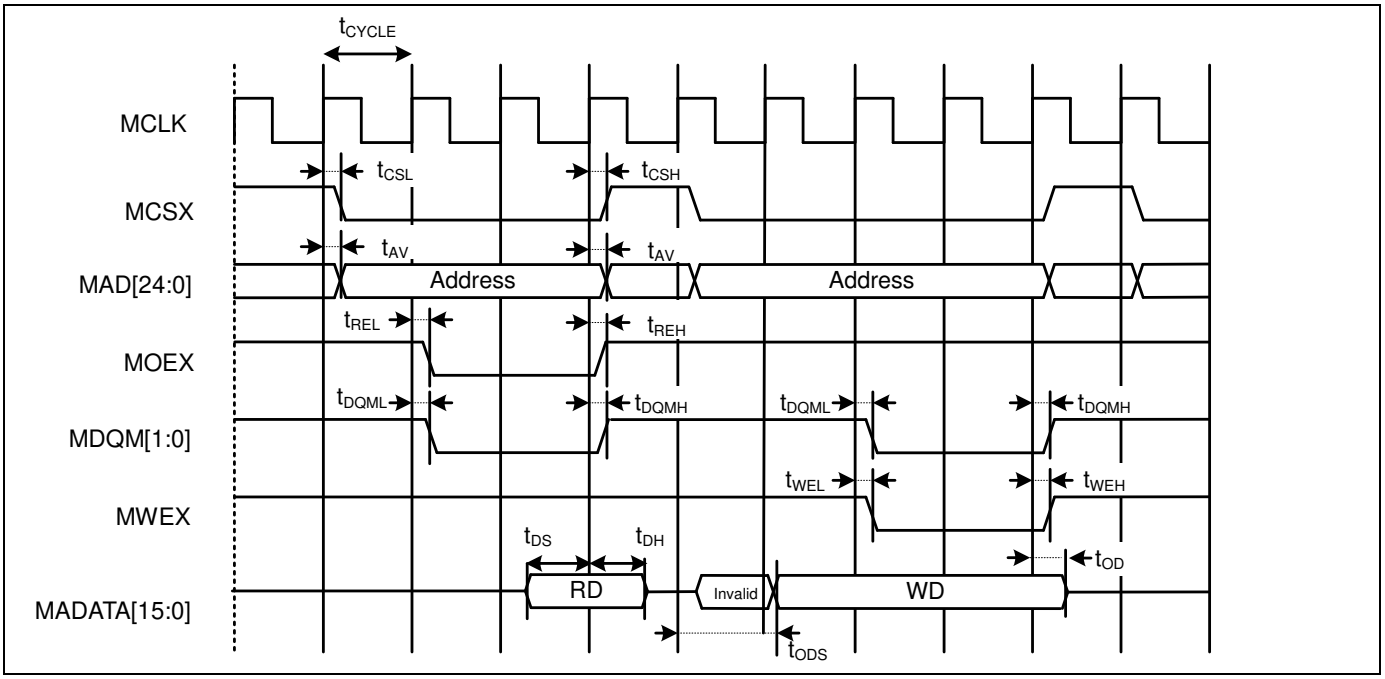
Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	t_{AV}	MCLK, MAD[24:0]	-	1	9	ns	
MCSX delay time	t_{CSL}	MCLK, MCSX	-	1	9	ns	
	t_{CSH}		-	1	9	ns	
MOEX delay time	t_{REL}	MCLK, MOEX	-	1	9	ns	
	t_{REH}		-	1	9	ns	
Data set up →MCLK ↑ time	t_{DS}	MCLK, MADATA[15:0]	-	19	-	ns	
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[15:0]	-	0	-	ns	
MWEX delay time	t_{WEL}	MCLK, MWEX	-	1	9	ns	
	t_{WEH}		-	1	9	ns	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	-	1	9	ns	
	t_{DQMH}		-	1	9	ns	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[15:0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[15:0]	-	1	18	ns	

Note:

- *When the external load capacitance C_L = 30 pF*



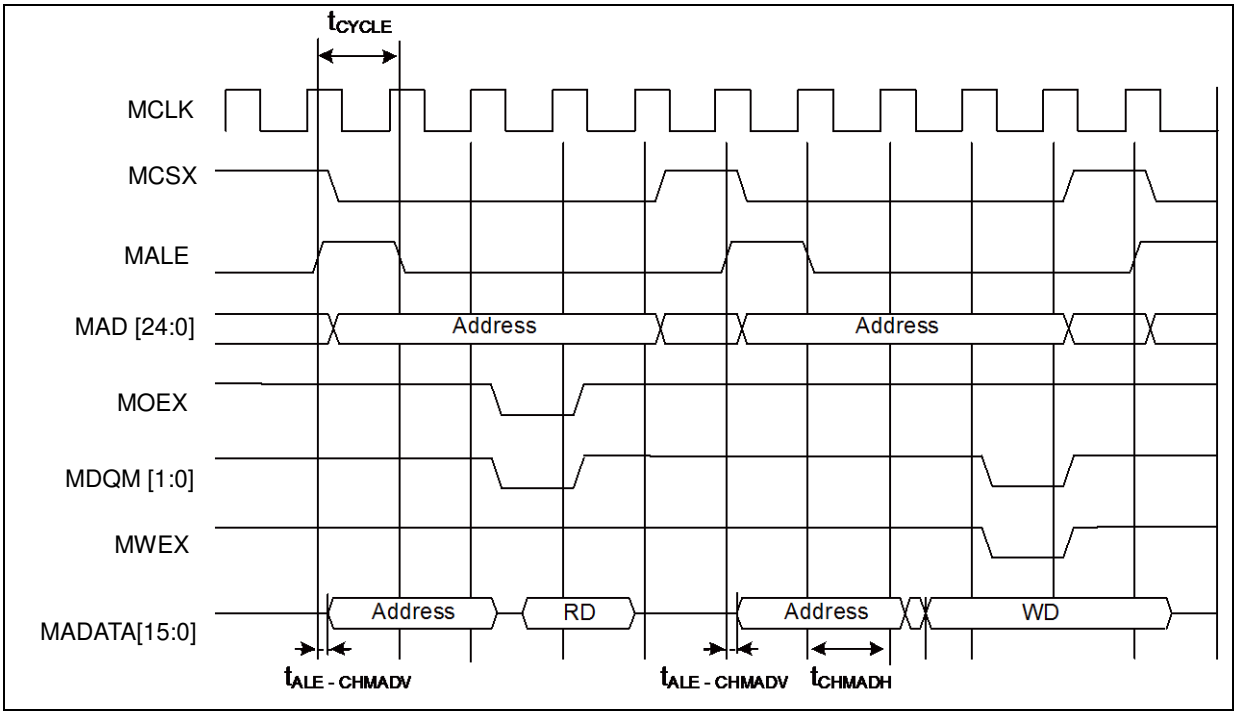
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MAD[24:0]	-	0	10	ns	
Multiplexed address hold time	t_{CHMADH}		-	MCLK×n+0	MCLK×n+10	ns	

Note:

- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*



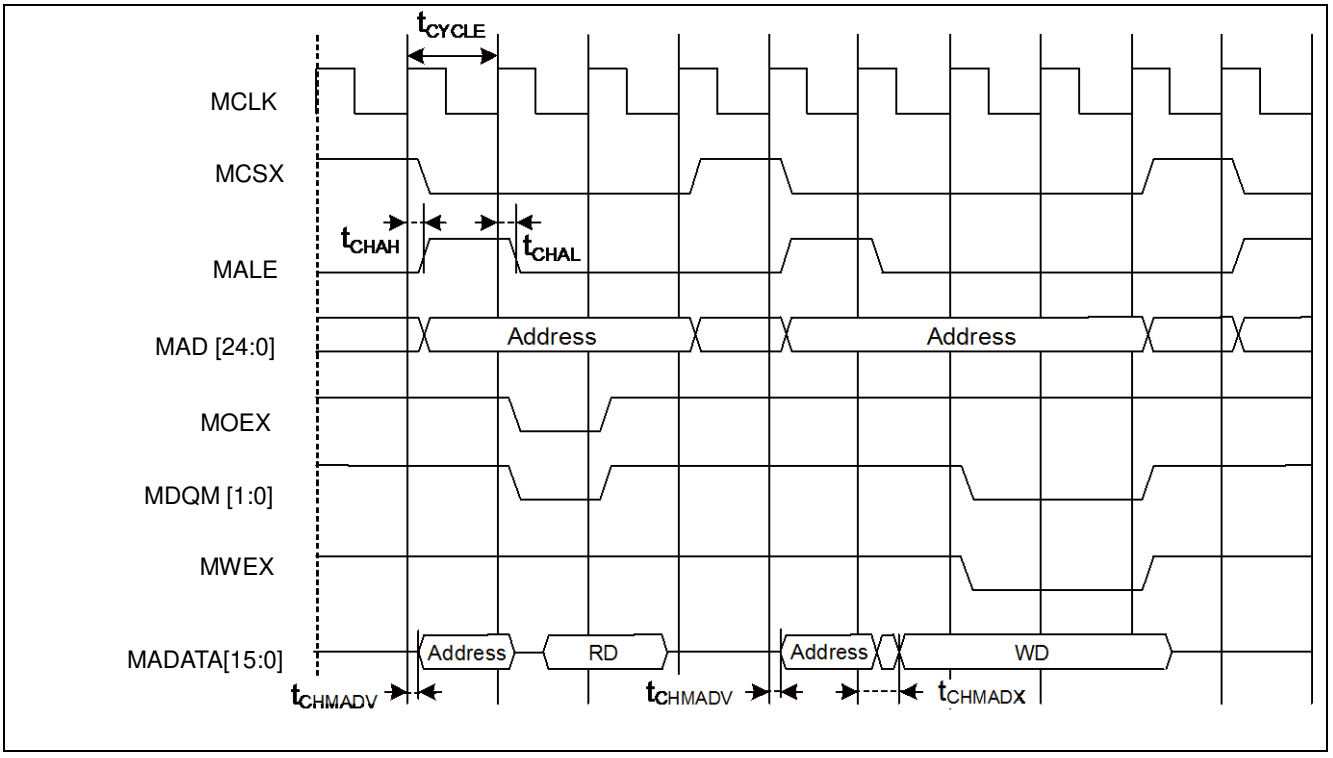
Multiplexed Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK, MALE	-	1	9	ns	
	t_{CHAH}		-	1	9	ns	
MCLK ↑ →Multiplexed address delay time	t_{CHMADV}	MCLK, MADATA[15:0]	-	1	t_{OD}	ns	
MCLK ↑ →Multiplexed data output time	t_{CHMADX}		-	1	t_{OD}	ns	

Note:

- *When the external load capacitance C_L = 30 pF*



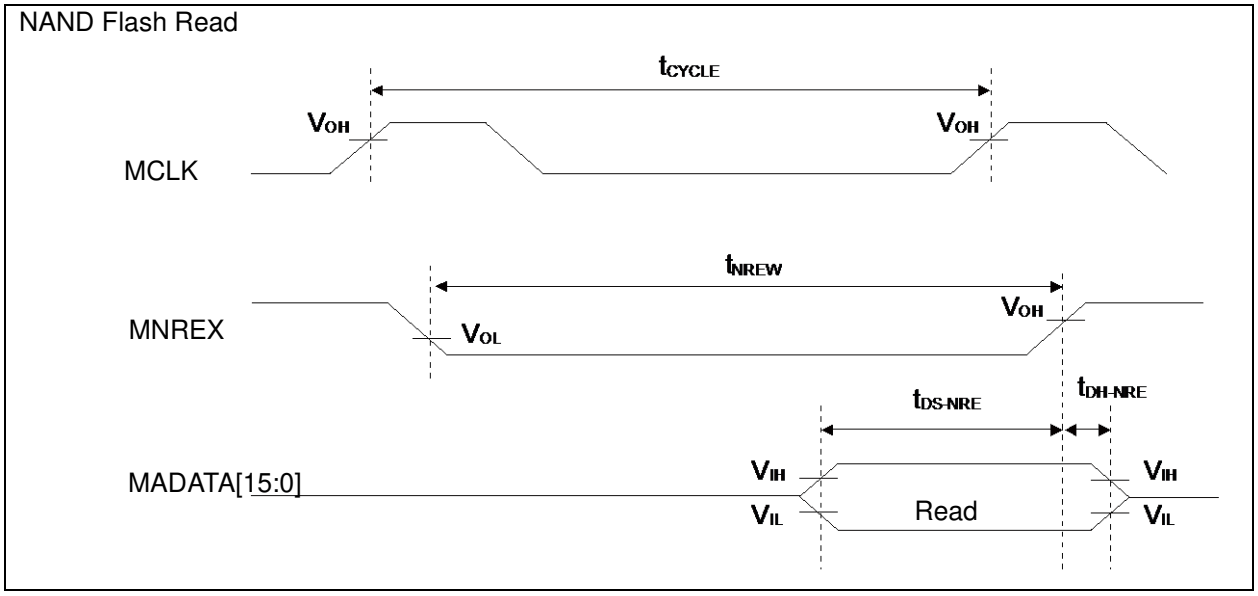
NAND Flash Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

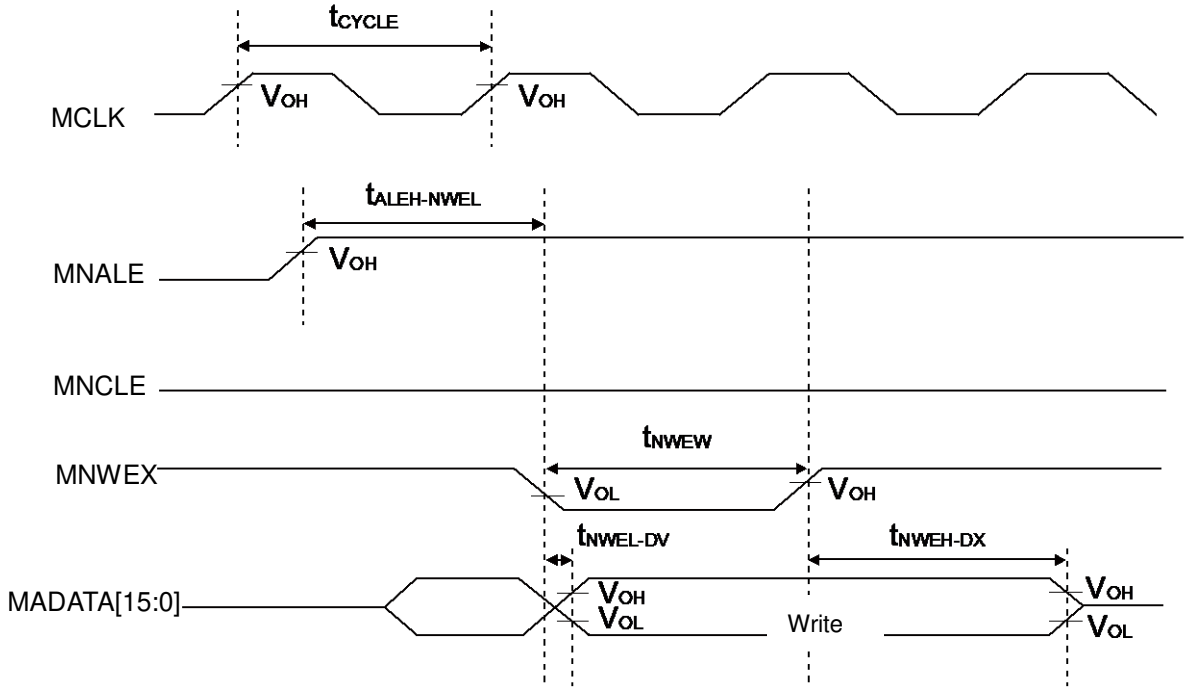
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	t_{NREW}	MNREX	-	MCLK×n-3	-	ns	
Data set up →MNREX ↑ time	t_{DS-NRE}	MNREX, MADATA[15:0]	-	20	-	ns	
MNREX ↑ → Data hold time	t_{DH-NRE}	MNREX, MADATA[15:0]	-	0	-	ns	
MNALE ↑ → MNWEX delay time	$t_{ALEH-NWEL}$	MNALE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNALE ↓ → MNWEX delay time	$t_{ALEL-NWEL}$	MNALE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNCLE ↑ → MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE, MNWEX	-	MCLK×m-9	MCLK×m+9	ns	
MNWEX ↑ → MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE, MNWEX	-	0	MCLK×m+9	ns	
MNWEX Min pulse width	t_{NWEW}	MNWEX	-	MCLK×n-3	-	ns	
MNWEX ↓ → Data output time	$t_{NWEL-DV}$	MNWEX, MADATA[15:0]	-	-9	9	ns	
MNWEX ↑ → Data hold time	$t_{NWEH-DX}$	MNWEX, MADATA[15:0]	-	0	MCLK×m+9	ns	

Note:

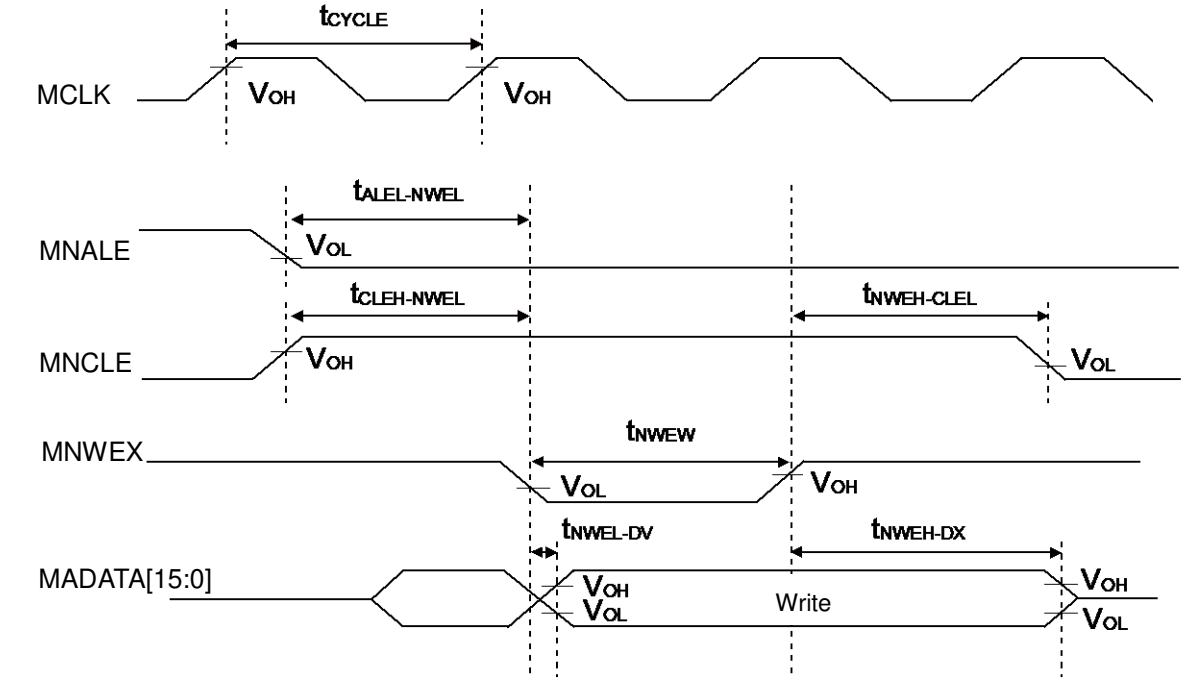
- *When the external load capacitance C_L = 30 pF (m=0 to 15, n=1 to 16)*



NAND Flash Address Write



NAND Flash Command Write

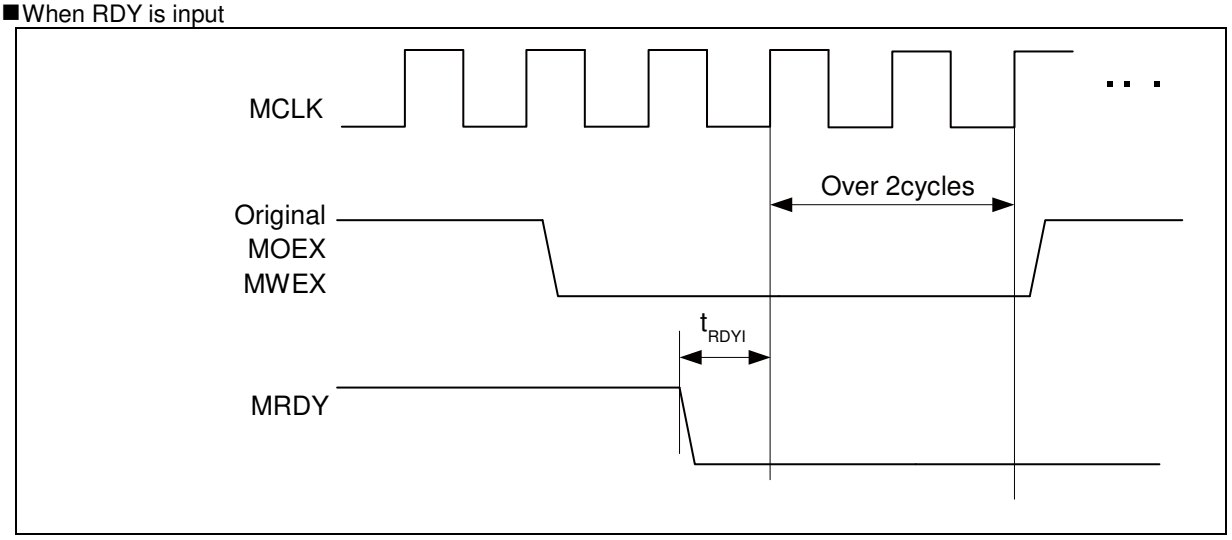


External Ready Input Timing

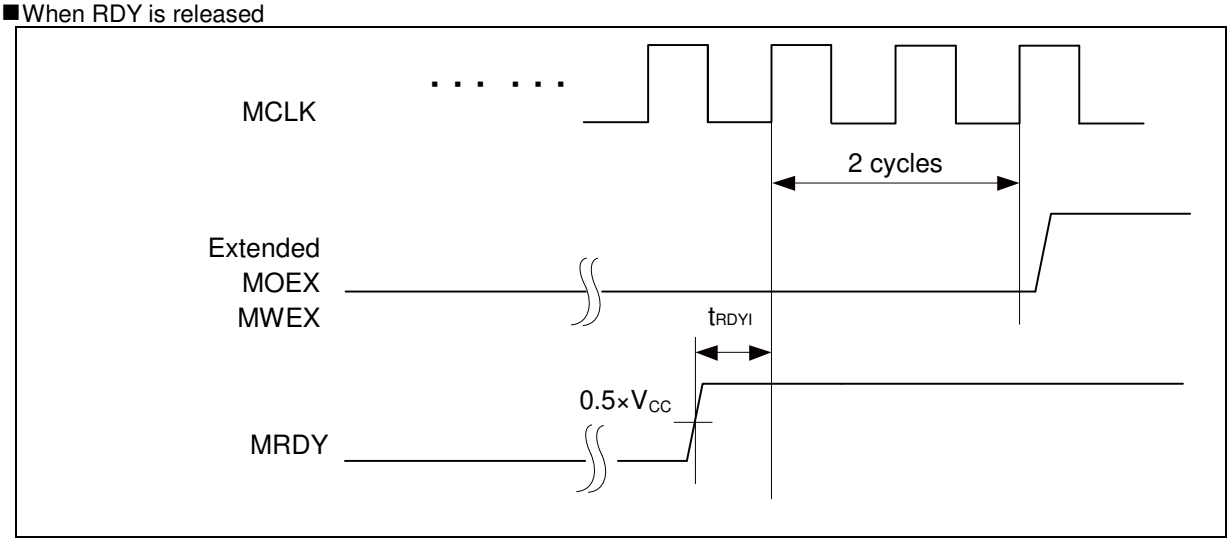
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	-	19	-	ns	

■When RDY is input



■When RDY is released



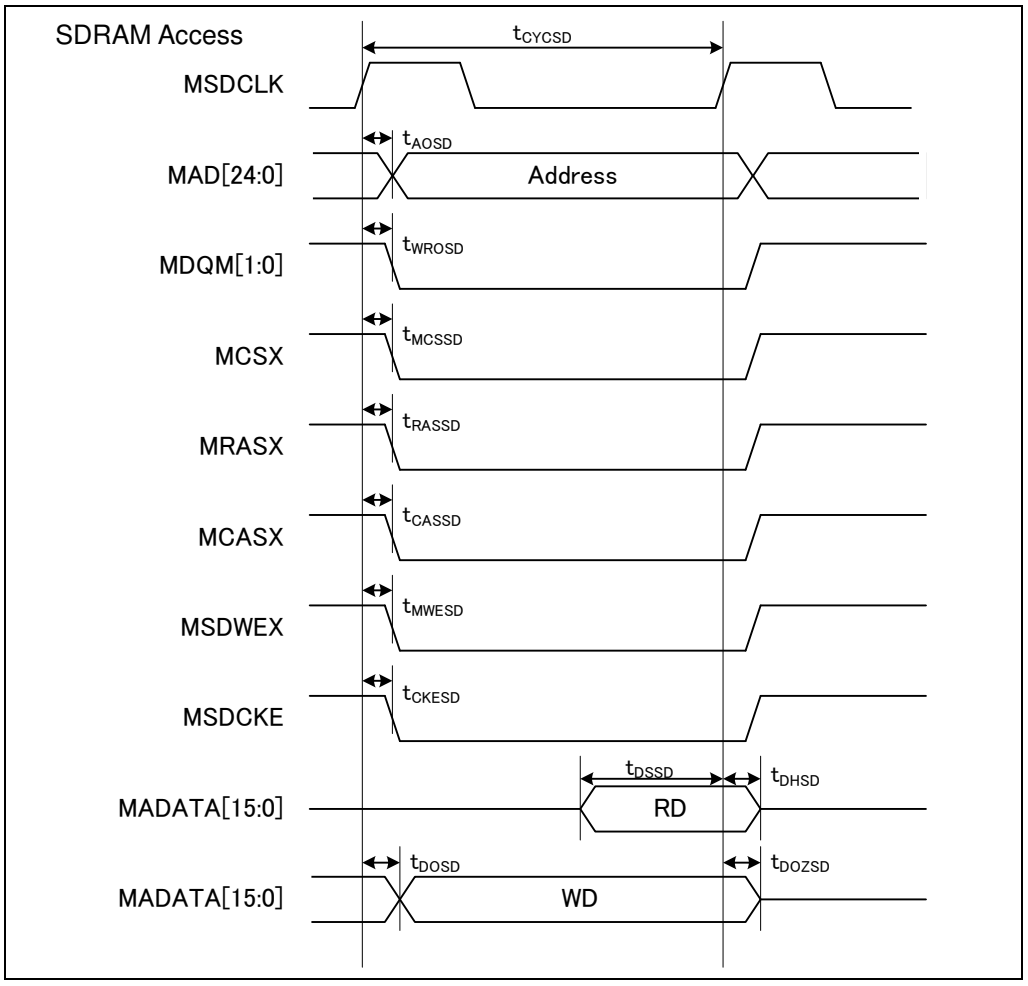
SDRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Value	Unit		Unit	Remarks
				Min	Max		
Output frequency	t_{CYCSD}	MSDCLK	-	-	50	MHz	
Address delay time	t_{AOSD}	MSDCLK, MAD[15:0]	-	2	12	ns	
MSDCLK ↑ → Data output delay time	t_{DOSD}	MSDCLK, MADATA[15:0]	-	2	12	ns	
MSDCLK ↑ → Data output Hi-Z time	t_{DOZSD}	MSDCLK, MADATA[15:0]	-	2	19.5	ns	
MDQM[1:0] delay time	t_{WROSD}	MSDCLK, MDQM[1:0]	-	1	12	ns	
MCSX delay time	t_{MCSSD}	MSDCLK, MCSX8	-	2	12	ns	
MRASX delay time	t_{RASSD}	MSDCLK, MRASX	-	2	12	ns	
MCASX delay time	t_{CASSD}	MSDCLK, MCASX	-	2	12	ns	
MSDWEX delay time	t_{MWESD}	MSDCLK, MSDWEX	-	2	12	ns	
MSDCKE delay time	t_{CKESD}	MSDCLK, MSDCKE	-	2	12	ns	
Data setup time	t_{DSSD}	MSDCLK, MADATA[15:0]	-	19	-	ns	
Data hold time	t_{DHSD}	MSDCLK, MADATA[15:0]	-	0	-	ns	

Note:

- *When the external load capacitance C_L = 30 pF*

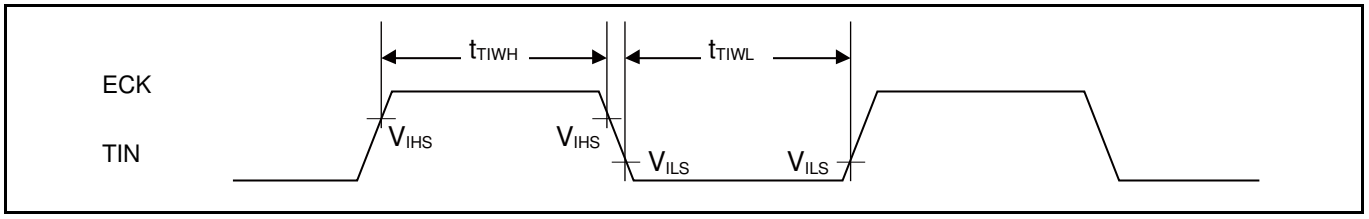

SDRAM Access
tCYCSD
MSDCLK
tAOSD
MAD[24:0]
Address
tWROSD
MDQM[1:0]
tMCSSD
MCSX
tRASSD
MRASX
tCASSD
MCASX
tMWESD
MSDWEX
tCKESD
MSDCKE
tDSSD
tDHSD
MADATA[15:0]
RD
tDOSD
tDOZSD
MADATA[15:0]
WD

12.4.11 Base Timer Input Timing

Timer Input Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

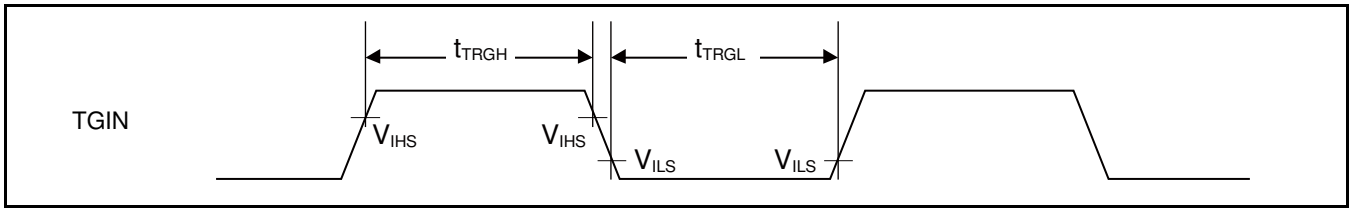
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger Input Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which the Base Timer is connected to, see 8. Block Diagram in this data sheet.

12.4.12 CSIO Timing

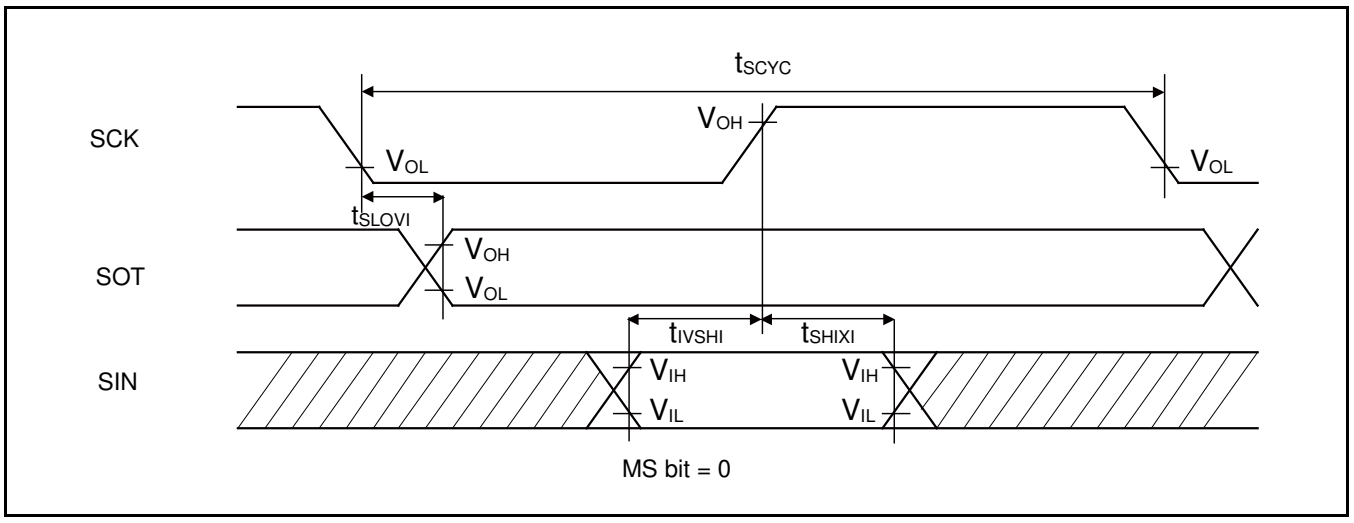
Synchronous Serial (SPI = 0, SCINV = 0)

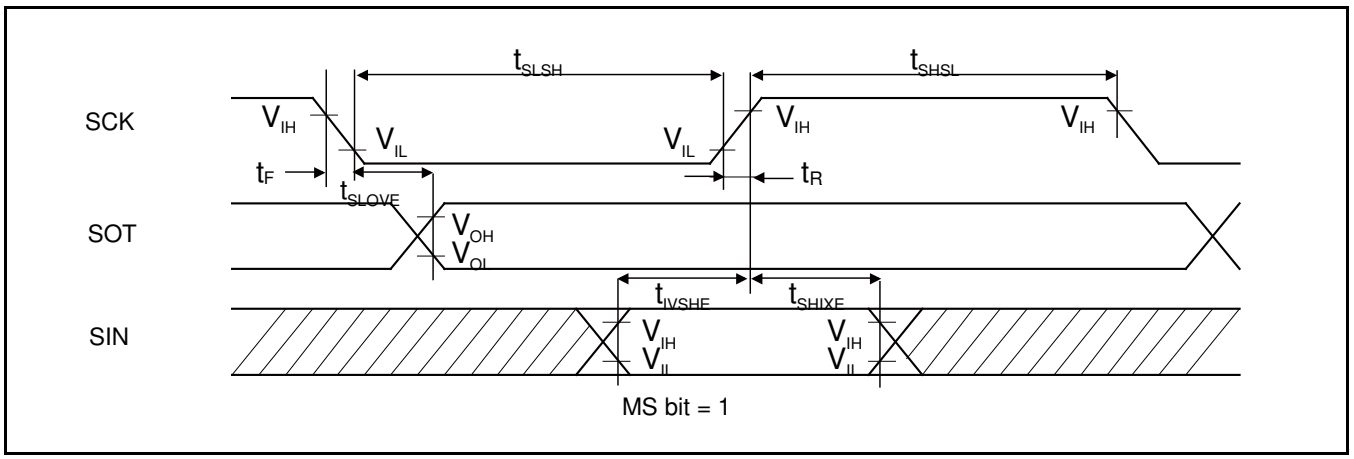
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Baud rate	-	-		-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*


tSCYC
SCK
VOH
VOL
VOL
tSLOVI
SOT
VOH
VOL
tIVSHI
tSHIXI
SIN
VIH
VIL
VIH
VIL
MS bit = 0


tSLSH
tSHSL
SCK
VIH
VIL
VIL
VIH
VIH
tF
tR
tSLOVE
SOT
VOH
VOL
tIVSHE
tSHIXE
SIN
VIH
VIL
VIH
VIL
MS bit = 1

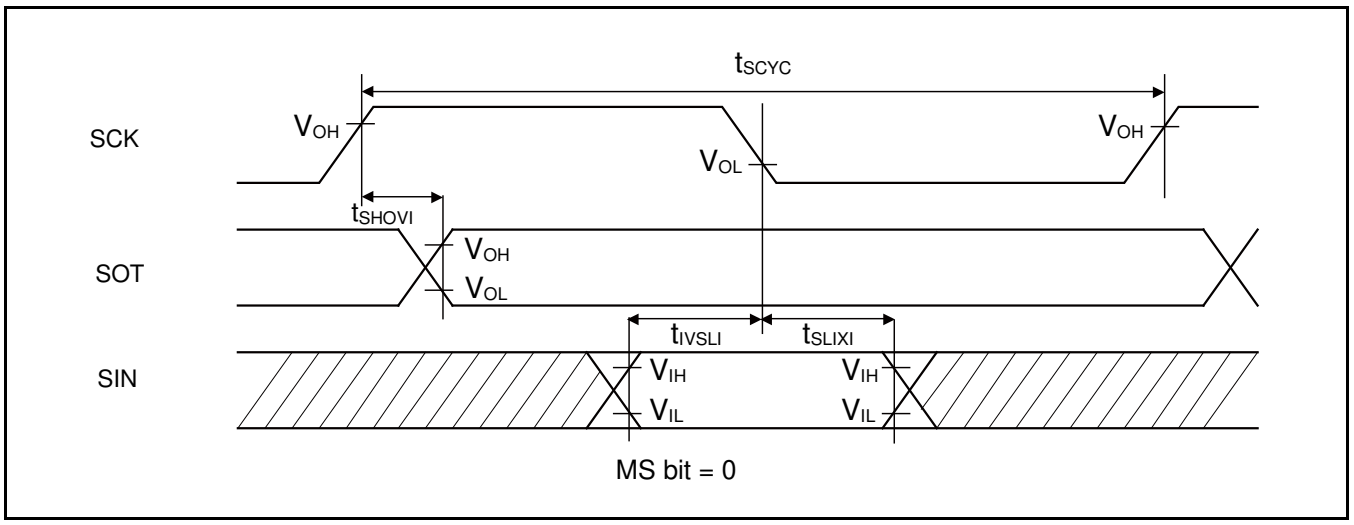
Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

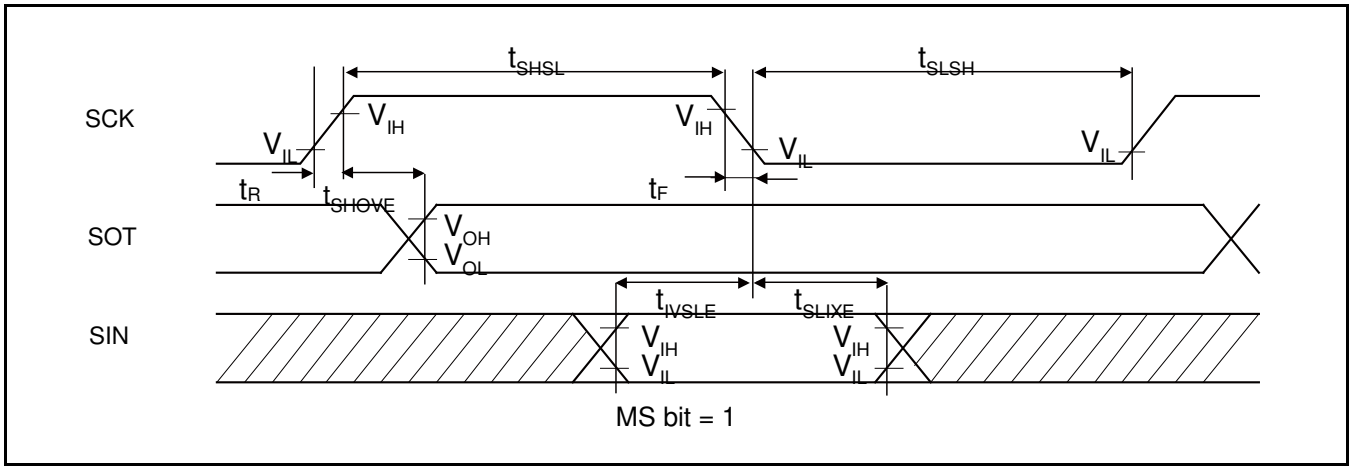
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Baud rate	-	-	-	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

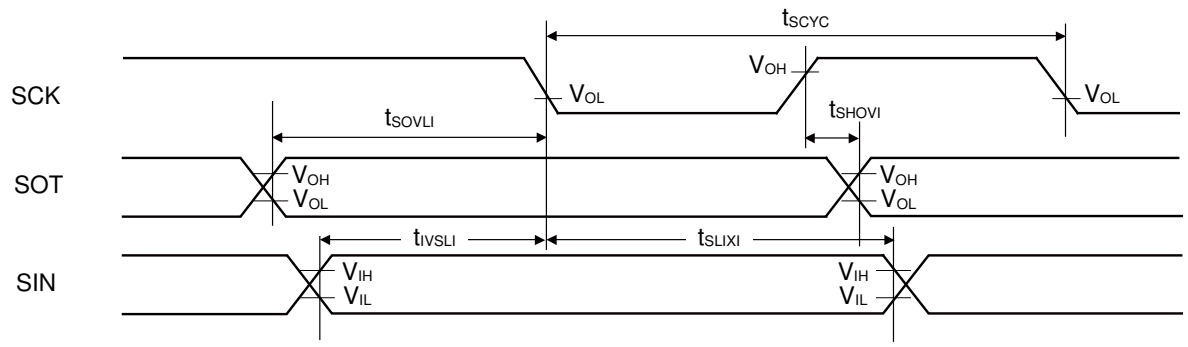
Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

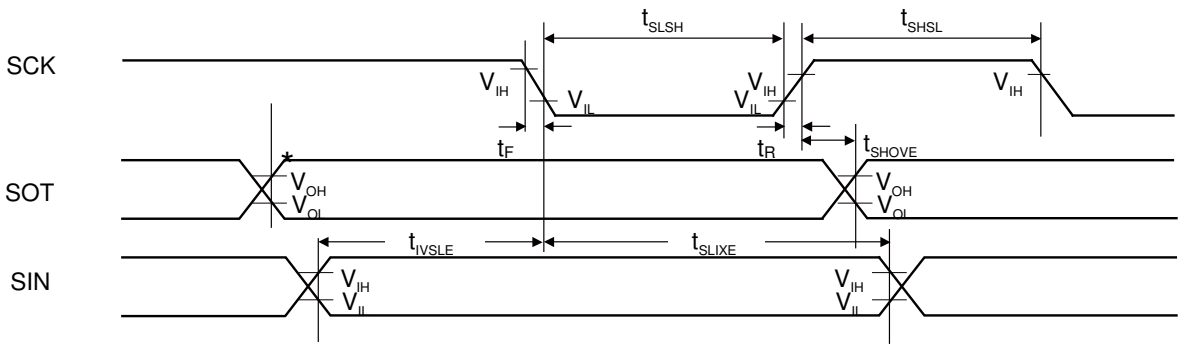
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Baud rate	-	-	-	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

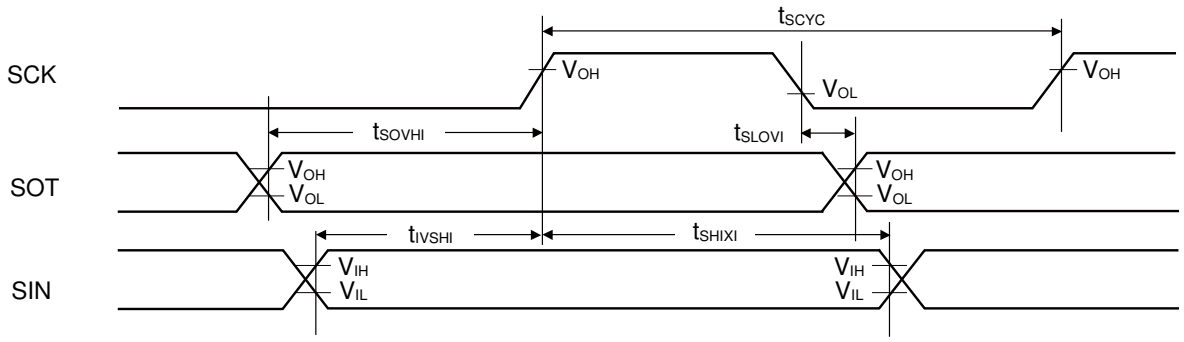
Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

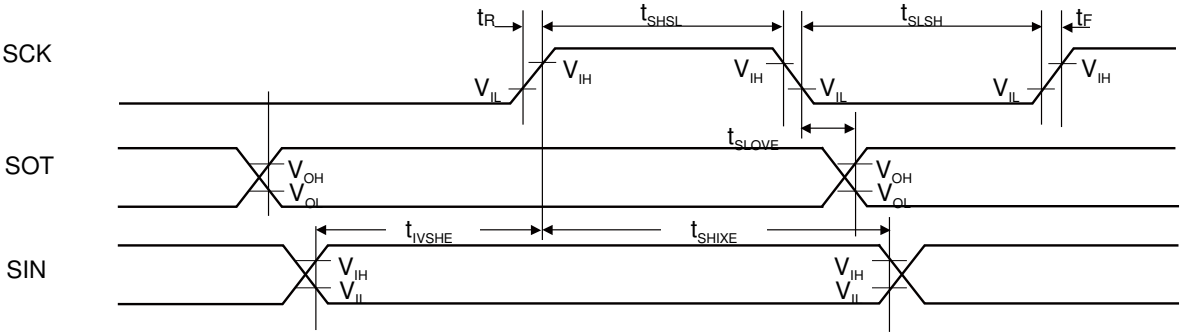
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Baud rate	-	-	-	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL=1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50+5t_{CYCP}	(*3)+50+5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	ns

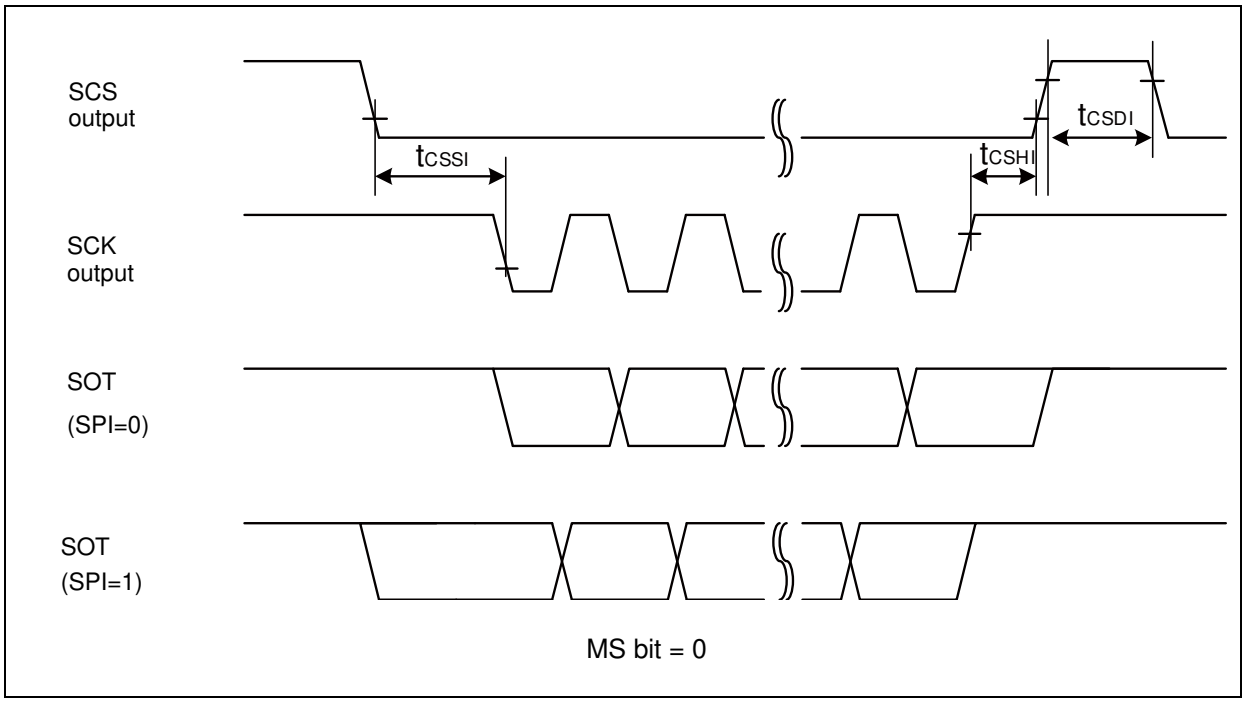
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

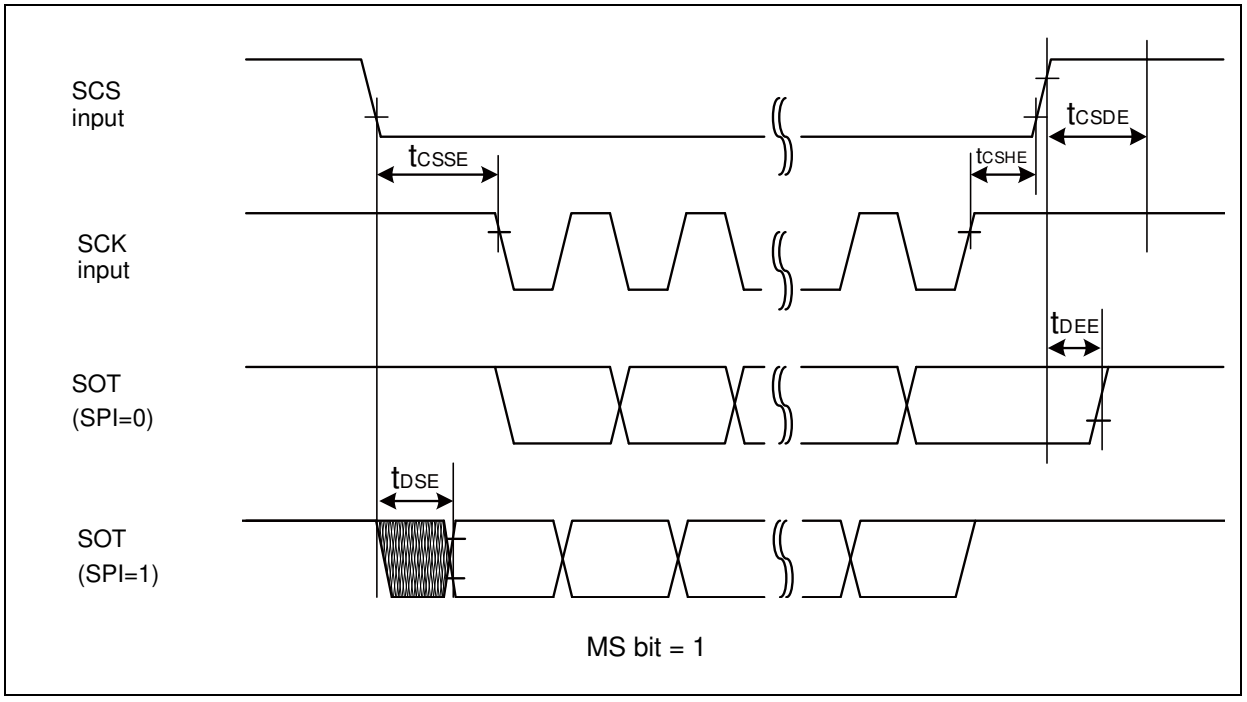
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL=1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↓→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50+5t_{CYCP}	(*3)+50+5t_{CYCP}	ns
SCS↓→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	ns

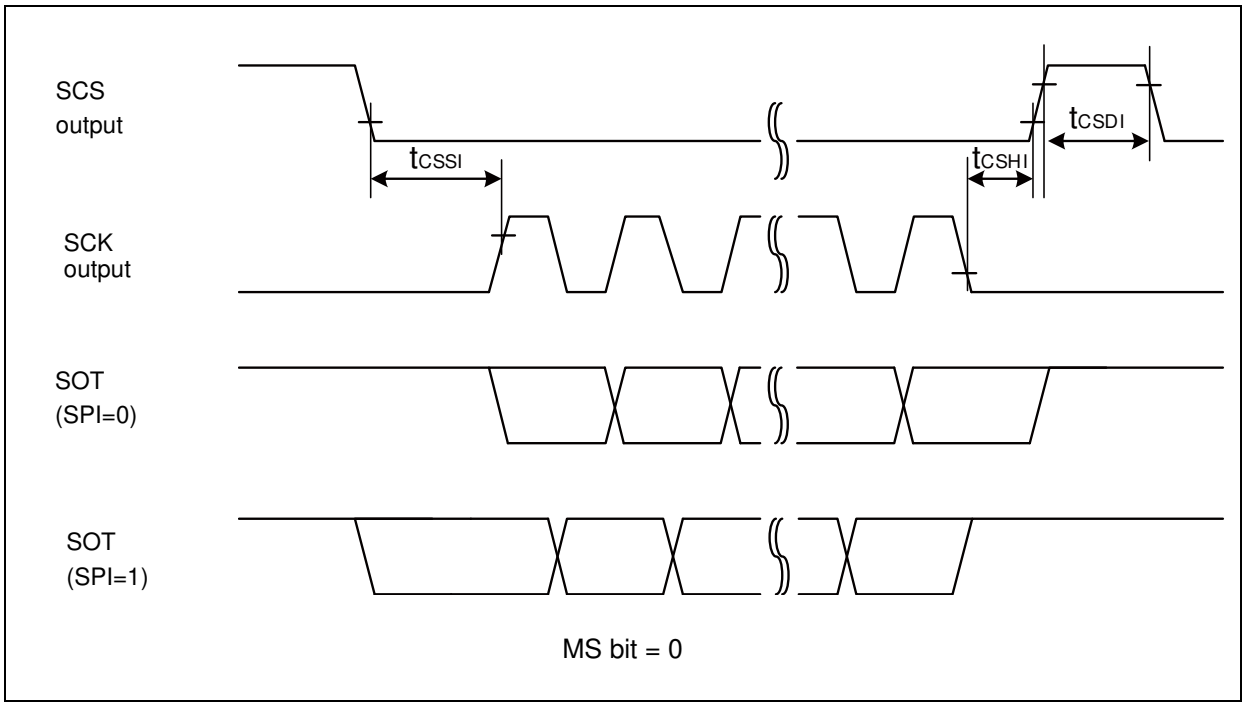
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

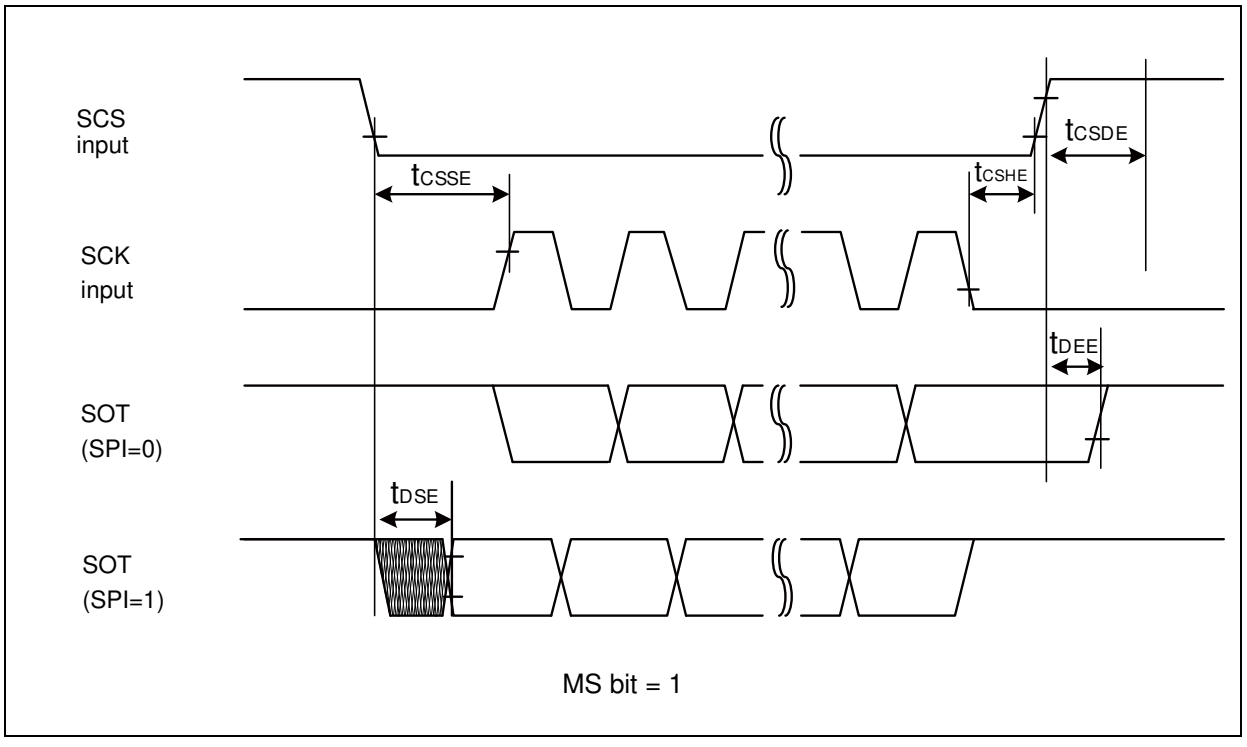
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL=0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50+5t_{CYCP}	(*3)+50+5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	ns

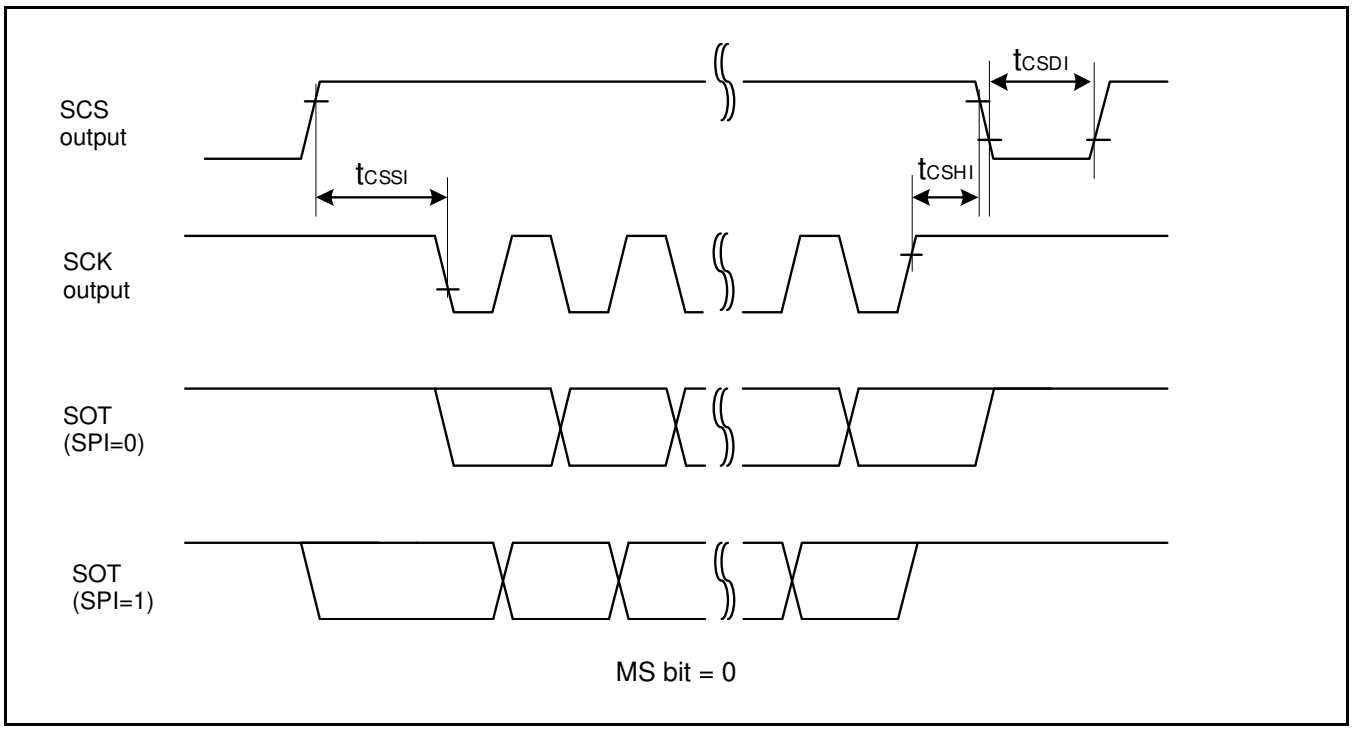
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

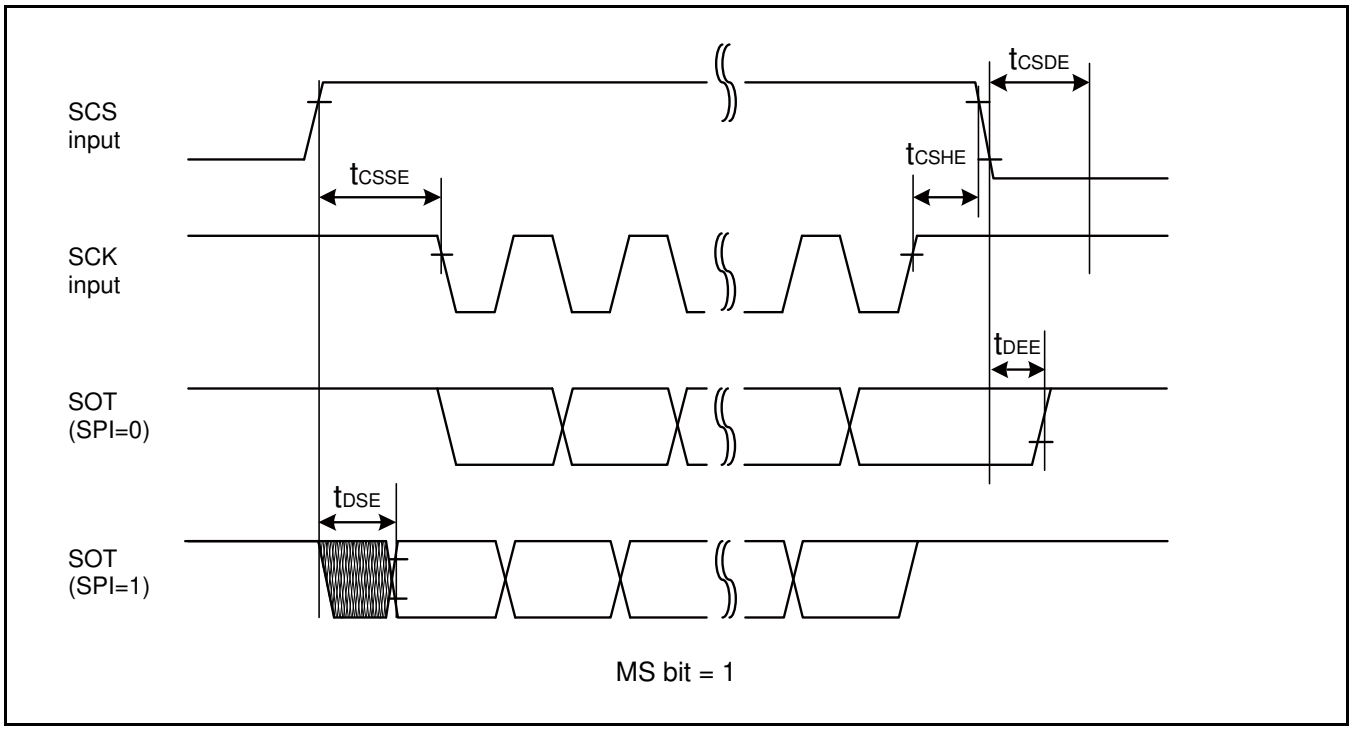
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*


SCS
output
SCK
output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSHI
tCSDI
MS bit = 0


SCS
input
SCK
input
SOT
(SPI=0)
SOT
(SPI=1)
tCSSE
tCSHE
tCSDE
tDEE
tDSE
MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL=0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50+5t_{CYCP}	(*3)+50+5t_{CYCP}	ns
SCS↑→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	ns

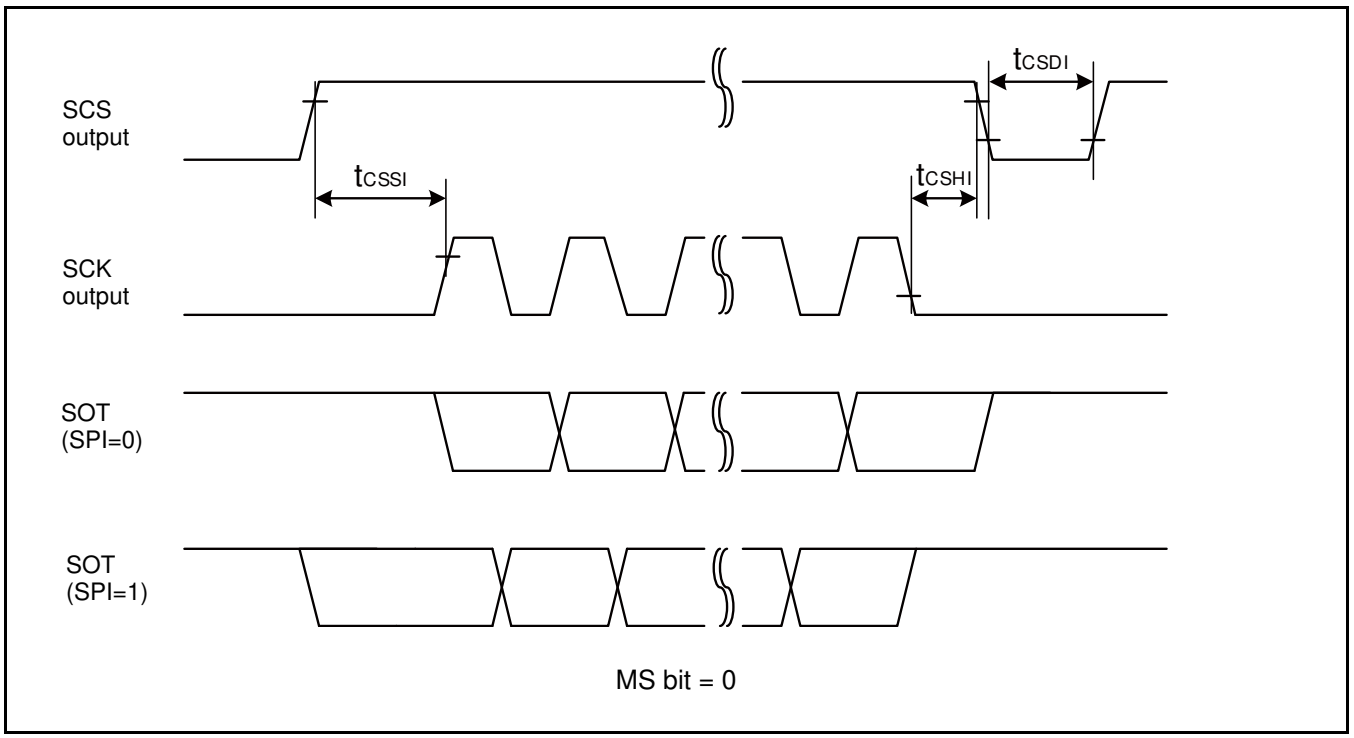
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

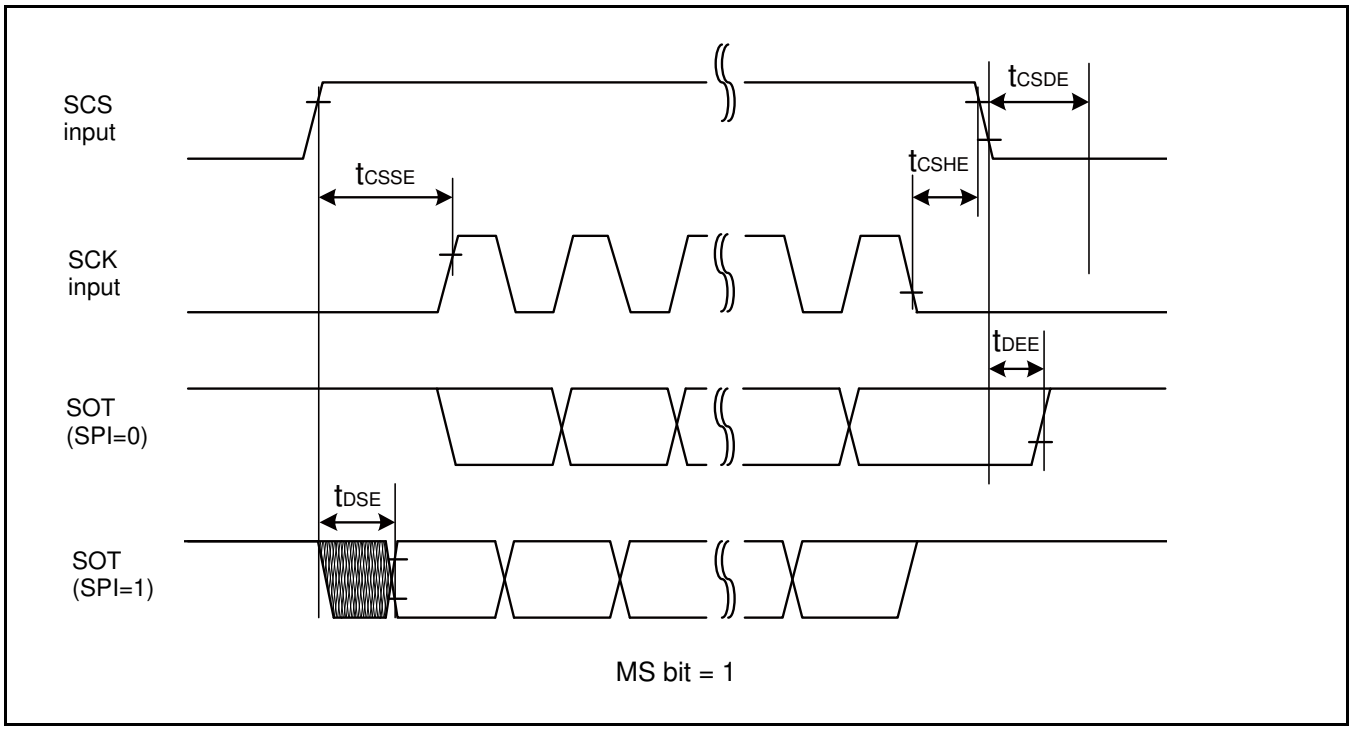
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*


SCS
output
SCK
output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSHI
tCSDI
MS bit = 0


SCS
input
SCK
input
SOT
(SPI=0)
SOT
(SPI=1)
tCSSE
tCSHE
tCSDE
tDEE
tDSE
MS bit = 1

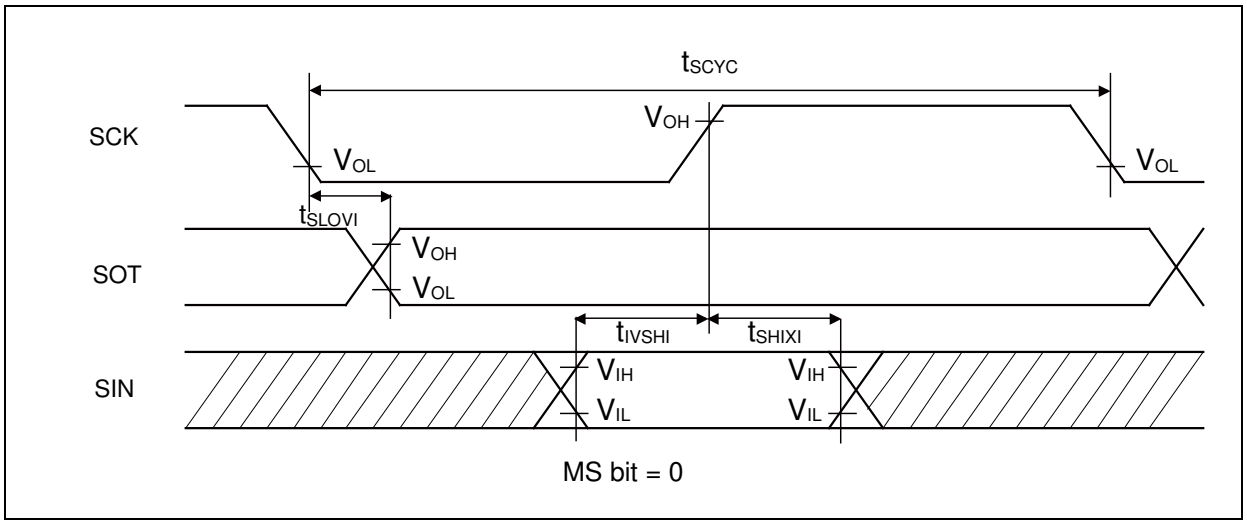
High-Speed Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

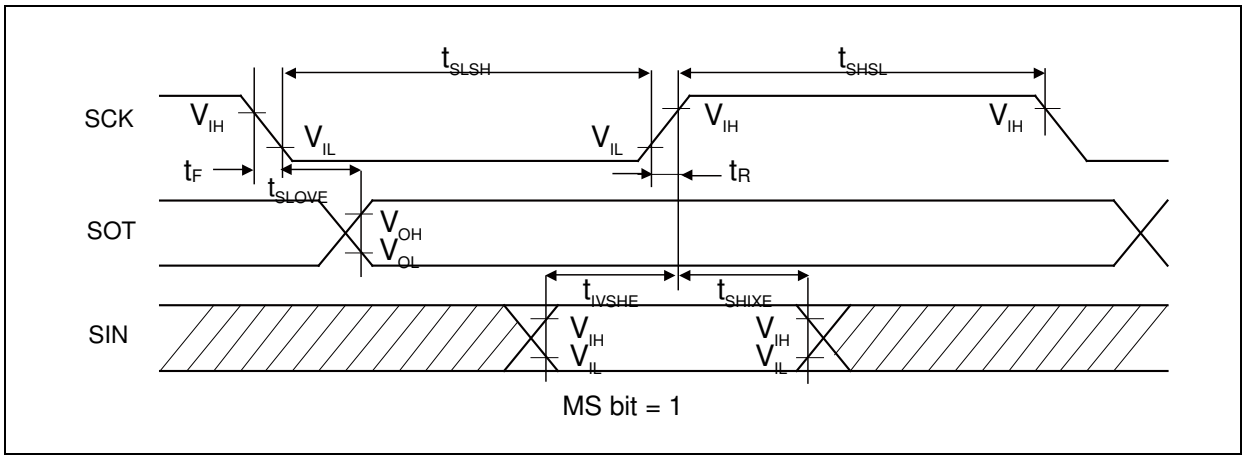
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 10	+ 10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14	-	ns
				12.5*		
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  SIN6_0, SOT6_0, SCK6_0, SCS60_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

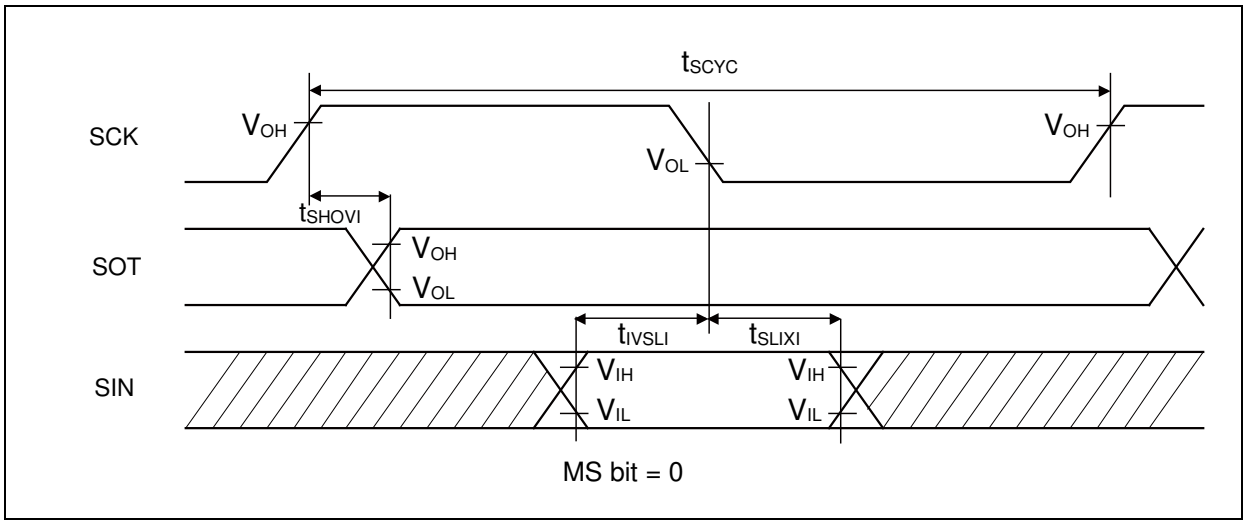
High-Speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

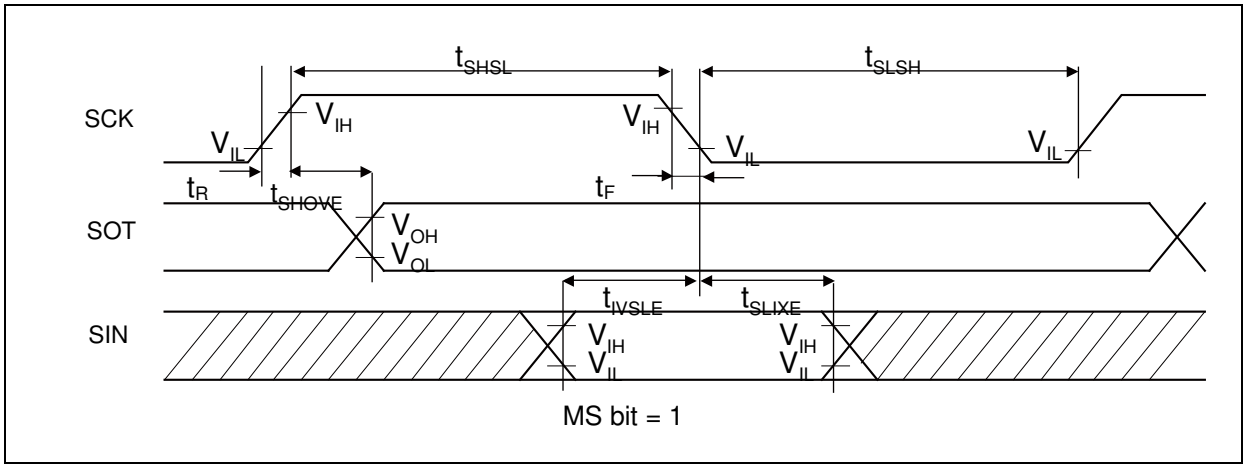
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14	-	ns
				12.5*		
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  SIN6_0, SOT6_0, SCK6_0, SCS60_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

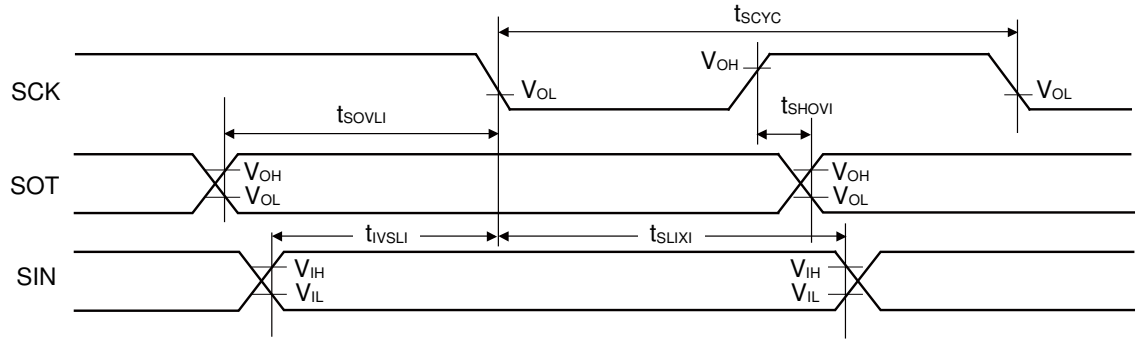
High-Speed Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

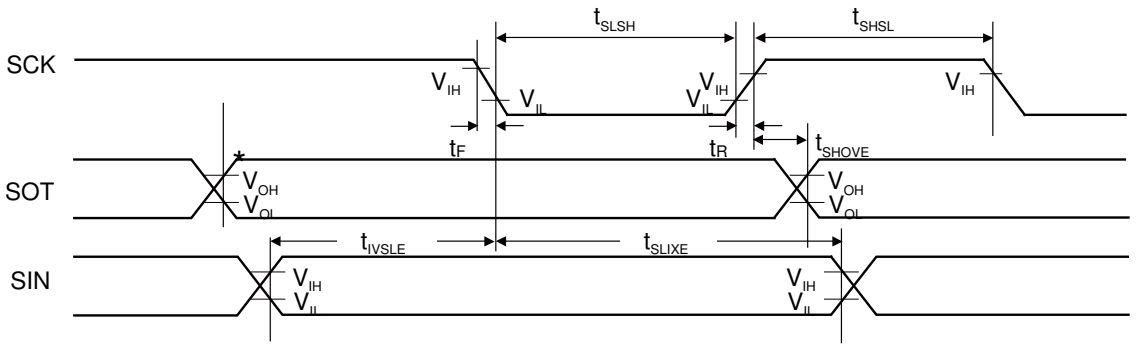
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  SIN6_0, SOT6_0, SCK6_0, SCS60_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

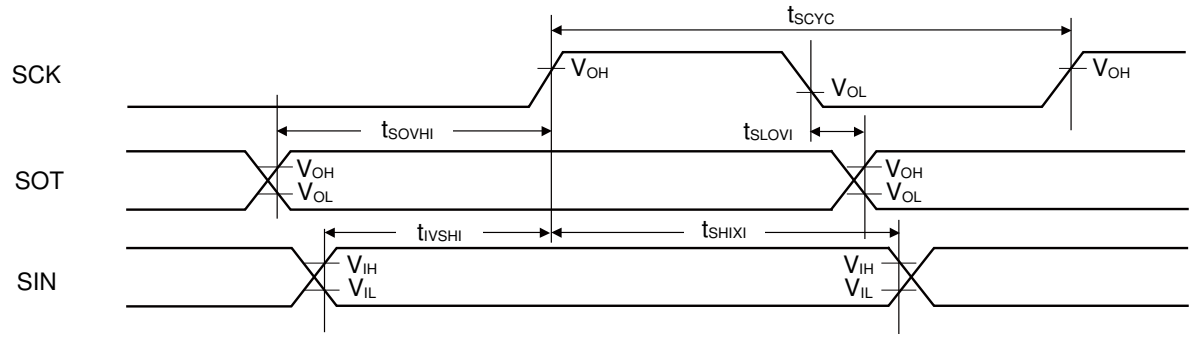
High-Speed Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

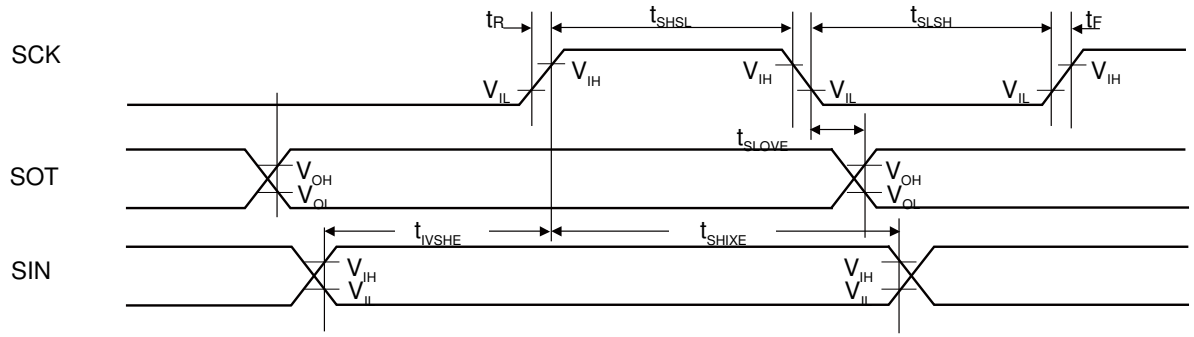
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 10	+ 10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  SIN6_0, SOT6_0, SCK6_0, SCS60_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL=1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	ns

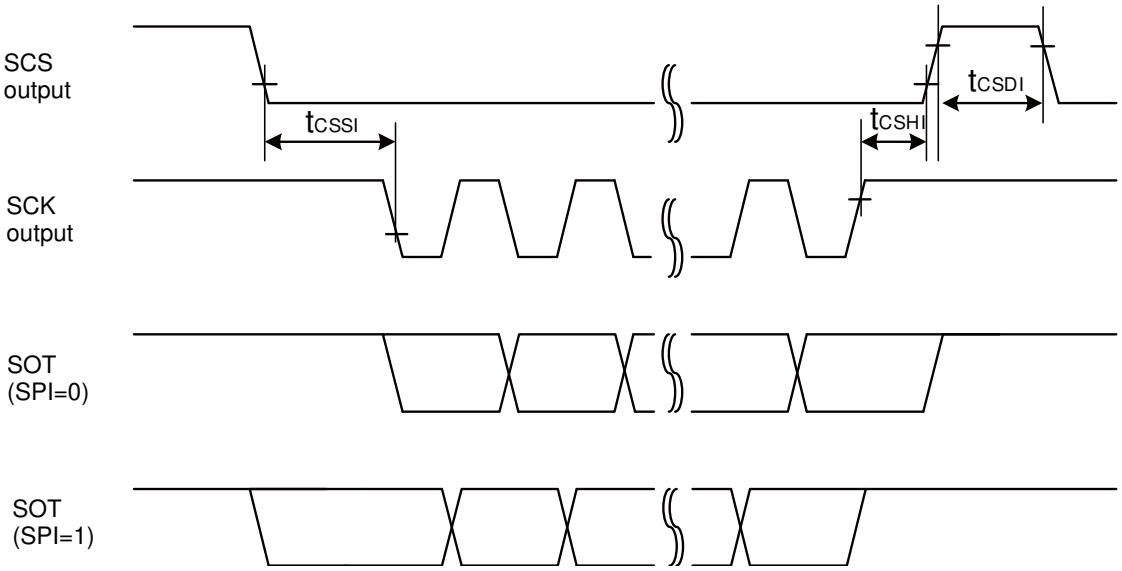
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

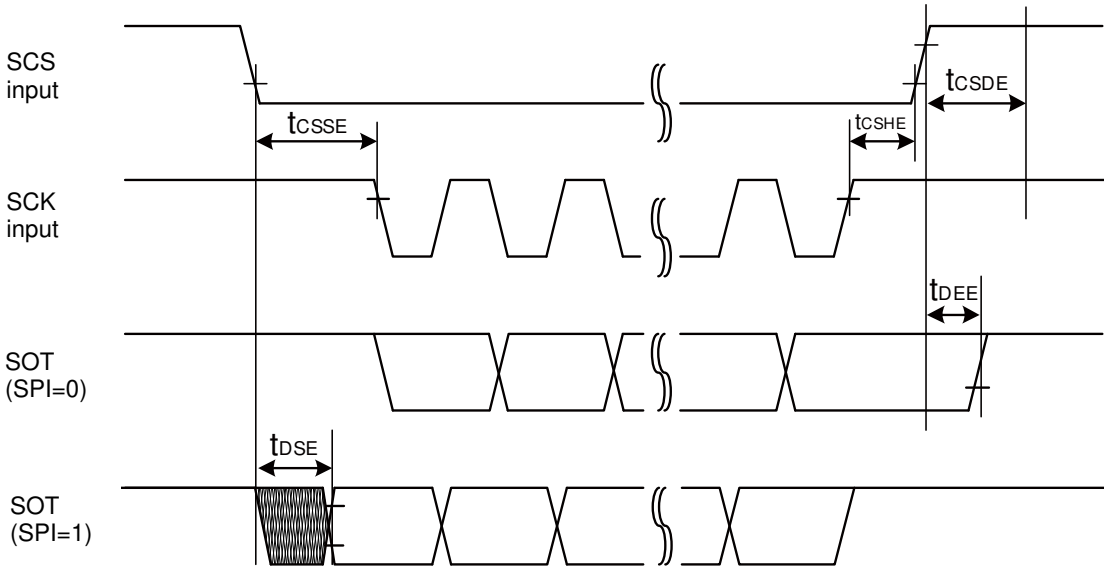
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL=1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↓→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	ns
SCS↓→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	ns

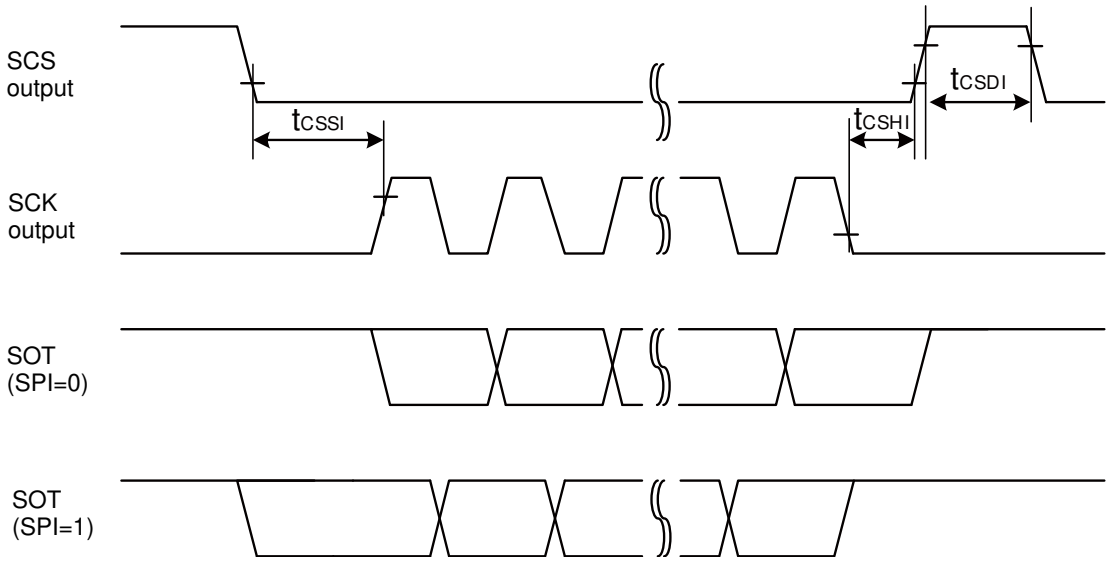
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

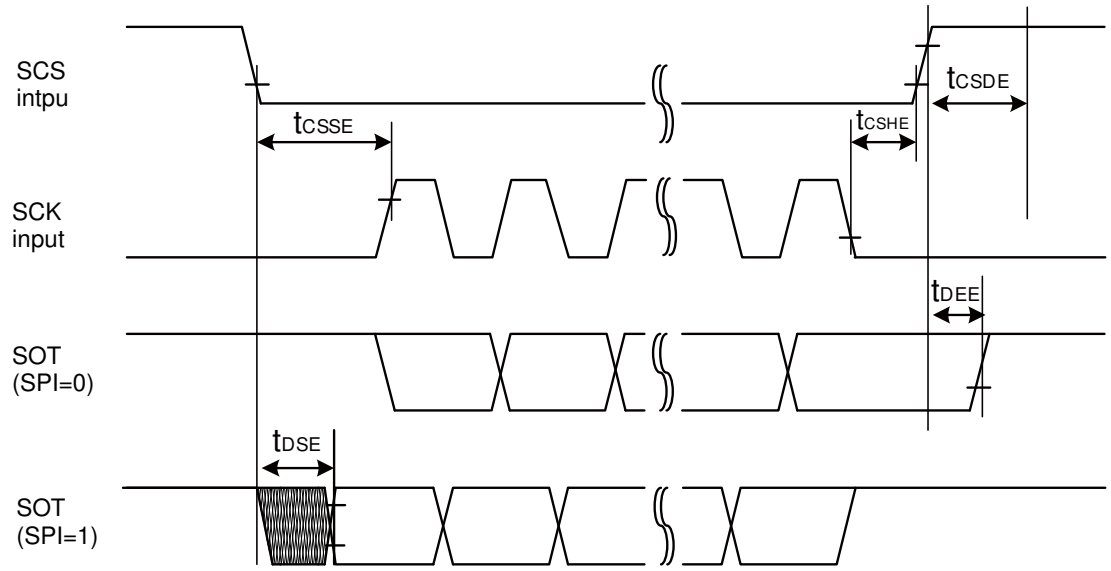
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL=0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	ns

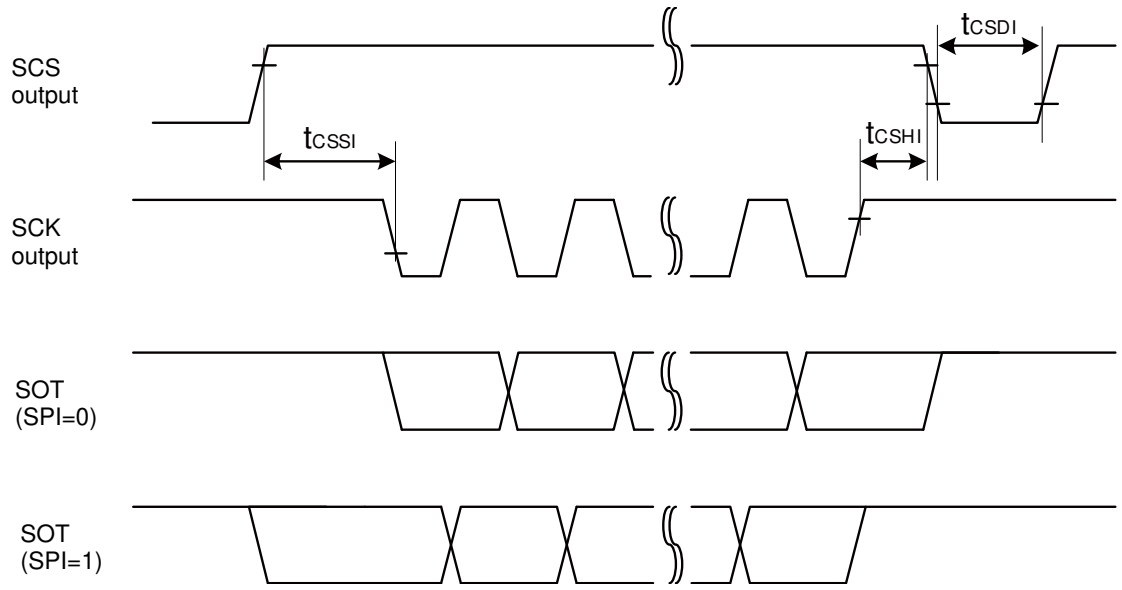
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

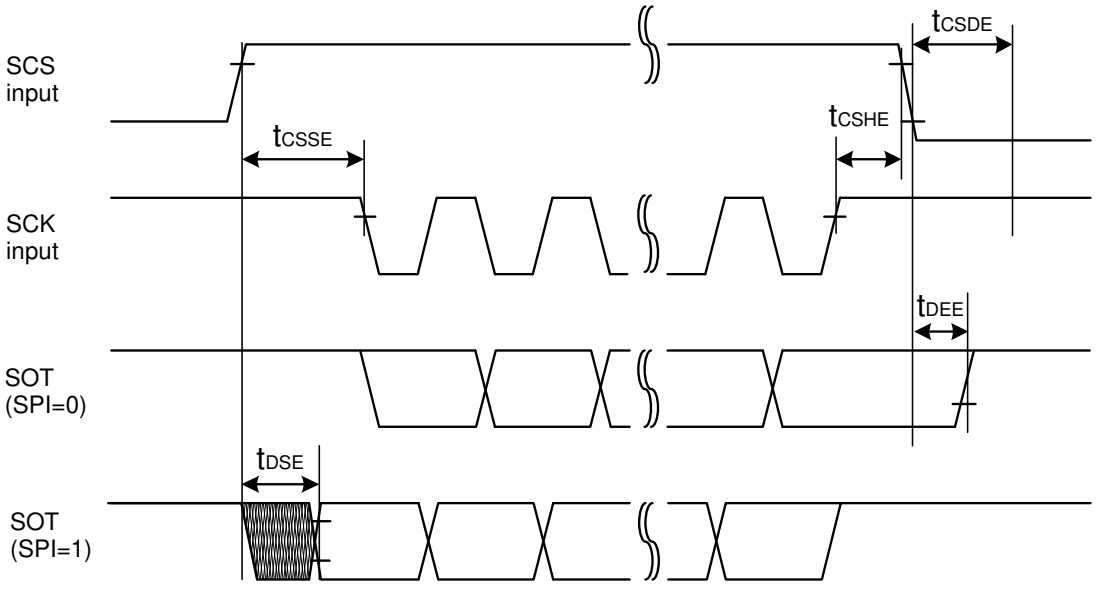
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL=0)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↑→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	ns
SCS↑→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	40	ns
SCS↓→SOT delay time	t_{DEE}		0	-	ns

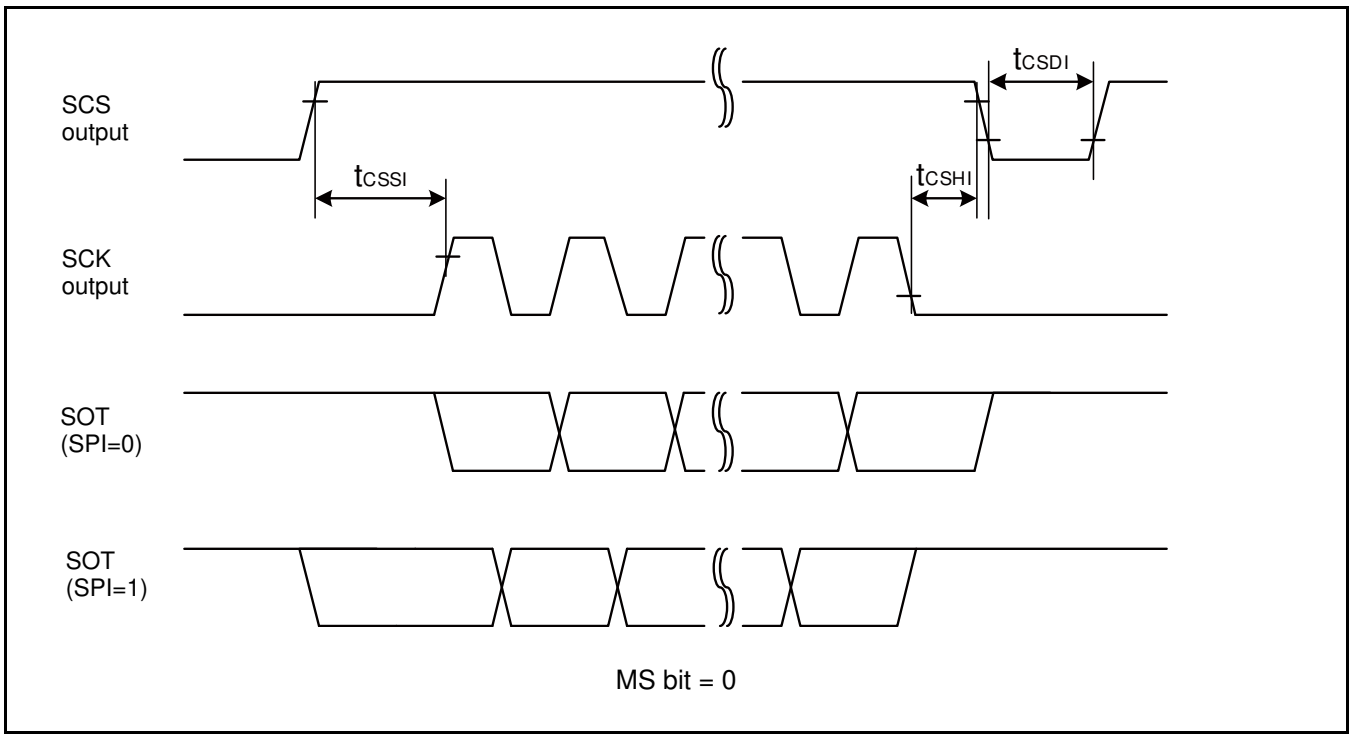
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

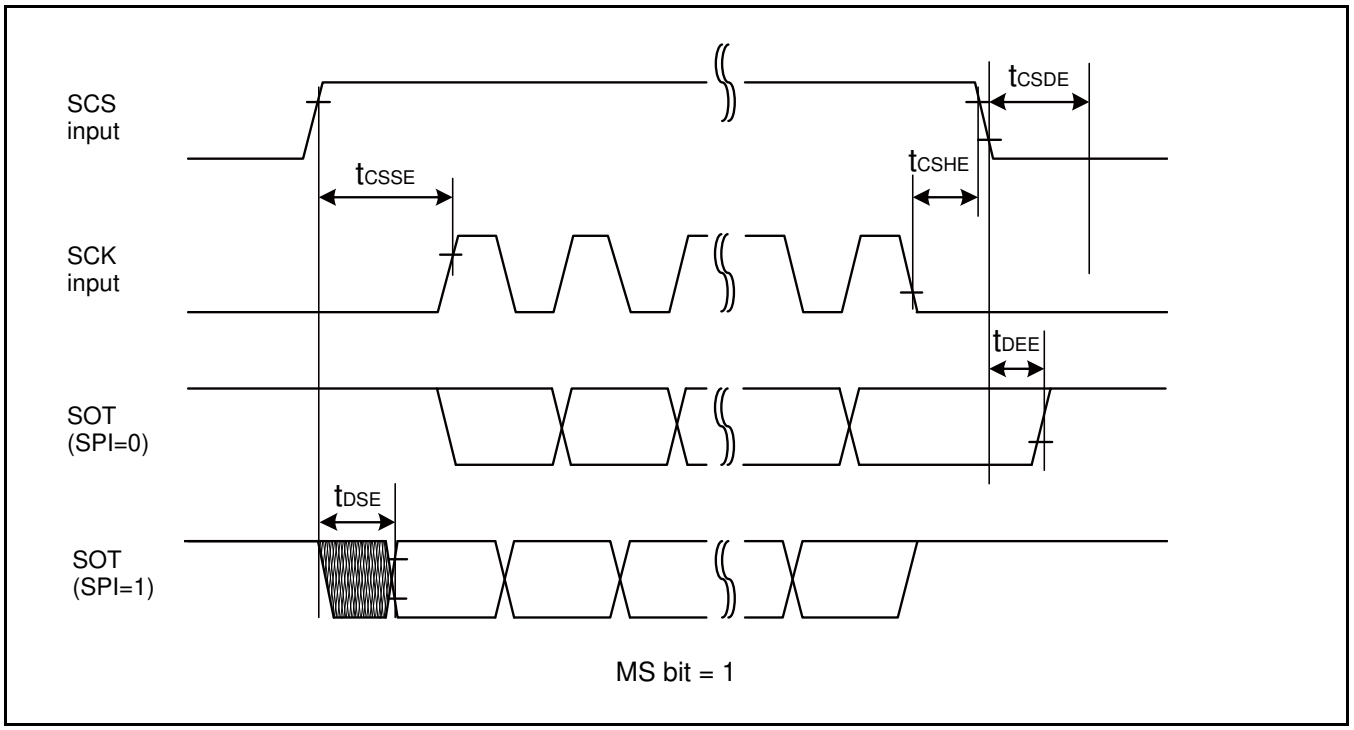
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



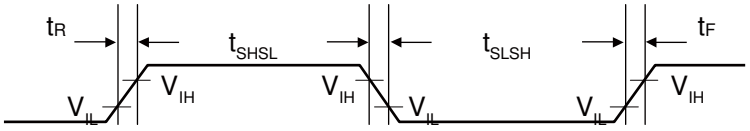
MS bit = 1

External Clock (EXT = 1): when in Asynchronous Mode Only

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	

SCK



12.4.13 External Input Timing

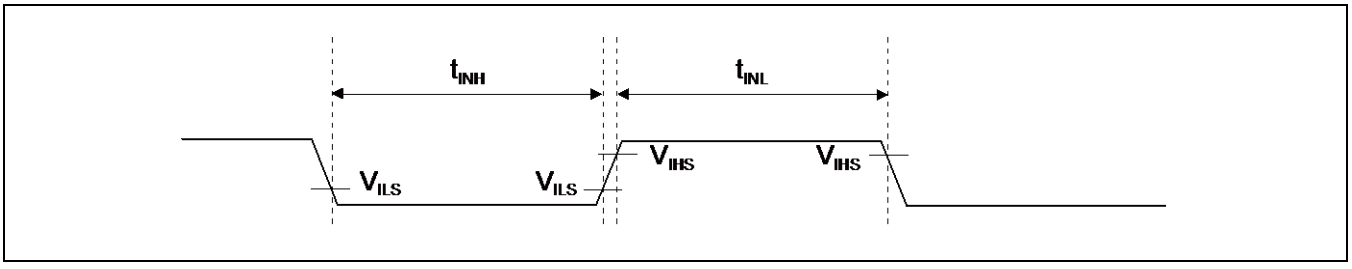
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCK0					Free-run timer input clock
		IC0x					Input capture
		DTTI0X	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INTxx, NMIX	-	$2t_{CYCP}$ + 100(*1)	-	ns	External interrupt, NMI
				500(*2)	-	ns	
		WKUPx	-	500(*3)	-	ns	Deep standby wake up

(*1): t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode. About the APB bus number which the Multi-function Timer and External interrupt are connected to, see 8. Block Diagram in this data sheet.

(*2): When in STOP mode, in timer mode.

(*3): When in deep standby RTC mode, in deep standby Stop mode.

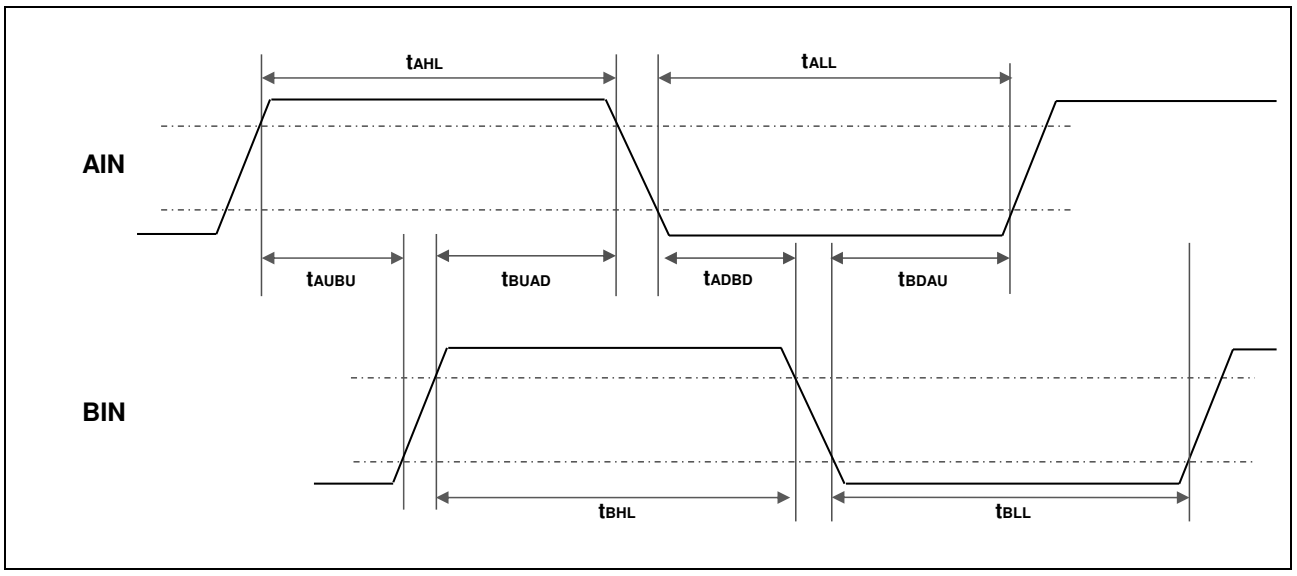


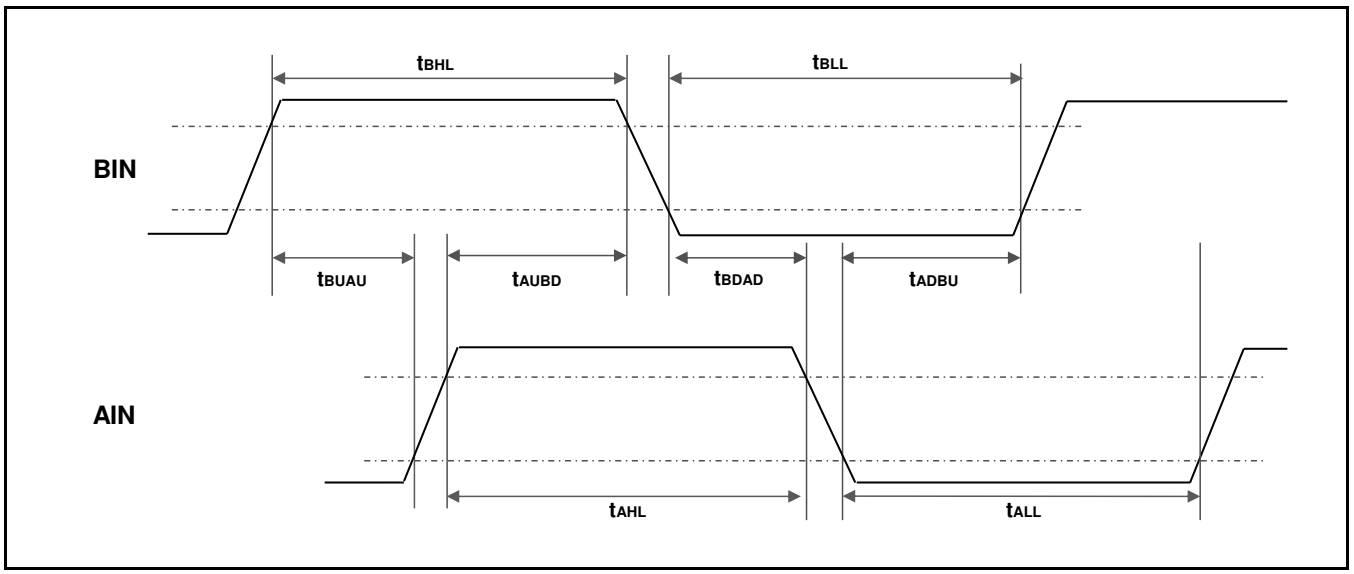
12.4.14 Quadrature Position/Revolution Counter Timing

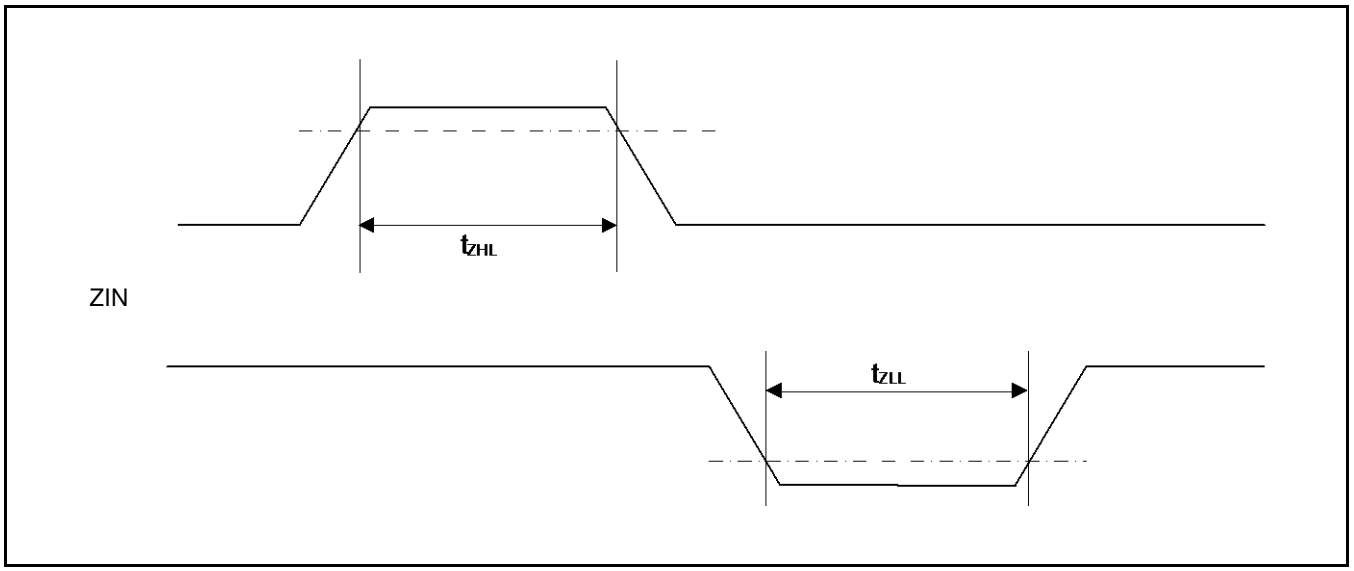
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

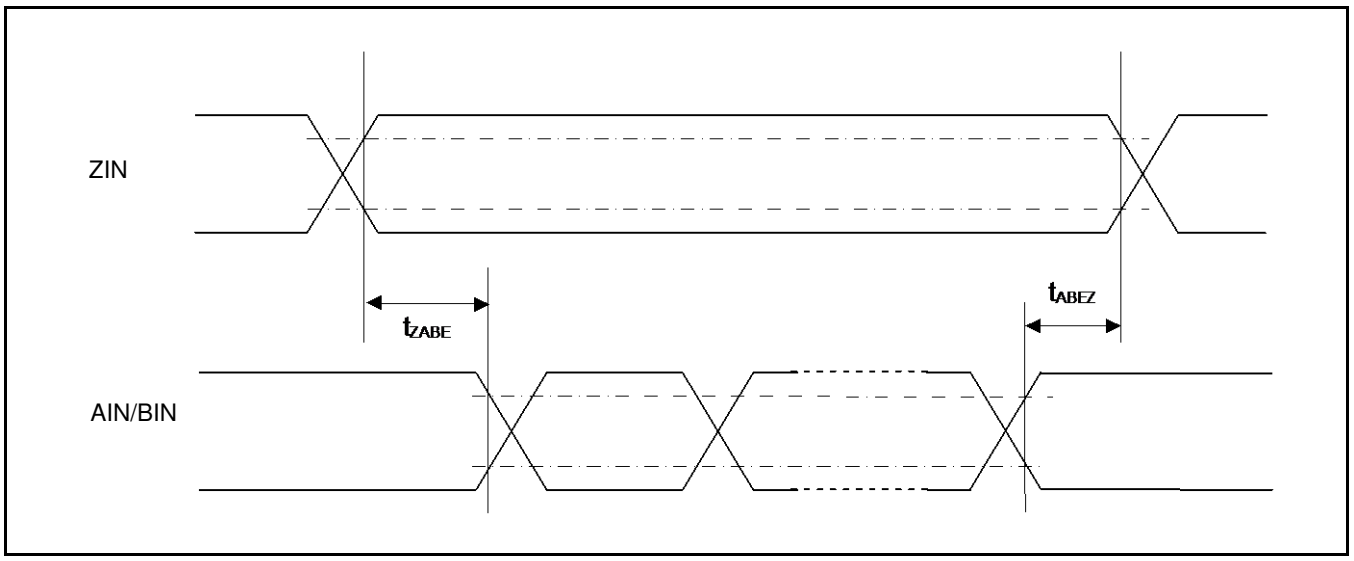
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rising time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC=0			
ZIN pin L width	t_{ZLL}	QCR:CGSC=0			
AIN/BIN rising and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC=1			
Determined ZIN level from AIN/BIN rising and falling time	t_{ABEZ}	QCR:CGSC=1			

*: t_{CYCP} indicates the APB bus clock cycle time except when in Stop mode, in timer mode.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see 8. Block Diagram in this data sheet.




tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
AIN/BIN
tZABE
tABEZ

12.4.15 I²C Timing

Standard Mode, Fast Mode

(V_{CC} = 2.7V to 3.6, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock L width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock H width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP} < 40 MHz	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	*5
		40 MHz ≤ t_{CYCP} < 60 MHz	4 t_{CYCP}*4	-	4 t_{CYCP}*4	-	ns	
		60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	6 t_{CYCP}*4	-	ns	
		80 MHz ≤ t_{CYCP} ≤ 100 MHz	8 t_{CYCP}*4	-	8 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast mode I²C bus device can be used on a Standard mode I²C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

*4: t_{CYCP} is the APB bus clock cycle time.

About the APB bus number that I²C is connected to, see 8. Block Diagram in this data sheet.

When the standard mode is used, please set to 2 MHz or more peripheral bus clock.

When fast mode is used, please set to 8MHz or more peripheral bus clock.

*5: The noise filter time can be changed by register settings.

Change the number of the noise filter steps according to APB bus clock frequency.

Fast Mode Plus (Fm+)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast Mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	1000	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock L width	t_{LOW}		0.5	-	µs	
SCL clock H width	t_{HIGH}		0.26	-	µs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		0.26	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	ns	*5
		80 MHz ≤ t_{CYCP} ≤100 MHz	8 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

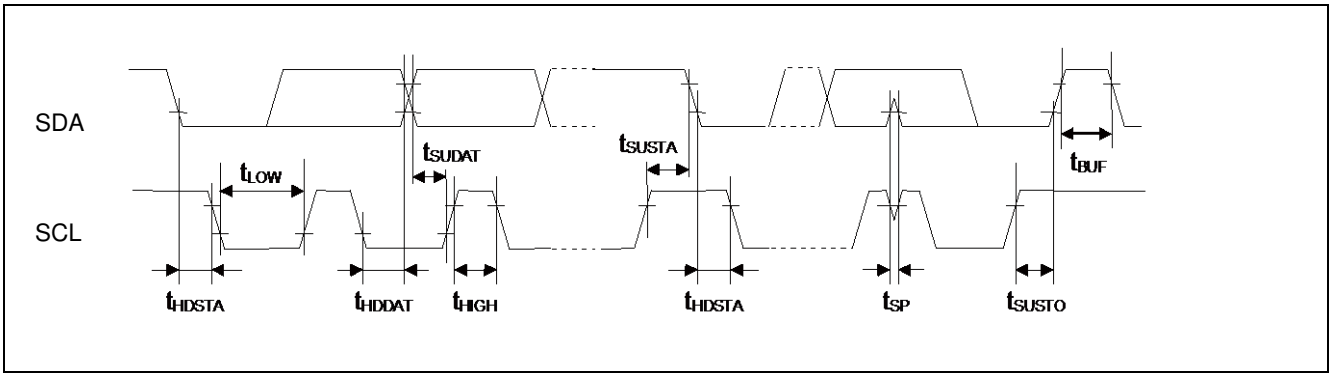
*2: The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast mode I^2C bus device can be used on a Standard mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see 8. Block Diagram in this data sheet.
To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

*6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register. See Chapter 12: I/O Port in "FM4 Family Peripheral Manual Main part (002-04856)" for the details.



12.4.16 SD Card Interface Timing

Default-Speed Mode

■Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1 card)	0	25	MHz
Clock frequency Identification Mode	f_{OD}	S_CLK		0*/100	400	kHz
Clock low time	t_{WL}	S_CLK		10	-	ns
Clock high time	t_{WH}	S_CLK		10	-	ns
Clock rising time	t_{TLH}	S_CLK		-	10	ns
Clock falling time	t_{THL}	S_CLK		-	10	ns

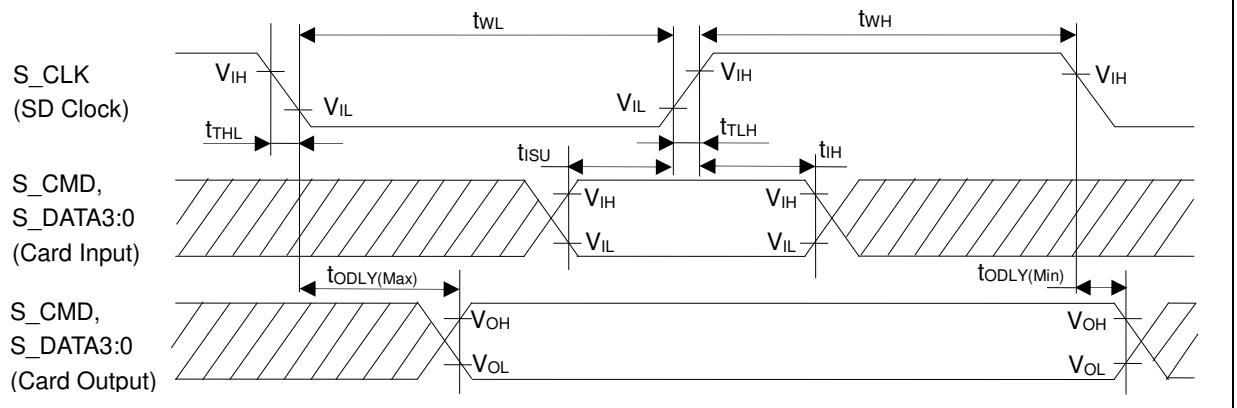
*: 0 Hz means the clock is stopped. The given minimum frequency range is for cases where a continuous clock is required.

■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input setup time	t_{ISU}	S_CMD, S_DATA3:0	C_{CARD} ≤ 10 pF (1 card)	5	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3:0		5	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer Mode	t_{ODLY}	S_CMD, S_DATA3:0	C_{CARD} ≤ 40 pF (1 card)	0	14	ns
Output Delay time during Identification Mode	t_{ODLY}	S_CMD, S_DATA3:0		0	50	ns



Default-Speed Mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *Please refer to: SD card interface Chapter 15 in FM4 Family Peripheral Manual Main part (002-04856) for Clock frequency (f_{PP}).*

High-Speed Mode

■Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1 card)	0	50	MHz
Clock low time	t_{WL}	S_CLK		7	-	ns
Clock high time	t_{WH}	S_CLK		7	-	ns
Clock rising time	t_{TLH}	S_CLK		-	3	ns
Clock falling time	t_{THL}	S_CLK		-	3	ns

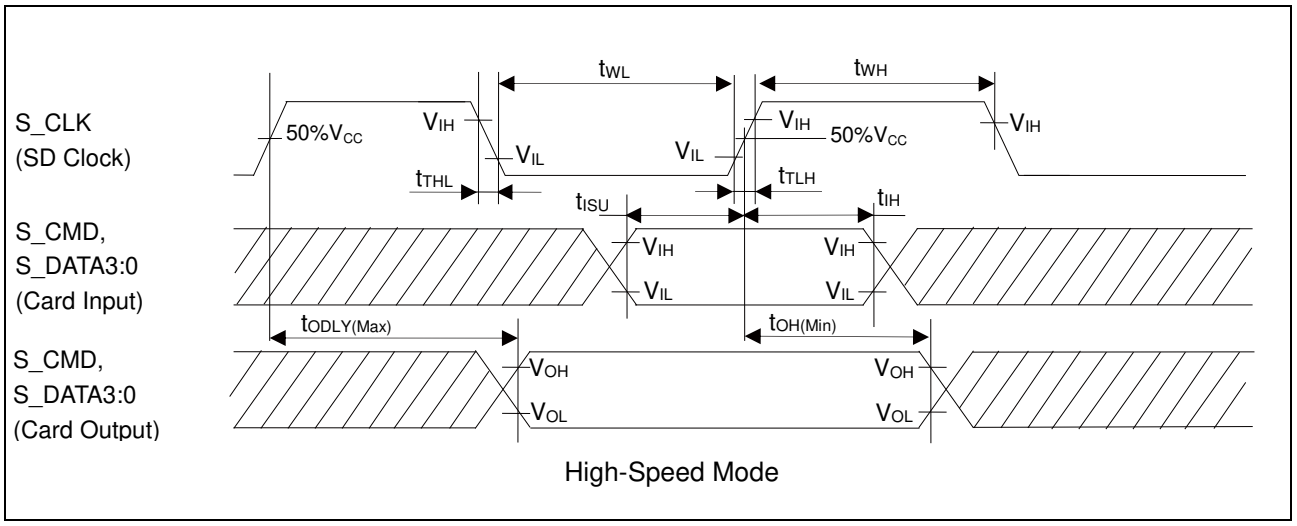
■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input setup time	t_{ISU}	S_CMD, S_DATA3:0	C_{CARD} ≤ 10 pF (1 card)	6	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3:0		2	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer Mode	t_{ODLY}	S_CMD, S_DATA3:0	C_L ≤ 40 pF (1 card)	0	14	ns
Output Hold time	t_{OH}	S_CMD, S_DATA3:0	C_L ≥ 15 pF (1 card)	2.5	-	ns
Total System capacitance for each line*	C_L	-	1 card	-	40	pF

*: In order to satisfy severe timing, host shall drive only one card.



High-Speed Mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *Please refer to: SD card interface Chapter 15 in FM4 Family Peripheral Manual Main part (002-04856) for Clock frequency (f_{PP}).*

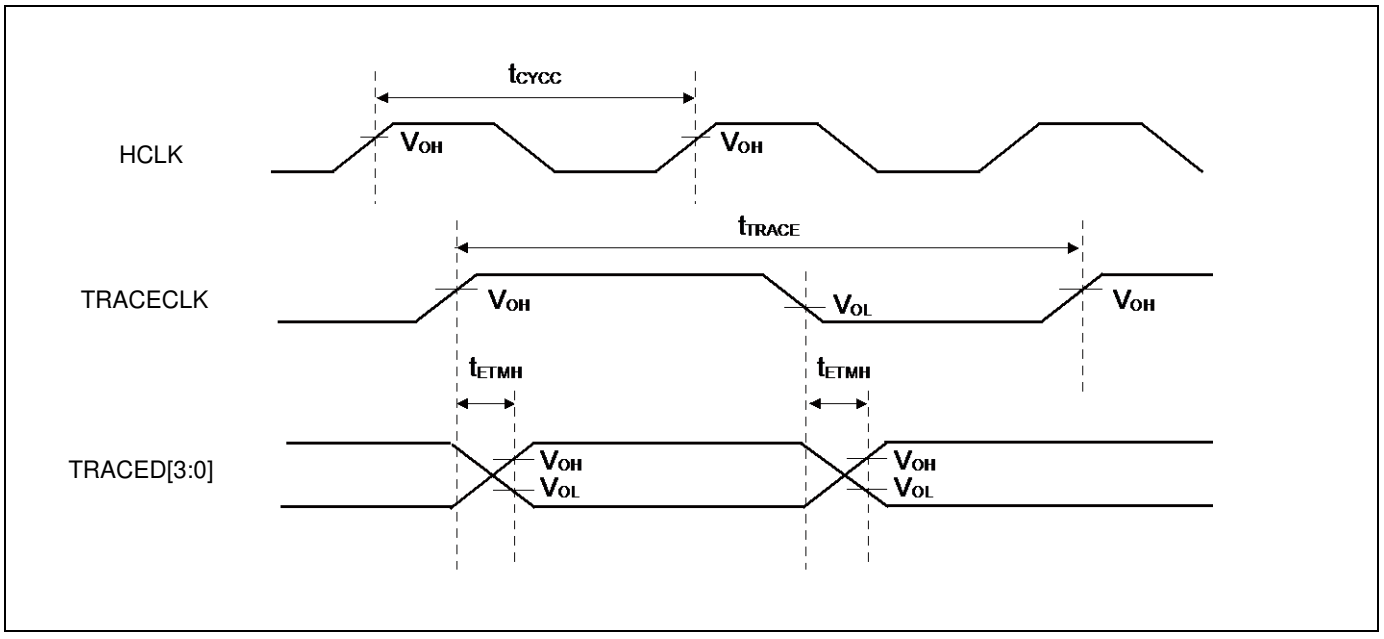
12.4.17 ETM Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[3:0]	-	2	15	ns	
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	-		32	MHz	
TRACECLK clock cycle	t_{TRACE}		-	31.25	-	ns	

Note:

- *When the external load capacitance C_L= 30 pF.*



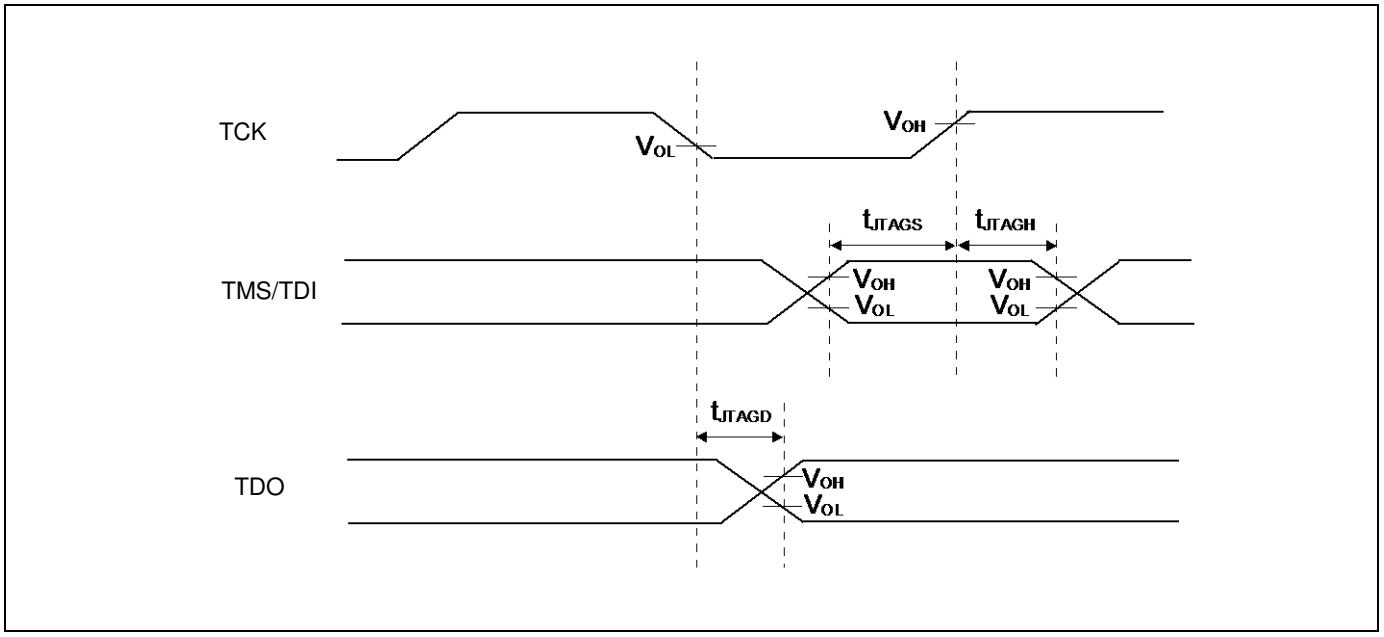
12.4.18 JTAG Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	-	15	-	ns	
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	-	15	-	ns	
TDO delay time	t_{JTAGD}	TCK, TDO	-	-	45	ns	

Note:

- *When the external load capacitance C_L= 30 pF.*



12.4.19 I²S Timing

Master Mode Timing

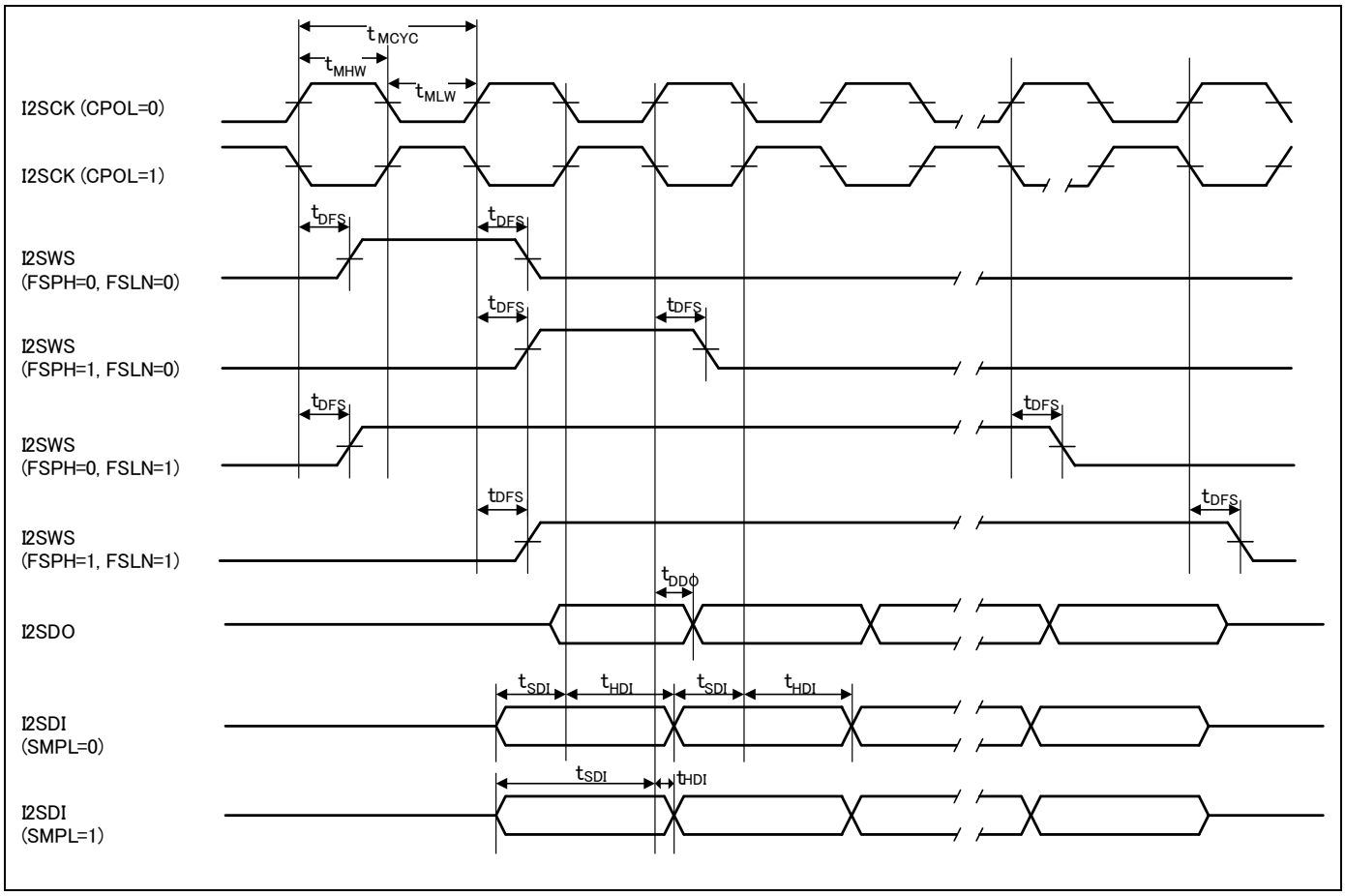
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	t_{MCYC}	I2SCK	-	-	12.288	MHz	
Output clock pulse width	t_{MHW}	I2SCK	-	45	55	%	
	t_{MLW}			45	55	%	
I2SCK→I2SWS delay time	t_{DFS}	I2SCK, I2SWS	-	0	24.0	ns	
I2SCK→I2SDO delay time*	t_{DDO}	I2SCK, I2SDO	-	0	24.0	ns	
I2SDI→I2SCK setup time	t_{HSDI}	I2SCK, I2SDI	-	25.0	-	ns	
I2SDI→I2SCK hold time	t_{HDI}		-	0	-	ns	
Input signal rising time	t_{RI}	I2SDI	-	-	5	ns	
Input signal falling time	t_{FI}		-	-	5	ns	

*: Except for the first bit of transmission frame

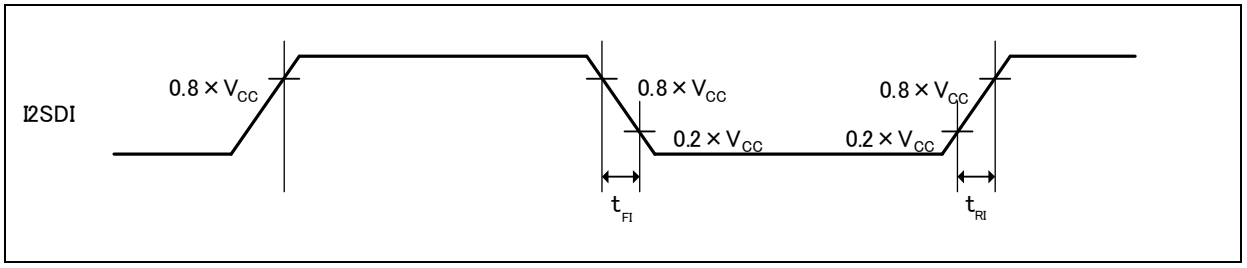
Notes:

- *When the external load capacitance C_L = 20 pF*
- *When I2SWS=48 kHz, I2MCLK=256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.
  See Chapter 7-2: I²S(Inter-IC Sound bus)Interface in FM4 Family Peripheral Manual Communication part (002-04862) for the details.



Note:

- *See Chapter 7-2: I²S(Inter-IC Sound bus)Interface in FM4 Family Peripheral Manual Communication part (002-04862) for the details of CPOL, FSPH, FSLIN, SMPL .*



Slave Mode Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

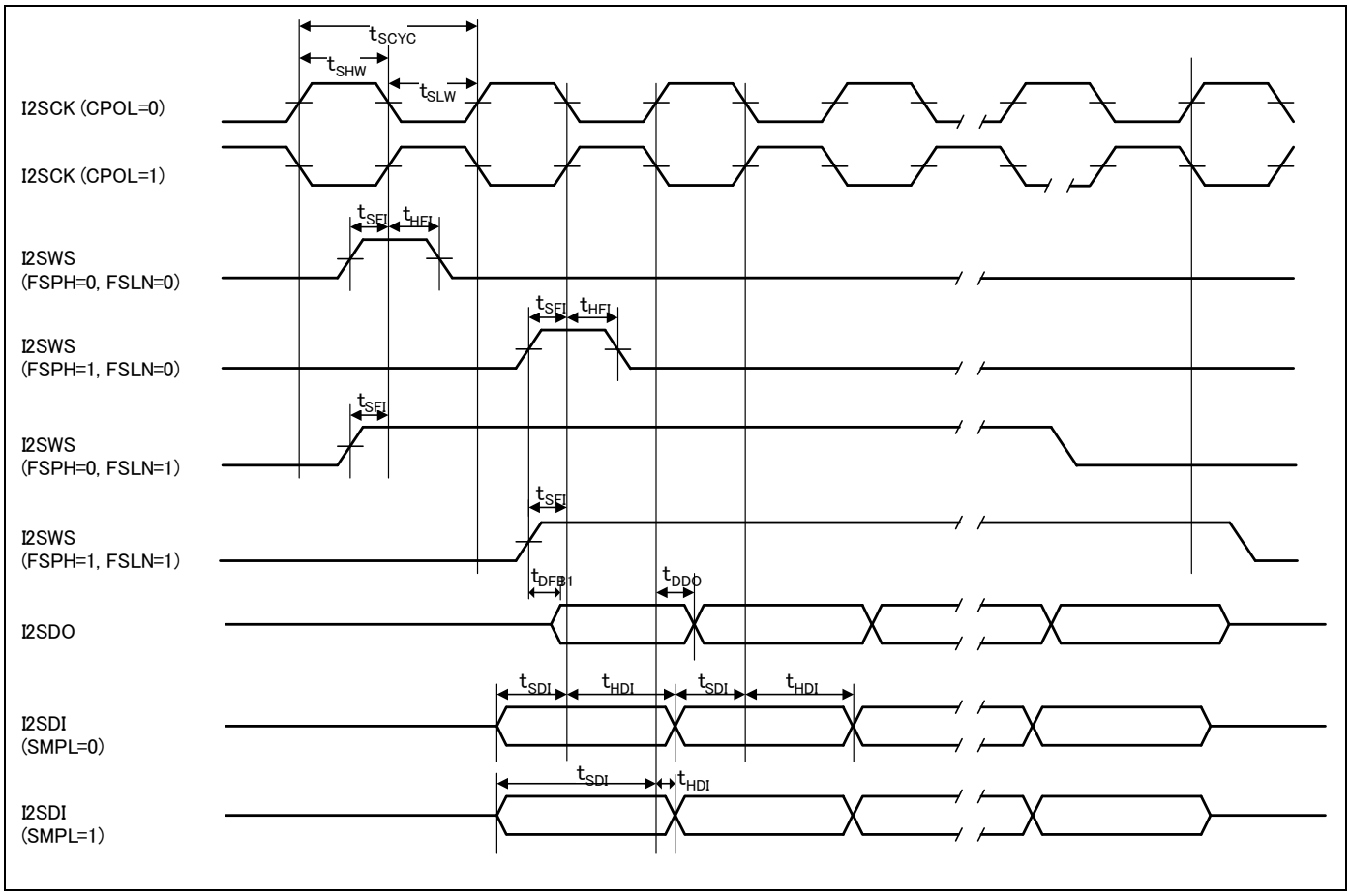
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	t_{SCYC}	I2SCK	-	-	12.288	MHz	
Input clock pulse width	t_{SHW}	I2SCK	-	45	55	%	
	t_{SLW}			45	55	%	
I2SWS→I2SCK Setup time	t_{SFI}	I2SCK, I2SWS	-	8	-	ns	
I2SWS→I2SCK Hold time	t_{HFI}	I2SCK, I2SWS	-	0	-	ns	
I2SCK↑→I2SDO Delay time*1	t_{DDO}	I2SCK, I2SDO	-	0	32	ns	
I2SCK↑→I2SDO Delay Time*2	t_{DFB1}		-	0	32	ns	
I2SDI→I2SCK↓ Setup time	t_{SDI}	I2SCK, I2SDI	-	8	-	ns	
I2SDI→I2SCK↓ Hold time	t_{HDI}		-	0	-	ns	
Input signal rising time	t_{RI}	I2SCK, I2SWS,I2SDI	-	-	5	ns	
Input signal falling time	t_{FI}		-	-	5	ns	

*1: Except for the first bit of transmission frame

*2: When FSPH register 1.

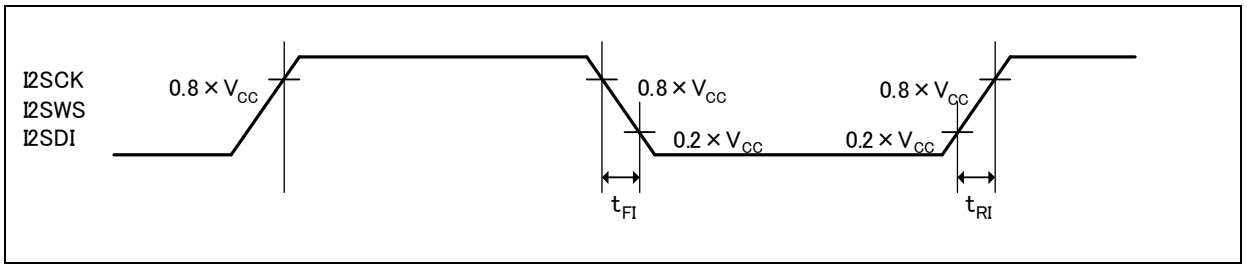
Notes:

- *When the external load capacitance C_L = 20 pF*
- *When I2SWS=48 kHz, I2MCLK=256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.
  See Chapter 7-2: I^2S(Inter-IC Sound bus)Interface in FM4 Family Peripheral Manual Communication part (002-04862) for the details.



Notes:

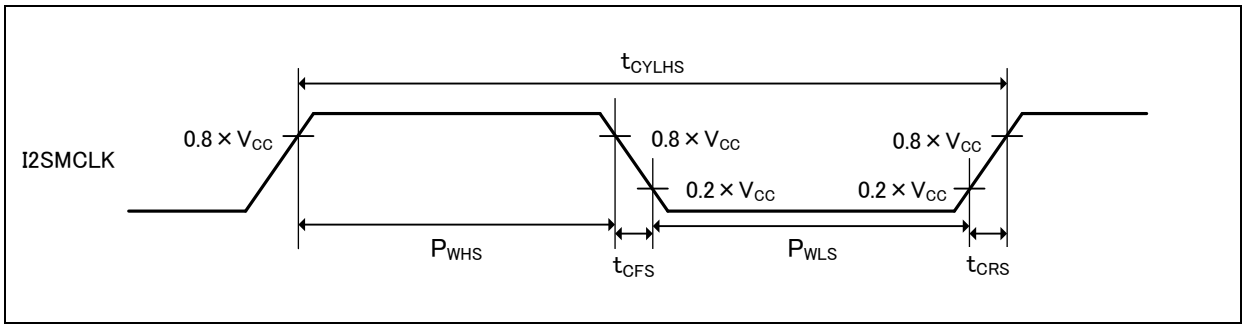
- *See Chapter 7-2: I²S(Inter-IC Sound bus)Interface in FM4 Family Peripheral Manual Communication part (002-04862) for the details of FSPH, FSLN, SMPL*
- *I2SCK input is selectable polarity by CPOL bit of CNTREG register*



▪ I2SMCLK Input Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CHS}	I2SCK	-	-	25	MHz	
Input clock cycle	t_{CYLHS}	-	-	40	-	ns	
Input clock pulse width	-	-	P_{WHS}/t_{CYLHS} P_{WLS}/t_{CYLHS}	45	55	%	When using external clock
Input clock rising time and falling time	t_{CFS} t_{CRS}	-	-	-	5	ns	When using external clock



▪ I2SMCLK Output Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

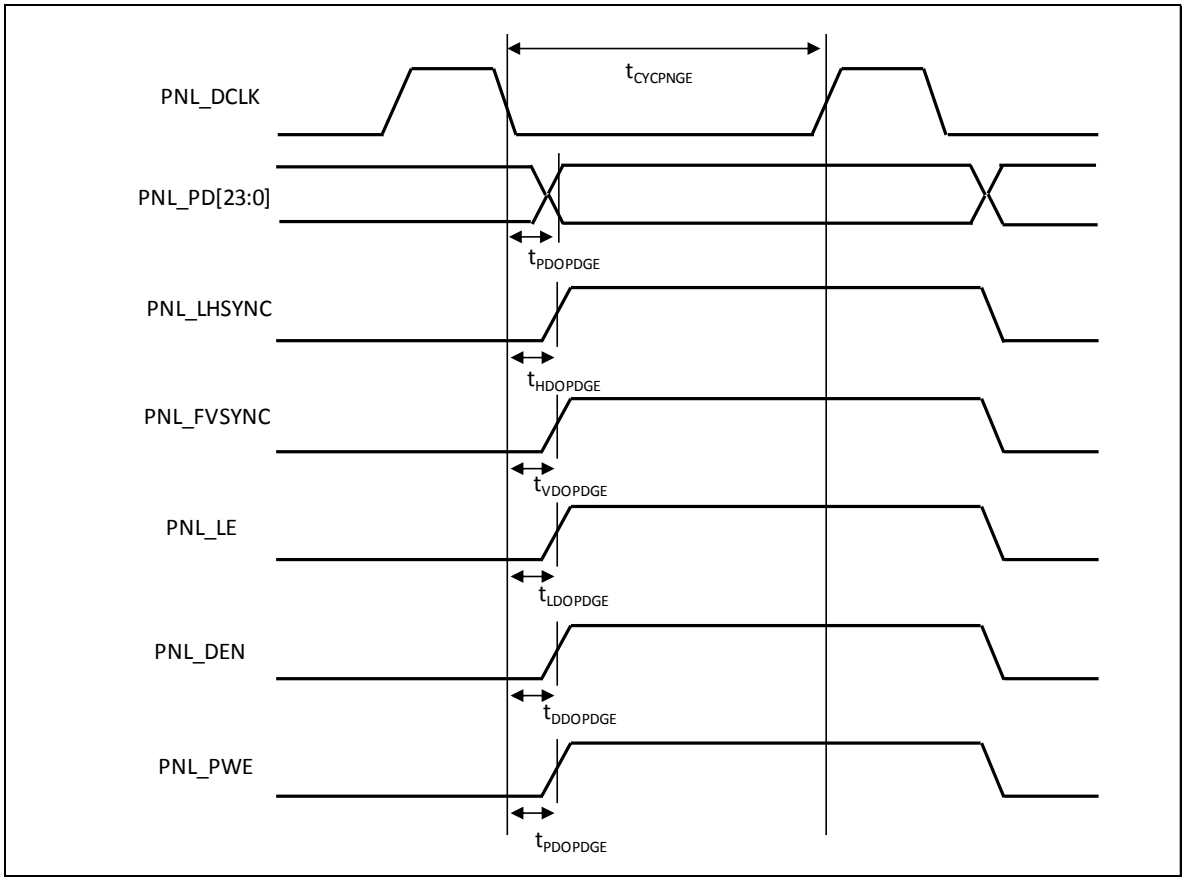
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CHS}	I2SCK	-	-	12.288	MHz	

12.4.20 GDC:Panel Output Timing

(V_{CC} = 3.0V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	$t_{CYCPNGE}$	PNL_DCLK	-	-	40	MHz
PNL_DCLK↓→PNL_PD[23:0] Output delay time	$t_{PDOPDGE}$	PNL_PD[23:0]	-	-4.5	4.5	ns
PNL_DCLK↓→PNL_LH_SYNC Output delay time	$t_{HDOPDGE}$	PNL_LH_SYNC	-	-4.5	4.5	ns
PNL_DCLK↓→PNL_FV_SYNC Output delay time	$t_{VDOPDGE}$	PNL_FV_SYNC	-	-4.5	4.5	ns
PNL_DCLK↓→PNL_LE Output delay time	$t_{LDOPDGE}$	PNL_LE	-	-4.5	4.5	ns
PNL_DCLK↓→PNL_DEN Output delay time	$t_{DDOPDGE}$	PNL_DEN	-	-4.5	4.5	ns
PNL_DCLK↓→PNL_PWE Output delay time	$t_{PDOPDGE}$	PNL_PWE		-4.5	4.5	ns

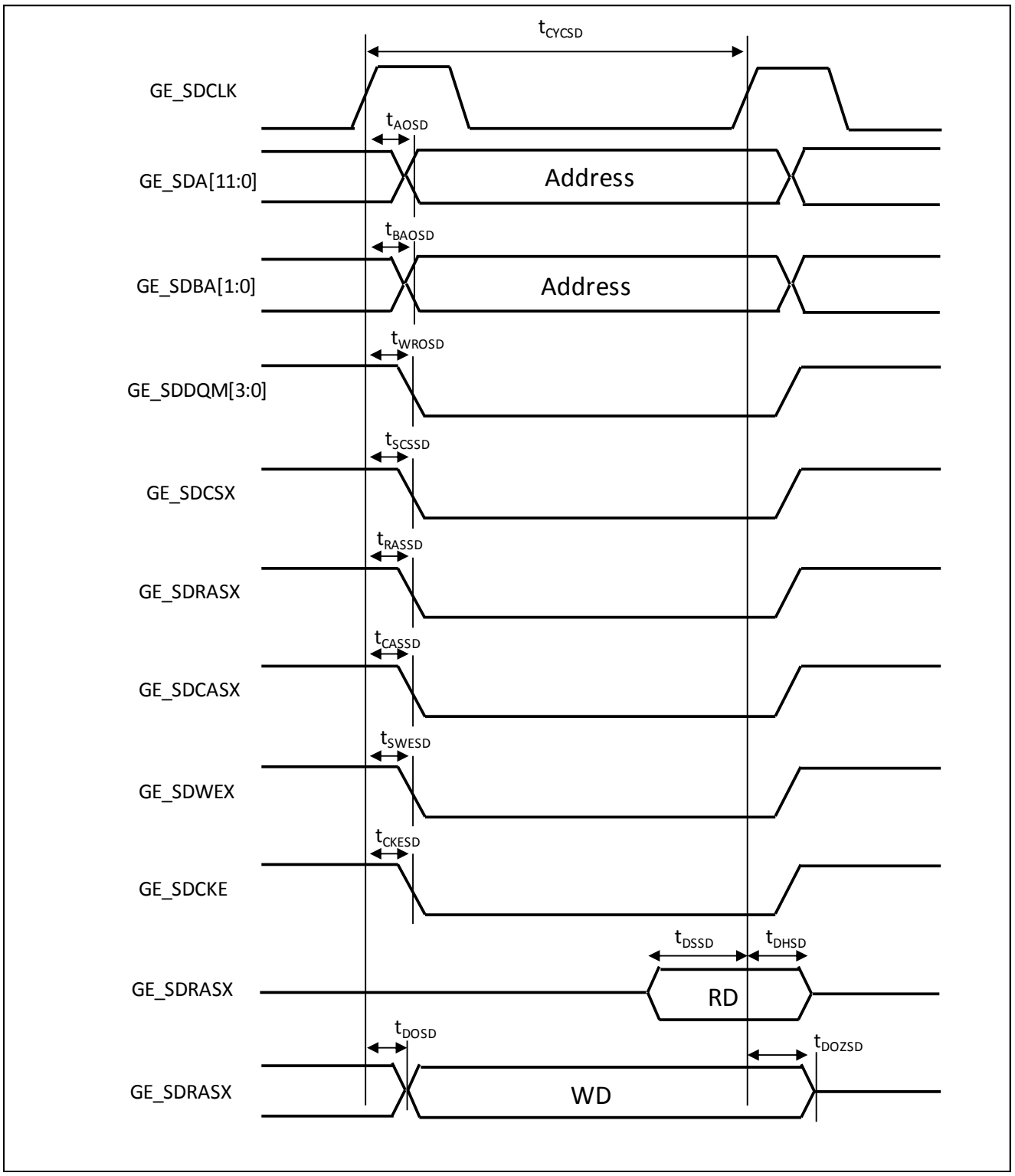
–



12.4.21 GDC: SDRAM-IF Timing

(V_{CC} = 3.0V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Output frequency	t_{CYCSD}	GE_SDCLK	-	80	MHz
Address delay time	t_{AOSD}	GE_SDCLK GE_SDA[11:0]	1	5	ns
Bank address delay time	t_{BAOSD}	GE_SDCLK GE_SDBA[1:0]	1	5	ns
GE_SDCLK↑→ Data output delay time	t_{DOSD}	GE_SDCLK GE_SDDQ[31:0]	1	5	ns
GE_SDCLK↑→ Data output Hi-Z time	t_{DOZSD}	GE_SDCLK GE_SDDQ[31:0]	1	5	ns
GE_SDDQM[3:0] delay time	t_{WROSD}	GE_SDCLK GE_SDDQM[3:0]	1	5	ns
GE_SDCSX delay time	t_{SCSSD}	GE_SDCLK GE_SDCSX	1	5	ns
GE_SDRASX delay time	t_{RASSD}	GE_SDCLK GE_SDRASX	1	5	ns
GE_SDCASX delay time	t_{CASSD}	GE_SDCLK GE_SDCASX	1	5	ns
GE_SDWEX delay time	t_{SWESD}	GE_SDCLK GE_SDWEX	1	5	ns
GE_SDCKE delay time	t_{CKESD}	GE_SDCLK GE_SDCKE	1	5	ns
Data setup time	t_{DSSD}	GE_SDCLK GE_SDDQ[31:0]	4	-	ns
Data hold time	t_{DHSD}	GE_SDCLK GE_SDDQ[31:0]	0	-	ns


tCYCSD
GE_SDCLK
tAOSD
GE_SDA[11:0]
Address
tBAOSD
GE_SDBA[1:0]
Address
tWROSD
GE_SDDQM[3:0]
tSCSSD
GE_SDCSX
tRASSD
GE_SDRASX
tCASSD
GE_SDCASX
tSWESD
GE_SDWEX
tCKESD
GE_SDCKE
tDSSD
tDHSD
GE_SDRASX
RD
tDOSD
tDOZSD
GE_SDRASX
WD

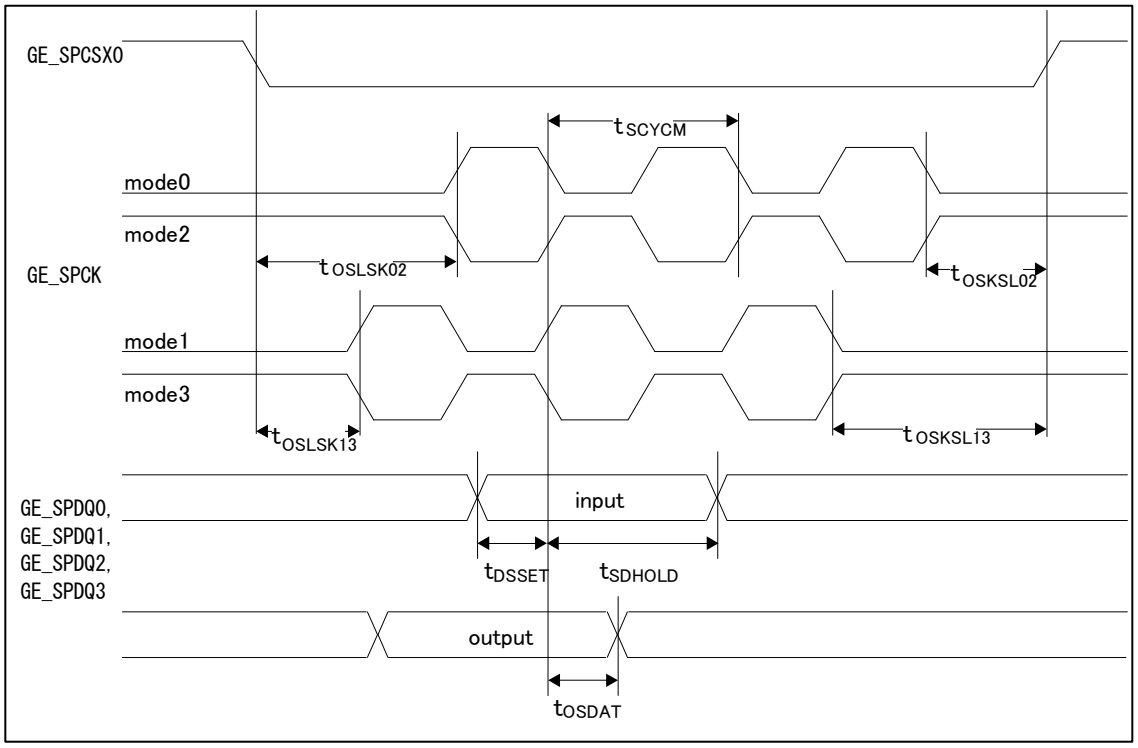
12.4.22 GDC: High-Speed Quad SPI Timing

(V_{CC} = 3.0V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock frequency	t_{SCYCM}	GE_SPCK	C_L=20 pF	-	80	MHz
Enabled CS→ CLK Starting Time (mode0/mode2)	$t_{OSLSK02}$	GE_SPCK, GE_SPCSX0		1.5×t_{SCYCM} – 4.25	-	ns
Enabled CS→ CLK Starting Time (mode1/mode3)	$t_{OSLSK13}$			t_{SCYCM} – 4.25	-	ns
CLK Last→ Disabled CS Time (mode0/mode2)	$t_{OSKSL02}$			t_{SCYCM}	-	ns
CLK Last→ Disabled CS Time (mode1/mode3)	$t_{OSKSL13}$			1.5×t_{SCYCM}	-	ns
SIO Data output time	t_{OSDAT}	GE_SPCK, GE_SPDQ0, GE_SPDQ1, GE_SPDQ2, GE_SPDQ3		-1.25	4.25	ns
SIO Setup	t_{DSSET}			4	-	ns
SIO Hold	t_{SDHOLD}			0.5×t_{SCYCM}	-	ns

Note:

- *See Chapter 8-3: High-Speed Quad SPI controller in FM4 Family Peripheral Manual Communication part (002-04862) for the detail of RTM mode.*

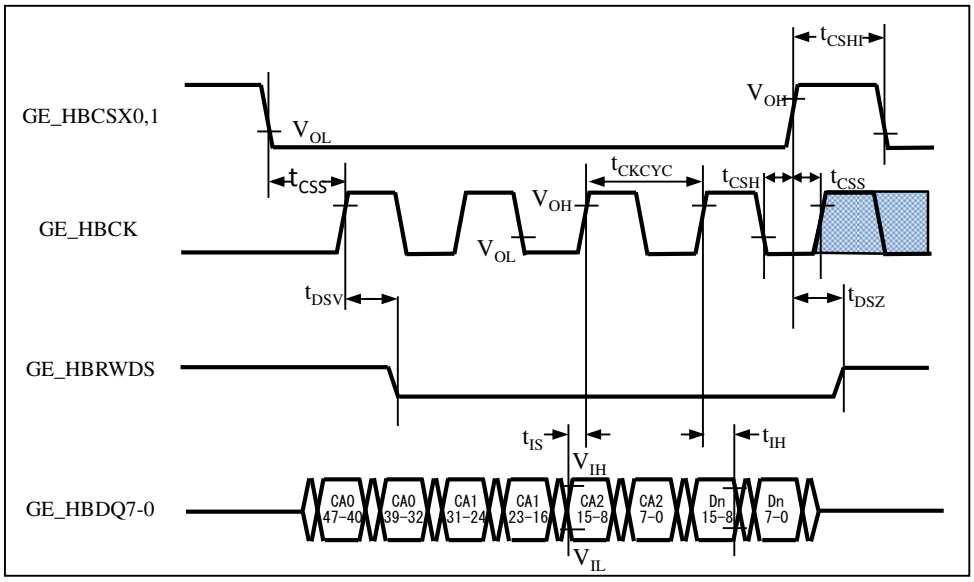

GE_SPCSX0
tSCYCM
mode0
mode2
GE_SPCK
tOSLSK02
tOSKSL02
mode1
mode3
tOSLSK13
tOSKSL13
GE_SPDQ0,
GE_SPDQ1,
GE_SPDQ2,
GE_SPDQ3
input
tDSSET
tSDHOLD
output
tOSDAT

12.4.23 GDC: HyperBus I/F Timing

HyperFlash Write

(V_{CC} = 3.0V to 3.6V, V_{SS} = 0V)

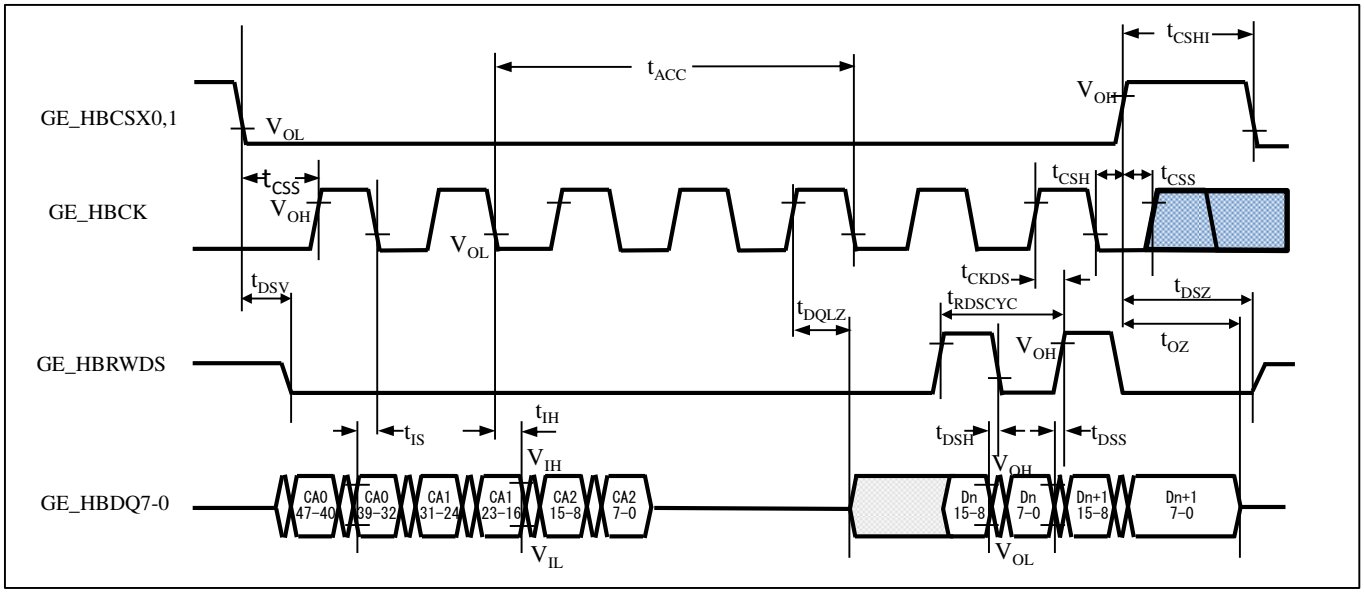
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Hyper Bus clock cycle	t_{CKCYC}	GE_HBCK	C_L=30 pF	10	-	ns
CS ↑ ↓→CK ↑ Chip Select setup time	t_{CSS}	GE_HBCSX1 GE_HBCSX0		3	-	ns
CS ↓ →RDS ↓ Chip select active to RDS valid(Low)	t_{DSV}	GE_HBRWDS		-	8	ns
DQ → CK ↑ ↓ Input setup time	t_{IS}	GE_HBDQ7- GE_HBDQ0		0.8	-	ns
CK ↑ ↓→ DQ Input hold time	t_{IH}	GE_HBDQ7- GE_HBDQ0		0.8	-	ns
CK ↓ → CS ↑ Chip select hold time	t_{CSH}	GE_HBCSX1 GE_HBCSX0		0	-	ns
CS ↑ → RDS(Hi-z) Chip select Inactive to RDS High-Z	t_{DSZ}	GE_HBCSX1 GE_HBCSX0		-	7	ns
CS ↑ → CS ↓ Chip select HIGH between operation	t_{CSHI}	GE_HBCSX1 GE_HBCSX0		8	-	ns



HyperFlash Read

(V_{CC} = 3.0V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Hyper Bus clock cycle	t_{RDSCYC}	GE_HBCK	C_L=30pF	10	-	ns
Read initial Access Time	t_{ACC}	GE_HBCK		-	120	ns
CS ↑ ↓→CK ↑ Chip Select setup time	t_{CSS}	GE_HBCSX1 GE_HBCSX0		3	-	ns
CS ↓ → RDS ↓ Chip select active to RDS valid (Low)	t_{DSV}	GE_HBRWDS		-	8	ns
DQ → CK ↑ ↓ Input setup time	t_{IS}	GE_HBDQ7- GE_HBDQ0		0.8	-	ns
CK ↑ ↓→ DQ Input hold time	t_{IH}	GE_HBDQ7- GE_HBDQ0		0.8	-	ns
CK ↓ → CS ↑ Chip select hold time	t_{CSH}	GE_HBCSX1 GE_HBCSX0		0	-	ns
CS ↑ → RDS(Hi-Z) Chip select Inactive to RDS High-Z	t_{DSZ}	GE_HBRWDS		-	7	ns
CK ↑ ↓ → DQ (Low Z) Clock to DQs Low Z	t_{DQLZ}	GE_HBDQ7- GE_HBDQ0		0	-	ns
RDS ↑ ↓→ DQ (valid) RDS transition to DQ valid	t_{DSS}	GE_HBDQ7- GE_HBDQ0		-0.8	+0.8	ns
RDS ↑ ↓→ DQ (invalid) RDS transition to DQ invalid	t_{DSH}	GE_HBDQ7- GE_HBDQ0		-0.8	+0.8	ns
CS ↑→ DQ (Hi-Z) Chip select Inactive to DQs High-Z	t_{OZ}	GE_HBDQ7- GE_HBDQ0		-	7	ns
CK ↑ ↓→ RDS ↑ ↓ CK transition to RDS transition	t_{CKDS}	GE_HBRWDS		1	7	ns
CS ↑→ CS ↓ Chip select HIGH between Operation	t_{CSHI}	GE_HBCSX1 GE_HBCSX0		8	-	ns



12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 3.6V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	-	± 4.5	LSB	AVRH=2.7 V to 3.6 V Offset calibration when used
Differential Nonlinearity	-	-	-	-	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 2	± 7	LSB	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 2	AVRH ± 7	LSB	
Total error	-	-	-	± 3	± 8	LSB	
Conversion time	-	-	1.0*1	-	-	µs	
Sampling time *2	t_S	-	0.3	-	10	µs	
Compare clock cycle*3	t_{CCK}	-	50	-	1000	ns	
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AV_{CC}	-	0.30	0.45	mA	A/D 1unit operation
			-	0.1	9.5	µA	When A/D stop
Reference power supply current(AVRH)	-	AVRH	-	0.66	1.18	mA	A/D 1unit operation AVRH=3.3 V
			-	0.2	3.2	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.8	kΩ	
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	t_{CCK} ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).

Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).

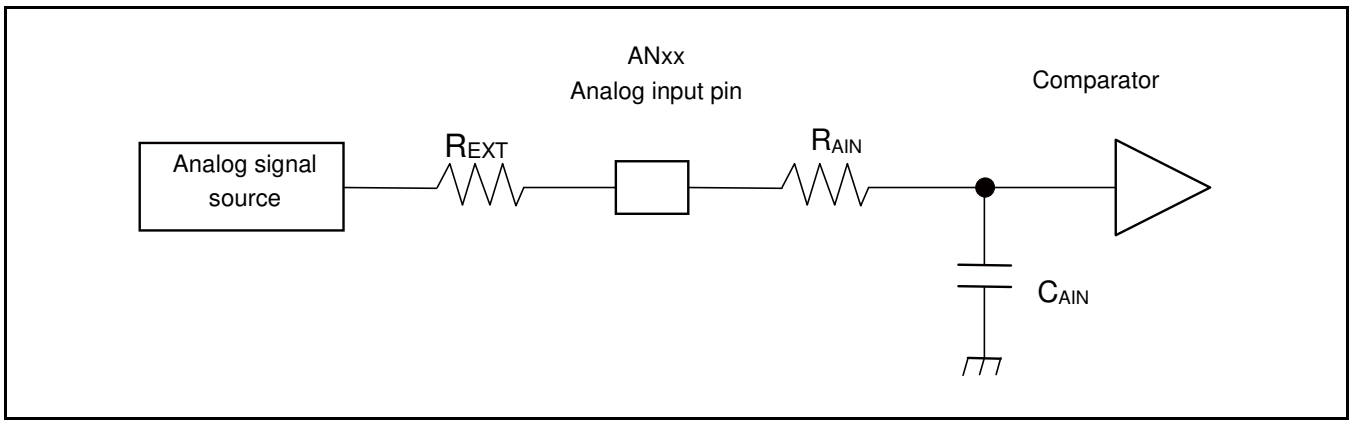
For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing.

For more information about the APB bus signal to which the A/D converter is connected, see 10. Block Diagram in this data sheet.

The sampling clock and compare clock are set at base clock (HCLK).

*2: A necessary sampling time changes by external impedance. Ensure that it set the sampling time to satisfy (Equation 1).

*3: The compare time (t_C) is the value of (Equation 2).



(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: Input resistance of A/D = 1.8 kΩ

C_{AIN}: Input capacity of A/D = 12.05 pF

R_{EXT}: Output impedance of external circuit

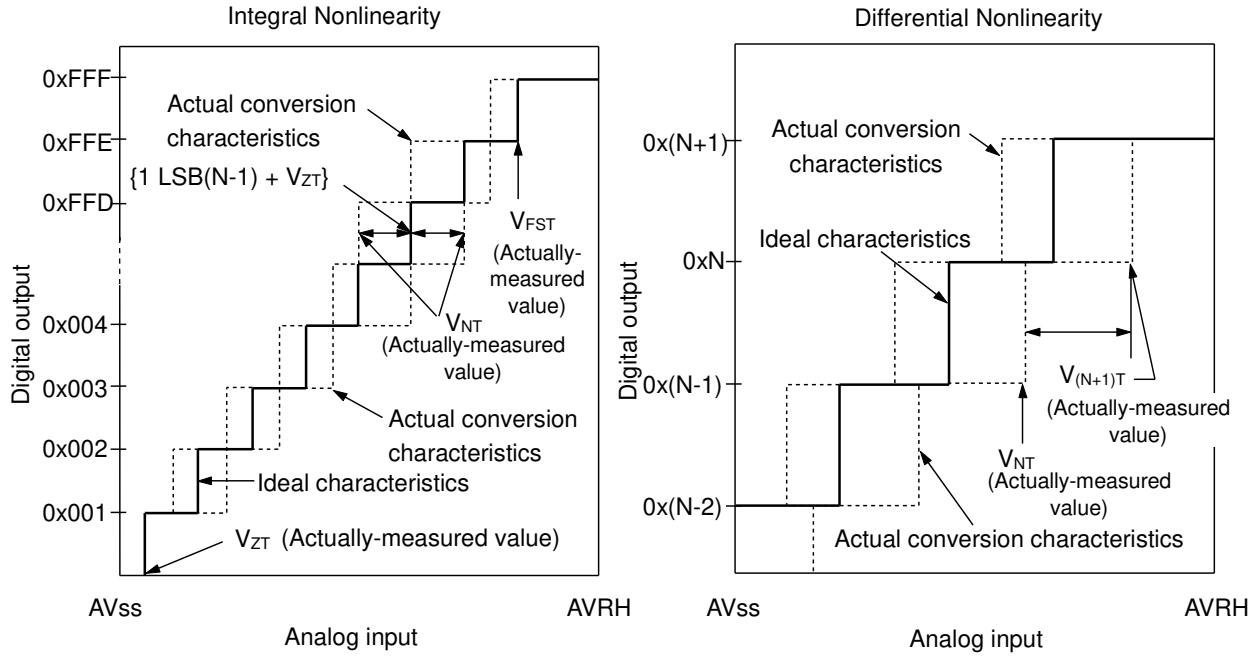
(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

t_{CCK}: Compare clock cycle

Definition of 12-bit A/D Converter Terms

- **Resolution:** Analog variation that is recognized by an A/D converter.
- **Integral Nonlinearity:** Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- **Differential Nonlinearity:** Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



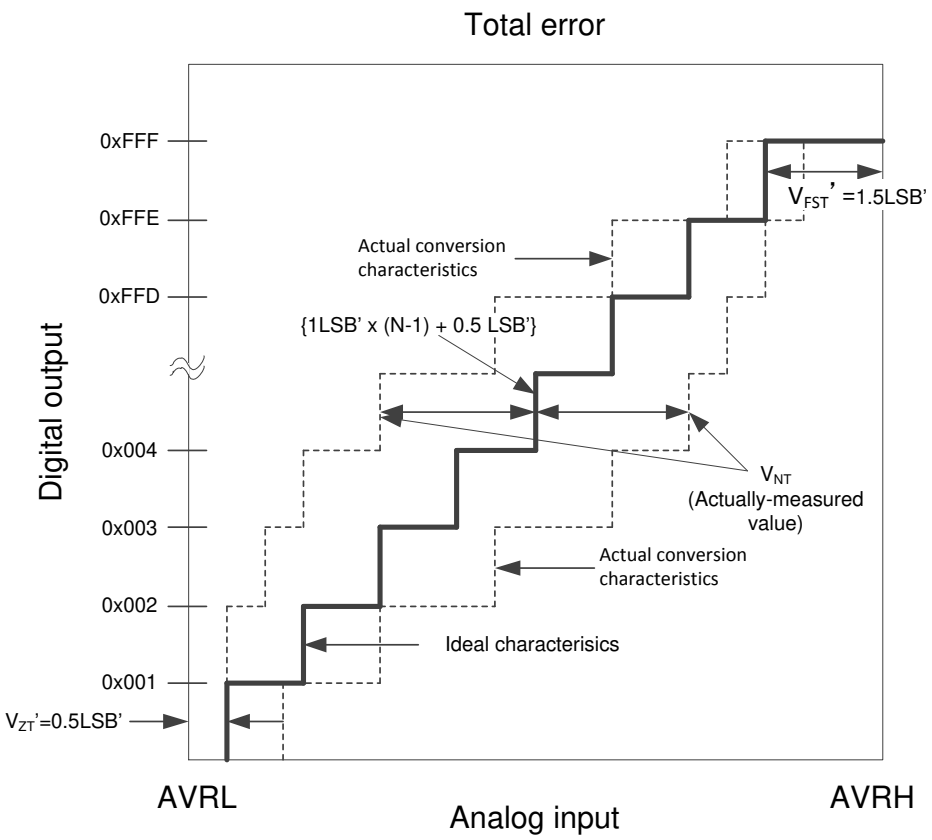
$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

■Total error: A difference between actual value and theoretical value.
The overall error includes zero-transition voltage, full-scale transition voltage and linearity error.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N-1) + 0.5\ LSB'\}}{1\ LSB'} \quad [LSB]$$

$$1\ LSB'\ (\text{ideal value}) = \frac{AVRH - AVRL}{4096} \quad [V]$$

V_{ZT}' (ideal value) = AVRL + 0.5 LSB' [V]

V_{FST}' (ideal value) = AVRH - 1.5 LSB' [V]

V_{NT}' : A voltage for causing transition of digital output from (N-1) to N

12.6 USB Characteristics

(V_{CC} = 3.0V to 3.6V, V_{SS} = 0V)

Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0/ UDM0	-	2.0	V_{CC} + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output H level voltage	V_{OH}		External pull-up resistance = 15kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistance = 15kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full-Speed	4	20	ns	*5
	Falling time	t_{FF}		Full-Speed	4	20	ns	*5
	Rising/falling time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rising time	t_{LR}		Low-Speed	75	300	ns	*7
	Falling time	t_{LF}		Low-Speed	75	300	ns	*7
	Rising/falling time matching	t_{LRFM}		Low-Speed	80	125	%	*7

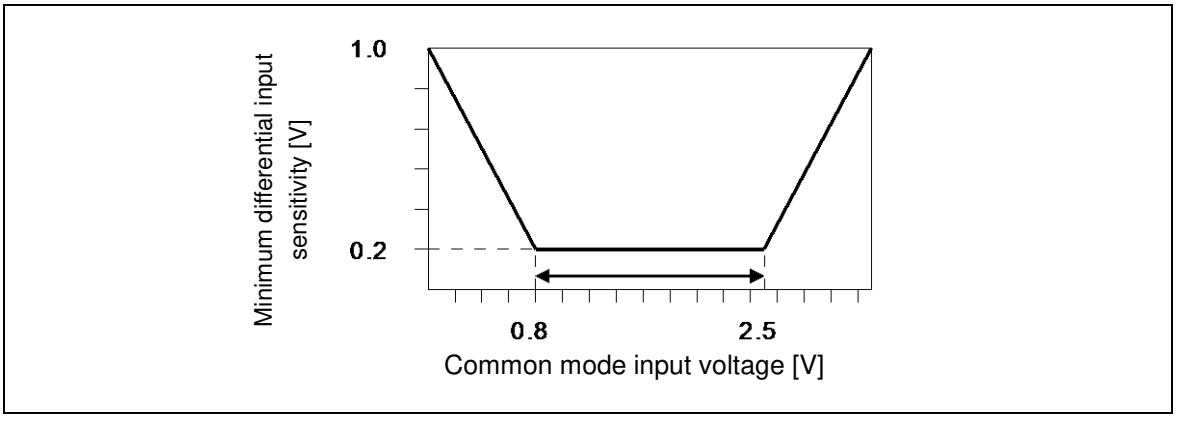
*1: The switching threshold voltage of Single-end-receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 V, V_{IH} (Min) = 2.0 V (TTL input standard).

There are some hysteresis to lower noise sensitivity.

*2: Use differential-Receiver to receive USB differential data signal.

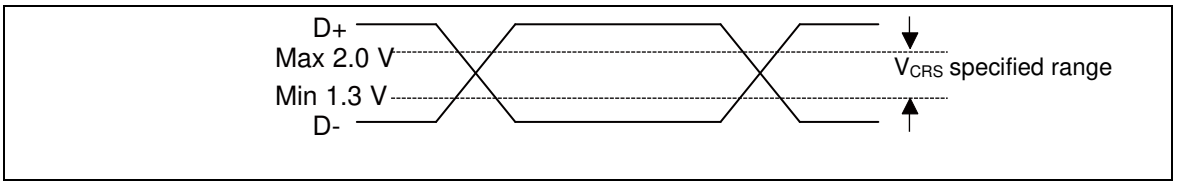
Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.

Above voltage range is the common mode input voltage range.

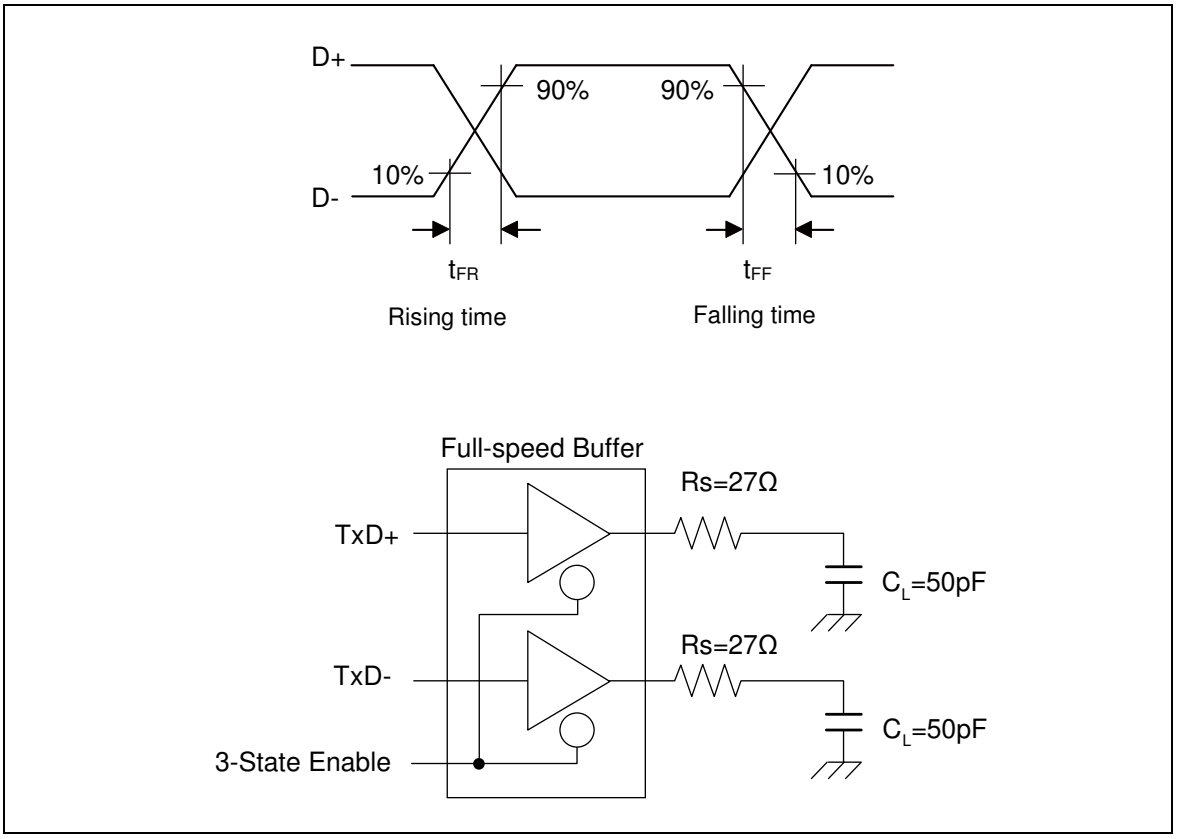


*3: The output drive capability of the driver is below 0.3 V at Low-state (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the V_{SS} and 15 kΩ load) at High-State (V_{OH}).

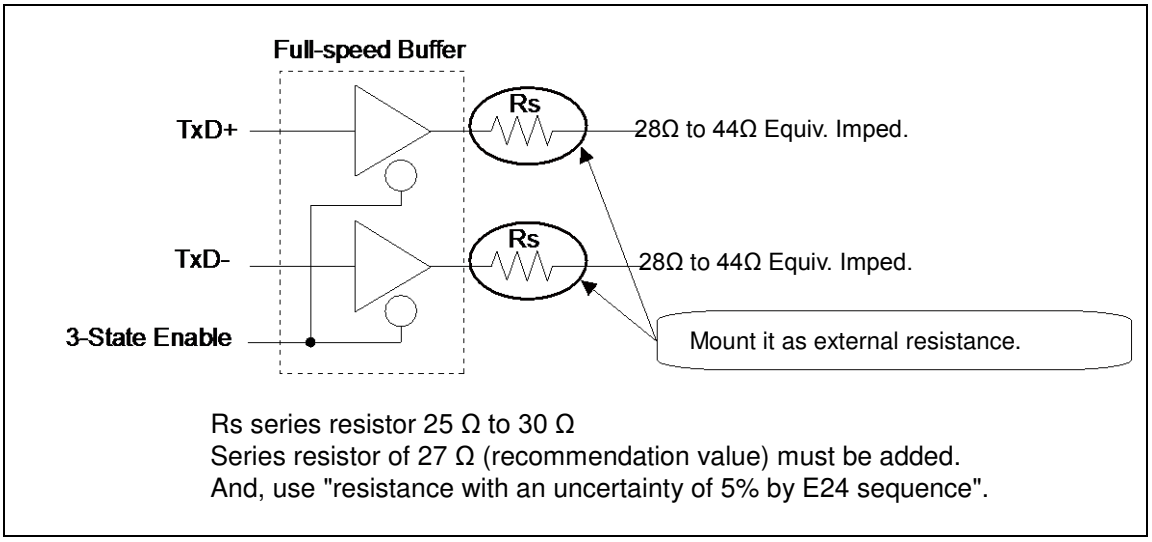
*4: The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 V to 2.0 V.



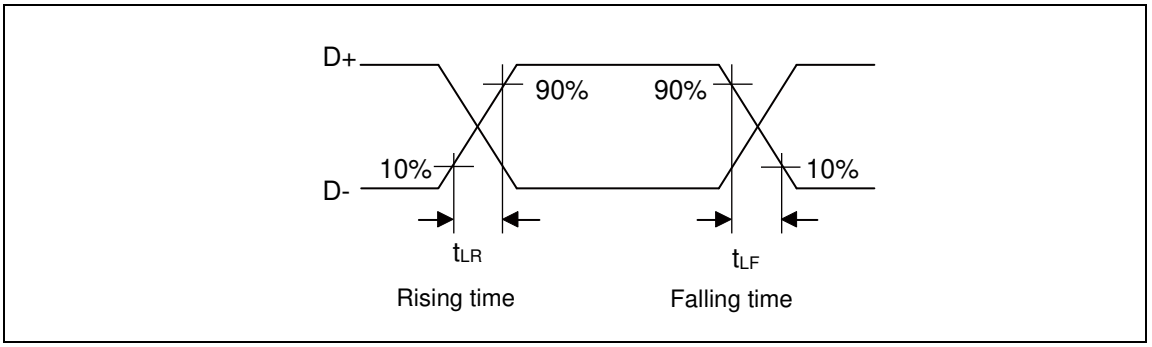
*5: They indicate Rising time (t_{FR}) and Falling time (t_{FF}) of the Full-speed differential data signal.
They are defined by the time between 10 % and 90 % of the output signal voltage.
For Full-speed buffer, t_{FR}/t_{FF} ratio is regulated as within ± 10 % to minimize RFI emission.



*6: USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15 % characteristic impedance (Differential Mode).
USB standard defines that output impedance of USB driver must be in range from 28 Ω to 44 Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommendation value 27 Ω) Series resistor Rs.



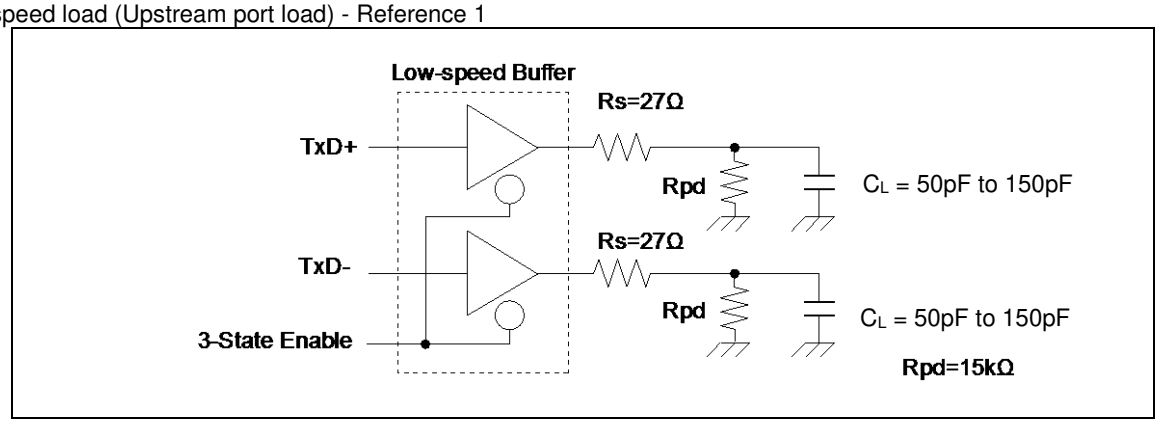
*7: They indicate rising time (t_{LR}) and Falling time (t_{LF}) of the Low-speed differential data signal.
They are defined by the time between 10 % and 90 % of the output signal voltage.



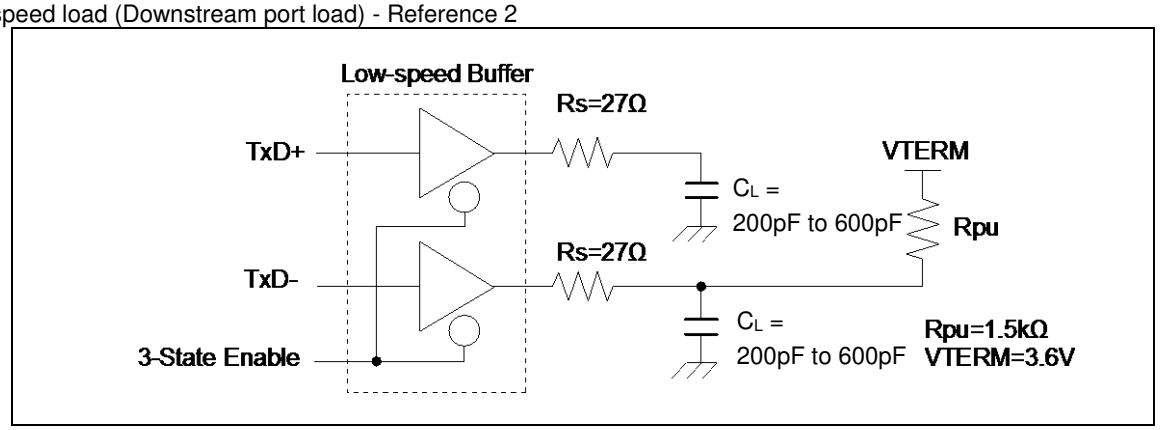
Note:

- *See Low-speed load (Compliance load) for conditions of external load.*

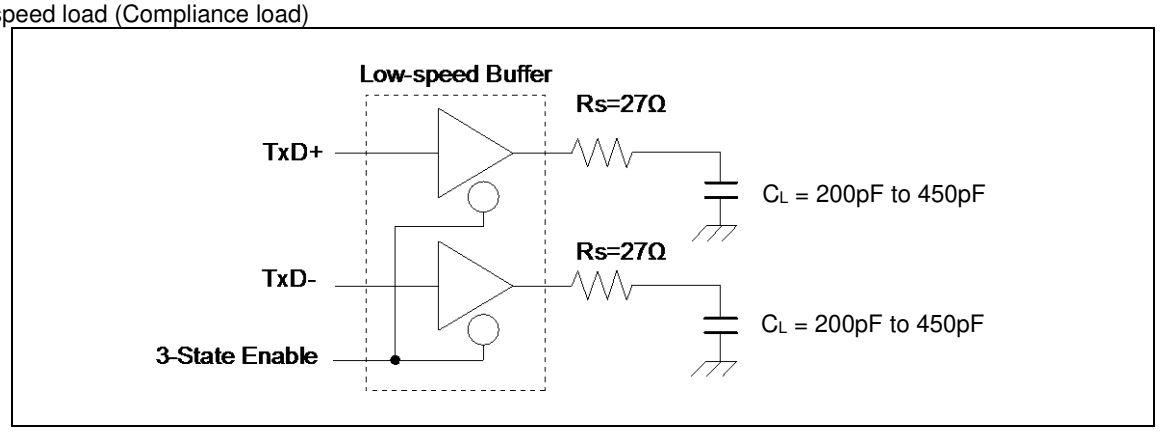
■Low-speed load (Upstream port load) - Reference 1



■Low-speed load (Downstream port load) - Reference 2



■Low-speed load (Compliance load)



12.7 Low-Voltage Detection Characteristics

12.7.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.46	2.55	2.64	V	When voltage drops
Released voltage	VDH	-	2.51	2.60	2.69	V	When voltage rises

12.7.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.80	2.90	3.00	V	When voltage drops
Released voltage	VDH		2.90	3.00	3.11	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.99	3.10	3.21	V	When voltage drops
Released voltage	VDH		3.09	3.20	3.31	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	3.18	3.30	3.42	V	When voltage drops
Released voltage	VDH		3.28	3.40	3.52	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	$4800 \times t_{CYCP}$*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.8 MainFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector	-	0.3	1.1	s	
Half word (16-bit) write time	Write cycles ≤ 100 times	-	12	100	µs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time		-	6.6	31	s	Includes write time prior to internal erase

Write Cycles and Data Hold Time

Erase/Write Cycles (cycle)	Data Hold Time (year)
1,000	20*
10,000	10*
100,000	5*

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

12.9 VFLASH Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (4 KB)	-	50	450	ms	
Block Erase Time (64 KB)	-	500	2000	ms	
Page Program Time	-	0.7	3	ms	
Chip erase time	-	11.2	64	s	

Erase Endurance

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Erase per sector	100k	-	-	cycle	

*: Data retention of 20 years is based on 1k erase cycle or less.

12.10 Standby Recovery Time

12.10.1 Recovery Cause: Interrupt/WKUP

The time from recovery cause reception of the internal circuit to the program operation start is shown.

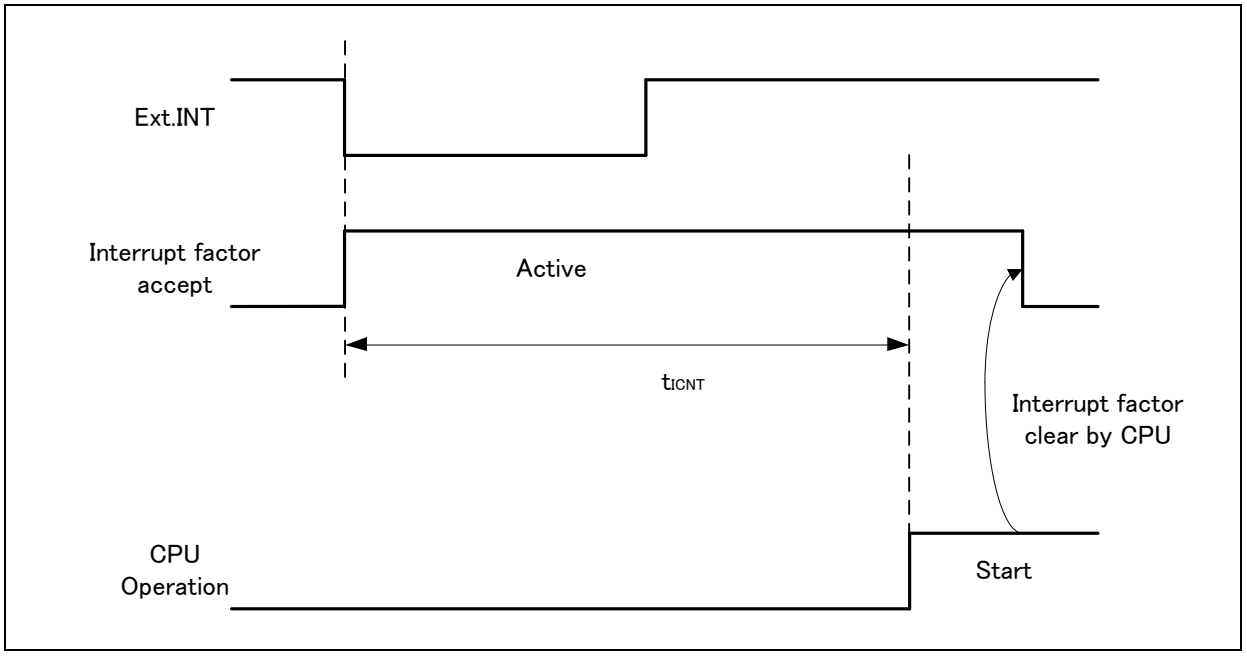
Recovery Count Time

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR timer mode		450	900	µs	
Sub timer mode		896	1136	µs	
RTC mode Stop mode (High-speed CR /Main/PLL run mode return)		316	581	µs	
RTC mode Stop mode (Low-speed CR/sub run mode return)		270	540	µs	
Deep standby RTC mode		365	667	µs	without RAM retention
Deep standby Stop mode		365	667	µs	with RAM retention

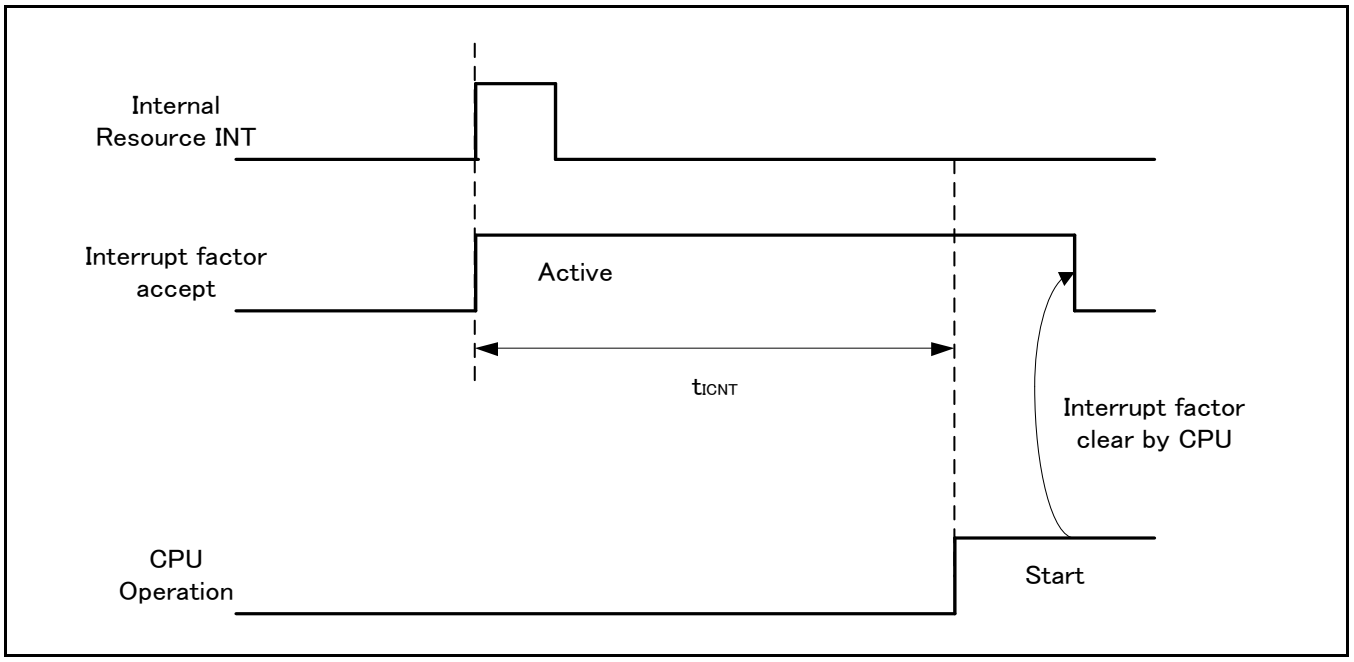
*: The maximum value depends on the built-in CR accuracy.

Example of standby recovery operation (when in external interrupt recovery*)



*: External interrupt is set to detecting fall edge.

Example of Standby Recovery Operation (when in Internal Resource Interrupt Recovery*)



*: Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See Chapter 6: The return factor from each low power consumption modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- *When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode" in "FM4 Family Peripheral Manual Main part (002-04856).*

12.10.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

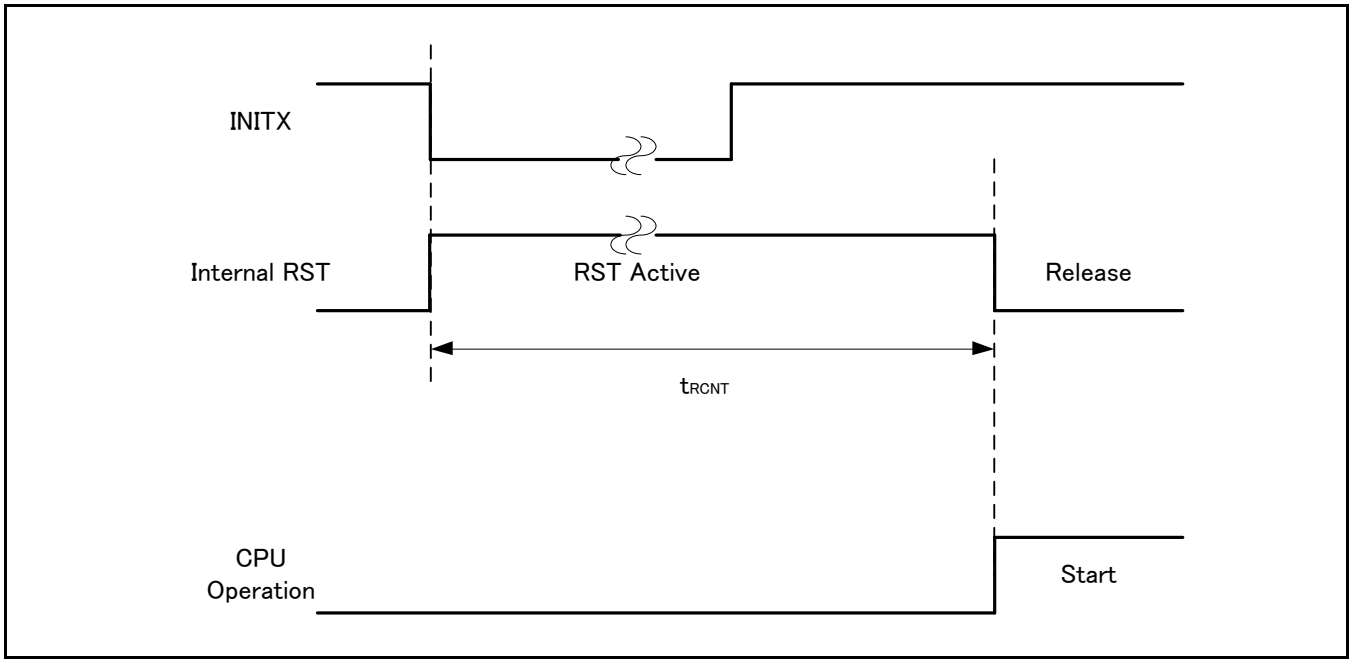
Recovery Count Time

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

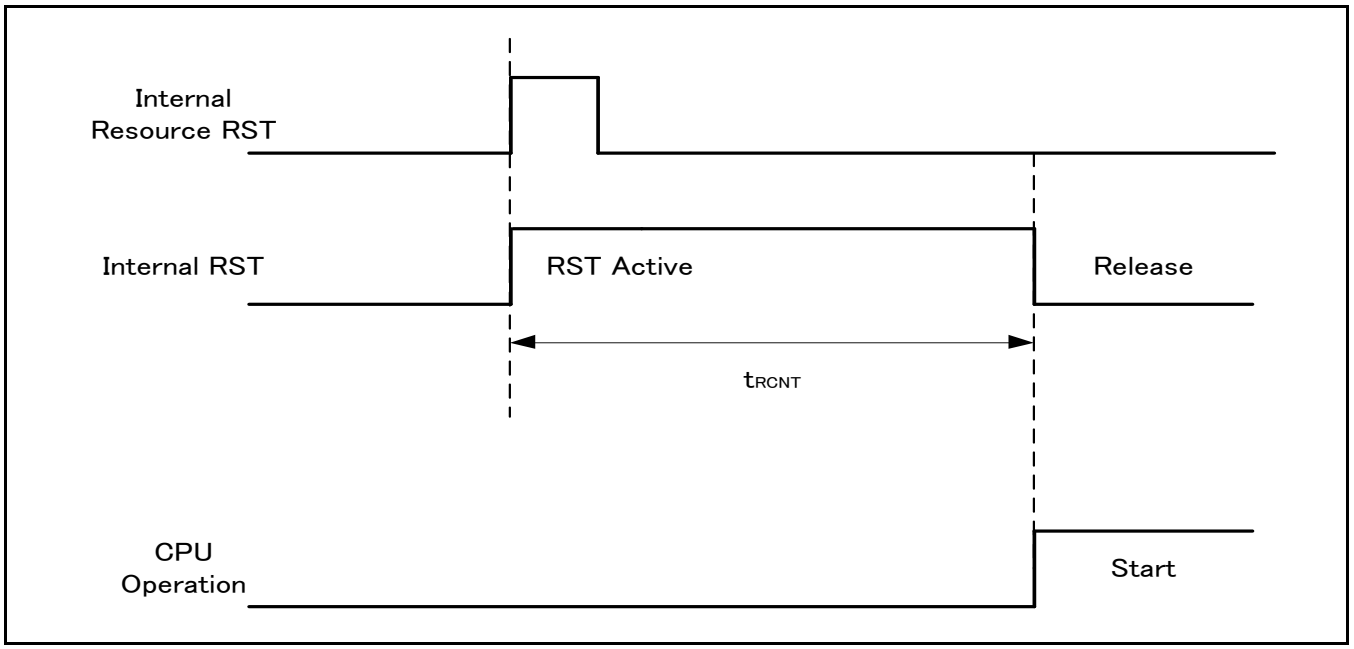
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	155	266	µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	µs	
Low-speed CR timer mode		315	567	µs	
Sub timer mode		315	567	µs	
RTC mode Stop mode		315	567	µs	
Deep standby RTC mode		336	667	µs	without RAM retention
Deep standby Stop mode		336	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)



Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)



*: Depending on the Low-Power consumption mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

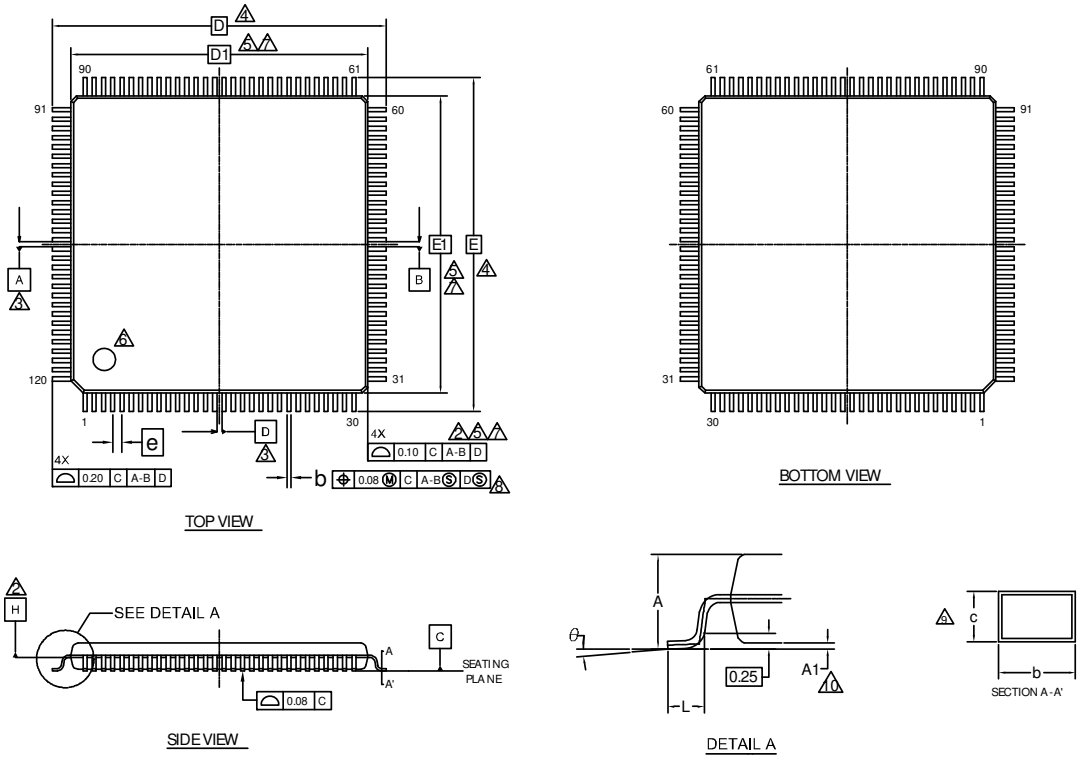
- *The return factor is different in each low power consumption mode.*
  See Chapter 6: The return factor from each low power consumption modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- *The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856)*
- *When the power-on reset/low-voltage detection reset, they are not included in the return factor. See 12.4.8 Power-on Reset Timing.*
- *In recovering from reset, CPU changes to High-speed Run mode. In the case of using the main clock and PLL clock, they need further main clock oscillation stabilization wait time and oscillation stabilization wait time of Main PLL clock.*
- *Internal resource reset indicates Watchdog reset and CSV reset.*

13. Ordering Information

Part Number	Package
S6E2DF5G0AGV20000	Plastic・LQFP (0.5 mm pitch), 120 pin (LQM120)
S6E2DF5GJAMV20000	
S6E2DF5J0AGV2000A	Plastic・LQFP (0.5 mm pitch), 176 pin (LQP176)
S6E2DF5G0AGB3000A	Plastic・FBGA (0.5 mm pitch), 161 pin (FDJ161)
S6E2DF5G0AGE20000	Plastic・Ex-LQFP (0.5 mm pitch), 120 pin (LEM120)

14. Package Dimensions

Package Type	Package Code
LQFP 120	LQM 120



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D	18.00 BSC		
D1	16.00 BSC		
e	0.50 BSC		
E	18.00 BSC		
E1	16.00 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

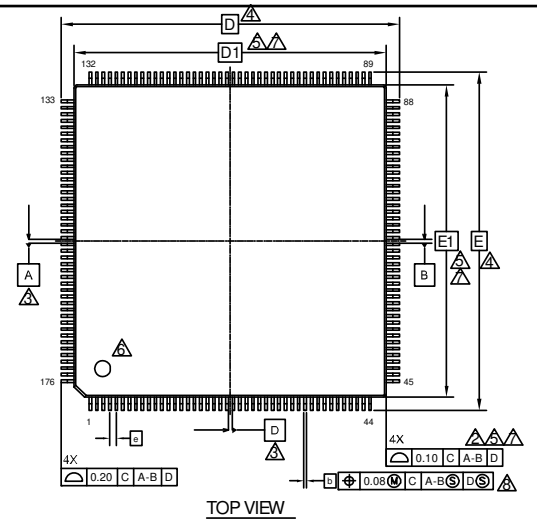
NOTES

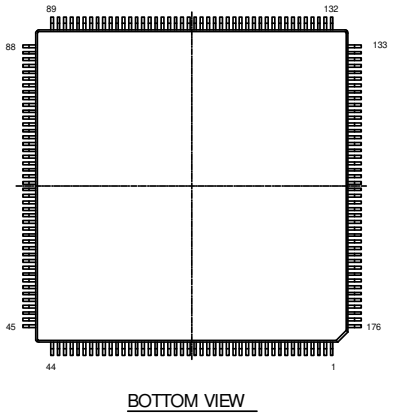
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

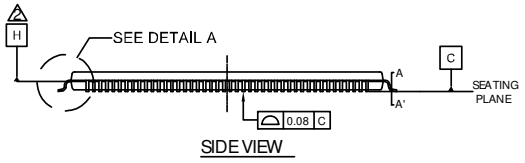
002-16172 **

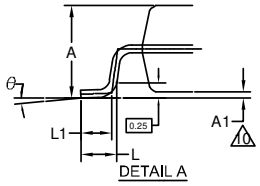
PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**

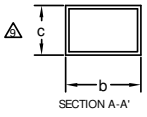
Package Type	Package Code
LQFP 176	LQP 176











SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC		
D1	24.00 BSC		
e	0.50 BSC		
E	26.00 BSC		
E1	24.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

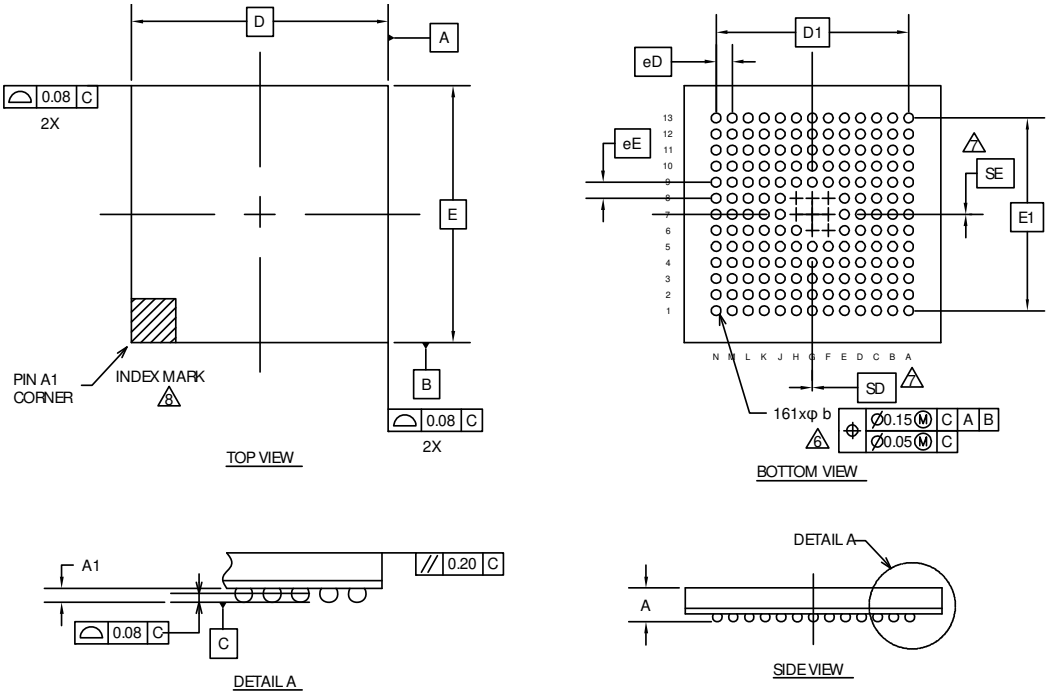
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15150 **

PACKAGE OUTLINE, 176 LEAD LQFP
24.0X24.0X1.7 MM LQP176 REV**

Package Type	Package Code
FBGA 161	FDJ 161



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.20	0.25	0.30
D		8.00 BSC	
E		8.00 BSC	
D1		6.00 BSC	
E1		6.00 BSC	
MD		13	
ME		13	
n		161	
Øb	0.25	0.30	0.35
eD		0.50 BSC	
eE		0.50 BSC	
SD / SE		0.00	

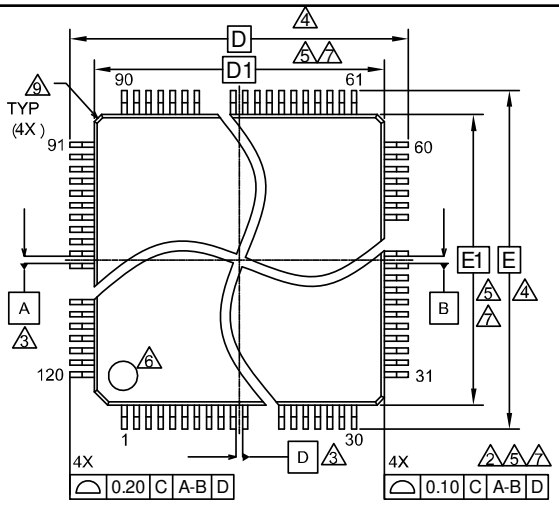
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. JEDEC SPECIFICATION NO. REF: N/A.

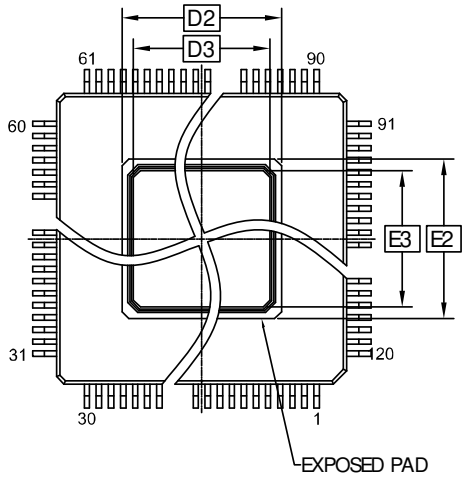
PACKAGE OUTLINE, 161 BALL FBGA
8.00X8.00X1.20 MM FDJ161 REV**

002-16413 **

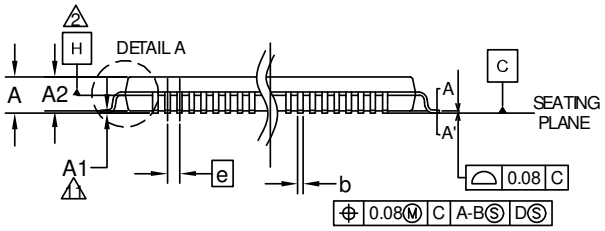
Package Type	Package Code
Ex-LQFP 120	LEM 120



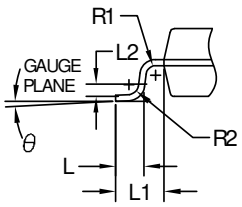
TOP VIEW



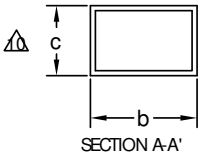
BOTTOM VIEW



SIDE VIEW



DETAIL A



SECTION A-A'

SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
A2	1.35	1.40	1.45
D		18.00 BSC.	
D1		16.00 BSC.	
D2		6.50 REF	
D3		5.30 REF	
E		18.00 BSC.	
E1		16.00 BSC.	
E2		6.50 REF	
E3		5.30 REF	
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	4°	8°
c	0.09	—	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L1		1.00 REF	
L2		0.25	
e		0.50 BSC.	

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-12611 **

PACKAGE OUTLINE, 120 LEAD TEQFP
16.0X16.0X1.7 MM LEM120 REV**

15. Errata

This chapter describes the errata for S6E2DF series. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

15.1 Part Numbers Affected

Part Number
S6E2DF5J0AGV20000, S6E2DF5J0AGV2000A

15.2 Qualification Status

Product Status: In Production

15.3 Errata Summary

This table defines the errata applicability to available devices.

Items	Part Number	Silicon Revision	Fix Status
SDRAM cannot be used as destination buffer of the GDC	Refer to 15.1	Rev A	No silicon fix planned. Workaround required.

SDRAM cannot be used as destination buffer of the GDC

1. PROBLEM DEFINITION

   Unnecessary data is written on the before and after the correct addresses if the GDC writes data to the external SDRAM, the CPU's internal SRAM0, SRAM2, or any memory devices connected to the External Bus Interface.

2. PARAMETERS AFFECTED

   N/A

3. TRIGGER CONDITION(S)

   The GDC generates either write data that is NOT size of multiples of 8 bytes multiplied by Burst Length or write address that is NOT aligned with 8 bytes multiplied by Burst Length to the external SDRAM, the CPU's internal SRAM0, SRAM2, or any memory devices connected to the External Bus Interface. The Burst Length means length of write burst transaction, and you can set it as 2 (16 bytes), or 4 (32 bytes).

4. SCOPE OF IMPACT

   The external SDRAM, the CPU's internal SRAM0, SRAM2, or any memory devices connected to the External Bus Interface cannot be used as destination buffer of the GDC.

5. WORKAROUND

   Keep Write data size and Base address according as following table when the GDC writes to the external SDRAM, the CPU's internal SRAM0, SRAM2, or any memory devices connected to the External Bus Interface.

Burst Length for write access	Write data size	Base address alignment for write data
2	Multiples of 16 bytes	16 bytes aligned address. E.g. 0xB000_0010, 0xB000_0020.
4	Multiples of 32 bytes	32 bytes aligned address. E.g. 0xB000_0020, 0xB000_0040.

6. FIX STATUS

   There is no fix planned. The workaround listed above should be used.

16. Major Changes

Spansion Publication Number: DS709-00031

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
1, 3 13, 14 15 178	Title 3. Product Lineup 4. Packages 15. Ordering Information	Deleted the following products. S6E2DF5JAA/ S6E2DF5GAA
6	2. Features External Bus Interface	Added the following description: ■ Maximum area size : Up to 256 Mbytes ■Modified the following description: ■ 0x6000_0000 to 0xDFFF_FFFF to 0x6000_0000 to 0x7FFF_FFFF
8	2. Features	Modified the ch. Number of I^2C (ch.7→ch.4)
15 16 20 to 52 81 178	4. Packages 5. Pin Assignment 6. Pin Descriptions 14.2. Recommended Operating 15. Ordering Information	Added the Ex-LQFP(TEQFP)(LEM120)
53	7. I/O Circuit Type	Modified the Type-A Circuit
54,55,58	7. I/O Circuit Type	Added the comment in TypeD/E/F/G/N
59	7. I/O Circuit Type	■Modified theType-Q Remarks CMOS level output → CMOS level hysteresis input
67	10. Block Diagram	Deleted the following products. ■S6E2DF5JAA/ S6E2DF5GAA
68	12. Memory Map	Modified the External Device Area / GDC Area
80 165	14.2. Recommended Operating 14.5 12-bit A/D Converter	Added the AVRL in Analog reference voltage.
82	14.2. Recommended Operating	Modified the TBD in Current Value Added the Note
84 to 93	14.3.1 Current Rating	Modified the TBD in Max spec Added the comment of VFLASH memory
93	14.3.1 Current Rating Table 14-11	Added the VFLASH memory current
95	14.4 AC Characteristics 14.4.1 Main Clock Input	Added the Master clock
97	14.4 AC Characteristics 14.4.5 Operating Conditions	Modified the I^2S PLL frequency (307.2→384) Modified the GDC clock frequency (400→160)
165	14.5 12-bit A/D Converter	Modified the Spec Modified the comment of Conversion time
172	14.7.2 Interrupt of Low-Voltage Detection	Modified the max value in LVD stabilization wait time. (6000→4800)
173	14.9 VFLASH Memory	Added the new
178	15. Ordering Information	Modified the Part Number (S6E2DF5G0AGB10000→ S6E2DF5G0AGB30000) Added the Package (Ex_LQFP)
181, 182	16. Package Dimensions	Added the FDJ161/LEM120

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: S6E2DF Series 32-bit ARM® Cortex®-M4F, FM4 Microcontroller
Document Number: 002-05042

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	AKIH	04/21/2015	New Spec.
*A	5123103	SHOY	03/04/2016	Added CCS/CCB settings in 7. HandlingDevices (Page58) and Table 12-10 Typical…*6,*7 (page 85). Changed PN: S6E2DH5G0AGZ20000 to S6E2DH5G0AGE20000 in 13. Ordering… (Page 174). Changed “GE_SPCSX_0” to “GE_SPCSX0” in 3. PinAssignment (Page 9, 11), 4. PinDescriptions (Page16, 42), 8. BlockDiagram (Page 61) and 12.4.22 GDC: … (Page 156,157) Changed “GE_HBCSX_0” to “GE_HBCSX0” in 3. PinAssignment (Page 9, 11), 4. PinDescriptions (Page 16, 42) , 8. BlockDiagram (Page 61) and 12.4.23 GDC: ... (Page 158,159) Changed “GE_HBCSX_1” to “GE_HBCSX1” in 3. PinAssignment (Page 9, 11), 4. PinDescriptions (Page 14, 42), 8. BlockDiagram (Page 61) and 12.4.23 GDC: … (Page 158,159) Updated VFLASH memory Standby current value to 35uA in Table 12-11 Typical… (Page 86). Changed “Ex_LQFP” to “Ex-LQFP” in 2. Packages (Page 8), 4. Pin Descriptions (Page 13 to 46), 12.2 Recommended… (Page 74) and 13. Ordering… (Page 174). Changed “VMAKEUP” to “VWAKEUP” in 8. BlockDiagram (Page 61). Changed “HW flow control (ch. 4, 5)” to “HW flow control (ch. 4)” in 8. BlockDiagram (Page 61). Added “(N.C.): Do not connect anything” in 3. Pin Assignment (Page 10). Added the Note in 4. Pin Descriptions (Page 46). Added Function of PNL_TSIG in 4. Pin Descriptions (Page 43). Changed “PFBGA” to “FBGA” in 12.2 Recommended… (Page 74) and 13. Ordering… (Page 174). New added errata in 15. Errata (Page 179 to 180).
*B	5634638	YSKA	02/21/2017	Changed an explanation from “from 01 to 99” to “from 00 to 99” in Real-Time Clock (RTC) (Page 3) of Features. Added an explanation in Notes on Power-on (Page 60) of 7. Handling Devices. Changed “VBAT Power-on Reset” to “Power-on Reset” in List of VBAT Domain Pin Status (Page 71) of 11. Pin Status in Each CPU State, and Added Remark *1. Added Remark *8 in Table 12-10 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode and VBAT (Page 85). Changed Parameter “Power supply rising time (t_{VCCR})” to “Power ramp rate (dV/dt)” in 12.4.8 Power-on Reset Timing, Changed the minimum to 0.6mV/µs, Changed the maximum to 1000mV/µs, and Added Remarks and Note. Deleted setting value “SPI=1” and “MS=0” at using chip select in 12.4.12 CSIO Timing, and Added “MS bit = 0” and “MS bit = 1” on the Figure (P113-120, P129-136).

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				Deleted following Part Numbers from 13. Ordering Information (Page 174). S6E2DF5J0AGV20000, S6E2DF5G0AGB30000 Added following Part Numbers to 13. Ordering Information (Page 174). S6E2DF5J0AGV2000A, S6E2DF5G0AGB3000A Updated figures in 14.Package Dimensions (Page 175 to 178). Added following Part Numbers to 15. Errata (Page 179). S6E2DF5J0AGV2000A Deleted Baud rate spec for High-Speed Synchronous Serial in “12.4.12 CSIO Timing”(Page 121-127)

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