## **SQ4080EY**

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## Automotive N-Channel 150 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY				
V <sub>DS</sub> (V)	150			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.085			
I <sub>D</sub> (A)	19			
Configuration	Single			
Package	SO-8			

#### **FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 %  $R_q$  and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

GO



COMPLIANT HALOGEN

N-Channel MOSFET

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ORDERING INFORMATION					
Package	SO-8				
Lead (Pb)-free and halogen-free	SQ4080EY (for detailed order number please see <u>www.vishav.com/doc?79771</u> )				

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage		V <sub>DS</sub>	150	V		
Gate-source voltage		V <sub>GS</sub>	± 20	V		
Continuous drain current	T <sub>C</sub> = 25 °C	1	18			
	T <sub>C</sub> = 125 °C	I <sub>D</sub>	10			
Continuous source current (diode conduction)		I <sub>S</sub>	6.5	А		
Pulsed drain current <sup>a</sup>		I <sub>DM</sub>	72			
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	20			
Single pulse avalanche energy		E <sub>AS</sub>	20	mJ		
Maximum power dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	PD	7.1	W		
	T <sub>C</sub> = 125 °C	L_D	2.4	٧V		
Operating junction and storage temperature rat	nge	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction to ambient	PCB mount <sup>b</sup>	R <sub>thJA</sub>	85	°C/W	
Junction to case (drain)		R <sub>thJF</sub>	25	C/ VV	

#### Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %

b. When mounted on 1" square PCB (FR4 material)

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		•					
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 250 \mu A$		150	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$		3	4	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 150 V	-	-	1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 150 V, T <sub>J</sub> = 125 °C	-	-	50	μA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 150 V, T <sub>J</sub> = 175 °C	-	-	150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	30	-	-	Α
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A	-	0.070	0.085	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A, T <sub>C</sub> = 125 °C	-	-	0.167	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 10 A, T <sub>C</sub> = 175 °C	-	-	0.220	
Forward Transconductance b	9 <sub>fs</sub>	V <sub>DS</sub>	= 15 V, I <sub>D</sub> = 10 A	-	51	-	S
Dynamic <sup>b</sup>	•				•		
Input Capacitance	C <sub>iss</sub>			-	1100	1590	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	= 0 V V <sub>DS</sub> = 75 V, f = 1 MHz	-	75	130	pF
Reverse Transfer Capacitance	C <sub>rss</sub>	1		-	33	55	
Total Gate Charge <sup>c</sup>	Qg			-	25	33	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 10 V$	$V_{DS} = 75 \text{ V}, \text{ I}_{D} = 5 \text{ A}$	-	5.2	-	nC
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>	1		-	8.7	-	1
Gate Resistance	Rg		f = 1 MHz		0.4	1	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	$V_{DD} = 20 \text{ V}, \text{ R}_{\text{L}} = 20 \Omega$ $\text{I}_{\text{D}} \cong 1 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 6 \Omega$		-	11.4	15	
Rise Time <sup>c</sup>	tr			-	3.2	4.5	ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	19.1	25	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	2.5	3.2	
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>						
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	72	Α
Forward Voltage	V <sub>SD</sub>	$I_{\rm F} = 3.5  \rm A,  V_{\rm GS} = 0$			0.75	1.1	V

Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

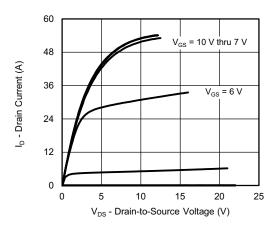
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

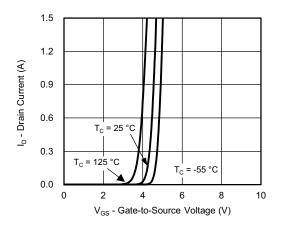


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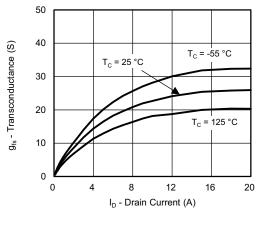
### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



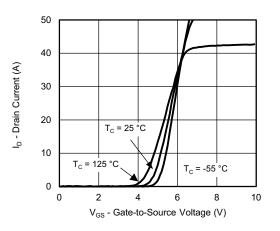
**Output Characteristics** 



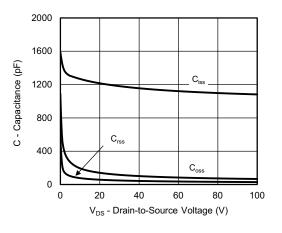
**Transfer Characteristics** 



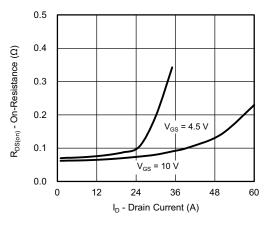
Transconductance



**Transfer Characteristics** 



Capacitance



**On-Resistance vs. Drain Current** 

S22-0060-Rev. B, 24-Jan-2022

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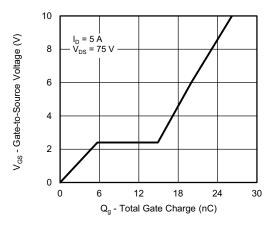
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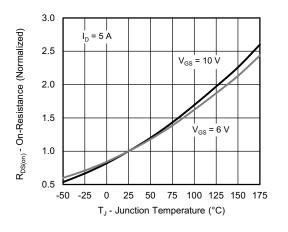
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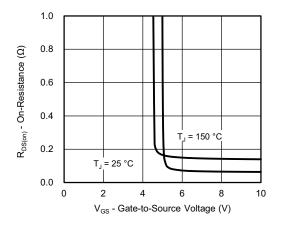
## **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



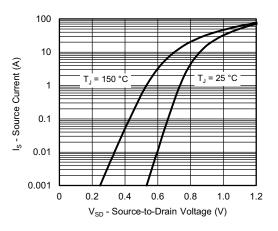
Gate Charge



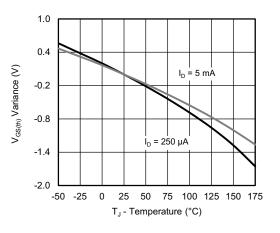
**On-Resistance vs. Junction Temperature** 



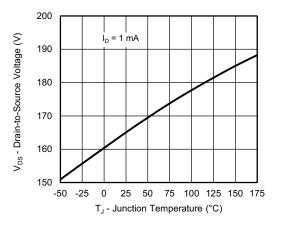
**On-Resistance vs. Gate-to-Source Voltage** 



Source Drain Diode Forward Voltage



**Threshold Voltage** 



Drain Source Breakdown vs. Junction Temperature

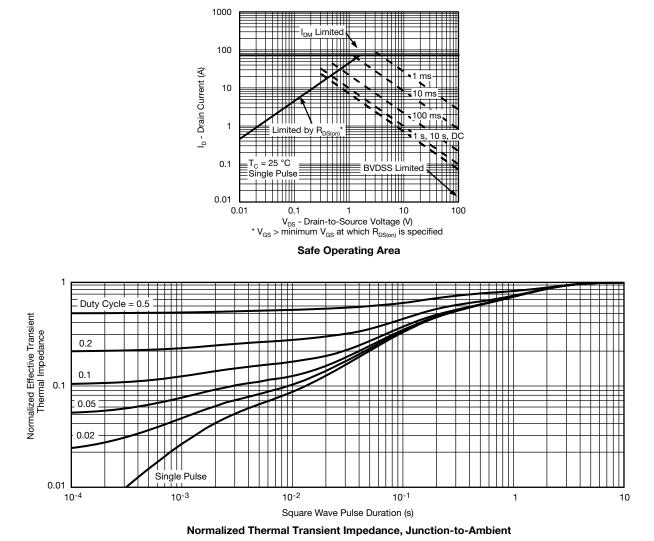
4

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#### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



#### Note

· The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

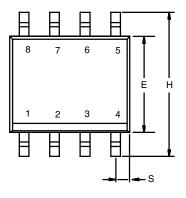
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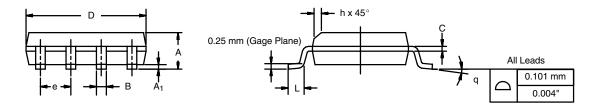


# Package Information

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# SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIM	IETERS	INCHES		
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

## **Application Note 826**

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**RECOMMENDED MINIMUM PADS FOR SO-8** 



Recommended Minimum Pads Dimensions in Inches/(mm)

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