



Z90233, Z90234, and Z90231

***eZVision 200 Television
Controllers with OSD***

Product Specification

PS010703-0502



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ZiLOG Worldwide Headquarters

532 Race Street
San Jose, CA 95126-3432
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com

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The Z90233/Z90234 and Z90231 are the ROM and OTP versions of the eZVision 200 television controller with OSD. Based on ZiLOG's powerful Z8 architecture, the Z90233/Z90234 and Z90231 contain 24 KB of program memory. The following enhanced features are included:

- Flexible inter-row spacing
- Higher character cell resolution (14 x 18)
- Background mesh effect
- Dedicated infrared capture registers
- On-chip analog-to-digital converter
- Hardware master mode I²C interface

The familiar Z8 architecture, in combination with these advanced features, makes the eZVision 200 an ideal choice for midrange televisions in both PAL and NTSC markets.

The eZVision 200 family consists of three basic device types:

- The Z90233 and Z90234 masked ROM
- The Z90231 OTP
- The Z90239 In-Circuit Emulator (ICE) chip

The OTP supports a field-programmable 24 KB program ROM. The ICE chip is used in the Z90239 emulator and protopak. The Z90233/Z90234 masked ROM supports a 16/32-KB system ROM (selectable through a mask option).

The eZVision 200 family takes full advantage of the Z8 microcontroller's expanded register file space to offer greater flexibility in OSD creations that simulate bitmap graphics, icons, and animation.

Product Block Diagram

Figure 1 is the product block diagram for the eZVision 200 television controllers.

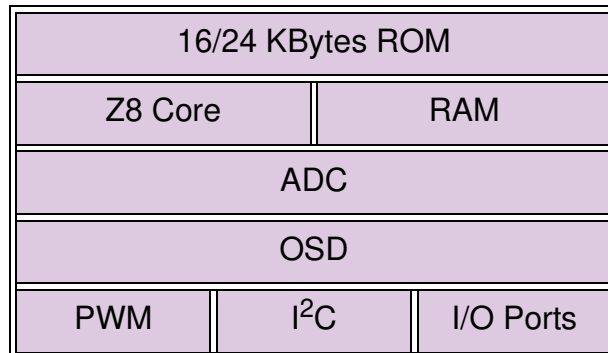


Figure 1. Product Block Diagram

On-Screen Display (OSD) Features

The eZVision 200 television controllers have the following OSD features:

- Displays of up to 10 rows by 24 columns with 256 characters
- Provides character cell resolution of 14 pixels by 18 scan lines
- Offers variable inter-row spacing from 0–15 horizontal scan lines
- Uses color palette table to program foreground and background of character

Microcontroller Features

The eZVision 200 television controllers have the following microcontroller features:

- Incorporates Z8[®] MCU core at 6 MHz
- Z90233 and Z90234 have 16K and 24K masked ROM, respectively
- 236 bytes of system RAM
- Ten 6-bit pulse width modulators
- One 14-bit pulse width modulator
- On-chip infrared (IR) capture registers



- Four channels of 4-bit analog-to-digital converter
- 27 general-purpose I/O pins
- Provides I²C master serial communication port
- 42-pin SDIP and 44-pin PQFP packages
- Can be emulated with 124-pin PGA package (Z90239)

Block Diagram of eZVision 200

Figure 2 is a block diagram of the eZVision 200 family.

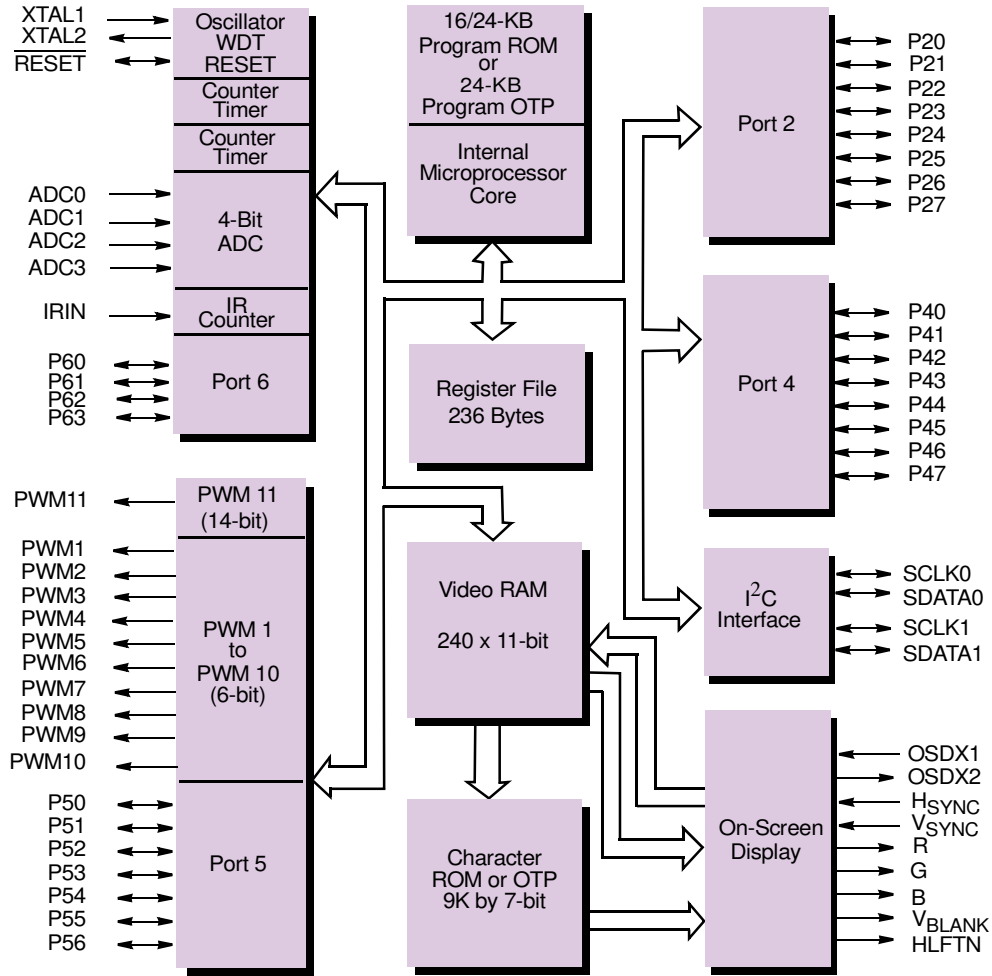


Figure 2. Block Diagram

Pin-Outs and Pin Direction

Figure 3 identifies the pins for the 42-pin shrink dual in-line package (SDIP); Figure 4 on page 6 identifies the pins for the 44-pin plastic quad flat package (PQFP). Table 6 on page 6 describes the pins.

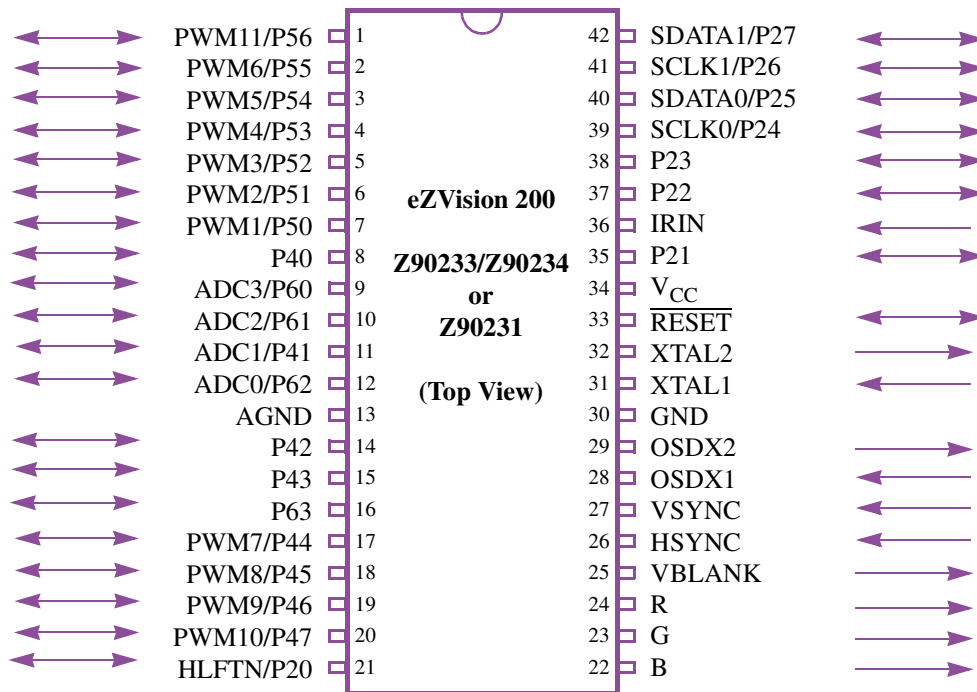


Figure 3. 42-Pin SDIP

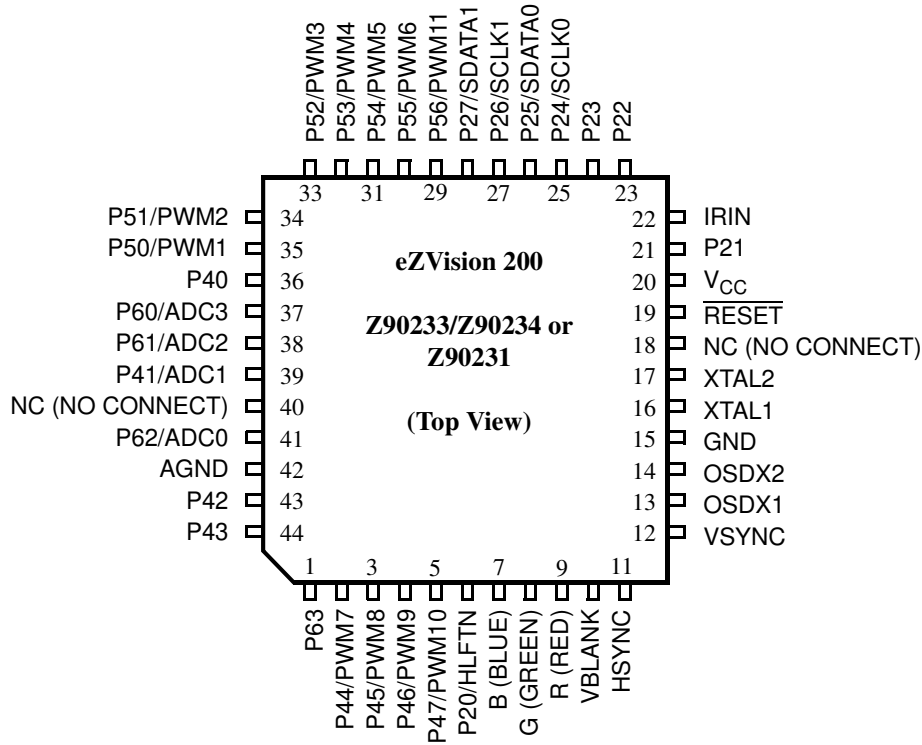


Figure 4. 44-Pin PQFP

Table 6. Pin Descriptions for the Z90233, Z90234, and Z90231

| Name | 42-Pin SDIP Pin Number | 44-Pin PQFP Pin Number | Function | Direction | Reset State |
|-----------------|----------------------------------|------------------------------------|--------------------------------------|-----------|-------------|
| V _{CC} | 34 | 20 | +5 Volts | PWR | PWR |
| GND, AGND | 30, 13 | 15, 42 | 0 Volts | PWR | PWR |
| IRIN | 36 | 22 | Infrared remote capture input | I | I |
| PWM11 | 1 | 29 | 14-bit pulse width modulator output* | O | I |
| PWM10–PWM1 | 20, 19, 18, 17, 2, 3, 4, 5, 6, 7 | 5, 4, 3, 2, 30, 31, 32, 33, 34, 35 | 6-bit pulse width modulator output* | O | I |
| P56–P50 | 7, 6, 5, 4, 3, 2, 1 | 29, 30, 31, 32, 33, 34, 35 | Bit-programmable input/output ports | I/O | I |



Table 6. Pin Descriptions for the Z90233, Z90234, and Z90231 (Continued)

| Name | 42-Pin SDIP Pin Number | 44-Pin PQFP Pin Number | Function | Direction | Reset State |
|-----------|-----------------------------------|----------------------------------|--|-----------|----------------|
| P27–P20 | 42, 41, 40, 39, 38, 37, 35, 21 | 28, 27, 26, 25, 24, 23, 21, 6 | Bit-programmable input/output ports | I/O | I |
| HLFTN | 21 | 6 | Half tone output | O | I |
| SDATA0, 1 | 40, 42 | 26, 28 | I ² C data | I/O | I |
| SCLK0, 1 | 39, 41 | 25, 27 | I ² C clock | I/O | I |
| P63–P60 | 16, 12, 10, 9 | 1, 41, 38, 37 | Bit-programmable input/output ports | I/O | I |
| P47–P40 | 20, 19, 18, 17, 15, 14, 11, 8 | 5, 4, 3, 2, 44, 43, 39, 36 | Bit-programmable input/output ports | I/O | I |
| XTAL1 | 31 | 16 | Crystal oscillator input | I | I |
| XTAL2 | 32 | 17 | Crystal oscillator output | O | O |
| OSDX1 | 28 | 13 | Dot clock oscillator input | I | I |
| OSDX2 | 29 | 14 | Dot clock oscillator output | O | O |
| HSYNC | 26 | 11 | Horizontal sync | I | I |
| VSYNC | 27 | 12 | Vertical sync | I | I |
| VBLANK | 25 | 10 | Video blank | O | O |
| R, G, B | 24, 23, 22 | 9, 8, 7 | Video R, G, B | O | O |
| ADC3–ADC0 | 9, 10, 11, 12 | 37, 38, 39, 41 | 4-bit analog-to-digital converter input | AI | I |
| RESET | 33 | 19 | Device reset | I/O | I |

► **Note:** *These pins are input on POR. They must be configured to be output ports for PWM applications.

Absolute Maximum Ratings

Stresses greater than those listed in Table 7 can cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability.

Table 7. Absolute Maximum Ratings

| Symbol | Parameters | Min | Max | Units | Notes |
|-----------|-----------------------|------|--------------|-------|------------|
| V_{DD} | Power Supply Voltage | -0.3 | +7 | V | |
| V_I | Input Voltage | -0.3 | $V_{DD}+0.3$ | V | |
| V_O | Output Voltage | -0.3 | $V_{DD}+0.3$ | V | |
| I_{OH} | Output Current High | | -10 | mA | per pin |
| I_{OH} | Output Current High | | -100 | mA | per device |
| I_{OL} | Output Current Low | | 20 | mA | per pin |
| I_{OL} | Output Current Low | | 200 | mA | per device |
| T_A | Operating Temperature | 0 | 70 | °C | |
| T_{STG} | Storage Temperature | -55 | 150 | °C | |

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 5).

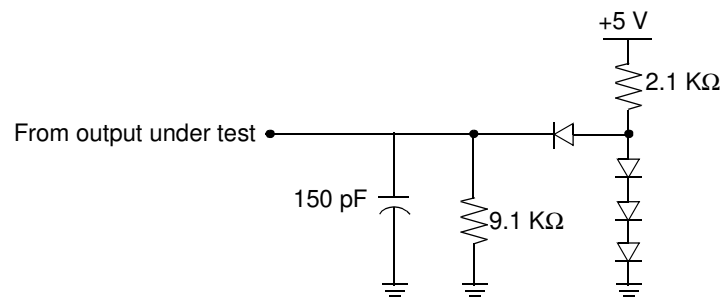


Figure 5. Test Load Diagram



DC Characteristics

Table 8 lists the DC characteristics.

Table 8. DC Characteristics

| Symbol | Parameter | Min | Typical | Max | Units | Conditions |
|--------------|------------------------|--------------|---------|--------------|---------|---------------------------------------|
| V_{DD} | Power Supply Voltage | 4.5 | 5.00 | 5.5 | V | |
| V_{IH} | Input Voltage High | $0.7V_{DD}$ | | V_{DD} | V | |
| V_{IL} | Input Voltage Low | 0 | | $0.2V_{DD}$ | V | |
| V_{IHC} | Input XTAL/Osc in High | $0.7V_{DD}$ | | VCC | V | |
| V_{ILC} | Input XTAL/Osc in Low | 0 | | $0.07V_{DD}$ | V | |
| V_{OH_ST} | Output Voltage High | $V_{DD}-0.4$ | 4.75 | | V | $I_{OH}=-2$ mA for standard drive |
| V_{OL_ST} | Output Voltage Low | | 0.16 | 0.4 | V | $I_{OL}=-2.00$ mA for standard drive |
| V_{OH_LE} | Output Voltage High | | | $V_{DD}-0.4$ | V | $I_{OH}=-0.3$ mA for low EMI drive |
| V_{OL_LE} | Output Voltage Low | 0.4 | | | V | $I_{OL}=0.3$ mA for low EMI drive |
| V_{OH_LE} | Output Voltage High | $V_{DD}-0.4$ | | | V | $I_{OH}=-0.2$ mA for low EMI XTAL/Osc |
| V_{OL_LE} | Output Voltage Low | | | 0.4 | V | $I_{OL}=0.2$ mA for low EMI XTAL/Osc |
| V_{HY} | Schmitt Hysteresis | $0.1V_{DD}$ | 0.8 | | V | |
| I_{IR} | Reset Input Current | | -46 | -80 | μ A | $V_{RL}=0$ V |
| I_{IL} | Input Leakage | -3.0 | 0.01 | 3.0 | μ A | 0 V, V_{DD} |
| I_{OL} | Tri-State Leakage | -3.0 | 0.02 | 3.0 | μ A | 0 V, V_{DD} |
| I_{CC} | Supply Current | | 25 | 40 | mA | All inputs at rail; outputs floating |
| I_{CC1} | HALT Mode Current | | 3.2 | 6 | mA | All inputs at rail; outputs floating |
| I_{CC2} | STOP Mode Current | | | 50 | μ A | All inputs at rail; outputs floating |

Notes: $T_A=0$ °C to +70 °C; $V_{DD}=+4.5$ V to +5.5 V; $F_{OSC}=6$ MHz

Typical values measured at 25 °C.

Minimum and maximum values indicated from 0 °C to 70 °C.



AC Characteristics

Table 9 lists the AC characteristics. Figure 6 shows the AC timing diagram.

Table 9. AC Characteristics

| No. | Symbol | Parameter | Minimum | Maximum | Units |
|-----|--------------------------------|--|-----------|-----------|-------|
| 1 | T_{pC} | Input clock period | 166 | 1000 | ns |
| 2 | T_{rC}, T_{fC} | Clock input rise and fall | | 25 | ns |
| 3 | T_{wC} | Input clock width | 35 | | ns |
| 4 | $T_{wH_{SYNC}L}$ | Timer input low width | 70 | | ns |
| 5 | $T_{wH_{SYNC}H}$ | Timer input high width | $3T_{pC}$ | | |
| 6 | $T_{pH_{SYNC}}$ | Timer input period | $8T_{pC}$ | | |
| 7 | $T_{rH_{SYNC}}, T_{fH_{SYNC}}$ | Timer input rise and fall | | 100 | ns |
| 8 | T_{wIL} | Interrupt request input low | 70 | | ns |
| 9 | T_{wIH} | Interrupt request input high | $3T_{pC}$ | | |
| 10 | T_dPOR | Power-on reset delay | 5 | 25 | ms |
| 11 | $T_dLVIREs$ | Low-voltage detect to internal RESET condition | 200 | | ns |
| 12 | T_wRES | Reset minimum width | $5T_{pC}$ | | |
| 13 | T_dH_sOI | H_{sync} start to V_{OSC} stop | $2T_{pV}$ | $3T_{pV}$ | |
| 14 | T_dH_sOh | H_{sync} start to V_{OSC} start | | $1T_{pV}$ | |

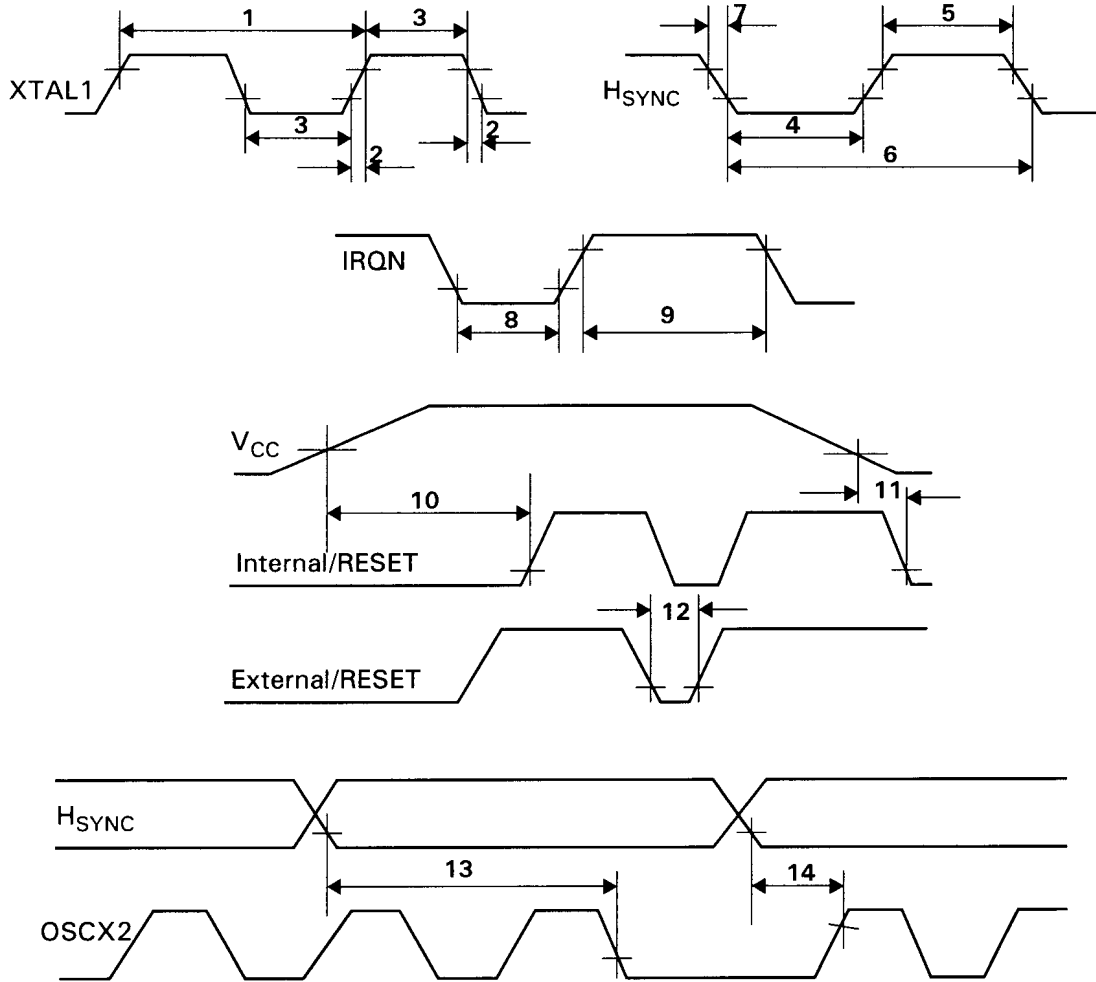


Figure 6. AC Timing Diagram

Development Tools and Support

Available in OTP and masked ROM versions, the Z90231 and Z90233/Z90234 fulfill prototype and production requirements. The Z90231 uses ICEbox™ (In-Circuit Emulator) tools (Z9025900ZEM) to make programming and debugging applications easy and convenient.

The ZiLOG Developer Studio (ZDS) is a complete software program that provides easy code generation and program management.

For code development, ZiLOG offers its specialized application program interface (API) for OSD. The API deals directly with proper sequencing and timing when interfacing with hardware, shielding the user application programmer from tedious and error-prone details.

The Z8933200ZCO, an OSD evaluation board, is used to synchronize the emulator with a video display. Refer to Figure 7 for a suggested code development environment.

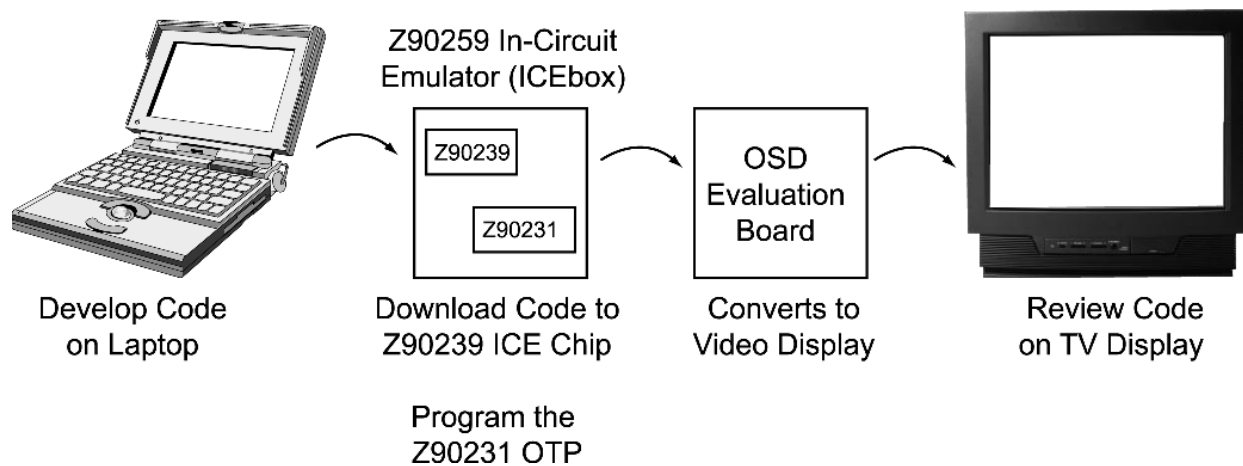


Figure 7. Code Development Environment

ZiLOG also offers the Z9020900TSC Protopak to verify code on a television.



Related Products

Table 10 lists the related TV controllers and vertical blanking interval (VBI) decoders.

Table 10. Related Products

| | |
|--------|--|
| Z9037x | eZVision 300 dual-scan TV controller for progressive scan and standard interlaced scan |
| Z9036x | eZVision 300 advanced TV controller with 32 KWords of ROM |
| Z86129 | eZSelect closed caption decoder (CCD) |
| Z86229 | eZSelect CCD with second I ² C address select |
| Z86131 | eZSelect auto time set |
| Z86130 | eZSelect smart V-chip |
| Z86230 | eZSelect smart V-chip with second I ² C address select |

Electrical Features Summary

- 40 mA maximum supply current
- 4.50 V to 5.50 V operating range



eZVision 200 Device Selection

Table 11 lists the differences among the eZVision 200 family television controllers.

Table 11. eZVision 200 Family Television Controllers

| Device | Application | ROM (Bytes) | RAM (Bytes) | Pkg | I ² C | IR Capture | ADC | Bit I/O (max) | PWM (6/14-bit) |
|--------|------------------------|-------------|-------------|----------------------------|------------------|------------|-------|---------------|----------------|
| Z90233 | TV receiver controller | 16K | 236 | 42-pin SDIP 44-pin PQFP | Yes | Yes | 4 Ch. | 27 | 10/2 |
| Z90234 | TV receiver controller | 24K | 236 | 42-pin SDIP 44-pin PQFP | Yes | Yes | 4 Ch. | 27 | 10/2 |
| Z90231 | TV receiver controller | 24K OTP | 236 | 42-pin SDIP 44-pin PQFP | Yes | Yes | 4 Ch. | 27 | 10/2 |
| Z90255 | TV receiver controller | 32K | 300 | 42-pin SDIP | Yes | Yes | 4 Ch. | 27 | 10/2 |
| Z90251 | TV receiver controller | 32K OTP | 300 | 42-pin SDIP | Yes | Yes | 4 Ch. | 27 | 10/2 |



Ordering Information

Table 12 lists the ordering information for the eZVision 200 television controllers.

Table 12. Ordering Information

| Part | PSI | Description |
|-------------|--|--|
| Z90233 | Z9023306PSC Rxxxx* Z9023306FSC Rxxxx* | 16 KB masked ROM 42 SDIP 16 KB masked ROM 44 PQFP |
| Z90234 | Z9023406PSC Rxxxx* Z9023406FSC Rxxxx* | 24 KB masked ROM 42 SDIP 24 KB masked ROM 44 PQFP |
| Z90231 | Z9023106PSC Z9023106FSC | 24 KB OTP 42 SDIP 24 KB OTP 44 PQFP |
| Z90251 | Z9025106PSC | 32 KB OTP TV controller |
| Z90255 | Z9025506PSC Rxxxx* | 32 KB masked ROM TV controller |
| Z9025900ZEM | Z9025900ZEM | Emulator/programmer |
| Z9020900TSC | Z9020900TSC | Protopak |
| Z8933200ZCO | Z8933200ZCO | OSD evaluation board |

* xxxx is a unique ROM number assigned to each customer code.