Product Brief

MCF5275PB/D
Rev. 0, 4/2004

MCF5275 Family Integrated Microprocessor Product Brief

The MCF5275 family is a highly integrated implementation of the ColdFire® family of reduced instruction set computing (RISC) microprocessors. This document describes pertinent electrical and physical characteristics of the MCF5275 family. The MCF5275 family includes the MCF5275, MCF5275L, MCF5274 and MCF5274L microprocessors. The differences between these parts are summarized below in Table 1. This document is written from the perspective of the MCF5275 and unless otherwise noted, the information applies also to the MCF5275L, MCF5274 and MCF5274L.

The MCF5275 family delivers a new level of performance and integration on the popular version 2 ColdFire core with over 144 (Dhrystone 2.1) MIPS @ 150 MHz. These highly integrated microprocessors build upon the widely used peripheral mix on the popular MCF5272 ColdFire microprocessor (10/100 Mbps Ethernet MAC and USB device) by adding a second 10/100 Mbps Ethernet MAC (MCF5274 & MCF5275) and hardware encryption (MCF5275L and MCF5275). In addition, the MCF5275 family features an enhanced Multiply Accumulate Unit (EMAC), large on-chip memory (64 Kbytes SRAM, 16 Kbytes configurable cache), and a 16-bit DDR SDRAM memory controller.

These devices are ideal for cost-sensitive applications requiring significant control processing for file management, connectivity, data buffering, and user interface, as well as signal processing in a variety of key markets such as security, imaging, networking, gaming, and medical. This leading package of integration and high performance allows fast time to market through easy code reuse and extensive third party tool support.

To locate any published errata or updates for this document, refer to the ColdFire products website at http://www.motorola.com/coldfire.

Table 1. Comparison of the MCF5275 Family Configurations

Module	5274L	5275L	5274	5275
ColdFire Version 2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	x	x	x	x
System Clock	up to 150 MHz			
Performance Dhrystone/MIPS	144/2.1			
Instruction/Data Cache	16 Kbytes (configurable)			
Static RAM (SRAM)	64 Kbytes			
Interrupt Controllers (INTC)	2	2	2	2
Edge Port Module (EPORT)	x	x	x	x
External Interface Module (EIM)	x	x	x	x

Table 1. Comparison of the MCF5275 Family Configurations

Module	5274L	5275L	5274	5275
4-channel Direct-Memory Access (DMA)	x	x	x	x
DDR SDRAM Controller	x	x	x	x
Fast Ethernet Controller (FEC)	1	1	2	2
Watchdog Timer Module (WDT)	x	x	x	x
4-channel Programmable Interval Timer Module (PIT)	x	x	x	x
32-bit DMA Timers	4	4	4	4
USB	x	x	x	x
QSPI	x	x	x	x
UART(s)	3	3	3	3
I^2C	x	x	x	x
PWM	4	4	4	4
General Purpose I/O Module (GPIO)	x	x	x	x
CIM = Chip Configuration Module + Reset Controller Module	x	x	x	x
Debug BDM	x	x	x	x
JTAG - IEEE 1149.1 Test Access Port	x	x	x	x
Cryptography - Security module for data packet processing	—	x	—	x
Package	196 MAPBGA	196 MAPBGA	256 MAPBGA	256 MAPBGA

1.1 Block Diagram

The superset device in the MCF5275 family is the MCF5275. It comes in a 256 Mold Array Process Ball Grid Array (MAPBGA) package. Figure 2 shows a top-level block diagram of the MCF5275.

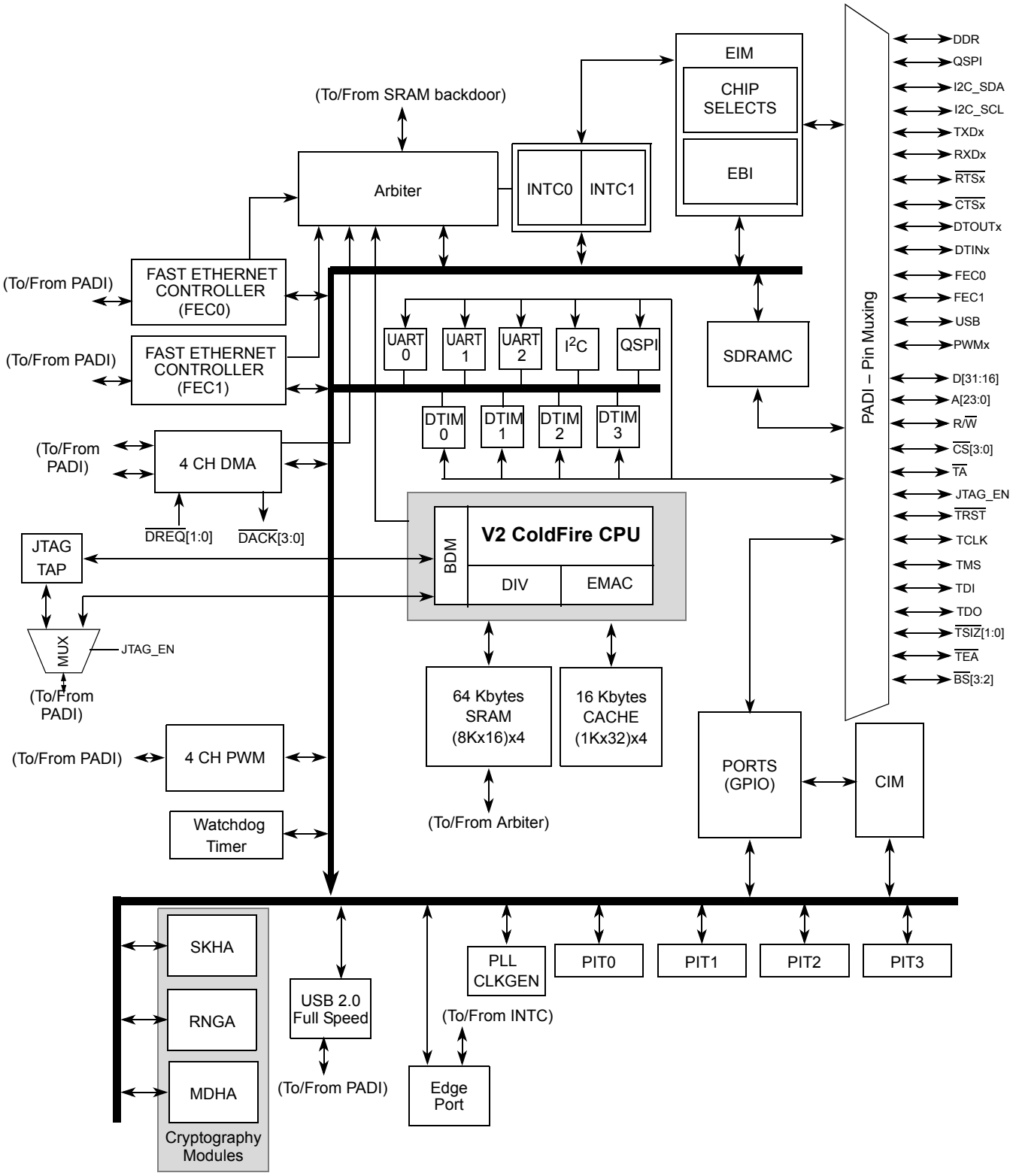

Figure 2. MCF5275 Block Diagram

1.2 Features

This document contains information on a new product. Specifications and information herein are subject to change without notice.

1.2.1 Feature Overview

- ColdFire version 2 variable-length RISC processor
  - Static operation
  - 32-bit address and data path on-chip
  - 150 MHz processor core and 75 MHz bus frequency
  - Sixteen general-purpose 32-bit data and address registers
  - Enhanced multiply accumulate unit (EMAC) for DSP and fast multiply operations
- System debug support
  - Real time trace for determining dynamic execution path while in emulator mode
  - Background debug mode (BDM) for debug features while halted
  - Real time debug support, with two user visible hardware breakpoint registers (PC and address with optional data) that can be configured into a 1- or 2-level trigger
- On chip memories
  - 16 Kbyte cache, configurable as I-cache or I-cache and D-cache
  - 64 Kbyte dual-ported SRAM on CPU internal bus with standby power supply support
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Very rapid response to interrupts from the low-power sleep mode (wake-up feature)
- Up to two Fast Ethernet Media Access Controllers (FEC MAC)
  - 10 base T capability, half or full duplex throughput
  - 100 base T capability, half or full duplex throughput
  - On chip transmit and receive FIFOs
  - Built-in DMA controller
  - Memory-based flexible descriptor rings
  - Media independent interface (MII)
- USB Device Module
  - Supports full-speed 12-Mbps and low-speed 1.5-Mbps USB devices
  - Full compliance with the *Universal Serial Bus Specification, Revision 2.0*
  - Automatic hardware processing of USB standard device requests
  - Supports external USB transceiver
  - Protocol control and administration for up to four endpoints (programmable types)
  - One FIFO RAM per endpoint (2-Kbyte total)
  - Dedicated 1-Kbyte descriptor RAM, accessible from the Slave bus

  - Remote wake-up
- Hardware cryptography accelerator (optional)
  - Random number generator
  - DES/3DES/AES block cipher engine
  - MD5/SHA-1/HMAC accelerator
- Three Universal Asynchronous/synchronous Receiver Transmitters (UARTs)
  - Serial communication channel
  - 16-bit divider for clock generation
  - Internal channel control logic
  - Interrupt control logic
  - Maskable interrupts
  - DMA support
  - Programmable clock-rate generator
  - Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
  - Up to 2 stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines
  - Transmit and receive FIFO buffers
- I^2C Module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master or slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued Serial Peripheral Interface (QSPI)
  - Full-duplex, three-wire synchronous transfer
  - Up to four chip selects available
  - Master operation
  - Programmable master bit rates
  - Up to 16 pre-programmed transfers
- Four 32-bit Timers with DMA request capability
- Pulse width modulation (PWM) unit
  - Four identical channels
- Software Watchdog Timer
  - 16-bit counter
  - Low power mode support
- Phase Locked Loop (PLL)
  - Reference crystal 8 to 25 MHz
  - Low power modes supported

  - Separate CLKOUT and $\overline{\text{DDR\_CLKOUT}}$ signals
- Four Programmable Interrupt Timers (PITs)
- Interrupt Controllers (x2)
  - Support for 58 interrupt sources, organized as follows:
    - 51 fully-programmable interrupt sources
    - 7 fixed-level external interrupt sources
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA Controller
  - Four fully programmable channels
  - Dual-address and single-address transfer support with 8-, 16-, and 32-bit data capability
  - Source/destination address pointers that can increment or remain constant
  - 24-bit transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Two-bus-clock internal access
  - External request pins for each channel
- External Memory Interface
  - External glueless connections to 8- and 16-bit external memory devices (e.g., SRAM, flash, ROM, etc.)
  - Glueless interface to SRAM devices with or without byte strobe inputs
  - Programmable wait state generator
  - 16-bit external bidirectional data bus
  - 24-bit address bus
  - Eight chip selects
  - Byte/write enables
  - Ability to boot from external memories that are 8 or 16 bits wide
- DDR SDRAM controller
  - Supports 16-bit wide memory devices
  - Supports Dual Data Rate (DDR) SDRAM.
  - Page mode support
  - Programmable refresh interval timer.
  - Sleep mode and self-refresh.
  - Supports 16-byte (4-beat, 4-byte) critical-word-first burst transfer.
  - Memory sizes from 8 Mbyte to 128 MByte
  - 150 MHz data transfer rate (DDR)

  - Two independent chip selects
- Reset
  - Separate Reset In and Reset Out signals
  - Six sources of reset (POR, External, Software, Watchdog, Loss of clock/lock)
  - Status flag indication of source of last reset
- Chip Configurations
  - System configuration during reset
  - Bus Monitor, Abort Monitor
  - Configurable output pad drive strength
  - Unique Part Identification and Part Revision Numbers
- General Purpose I/O interface
  - Up to 65 bits of general purpose I/O
  - Coherent 32-bit control
  - Bit manipulation supported via set/clear functions
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing
  - Unique JTAG Part Identification and Part Revision Numbers

1.2.2 V2 Core Overview

The ColdFire V2 core is comprised of two separate pipelines that are decoupled by an instruction buffer. The two-stage Instruction Fetch Pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the Operand Execution Pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire Instruction Set Architecture Revision A with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the V2 core includes the enhanced multiply-accumulate unit (EMAC) for improved signal processing capabilities. The EMAC implements a 4-stage execution pipeline, optimized for 32 x 32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers as well as signed fractional operands as well as a complete set of instructions to process these data types. The EMAC provides superb support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Debug Module

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, users can access real-time trace and debug information. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators. The debug interface is a superset of the BDM interface provided on Motorola's 683xx family of parts.

The on-chip breakpoint resources include a total of 6 programmable registers—a set of address registers (with two 32-bit registers), a set of data registers (with a 32-bit data register plus a 32-bit data mask register), and one 32-bit PC register plus a 32-bit PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception.

To support program trace, the Version 2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate.

1.2.4 JTAG

The MCF5275 microprocessor family support circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 326-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF5275 Family implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the microprocessor for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-chip Memories

The 64 Kbyte data RAM and the 16 Kbyte cache RAM for the processors are built using a RAM compiler. Both RAM blocks connect directly to the RAM controller via a standard single-port synchronous SRAM interface.

1.2.5.1 Cache

The 16-Kbyte cache can be configured into one of three possible organizations: a 16-Kbyte instruction cache, a 16-Kbyte data cache or a split 8-Kbyte instruction/8-Kbyte data cache. The configuration is software-programmable by control bits within the privileged Cache Configuration Register (CACR). In all configurations, the cache is a direct-mapped single-cycle memory.

1.2.5.2 SRAM

The SRAM module provides a general-purpose 64-Kbyte memory implemented as four 16-Kbyte blocks that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 64-Kbyte boundary within the 4-Gbyte address space. The memory is ideal for storing critical code or data structures, for use as the system stack, or for storing FEC data buffers. Because the SRAM module is

physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by non-core bus masters, for example the DMA and/or the FECs. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance. As an example, system performance can be increased significantly if Ethernet packets are moved from the FEC into the SRAM (rather than external memory) prior to any processing.

1.2.6 Power Management

The MCF5275 family incorporates several low power modes of operation which are entered under program control and exited by several external trigger events. An integrated Power-On Reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises.

1.2.7 Fast Ethernet Controller (FEC)

The MCF5275 family contains up to two 10/100 BaseT fast Ethernet Controllers (FECs). Refer to Table 1 for device configurations. Both Fast Ethernet Controller 0 (FEC0) and Fast Ethernet Controller 1 (FEC1) are part of the ColdFire platform. The MCF5274L and MCF5275L contain Ethernet Controller 0 (FEC0) only.

Each FEC includes these distinctive features:

- IEEE 802.3 MAC (compliant with IEEE 802.3 1998 edition)
- Built-in FIFO and DMA controller
- Support for different Ethernet physical interfaces:
  - 100Mbps IEEE 802.3 MII
  - 10Mbps IEEE 802.3 MII
- Support for full-duplex operation (200Mbps throughput) with a minimum system clock of 50MHz
- Support for half-duplex operation (100Mbps throughput) with a minimum system clock rate of 25MHz
- IEEE 802.3 full duplex flow control
- Programmable max frame length supports IEEE 802.1 VLAN tags and priority
- Retransmission from transmit FIFO following a collision (no system bus utilization)
- Automatic internal flushing of the receive FIFO for runts (collision fragments) and address recognition rejects (no system bus utilization)
- Address recognition
  - Frames with broadcast address may be always accepted or always rejected
  - Exact match for single 48-bit individual (unicast) address
  - Hash (64-bit hash) check of individual (unicast) addresses
  - Hash (64-bit hash) check of group (multicast) addresses
  - Promiscuous mode
- RMON and IEEE statistics
- Interrupts for network activity and error conditions

1.2.8 Universal Serial Bus (USB)

The USB controller supports device mode data communications with a USB host (typically a PC).

The programmable USB registers allow the user to enable or disable the module, control characteristics of individual endpoints, and monitor traffic flow through the module without ever seeing the low-level details of the USB protocol.

The USB module provides the following features to the user:

- Supports full-speed 12-Mbps USB devices and low-speed 1.5-Mbps devices
- Full compliance with the *Universal Serial Bus Specification, Revision 2.0*
- Automatic hardware processing of USB standard device requests
- USB device controller with protocol control and administration for up to eight endpoints, 16 interfaces, and 16 configurations. Endpoint types are programmable with support for up to eight control, interrupt, bulk, or isochronous endpoints
- Independent interrupts for each endpoint
- Supports remote wake-up via a register bit
- Detects start-of-frame and missed start-of-frame for isochronous endpoint synchronization
- Notification of start-of-frame, reset, suspend, and resume events

1.2.9 Cryptography

Some of the MCF5275 family devices incorporate small, fast, and dedicated hardware accelerators for random number generation, message digest and hashing, and the DES, 3DES, and AES block cipher functions. This allows for the implementation of common Internet security protocol cryptography operations with performance well in excess of software-only algorithms. Refer to Table 1 for device configurations.

1.2.10 UARTs

The MCF5275 family of microprocessors each contain three (3) UARTs that function independently. Any of the three UARTs can be clocked by the system bus clock, eliminating the need for an external crystal.

Each UART module contains the following major functional features:

- Serial communication channel
- 16-bit divider for clock generation
- Internal channel control logic
- Interrupt control logic
- Maskable interrupts
- DMA support
- Programmable clock-rate generator
- Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
- Up to 2 stop bits in 1/16 increments
- Error-detection capabilities
- Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines

- Transmit and receive FIFO buffers
- UART Modes of Operation:
  - — Full-duplex
  - — Auto-echo loopback
  - — Local loopback
  - — Remote loopback

1.2.11 I^2C Bus

The I^2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I^2C allows additional devices to be connected to the bus for expansion and system development.

The I^2C includes these distinctive features:

- Compatibility with I^2C bus standard
- Multiple-master operation
- Software programmable for one of 64 different serial clock frequencies
- Software selectable acknowledge bit
- Interrupt driven, byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection
- DMA support

1.2.12 QSPI

The queued serial peripheral interface module provides a serial peripheral interface with queued transfer capability. It allows users to enqueue up to 16 transfers at once, eliminating CPU intervention between transfers. Transfer RAMs in the QSPI are indirectly accessible using address and data registers.

The QSPI contains the following features:

- Programmable queue to support up to 16 transfers without user intervention
- Supports transfer sizes of 8 to 16 bits in 1-bit increments
- Four peripheral chip-select lines
- Baud rates from 146.3 Kbps to 18.75 Mbps at 75 MHz
- Programmable delays before and after transfers
- Programmable clock phase and polarity
- Supports wraparound mode for continuous transfers

1.2.13 DMA Timers (DTIM0–DTIM3)

There are four independent, general purpose 32-bit platform timers (DTIM0, DTIM1, DTIM2, DTIM3) on the MCF5275 family of microprocessors. The output of an 8-bit prescaler clocks each timer.

Each of the platform timer modules has these distinctive features:

- Programmable sources for the clock input, including external clock
- Input capture capability with programmable trigger edge on input pin
- Output compare with programmable mode for the output pin
- Free run and restart modes
- Maskable interrupts on input capture or reference compare
- DMA support

Each of the four timer modules has four operating modes:

- Capture mode
- Output mode
- Reference compare mode

1.2.14 Pulse Width Modulation (PWM) Module

The Pulse Width Modulation (PWM) module generates a synchronous series of pulses having programmable duty cycle. With a suitable low-pass filter, the PWM can be used as a digital-to-analog converter.

The PWM module has six channels with independent control of left and center aligned outputs on each channel. The MCF5275 family uses four of these channels namely 0, 1, 2 and 3. The emergency shutdown functionality (channel 5 only) is not used for the MCF5275 family.

Each of the PWM channels has a programmable period and duty cycle as well as a dedicated counter. A flexible clock select scheme allows a total of four different clock sources to be used with the counters. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The PWM outputs can be programmed as left aligned outputs or center aligned outputs

Summary of the main features include:

- Independent PWM channels with programmable period and duty cycle
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel
- Period and duty cycle are double buffered. Change takes effect when the end of the effective period is reached (PWM counter reaches zero) or when the channel is disabled.
- Programmable center or left aligned outputs on individual channels
- 16-bit PWM resolution available by concatenating 8-bit channels
- Four clock sources (A, B, SA and SB) provide for a wide range of frequencies.
- Programmable Clock Select Logic

1.2.15 Software Watchdog Timer (WDT)

The watchdog timer is a 16-bit timer for helping software recover from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.16 Phase Locked Loop (PLL)

The clock module contains a crystal oscillator (OSC), phase-locked loop (PLL), reduced frequency divider (RFD), status/control registers, and control logic. To improve noise immunity, the PLL and OSC have their own power supply inputs, VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.17 Interrupt Controllers (INTC0/INTC1)

There are two interrupt controllers which support 58 interrupt sources on the MCF5275. Each interrupt controller is organized as 7 levels with 9 interrupt sources per level. Each interrupt source has a unique interrupt vector, and 51 of the 58 sources of a given controller provide a programmable level [1-7] and priority within the level.

1.2.18 Direct Memory Access Controller (DMAC)

The Direct Memory Access Controller (DMA) Module provides an efficient way to move blocks of data with minimal processor interaction. The DMA module provides four channels that allow byte, word, or longword operand transfers. These transfers can be single or dual address to off-chip devices or dual address to on-chip devices.

The DMA contains the following features:

- Four fully independent, programmable DMA controller channels/bus modules
- Auto-alignment feature for source or destination accesses
- Single- and dual-address transfers
- Up to four external request pins ($\overline{\text{DREQ}}$[3:0])
- Channel arbitration on transfer boundaries
- Data transfers in 8-, 16-, 32- or 128-bit blocks via a 16-byte buffer
- Supports continuous-mode and cycle-steal transfers
- Independent transfer widths for source and destination
- Independent source and destination address registers
- Provide two clock data transfers

1.2.19 External Interface Module (EIM)

The external interface module on MCF5275 family of devices handles the transfer of information between the internal core and memory, peripherals, or other processing elements in the external address space.

Programmable chip select outputs provide signals to enable external memory and peripheral circuits, providing all handshaking and timing signals for automatic wait-state insertion and data bus sizing.

Base memory address and block size are programmable, with some restrictions. For example, the starting address must be on a boundary that is a multiple of the block size. Each chip select is general purpose; however, any one of the chip selects can be programmed to provide read and write enable signals suitable for use with most popular static RAMs and peripherals. Data bus width (8-bit, 16-bit, or 32-bit) is programmable on all chip selects, and further decoding is available for protection from user mode access or read-only access.

The key features of the EIM are summarized below:

- Eight independent, user-programmable chip-select signals (CS[7:0]) that interface with various memory types and peripherals
- Address masking for 64 Kbyte to 4 gigabyte memory block sizes
- Programmable wait states and port sizes
- External master access to chip selects

1.2.20 Double Data Rate (DDR) Synchronous DRAM (SDRAM) Controller

The SDRAMC provides a 16-bit glueless external interface to double-data-rate (DDR) SDRAM memory devices. It is responsible for providing address, data and control signals for up to two independent chip-selects.

The SDRAMC includes the following features:

- Supports a glueless interface to DDR SDRAMs
- 16-bit fixed memory port width
- 32-bit data bus interface to Coldfire core
- 16 bytes (8 beat x 16-bit) critical word first burst transfer
- Up to 14 row address lines, up to 12 column address lines, maximum of two chip selects. The maximum row bits plus column bits is 24.
- Supported SDRAM devices include: 8, 16, 32, 64, and 128Mbyte
- Minimum memory configuration of 8 Mbyte—12 bit row address (RA), 8 bit column address (CA), 2 bit bank address (BA) and one chip select
- Supports page mode to maximize the data rate
- Supports sleep mode and self-refresh mode
- Error detect and parity check are not supported

1.2.21 Resets

The Reset Controller is provided to determine the cause of reset, assert the appropriate reset signals to the system, and then to keep a history of what caused the reset.

The MCF5275 family has six (6) sources of reset:

- External
- Power On Reset (POR)
- Watchdog timer
- PLL Loss of Lock

- PLL Loss of Clock
- Software

External reset on the RSTOUT pin is software-assertable independent of chip reset state. There are also software-readable status flags indicating the cause of the last reset.

1.2.22 General Purpose I/O

Most peripheral I/O pins on MCF5275 family of devices are muxed with GPIO, adding flexibility and usability to all signals on the chip.

2 Device/Family Documentation List

Table 3. MCF5275 Family Documentation

Motorola Document Number	Title	Revision	Status
MCF5275EC/D	MCF5275 RISC Microprocessor Hardware Specification	0	This Document
MCF5275/D	MCF5275 Advance Information Manual	0	In Process
MCF5275PB/D	MCF5275 Product Brief	0	Available
MCF5275FS	MCF5275 Fact Sheet	0	In Process
CFPRODFACT/D	The ColdFire Family of 32-Bit Microprocessors Family Overview and Technology Roadmap	0	Available
MCF5XXXWP	MCF5XXXWP WHITE PAPER: Motorola ColdFire VL RISC Processors	0	Available
MAPBGAPP	MAPBGA 4-Layer example	0	Available
CFPRM/D	ColdFire Family Programmer's Reference Manual	2	Available

2.1 Document Revision History

Table 4 provides a revision history for this document.

Table 4. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial Release

HOW TO REACH US:

USA / EUROPE / Locations Not Listed:

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P.O. Box 5405
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MCF5275PB/D, **Rev. 0, 4/2004**

Freescale Semiconductor, Inc.