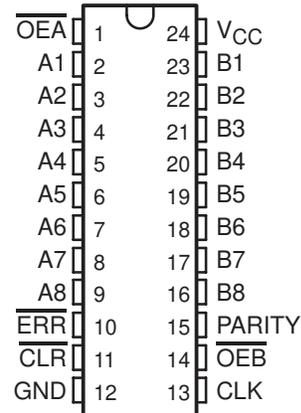# SN74ALS29833
8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

SDAS119D – FEBRUARY 1987 – REVISED JANUARY 1995

- **Functionally Similar to AMD's AM29833**
- **High-Speed Bus Transceiver With Parity Generator/Checker**
- **Parity-Error Flag With Open-Collector Outputs**
- **Register for Storing the Parity-Error Flag**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)

$\overline{OEA}$	1	24	V_{CC}
A1	2	23	B1
A2	3	22	B2
A3	4	21	B3
A4	5	20	B4
A5	6	19	B5
A6	7	18	B6
A7	8	17	B7
A8	9	16	B8
$\overline{ERR}$	10	15	PARITY
$\overline{CLR}$	11	14	$\overline{OEB}$
GND	12	13	CLK

description

The SN74ALS29833 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the parity-error ($\overline{ERR}$) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{OEA}$, $\overline{OEB}$) inputs can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with an open-collector $\overline{ERR}$ flag. $\overline{ERR}$ is clocked into the register on the rising edge of the clock (CLK) input. The error-flag register is cleared with a low pulse on the clear ($\overline{CLR}$) input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The SN74ALS29833 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai $\sum$ of Hs	Bi† $\sum$ of Ls	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd / Even	NA	NA	A	L / H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd / Even	B	NA	NA	H / L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Clear error-flag register
H	H	H	No↑	X	X	Z	Z	Z	NC	Isolation§
		L	No↑	X					H	
		H	↑	Odd					H	
		H	↑	Even					L	
L	L	X	X	Odd / Even	NA	NA	A	H / L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ Output states shown assume $\overline{ERR}$ was previously high.
§ In this mode, $\overline{ERR}$, when clocked, shows inverted parity of the A bus.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.
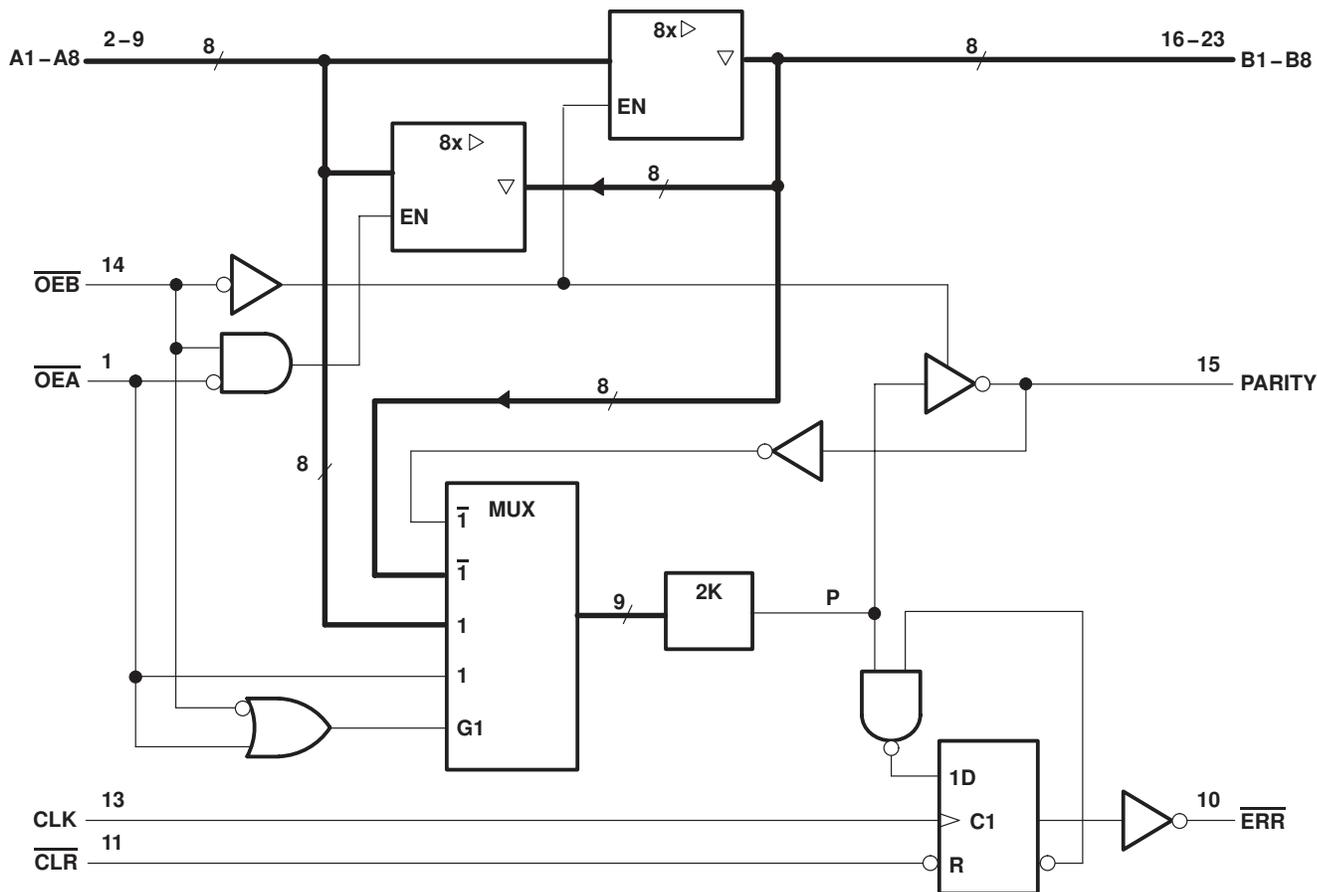
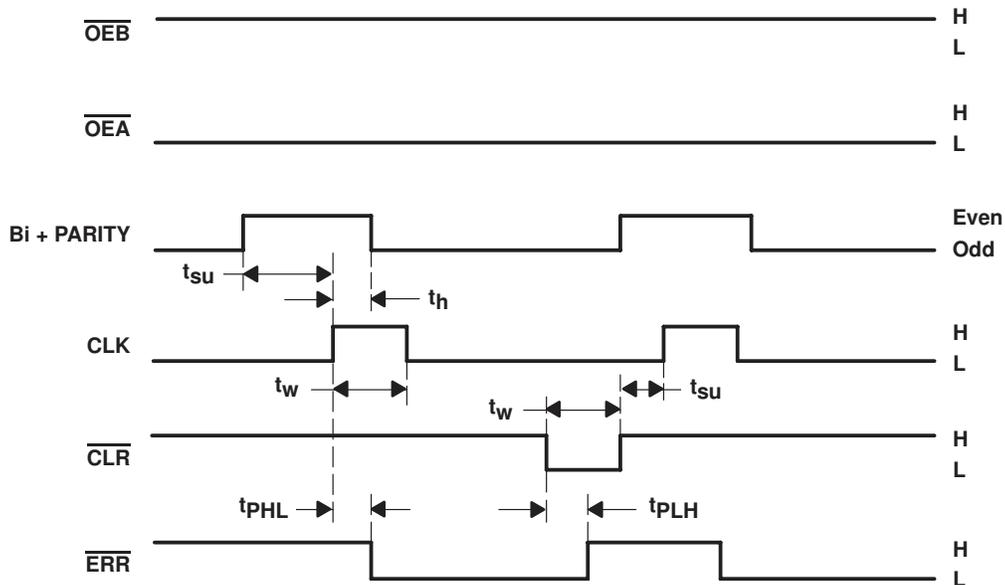Copyright © 1995, Texas Instruments Incorporated

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SN74ALS29833
8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

logic diagram (positive logic)

error-flag waveforms

ERROR-FLAG FUNCTIONS

INPUTS		INTERNAL TO DEVICE	OUTPUT PRESTATE	OUTPUT	FUNCTION
$\overline{\text{CLR}}$	CLK	POINT P	$\overline{\text{ERR}}_{n-1}$†	$\overline{\text{ERR}}$	
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

† $\overline{\text{ERR}}_{n-1}$ represents the state of $\overline{\text{ERR}}$ before any changes at $\overline{\text{CLR}}$, CLK, or point P.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 7 V
Voltage applied to a disabled I/O port .... 5.5 V
Operating free-air temperature range, T_A .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage, $\overline{\text{ERR}}$			5.5	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration	CLK high	10		ns
		CLK low	10		
		$\overline{\text{CLR}}$ low	10		
t_{su}	Setup time before CLK↑	Bi and PARITY	17		ns
		$\overline{\text{CLR}}$ inactive	15		
t_h	Hold time, Bi and PARITY after CLK↑		0		ns
T_A	Operating free-air temperature		0	70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.75$ V,	$I_I = -18$ mA			−1.2	V
V_{OH}	All I/Os except $\overline{ERR}$	$V_{CC} = 4.75$ V	$I_{OH} = -15$ mA	2.4			V
			$I_{OH} = -24$ mA	2			
I_{OH}	$\overline{ERR}$	$V_{CC} = 4.75$ V,	$V_{OH} = 5.5$ V			0.1	mA
V_{OL}		$V_{CC} = 4.75$ V,	$I_{OL} = 48$ mA		0.35	0.5	V
I_I		$V_{CC} = 5.25$ V,	$V_I = 5.5$ V			0.1	mA
I_{IH}‡		$V_{CC} = 5.25$ V,	$V_I = 2.7$ V			20	µA
I_{IL}‡	Data	$V_{CC} = 5.25$ V,	$V_I = 0.4$ V			−0.2	mA
	Control					−0.75	
I_O§		$V_{CC} = 5.25$ V,	$V_O = 0$	−75		−250	mA
I_{CC}		$V_{CC} = 5.25$ V			70	100	mA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
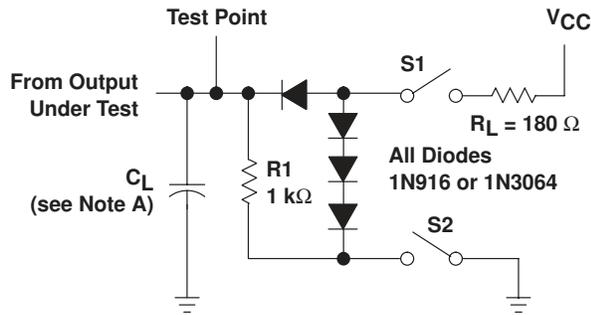
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC} = 4.75$ V to 5.25 V, T_A = MIN to MAX¶		UNIT
				MIN	MAX	
t_{PLH}	A or B	B or A	$C_L = 50$ pF		8	ns
t_{PHL}					8	
t_{PLH}	A or B	B or A	$C_L = 300$ pF		15	ns
t_{PHL}					15	
t_{PLH}	A	PARITY	$C_L = 50$ pF		15	ns
t_{PHL}					19	
t_{PLH}	A	PARITY	$C_L = 300$ pF		22	ns
t_{PHL}					24	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	$C_L = 50$ pF		17	ns
t_{PZL}					17	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	$C_L = 300$ pF		23	ns
t_{PZL}					23	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	$C_L = 5$ pF		9	ns
t_{PLZ}					9	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	$C_L = 50$ pF		15	ns
t_{PLZ}					8	
t_{PHL}	CLK	$\overline{ERR}$	$C_L = 50$ pF		13	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	$C_L = 50$ pF		13	ns
t_{PLH}	$\overline{OEA}$	PARITY	$C_L = 50$ pF		17	ns
t_{PHL}					19	
t_{PLH}	$\overline{OEA}$	PARITY	$C_L = 300$ pF		22	ns
t_{PHL}					25	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

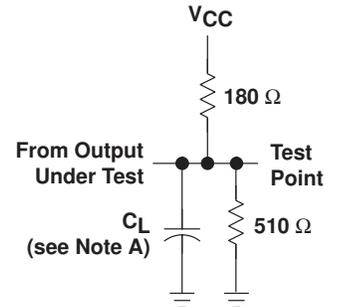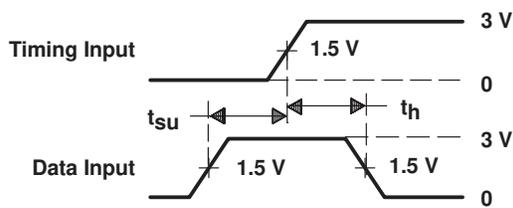## PARAMETER MEASUREMENT INFORMATION

TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

SWITCH POSITION TABLE
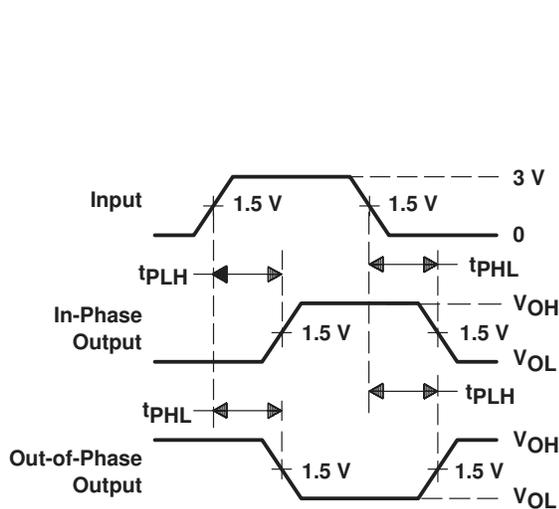
LOAD CIRCUIT 1
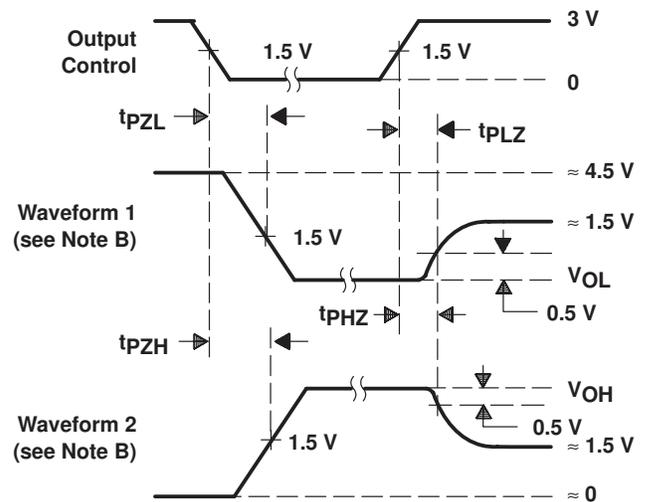ALL OUTPUTS EXCEPT FOR ERROR FLAG

LOAD CIRCUIT 2
ERROR-FLAG OUTPUT

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
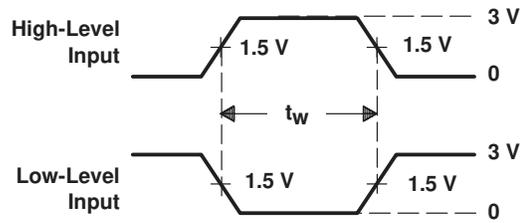
VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SN74ALS29833DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS29833DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74ALS29833NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
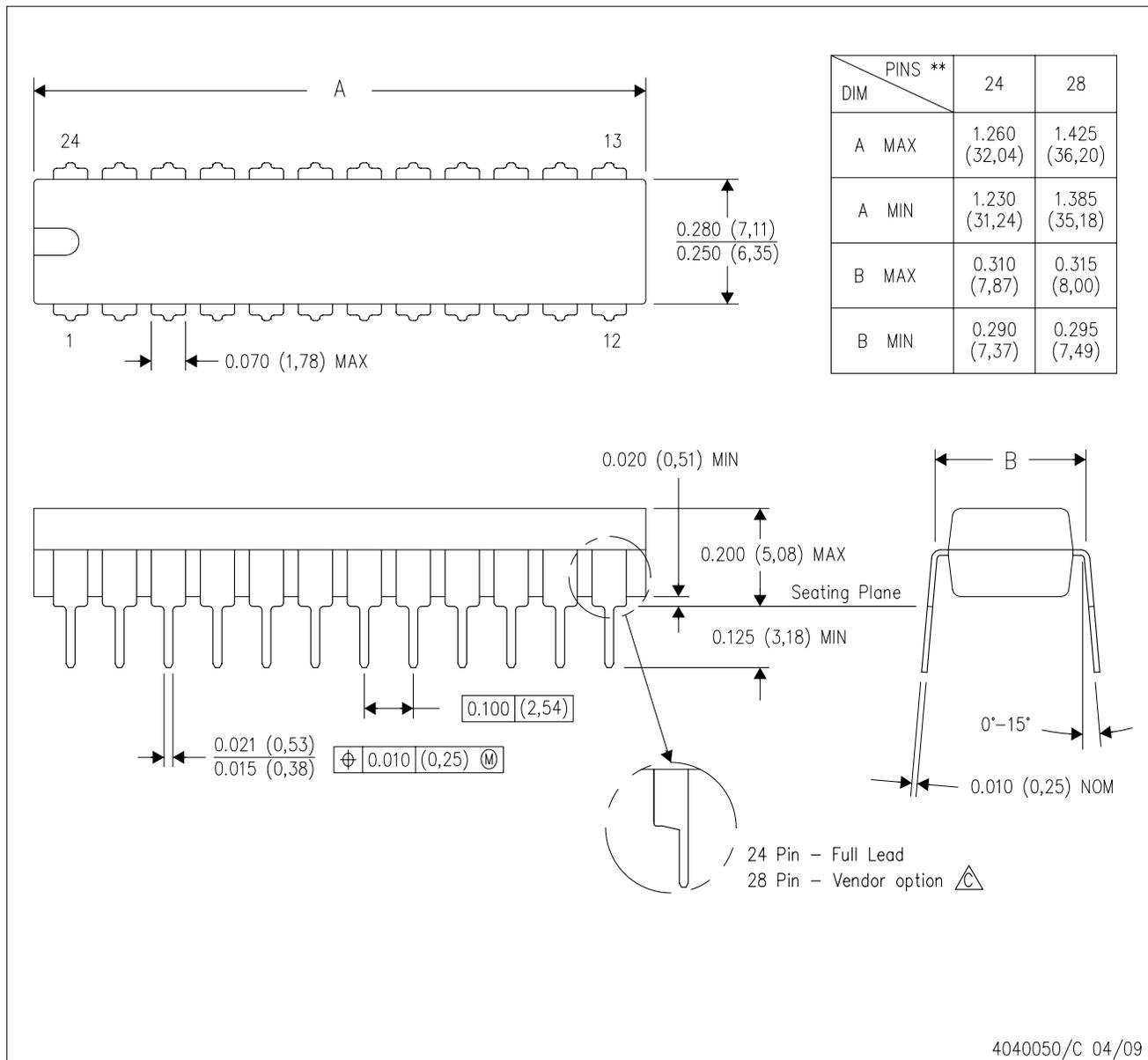
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NT (R−PDIP−T**)

24 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE
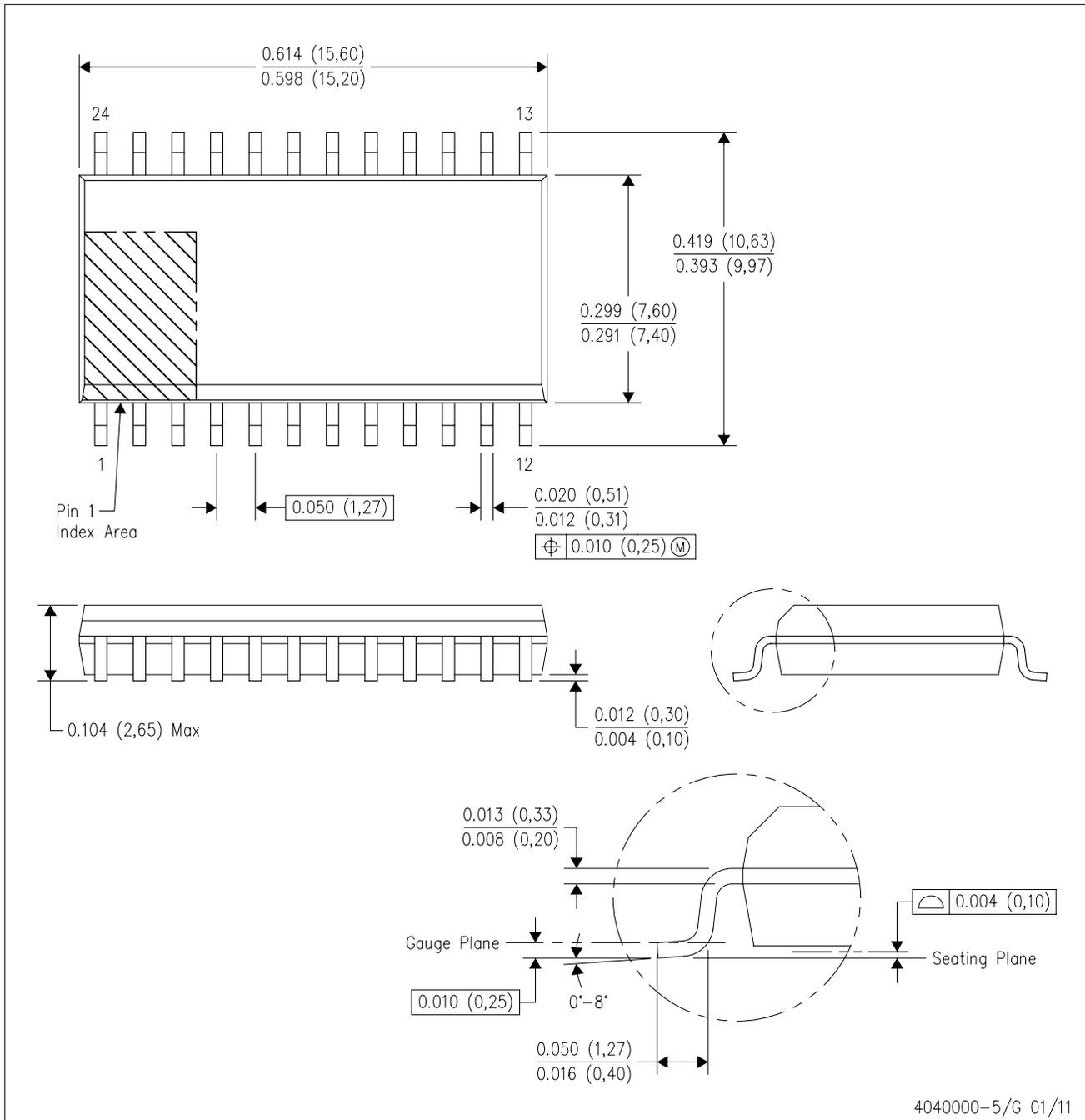
DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

A

24   13

0.280 (7,11)
0.250 (6,35)

1   12

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

$\oplus$ 0.010 (0,25) Ⓜ

B

0°−15°

0.010 (0,25) NOM

24 Pin − Full Lead
28 Pin − Vendor option ⚠C

4040050/C 04/09

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
      ⚠C The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

$\frac{0.614\ (15,60)}{0.598\ (15,20)}$

24   13

$\frac{0.419\ (10,63)}{0.393\ (9,97)}$

$\frac{0.299\ (7,60)}{0.291\ (7,40)}$

1   12

Pin 1
Index Area

0.050 (1,27)

$\frac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$\frac{0.012\ (0,30)}{0.004\ (0,10)}$

$\frac{0.013\ (0,33)}{0.008\ (0,20)}$

⌒ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

$\frac{0.050\ (1,27)}{0.016\ (0,40)}$

4040000−5/G 01/11

NOTES: A.   All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AD.

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