

Rev. 1.3

# AS7C34096A-8TIN 512K X 8 BIT HIGH SPEED CMOS SRAM

# **REVISION HISTORY**

<b>Revision</b>	Description	Issue Date
Rev. 1.0	Initial Issue	July.12. 2012
Rev. 1.1	."CE# $\geq$ V <sub>CC</sub> - 0.2V" revised as "CE# $\leq$ 0.2" for TEST CONDITION of Average Operating Power supply Current lcc1 on page3	July.19. 2012
Rev.1.2	Add "Green package available" on page 1	Nov. 02. 2012
Rev.1.3	<ol> <li>Revise "TEST CONDITION" for VOH, VOL on page 3 IOH = -8mA revised as -4mA IOL =4mA revised as 8mA</li> <li>Revise VIH(max) &amp; VIL(min) note on page 3 VIH(max) = VCC + 2.0V for pulse width less than 6ns. VIL(min) = VSS - 2.0V for pulse width less than 6ns.</li> </ol>	June. 04. 2013



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# AS7C34096A-8TIN 512K X 8 BIT HIGH SPEED CMOS SRAM

## **FEATURES**

- Fast access time : 8ns
- Low power consumption:
   Operating current:
   50mA(TYP.)
   Standby current:
   2mA(TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Temperature range Industrial -40°~85°C
- Tri-state output
- Green package/ROHS compliant (N)
- Data retention voltage : 1.5V (MIN.)
- Package : 44-pin 400 mil TSOP-II

## **GENERAL DESCRIPTION**

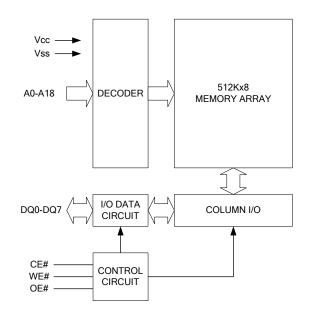
The AS7C34096A is a 4,194,304-bit high speed CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C34096A operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

### PRODUCT FAMILY

Product	Operating		Speed	Power Dissipation		
Family	Temperature	Vcc Range	Speed	Standby(IsB1,TYP.)	Operating(Icc1,TYP.)	
AS7C34096A(I)	-40° ~ 85℃	3.0 ~ 3.6V	8ns	2mA	50mA	

# FUNCTIONAL BLOCK DIAGRAM



# **PIN DESCRIPTION**

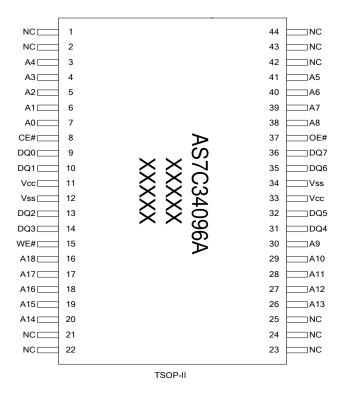
SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

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# **PIN CONFIGURATION**





### **ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	VT1	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	VT2	-0.5 to Vcc+0.5	V
Operating Temperature	Та	-40 to 85(I grade)	°C
Storage Temperature	Tstg	-65 to 150	°C
Power Dissipation	PD	1	W
DC Output Current	Ιουτ	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

## TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	Н	Х	Х	High-Z	ISB,ISB1
Output Disable	L	Н	Н	High-Z	Icc,Icc1
Read	L	L	Н	Dout	Icc,Icc1
Write	L	Х	L	Din	Icc,Icc1

Note:  $H = V_{IH}$ ,  $L = V_{IL}$ , X = Don't care.

# **DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION		MIN.	<b>TYP.</b> <sup>*4</sup>	MAX.	UNIT
Supply Voltage	Vcc	-8		3.0	3.3	3.6	V
Input High Voltage	VIH			2.2	-	Vcc+0.3	V
Input Low Voltage	Vı∟ <sup>*2</sup>			- 0.3	-	0.8	V
Input Leakage Current	Iu	V <sub>CC</sub> ≧ V <sub>IN</sub> ≧ V <sub>SS</sub>		- 1	-	1	μA
Output Leakage Current	Ilo	Vcc ≧ Vou⊤ ≧ Vss, Output Disabled		- 1	-	1	μA
Output High Voltage	Vон	Iон <b>= -4mA</b>		2.4	-	-	V
Output Low Voltage	Vol	l <sub>o∟</sub> = 8mA		-	-	0.4	V
Average Operating Power supply Current	lcc	Cycle time = Min. CE# = V <sub>IL</sub> , I⊭ <sub>O</sub> = 0mA, Others at VIL or VIH	-8	-	65	80	mA
Average Operating Power supply Current	Icc1	CE# $\leq 0.2$ , Others at 0.2V or Vcc-0.2V I <sub>VO</sub> = 0mA;f=max	-8	-	50	60	mA
Standby Dowor	Isb	CE# =V⊮, Others at V∟ or V	Vін	-	-	30	mA
Standby Power Supply Current	I <sub>SB1</sub>	$\begin{array}{llllllllllllllllllllllllllllllllllll$	/	-	2	10	mA

Notes:

1. VIH(max) = Vcc + 2.0V for pulse width less than 6ns.

2.  $V_{IL}(min) = V_{SS} - 2.0V$  for pulse width less than 6ns.

3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.

4. Typical values are included for reference only and are not guaranteed or tested.

Typical valued are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> =  $25^{\circ}$ C

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### **CAPACITANCE** (T<sub>A</sub> = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	Cin	-	8	pF
Input/Output Capacitance	CI/O	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

## AC TEST CONDITIONS

Speed	8ns
Input Pulse Levels	0.2V to Vcc - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL$ , $I_{OH}/I_{OL} = -4mA/8mA$

## **AC ELECTRICAL CHARACTERISTICS**

#### (1) READ CYCLE

PARAMETER	SYM.	AS7C34	1096A-8	UNIT
	511.	MIN.	MAX.	
Read Cycle Time	trc	8	-	ns
Address Access Time	taa	-	8	ns
Chip Enable Access Time	<b>t</b> ace	-	8	ns
Output Enable Access Time	toe	-	4.5	ns
Chip Enable to Output in Low-Z	tclz*	2	-	ns
Output Enable to Output in Low-Z	tolz*	0	-	ns
Chip Disable to Output in High-Z	tснz*	-	3	ns
	tонz*	-	3	ns
Output Hold from Address Change	tон	2	-	ns

#### (2) WRITE CYCLE

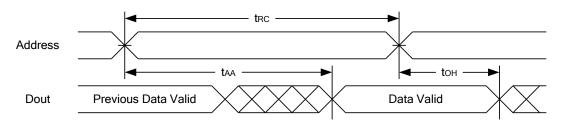
PARAMETER	SYM.	AS7C34	AS7C34096A-8		
FARAIVIETER	5 T WI.	MIN.	MAX.	UNIT	
Write Cycle Time	twc	8	-	ns	
Address Valid to End of Write	taw	6.5	-	ns	
Chip Enable to End of Write	tcw	6.5	-	ns	
Address Set-up Time	tas	0	-	ns	
Write Pulse Width	twp	6.5	-	ns	
Write Recovery Time	twr	0	-	ns	
Data to Write Time Overlap	tow	5	-	ns	
Data Hold from End of Write Time	tон	0	-	ns	
Output Active from End of Write	tow*	2	-	ns	
Write to Output in High-Z	twnz*	-	3	ns	

\*These parameters are guaranteed by device characterization, but not production tested.

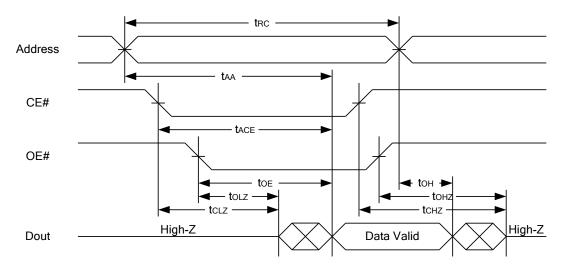


#### TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



Notes :

1.WE# is high for read cycle.

2.Device is continuously selected OE# = low, CE# = low.

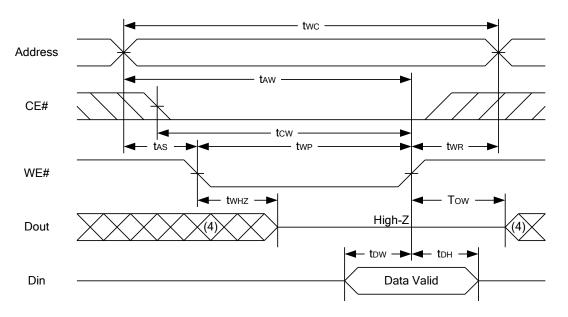
3.Address must be valid prior to or coincident with CE# = low,; otherwise tAA is the limiting parameter.

4.tclz, tolz, tcHz and toHz are specified with  $C_L$  = 5pF. Transition is measured ±500mV from steady state.

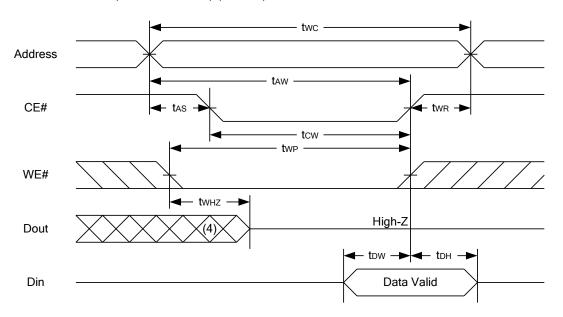
5.At any given temperature and voltage condition, t<sub>CHZ</sub> is less than t<sub>CLZ</sub>, t<sub>OHZ</sub> is less than t<sub>OLZ</sub>.



#### WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



#### WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



Notes :

2.A write occurs during the overlap of a low CE#, low WE#.

3. During a WE# controlled write cycle with OE# low, twp must be greater than twHz + tow to allow the drivers to turn off and data to be placed on the bus.

4. During this period, I/O pins are in the output state, and input signals must not be applied.5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state. 6 tow and twHz are specified with CL = 5pF. Transition is measured ±500mV from steady state.

<sup>1.</sup>WE#, CE# must be high during all address transitions.

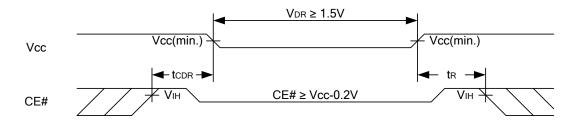


## **DATA RETENTION CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	Vdr	CE# ≧ V <sub>CC</sub> - 0.2V	1.5	-	3.6	V
Data Retention Current	ldr	Vcc = 1.5V CE# ≧ Vcc - 0.2V Others at 0.2V or Vcc – 0.2V	-	2	10	mA
Chip Disable to Data Retention Time	tcdr	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	tR		t <sub>RC∗</sub>	-	-	ns

tRC\* = Read Cycle Time

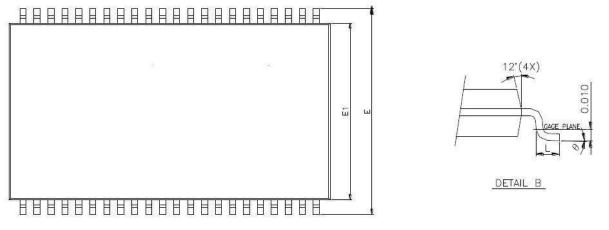
## **DATA RETENTION WAVEFORM**

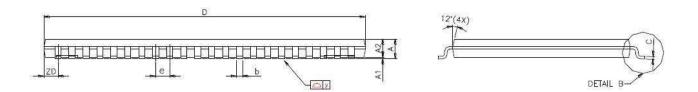




### PACKAGE OUTLINE DIMENSION

#### 44-pin 400mil TSOP- II Package Outline Dimension





SYMBOLS	DIMENS	IONS IN MILL	METERS	DIM	ENSIONS IN	MILS
STMBULS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
С	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
е	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
У	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°



# **ORDERING INFORMATION**

Package Type	Access Time (Speed)(ns)	Temperature Range(°C)	Packing Type	Alliance Memory Part No.
44Pin(400mil)	8	-40°C~85°C	Tray	AS7C34096A-8TIN
TSOP-II			Tape Reel	AS7C34096A-8TINTR



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