AS7C34096A-8TIN
512K X 8 BIT HIGH SPEED CMOS SRAM

REVISION HISTORY

Revision	Description	Issue Date
Rev. 1.0	Initial Issue	July.12. 2012
Rev. 1.1	."CE# $\geq V_{CC}$ - 0.2V" revised as "CE# ≤ 0.2" for TEST CONDITION of Average Operating Power supply Current Icc1 on page3	July.19. 2012
Rev.1.2	Add "Green package available" on page 1	Nov. 02. 2012
Rev.1.3	1. Revise "TEST CONDITION" for VOH, VOL on page 3 　　I_{OH} = -8mA revised as -4mA 　　I_{OL} =4mA revised as 8mA 2. Revise VIH(max) & VIL(min) note on page 3 　　VIH(max) = VCC + 2.0V for pulse width less than 6ns. 　　VIL(min) = VSS - 2.0V for pulse width less than 6ns.	June. 04. 2013

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FEATURES

- Fast access time : 8ns
- **Low power consumption:**
  Operating current:
    50mA(TYP.)
  Standby current:
    2mA(TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Temperature range - Industrial -40°~85℃
- Tri-state output
- Green package/ROHS compliant (N)
- Data retention voltage : 1.5V (MIN.)
- Package : 44-pin 400 mil TSOP-II
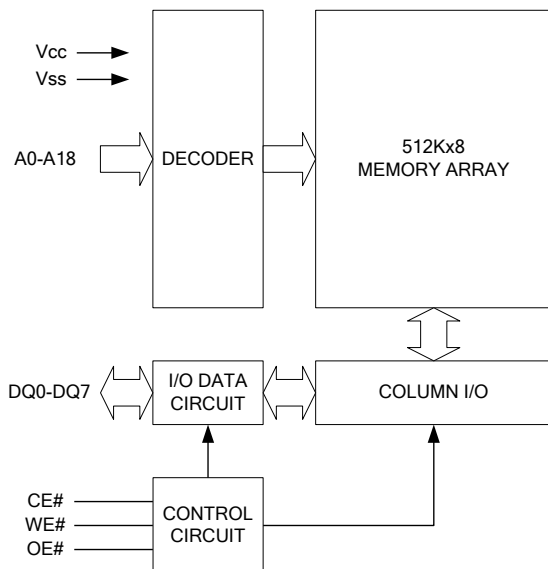
GENERAL DESCRIPTION

The AS7C34096A is a 4,194,304-bit high speed CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C34096A operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1},TYP.)	Operating(I_{cc1},TYP.)
AS7C34096A(I)	-40° ~ 85℃	3.0 ~ 3.6V	8ns	2mA	50mA

FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

PIN CONFIGURATION

Left	Pin		Pin	Right
NC	1		44	NC
NC	2		43	NC
A4	3		42	NC
A3	4		41	A5
A2	5		40	A6
A1	6		39	A7
A0	7		38	A8
CE#	8		37	OE#
DQ0	9		36	DQ7
DQ1	10		35	DQ6
Vcc	11		34	Vss
Vss	12		33	Vcc
DQ2	13		32	DQ5
DQ3	14		31	DQ4
WE#	15		30	A9
A18	16		29	A10
A17	17		28	A11
A16	18		27	A12
A15	19		26	A13
A14	20		25	NC
NC	21		24	NC
NC	22		23	NC

AS7C34096A
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TSOP-II

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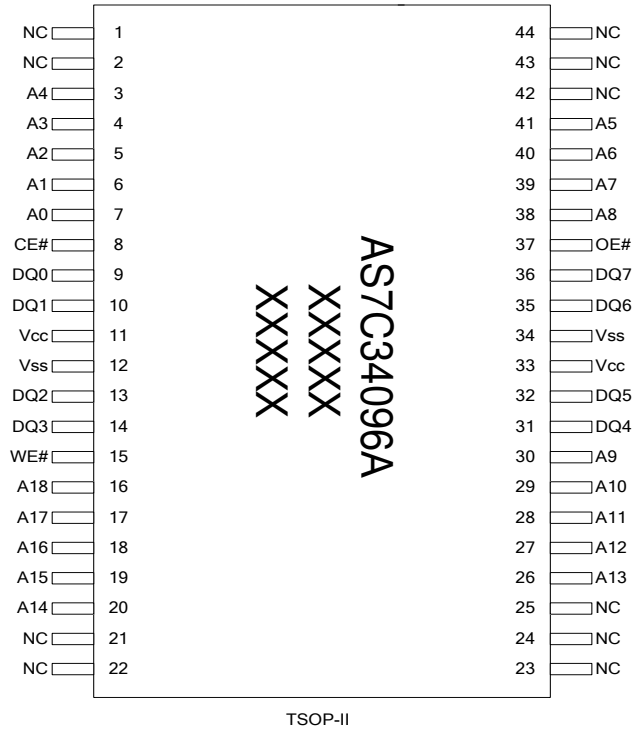
ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to V_{CC}+0.5	V
Operating Temperature	T_A	-40 to 85(I grade)	℃
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I_{SB},I_{SB1}
Output Disable	L	H	H	High-Z	I_{CC},I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC},I_{CC1}
Write	L	X	L	D_{IN}	I_{CC},I_{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.[4]	MAX.	UNIT
Supply Voltage	V_{CC}		-8	3.0	3.3	3.6	V
Input High Voltage	V_{IH}[1]			2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}[2]			- 0.3	-	0.8	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -4mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# = V_{IL}, $I_{I/O}$ = 0mA, Others at V_{IL} or V_{IH}	-8	-	65	80	mA
Average Operating Power supply Current	I_{CC1}	CE# $\leqq$ 0.2, Others at 0.2V or Vcc-0.2V $I_{I/O}$ = 0mA;f=max	-8	-	50	60	mA
Standby Power Supply Current	I_{SB}	CE# =V_{IH}, Others at V_{IL} or V_{IH}		-	-	30	mA
	I_{SB1}	CE# $\geqq$ V_{CC} - 0.2V, Others at 0.2V or V_{CC} - 0.2V		-	2	10	mA

Notes:
1. V_{IH}(max) = V_{CC} + 2.0V for pulse width less than 6ns.
2. V_{IL}(min) = V_{SS} - 2.0V for pulse width less than 6ns.
3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25℃

CAPACITANCE (T$_A$ = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C$_{IN}$	-	8	pF
Input/Output Capacitance	C$_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Speed	8ns
Input Pulse Levels	0.2V to V$_{CC}$ - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C$_L$ = 30pF + 1TTL, I$_{OH}$/I$_{OL}$ = -4mA/8mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS7C34096A-8 MIN.	AS7C34096A-8 MAX.	UNIT
Read Cycle Time	t$_{RC}$	8	-	ns
Address Access Time	t$_{AA}$	-	8	ns
Chip Enable Access Time	t$_{ACE}$	-	8	ns
Output Enable Access Time	t$_{OE}$	-	4.5	ns
Chip Enable to Output in Low-Z	t$_{CLZ}$*	2	-	ns
Output Enable to Output in Low-Z	t$_{OLZ}$*	0	-	ns
Chip Disable to Output in High-Z	t$_{CHZ}$*	-	3	ns
Output Disable to Output in High-Z	t$_{OHZ}$*	-	3	ns
Output Hold from Address Change	t$_{OH}$	2	-	ns

(2) WRITE CYCLE

| PARAMETER	SYM.	AS7C34096A-8 MIN.	AS7C34096A-8 MAX.	UNIT
Write Cycle Time	t$_{WC}$	8	-	ns
Address Valid to End of Write	t$_{AW}$	6.5	-	ns
Chip Enable to End of Write	t$_{CW}$	6.5	-	ns
Address Set-up Time	t$_{AS}$	0	-	ns
Write Pulse Width	t$_{WP}$	6.5	-	ns
Write Recovery Time	t$_{WR}$	0	-	ns
Data to Write Time Overlap	t$_{DW}$	5	-	ns
Data Hold from End of Write Time	t$_{DH}$	0	-	ns
Output Active from End of Write	t$_{OW}$*	2	-	ns
Write to Output in High-Z	t$_{WHZ}$*	-	3	ns

*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)
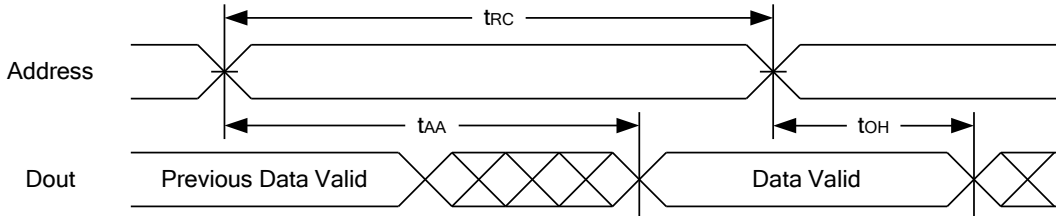
READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)
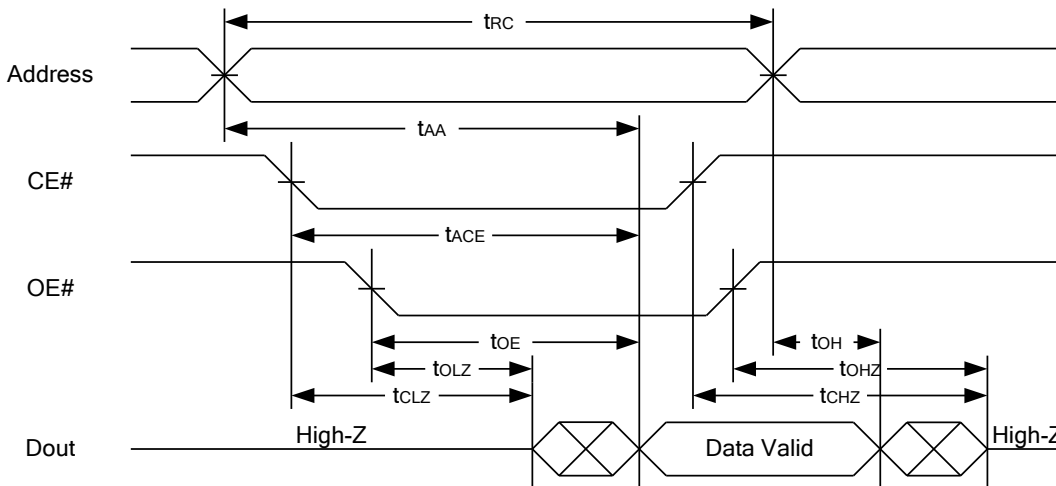
Notes :
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low,; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

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WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)

WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)

Notes :
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# $\geqq$ V_{CC} - 0.2V	1.5	-	3.6	V
Data Retention Current	I_{DR}	V_{CC} = 1.5V CE# $\geqq$ V_{CC} - 0.2V Others at 0.2V or Vcc – 0.2V	-	2	10	mA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t_R		t_{RC*}	-	-	ns

t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

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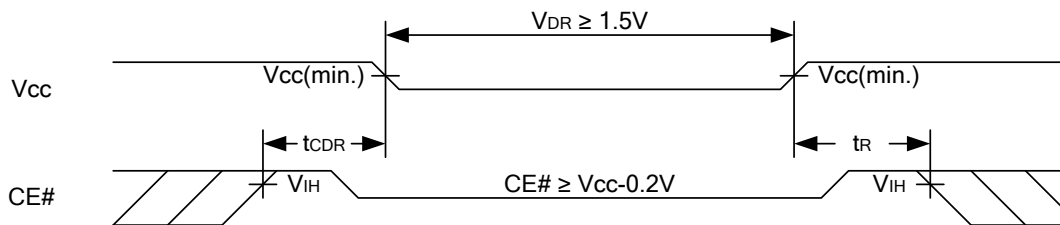
PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-Ⅱ Package Outline Dimension
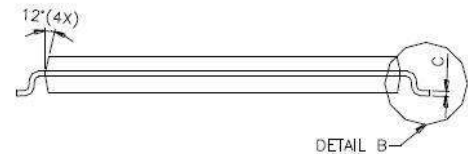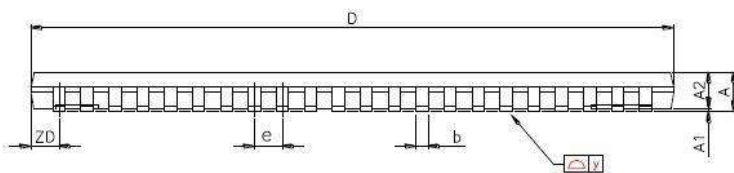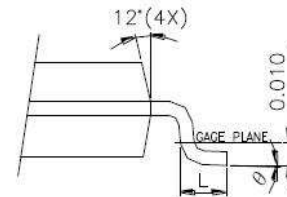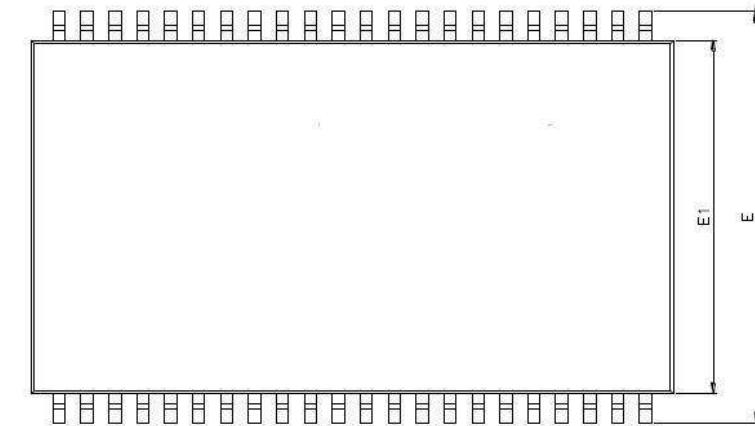
SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
Θ	0°	3°	6°	0°	3°	6°

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Temperature Range(°C)	Packing Type	Alliance Memory Part No.
44Pin(400mil) TSOP-II	8	-40°C~85°C	Tray	AS7C34096A-8TIN
			Tape Reel	AS7C34096A-8TINTR

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