2.7V to 5.5V, 3A 1ch Synchronous Buck Converter with Integrated FET

BD8962MUV

General Description

The BD8962MUV is ROHM's high efficiency step-down switching regulator designed to produce a voltage as low as 0.8V from a supply voltage of 5.5V/3.3V. It offers high efficiency by using synchronous switches and provides fast transient response to sudden load changes by implementing current mode control.

Features

- Fast Transient Response because of Current Mode Control System
- High Efficiency for all Load Ranges because of Synchronous Switches
- Soft-Start Function
- Thermal Shutdown and UVLO Functions
- Short Circuit Protection with Time Delay Function
- Shutdown Function

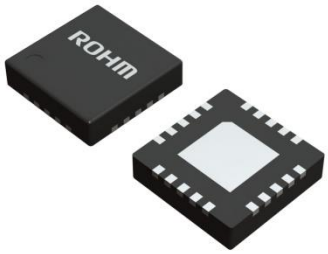
Applications

Power Supply for LSI including DSP, Microcomputer and ASIC

Key Specifications

- Input Voltage Range: 2.7V to 5.5V
- Output Voltage Range: 0.8V to 2.5V
- Average Output Current: 3.0A(Max)
- Switching Frequency: 1MHz(Typ)
- High Side FET ON-Resistance: 82mΩ(Typ)
- Low Side FET ON-Resistance: 70mΩ(Typ)
- Standby Current: 0μA(Typ)
- Operating Temperature Range: -40°C to +105°C

Packages W(Typ) x D(Typ) x H(Max)



VQFN020V4040
4.00mm x 4.00mm x 1.00mm

Typical Application Circuit

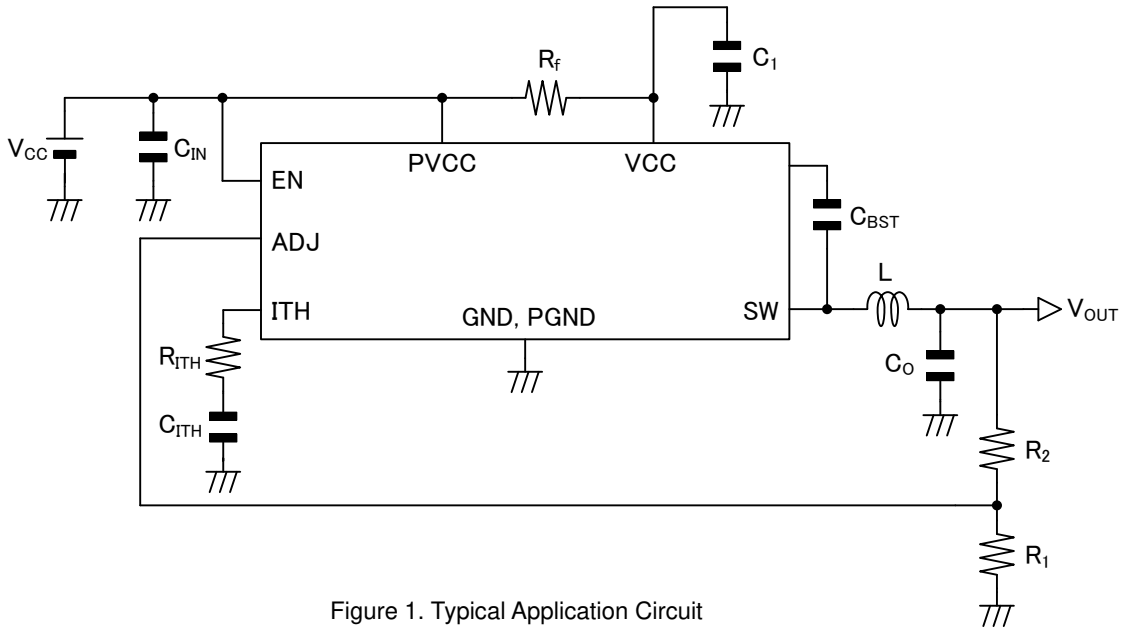


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○ This product has no designed protection against radioactive rays

Pin Configuration

(TOP VIEW)

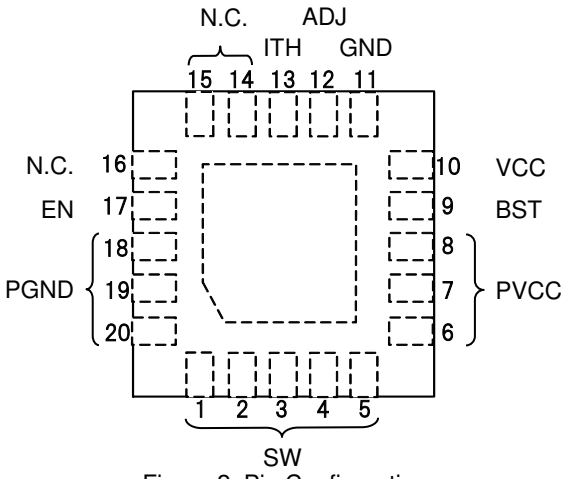
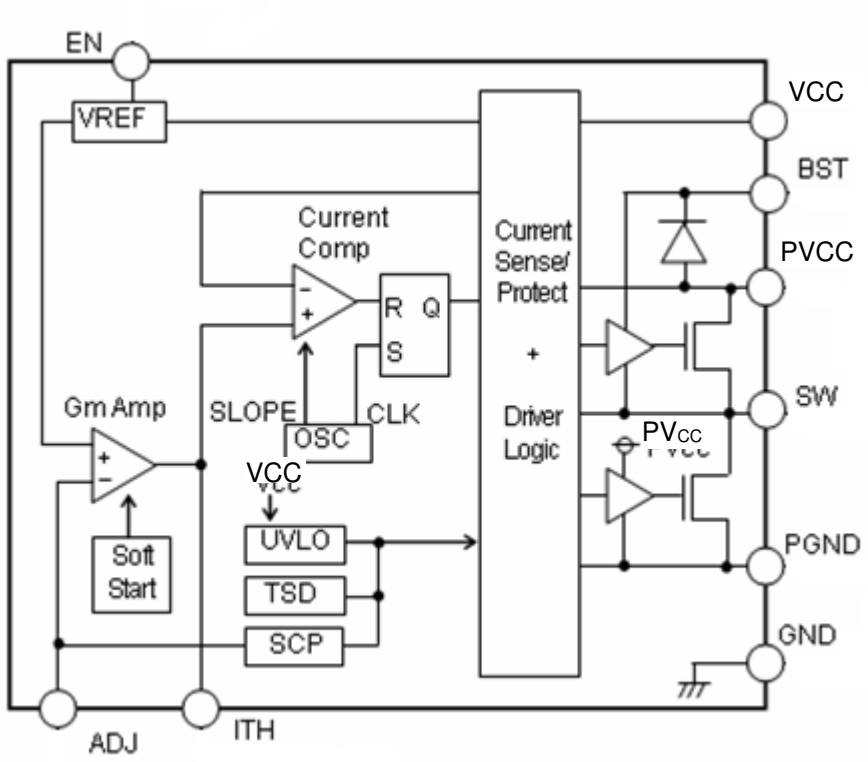


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	SW	Power switch node	11	GND	Ground pin
2	SW	Power switch node	12	ADJ	Output voltage detection pin
3	SW	Power switch node	13	ITH	GmAmp output pin/Connected to phase compensation capacitor
4	SW	Power switch node	14	N.C.	No connection
5	SW	Power switch node	15	N.C.	No connection
6	PVCC	Power switch supply pin	16	N.C.	No connection
7	PVCC	Power switch supply pin	17	EN	Enable pin(Active High)
8	PVCC	Power switch supply pin	18	PGND	Power switch ground pin
9	BST	Bootstrapped voltage input pin	19	PGND	Power switch ground pin
10	VCC	Power supply input pin	20	PGND	Power switch ground pin

Block Diagram



Absolute Maximum Ratings(Ta=25°C)

Parameter	Symbol	Rating	Unit
VCC Voltage	V_{CC}	-0.3 to +7 (Note 1)	V
PVCC Voltage	PV_{CC}	-0.3 to +7 (Note 1)	V
BST Voltage	V_{BST}	-0.3 to +13	V
BST_SW Voltage	V_{BST-SW}	-0.3 to +7	V
EN Voltage	V_{EN}	-0.3 to +7	V
SW,ITH Voltage	V_{SW}, V_{ITH}	-0.3 to +7	V
Power Dissipation 1	Pd1	0.34 (Note 2)	W
Power Dissipation 2	Pd2	0.70 (Note 3)	W
Power Dissipation 3	Pd3	1.21 (Note 4)	W
Power Dissipation 4	Pd4	3.56 (Note 5)	W
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

(Note 1) Pd should not be exceeded.
(Note 2) IC only
(Note 3) Mounted on a 1-layer 74.2mmx74.2mmx1.6mm glass-epoxy board, occupied copper foil area : 10.29mm^2
(Note 4) Mounted on a 4-layer 74.2mmx74.2mmx1.6mm glass-epoxy board, occupied copper foil area: 10.29mm^2 in each layer
(Note 5) Mounted on a 4-layer 74.2mmx74.2mmx1.6mm glass-epoxy board, occupied copper foil area : 5505mm^{2}in each layer

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-40°C to +105°C)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	2.7	3.3	5.5	V
	PV_{CC}	2.7	3.3	5.5	V
EN Voltage	V_{EN}	0	-	5.5	V
Output Voltage Setting Range	V_{OUT}	0.8	-	2.5 (Note 6)	V
SW Average Output Current	I_{SW}	-	-	3.0 (Note 7)	A

(Note 6) In case of setting the output voltage to 1.6V or more, V_{CC}Min = V_{OUT}+1.2V.
(Note 7) Pd should not be exceeded.

Electrical Characteristics(Ta=25°C V_{CC}=PV_{CC}=3.3V, V_{EN}=V_{CC}, R_1=10kΩ, R_2=5kΩ ,unless otherwise specified.)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Standby Current	I_{STB}	-	0	10	µA	EN=GND
Active Current	I_{CC}	-	250	500	µA	VCC current
EN Low Voltage	V_{ENL}	-	GND	0.8	V	Standby mode
EN High Voltage	V_{ENH}	2.0	V_{CC}	-	V	Active mode
EN Input Current	I_{EN}	-	1	10	µA	V_{EN}=3.3V
Oscillation Frequency	f_{OSC}	0.8	1	1.2	MHz	
High Side FET ON-Resistance	R_{ONH}	-	82	115	mΩ	PV_{CC}=3.3V
Low Side FET ON-Resistance	R_{ONL}	-	70	98	mΩ	PV_{CC}=3.3V
ADJ Voltage	V_{ADJ}	0.788	0.800	0.812	V	
ITH Sink Current	I_{THSI}	10	18	-	µA	V_{ADJ}=1V
ITH Source Current	I_{THSO}	10	18	-	µA	V_{ADJ}=0.6V
UVLO Threshold Voltage	V_{UVLO1}	2.400	2.500	2.600	V	V_{CC}=3.3V to 0V
UVLO Release Voltage	V_{UVLO2}	2.425	2.550	2.700	V	V_{CC}=0V to 3.3V
Soft Start Time	t_{SS}	2.5	5	10	ms	
Timer Latch Time	t_{LATCH}	0.5	1	2	ms	
Output Short Circuit Threshold Voltage	V_{SCP}	-	0.40	0.56	V	V_{ADJ} =0.8V to 0V

Typical Performance Curves

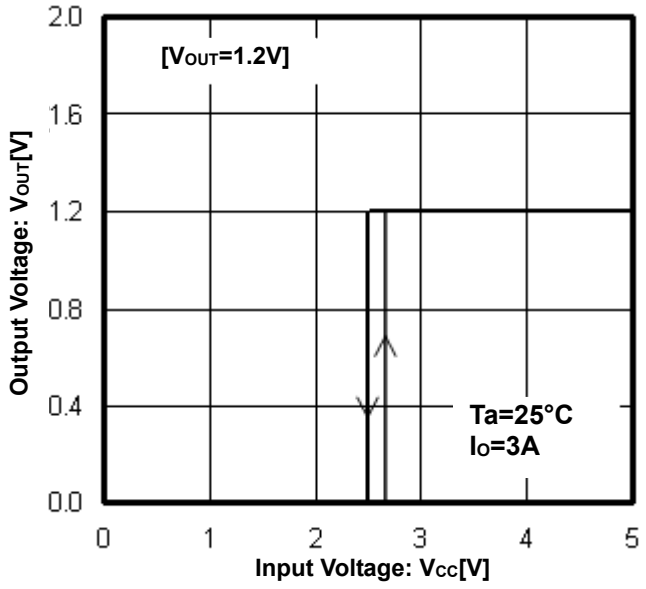


Figure 4. Output Voltage vs Input Voltage

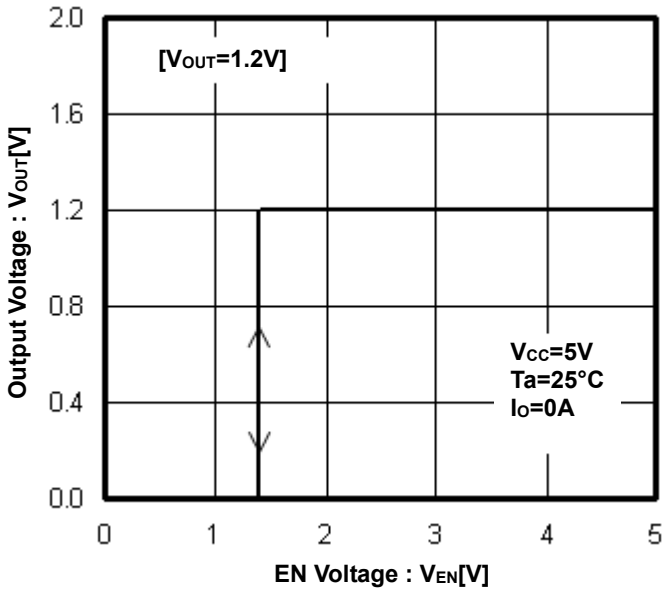


Figure 5. Output Voltage vs EN Voltage

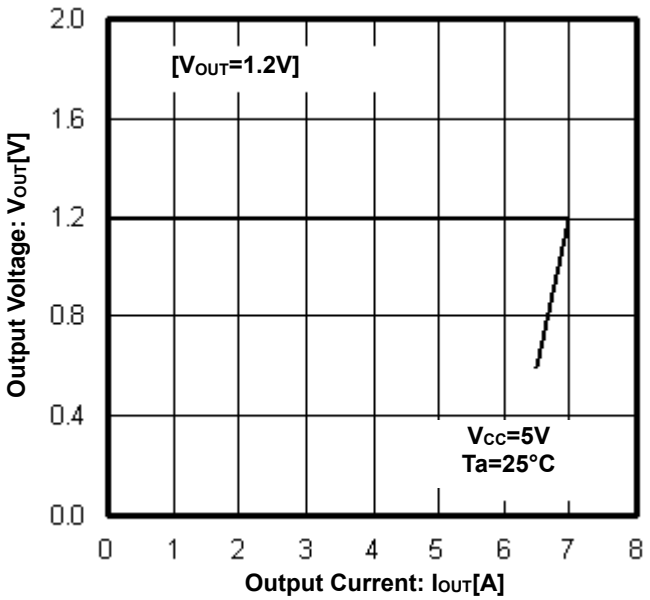


Figure 6. Output Voltage vs Output Current

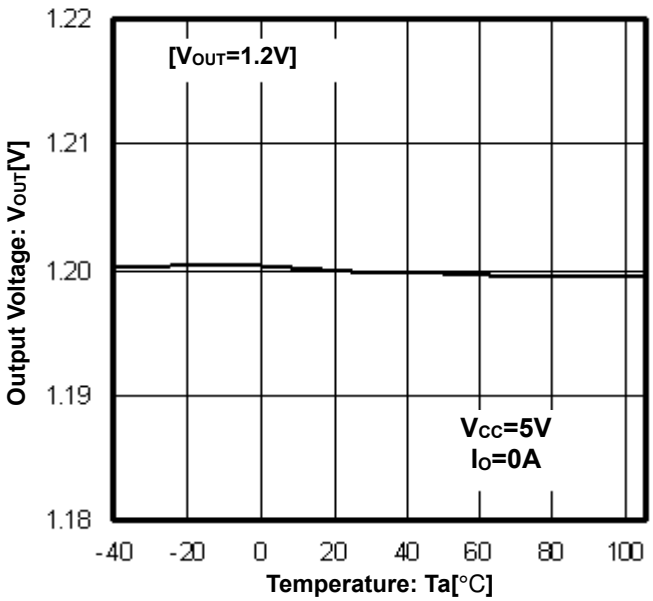


Figure 7. Output Voltage vs Temperature

Typical Performance Curves - continued

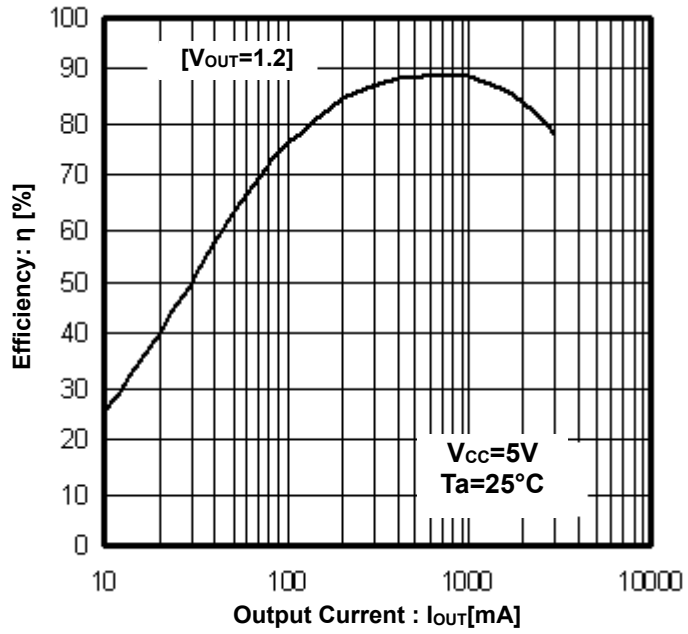


Figure 8. Efficiency vs Output Current

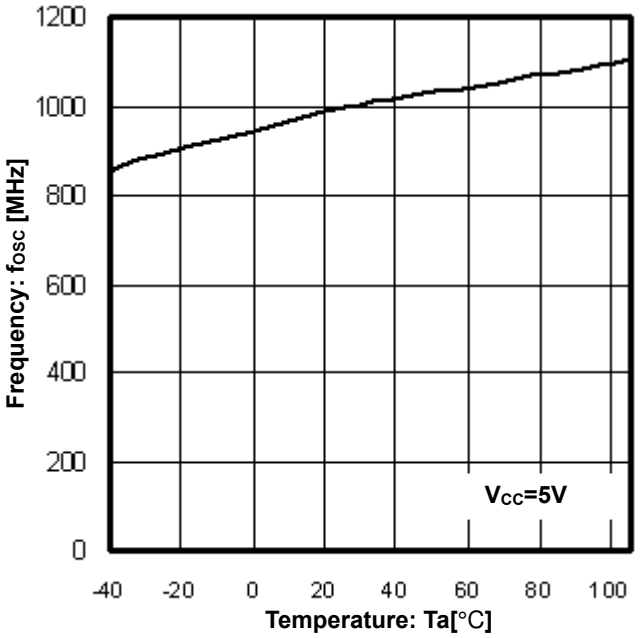


Figure 9. Frequency vs Temperature

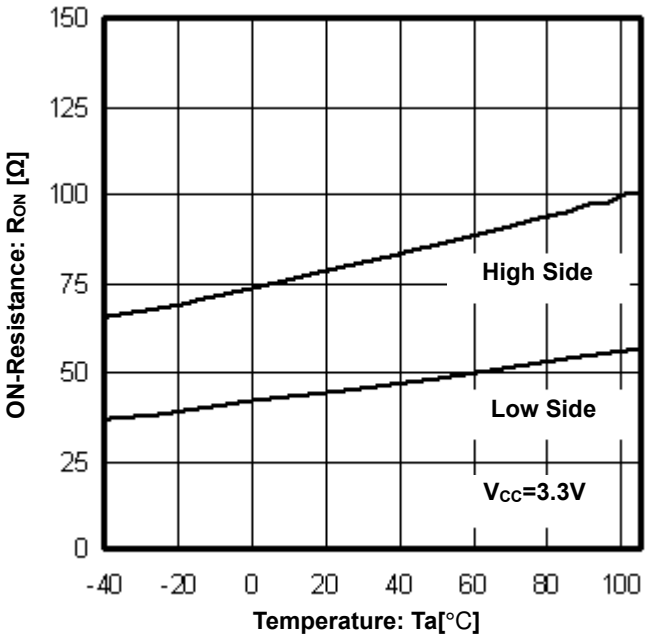


Figure 10. ON-Resistance vs Temperature

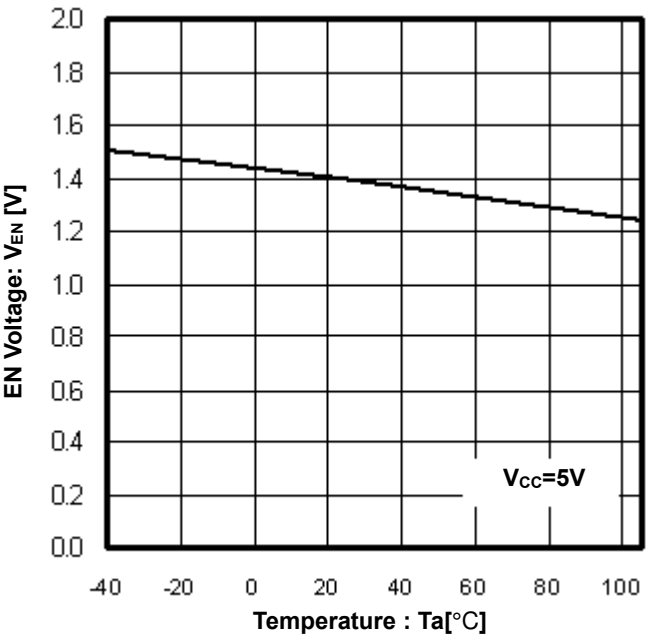


Figure 11. EN Voltage vs Temperature

Typical Performance Curves – continued

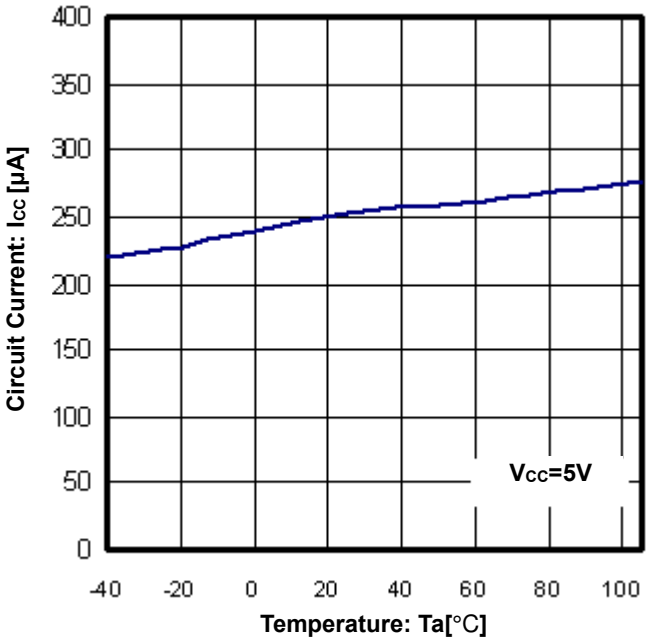


Figure 12. Circuit Current vs Temperature

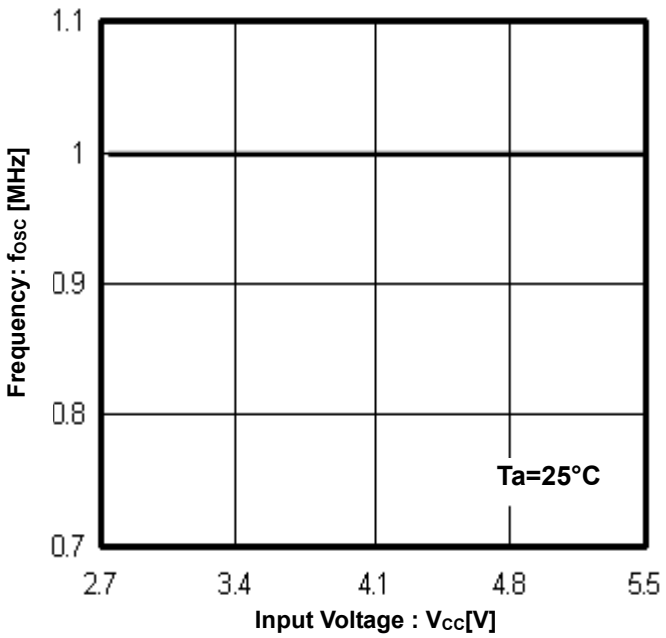


Figure 13. Frequency vs Input Voltage

Typical Waveforms

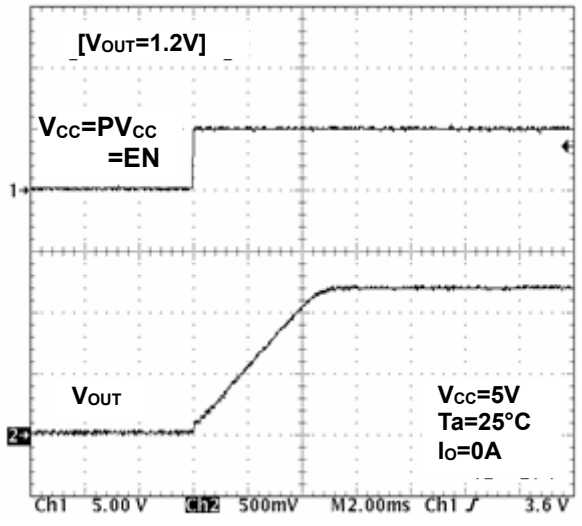


Figure 14. Soft Start Waveform

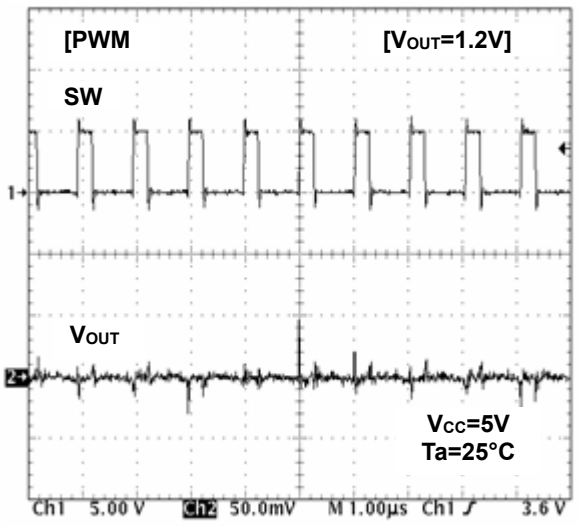


Figure 15. SW Waveform
(Io=10mA)

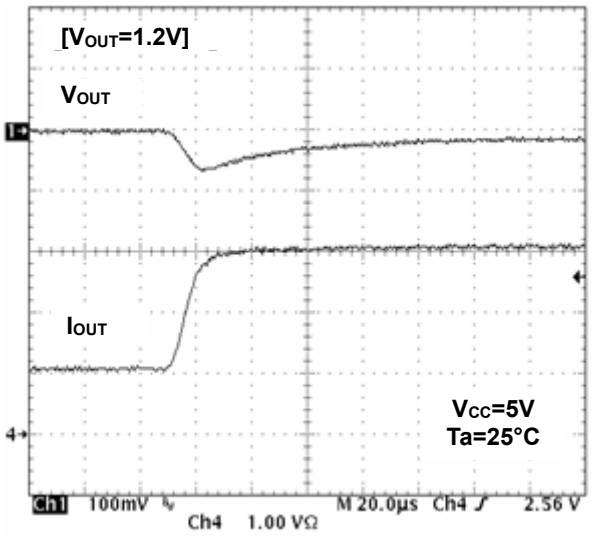


Figure 16. Transient Response
(Io=1A to 3A, 10µs)

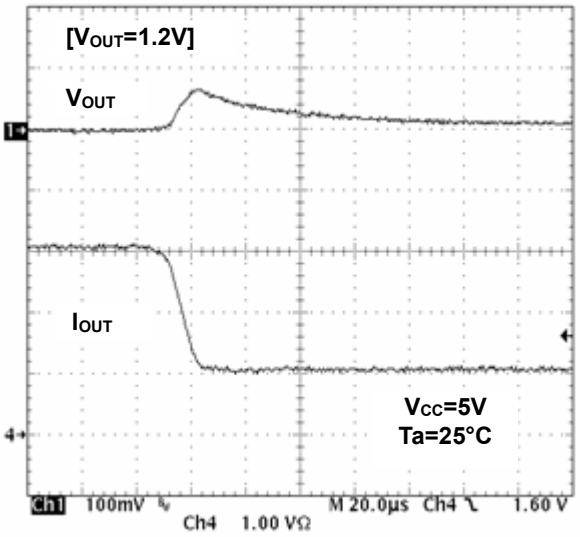


Figure 17. Transient Response
(Io=3A to 1A, 10µs)

Application Information

1. Operation

BD8962MUV is a synchronous step-down switching regulator that achieves fast transient response by employing current mode PWM control system.

(1) Synchronous Rectifier

Integrated synchronous rectification using two MOSFETs reduces power dissipation and increases efficiency when compared to converters using external diodes. Internal shoot-through current limiting circuit further reduces power dissipation.

(2) Current Mode PWM Control

PWM control signal of this IC depends on two feedback loops, the voltage feedback and the inductor current feedback.

(a) PWM (Pulse Width Modulation) control

The clock signal coming from OSC has a frequency of 1MHz. When OSC sets the RS latch, the P-Channel MOSFET is turned ON and the N-Channel MOSFET is turned OFF. The opposite happens when the current comparator (Current Comp) resets the RS latch i.e. the P-Channel MOSFET is turned OFF and the N-Channel MOSFET is turned ON. Current Comp's output is a comparison of two signals, the current feedback control signal "SENSE" which is a voltage proportional to the current IL, and the voltage feedback control signal, FB.

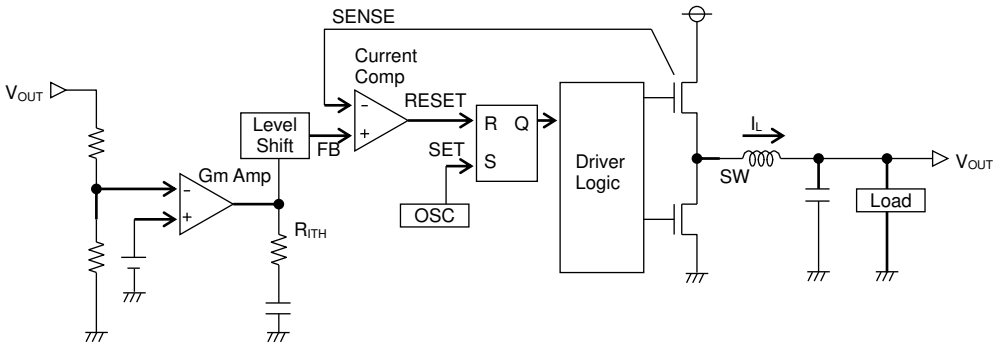


Figure 18. Diagram of Current Mode PWM Control

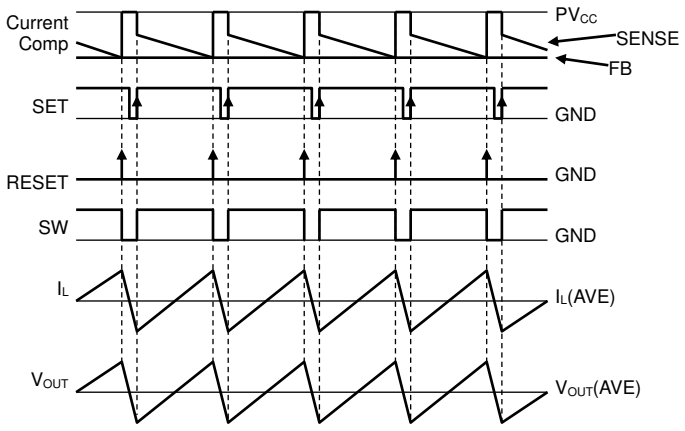


Figure 19. PWM Switching Timing Chart

2. Description of Operations

(1) Soft-Start Function
During start-up, the soft-start circuit gradually establishes the output voltage to limit the input current. This prevents the overshoot in the output voltage and inrush current.

(2) Shutdown Function
When the EN terminal is shifted to “Low”, the device operates in Standby Mode, and all the functional blocks including the reference voltage circuit, internal oscillator and drivers are turned OFF. Circuit current during standby is 0μA (Typ).

(3) UVLO Function
The UVLO circuit detects whether the input voltage is sufficient to obtain the output voltage of this IC. A hysteresis width of 50mV (Typ) is provided to prevent the output from chattering.

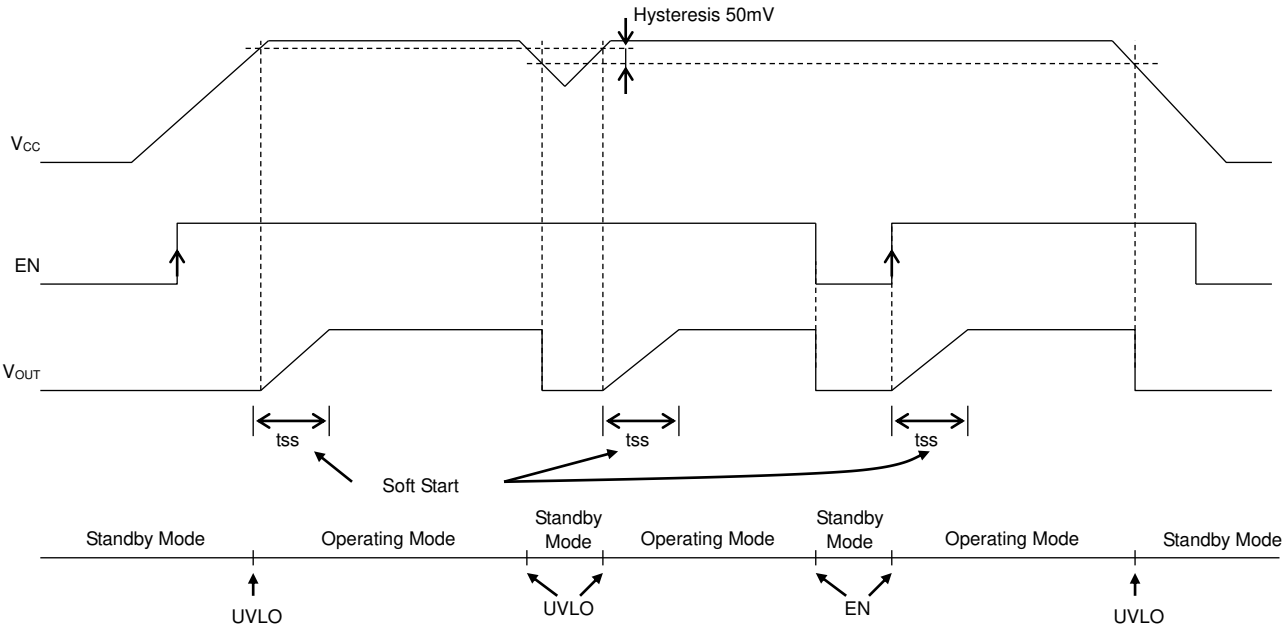


Figure 20. Soft Start, Shutdown, UVLO Timing Chart

(4) Short Circuit Protection with Time Delay Function
To protect the IC from breakdown, the short circuit protection turns the output OFF when the internal circuit limiter is activated continuously for a fixed time (t_{LATCH}) or more. The output that is kept OFF may be turned ON again by restarting EN or by resetting UVLO.

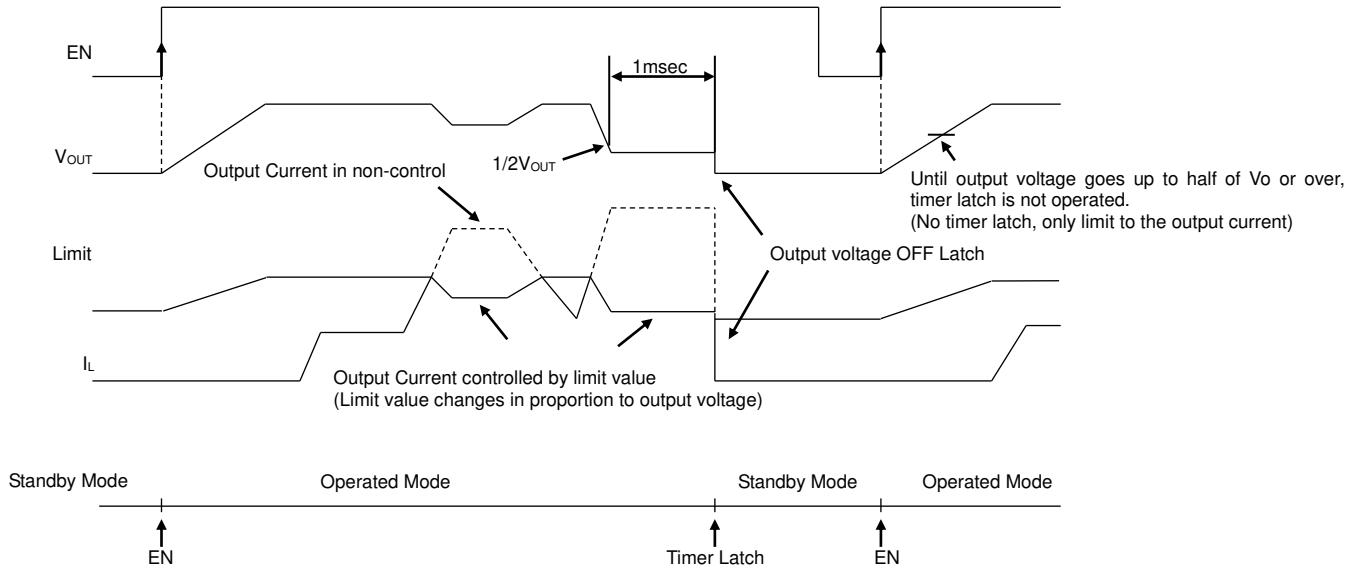
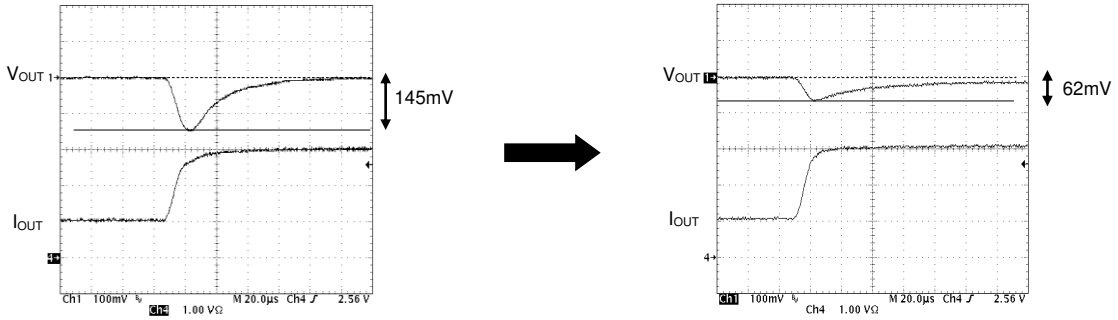


Figure 21. Short Current Protection Circuit with Time Delay Timing Chart

3. Information on Advantages

Advantage 1 : Offers fast transient response by using current mode control system

Conventional product (Load response I_O=1A to 3A) BD8962MUV (Load response I_O=1A to 3A)



Voltage drop due to sudden change in load was reduced by about 50%.

Figure 22. Comparison of Transient Response

Advantage 2 : Offers high efficiency for all load range because of its synchronous rectifier

For heavier load:
This IC utilizes the synchronous rectifying mode and uses low ON-Resistance MOSFET power transistors.

{ ON-Resistance of High Side MOSFET : 82mΩ(Typ)
{ ON-Resistance of Low Side MOSFET : 70mΩ(Typ)

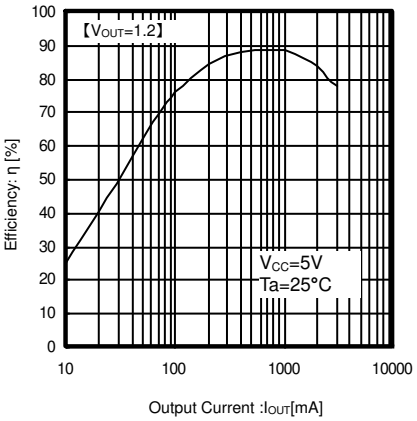


Figure 23. Efficiency

Advantage 3 : ・Supplied in smaller package due to integration of small-sized power MOSFETs

・Required output capacitor ,Co, for current mode control: 22µF ceramic capacitor
・Required inductance ,L, for the operating frequency of 1 MHz: 2.2µH inductor
・Integrates FET + Boot strap diode

Reduces the required mounting area

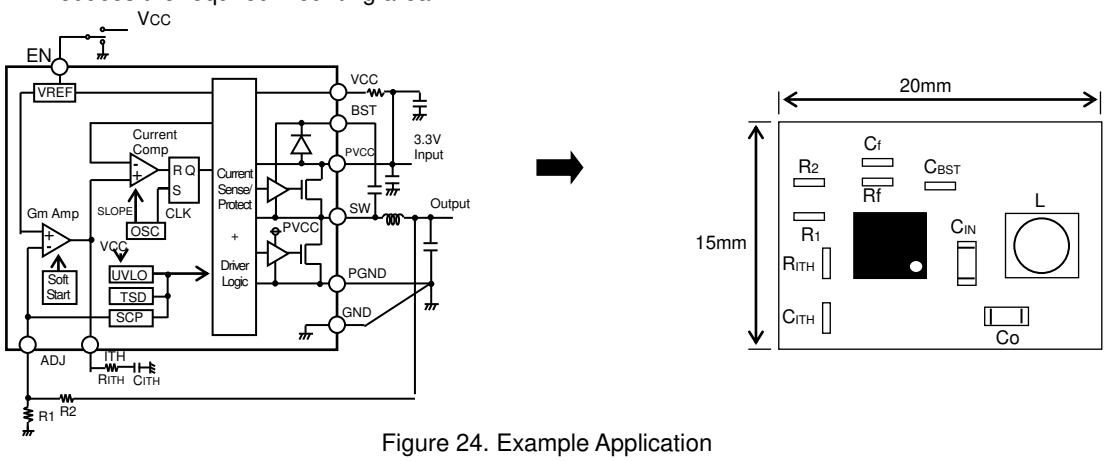


Figure 24. Example Application

4. Switching Regulator Efficiency

Efficiency η may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100 = \frac{P_{OUT}}{P_{IN}} \times 100 = \frac{P_{OUT}}{P_{OUT} + Pd\alpha} \times 100 \quad [\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors Pdα as follows:

Dissipation Factors:

(1) ON-Resistance Dissipation of Inductor and FET : Pd(I^2R)

$$Pd(I^2R) = {I_{OUT}}^2 \times (R_{COIL} + R_{ON})$$

Where:
R_{COIL} is the DC resistance of inductor
R_{ON} is the ON-Resistance of FET
I_{OUT} is the output current

(2) Gate Charge/Discharge Dissipation : Pd(Gate)

$$Pd(Gate) = C_{gs} \times f \times V^2$$

Where:
C_{gs} is the gate capacitance of FET
f is the switching frequency
V is the gate driving voltage of FET

(3) Switching Dissipation : Pd(SW)

$$Pd(SW) = \frac{{V_{IN}}^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$$

Where:
C_{RSS} is the reverse transfer capacitance of FET
I_{DRIVE} is the peak current of gate

(4) ESR Dissipation of Capacitor : Pd(ESR)

$$Pd(ESR) = {I_{RMS}}^2 \times ESR$$

Where:
I_{RMS} is the ripple current of capacitor
ESR is the equivalent series resistance

(5) Operating Current Dissipation of IC : Pd(IC)

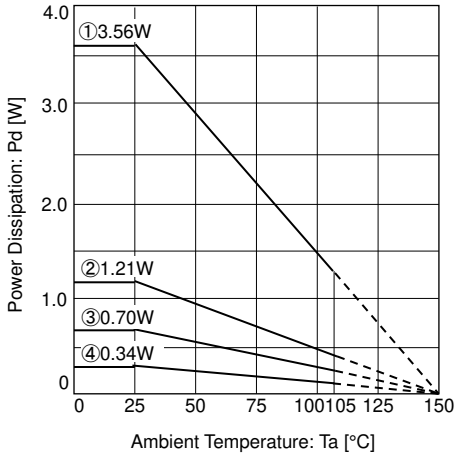
$$Pd(IC) = V_{IN} \times I_{CC}$$

Where:
I_{CC} is the circuit current

5. Consideration on Permissible Dissipation and Heat Generation

Since this IC functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to the DC resistance of inductor and ON-Resistance of FET are considered because conduction losses are more significant than other means of dissipation mentioned above including gate charge/discharge dissipation and switching dissipation.



① 4 layers (Copper foil area : 5505mm^2) copper foil in each layer
θ j-a=35.1°C/W
② 4 layers (Copper foil area : 10.29m^2) copper foil in each layer
θ j-a=103.3°C/W
③ 1 layers (Copper foil area : 10.29m^2)
θ j-a=178.6°C/W
④IC only.
θ j-a=367.6°C/W

Figure 25. Thermal Dissipation Curve (VQFN020V4040)

$$P = I_{OUT}{}^2 \times R_{ON}$$
$$R_{ON} = D \times R_{ONH} + (1 - D)R_{ONL}$$

Where:
D is the ON duty (=V_{OUT}/V_{CC})
R_{ONH} is the ON-Resistance of High Side MOSFET
R_{ONL} is the ON-Resistance of Low Side MOSFET
I_{OUT} is the Output Current

If V_{CC}=3.3V, V_{OUT}=1.8V, R_{ONH}=82mΩ, R_{ONL}=70mΩ
I_{OUT}=3A, for example,
D=V_{OUT}/V_{CC}=1.8/3.3=0.545
R_{ON}=0.545 x 0.082+(1-0.545) x 0.07
=0.0447+0.0319
=0.0766[Ω]

P=3^2 x 0.0766＝0.6894[W]

Since R_{ONH} is greater than R_{ONL} in this IC, the dissipation increases as the ON duty becomes greater. Taking into consideration the dissipation as shown above, thermal design must be carried out with allowable sufficient margin.

6. Selection of Externally Connected components

(1) Selection of Inductor (L)

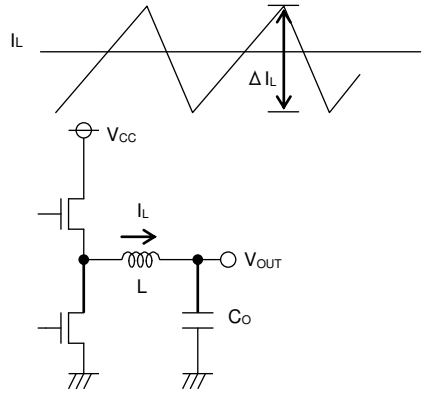


Figure 26. Output Ripple Current

The inductance significantly depends on output ripple current. As shown in equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{L\times V_{CC}\times f} \quad [A] \quad \cdot\cdot\cdot (1)$$

Appropriate ripple current at output should be +/-20% of the maximum output current.

$$\Delta I_L = 0.2\times I_{OUTMax} \quad [A] \quad \cdot\cdot\cdot (2)$$

$$L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{\Delta I_L \times V_{CC}\times f} \quad [H] \quad \cdot\cdot\cdot (3)$$

Where:
ΔI_L is the Output ripple current, and
f is the Switching frequency

Note: Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected to allow a sufficient margin with which the peak current may not exceed the inductor's current rating.

If V_{CC}=5.0V, V_{OUT}=2.5V, f=1MHz, ΔI_L=0.2A x 3A=0.6A, for example, (BD8962MUV)

$$L = \frac{(5-2.5)\times 2.5}{0.6\times 5\times 1M} = 2.08\mu \rightarrow 2.2 \quad [\mu H]$$

Note: Select an inductor with low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

(2) Selection of Output Capacitor (C_O)

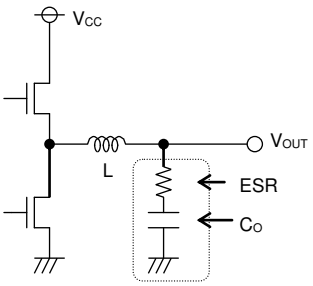


Figure 27. Output Capacitor

Output capacitor should be selected with consideration on the stability region and the equivalent series resistance required in smoothing the ripple voltage.

Output ripple voltage is determined by equation (4) :

$$\Delta V_{OUT} = \Delta I_L \times ESR \quad [V] \quad \cdot\cdot\cdot (4)$$

Where:
ΔI_L is the Output ripple current, and
ESR is the Equivalent series resistance of output capacitor

Note: Rating of the capacitor should be determined to allow a sufficient margin against output voltage. A 22µF to 100µF ceramic capacitor is recommended. Less ESR allows reduction in output ripple voltage.

(3) Selection of Input Capacitor (C_{IN})

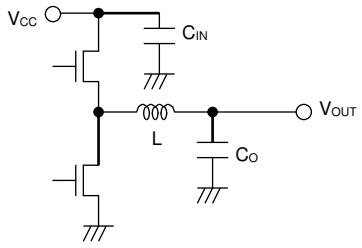


Figure 28. Input Capacitor

The input capacitor must be a low ESR capacitor with a capacitance sufficient to cope with high ripple current. This is to prevent high transient voltage. The ripple current I_{RMS} is given by equation (5):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{CC} - V_{OUT})}}{V_{CC}} \quad [A] \quad \cdot\cdot\cdot (5)$$

< Worst case > I_{RMSMax}

When $V_{CC} = 2 \times V_{OUT}, I_{RMS} = \frac{I_{OUT}}{2}$

If V_{CC}=3.3V, V_{OUT}=1.8V, and I_{OUTMax}=3A, (BD8962MUV)

$$I_{RMS} = 3 \times \frac{\sqrt{1.8(3.3-1.8)}}{3.3} \approx 1.49 \quad [A_{RMS}]$$

A low ESR 22µF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

(4) Calculating R_{ITH}, C_{ITH} for Phase Compensation

Since the Current Mode Control is designed to limit the inductor current, a pole (phase lag) appears in low frequencies due to RC filter consisting of an output capacitor and load resistance, while a zero (phase lead) appears in high frequencies due to the output capacitor and its ESR. Therefore, phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

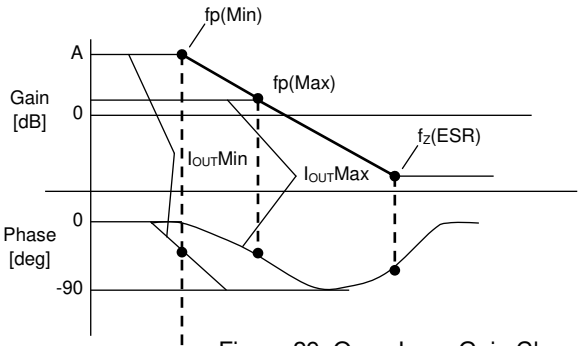


Figure 29. Open Loop Gain Characteristics

$$fp = \frac{1}{2\pi \times R_O \times C_O}$$

$$f_Z(ESR) = \frac{1}{2\pi \times ESR \times C_O}$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency decreases.

$$fp(Min) = \frac{1}{2\pi \times R_{OMax} \times CO} \quad [Hz] \leftarrow with\ lighter\ load$$

$$fp(Max) = \frac{1}{2\pi \times R_{OMin} \times CO} \quad [Hz] \leftarrow with\ heavier\ load$$

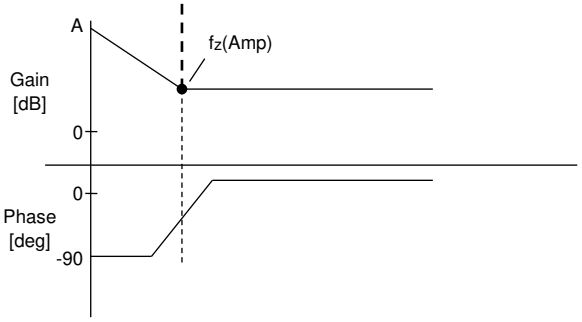


Figure 30. Error Amp Phase Compensation Characteristics

Zero at power amplifier

Increasing the capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR is reduced to half.)

$$f_Z(Amp) = \frac{1}{2\pi \times R_{ITH} \times C_{ITH}}$$

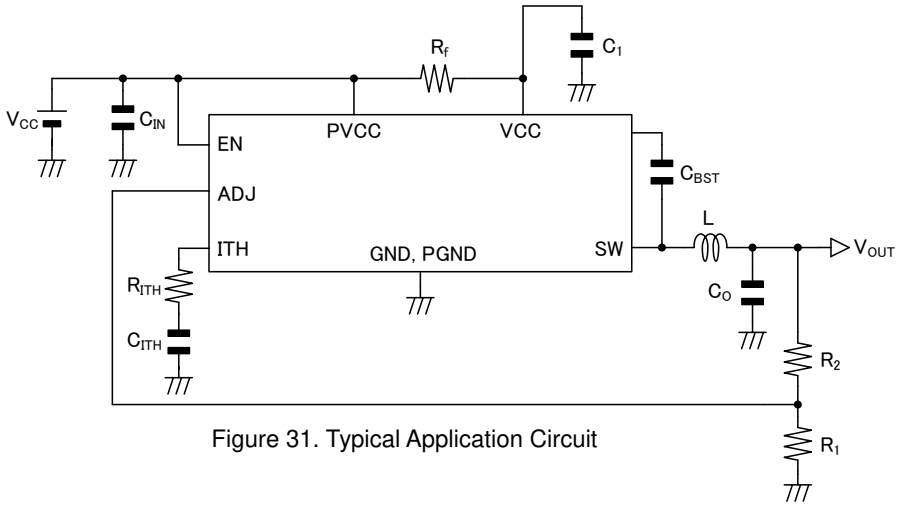


Figure 31. Typical Application Circuit

Stable feedback loop may be achieved by canceling the pole fp (Min) produced by the output capacitor and the load resistance with RC zero correction by the error amplifier.

$$f_Z(Amp) = fp(Min)$$
$$\rightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times R_{OMax} \times C_O}$$

(5) Setting the Output Voltage

The output voltage V_{OUT} is determined by equation (6):

$$V_{OUT} = (R_2 / R_1 + 1) \times V_{ADJ} \quad \cdot\cdot\cdot (6)$$

Where:
V_{ADJ} is the Voltage at ADJ terminal (0.8V Typ)
The required output voltage may be determined by adjusting R_1 and R_2.

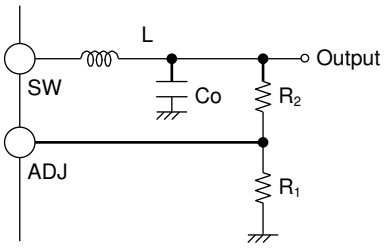


Figure 32. Determination of Output Voltage

〔 Output Voltage Range: 0.8V to 2.5V 〕

Use 1 kΩ to 100 kΩ resistor for R_1. When using a resistor with resistance higher than 100 kΩ, check the setup carefully for ripple voltage etc.

The lower limit of input voltage depends on the output voltage. Basically, it is recommended to use given condition:

$$V_{CCMin} = V_{OUT} + 1.2V$$

Figure 33. shows the necessary output current value at the lower limit of input voltage. (DCR of inductor: 20mΩ)
These data show characteristic value of the IC. It doesn't guarantee the operating range.

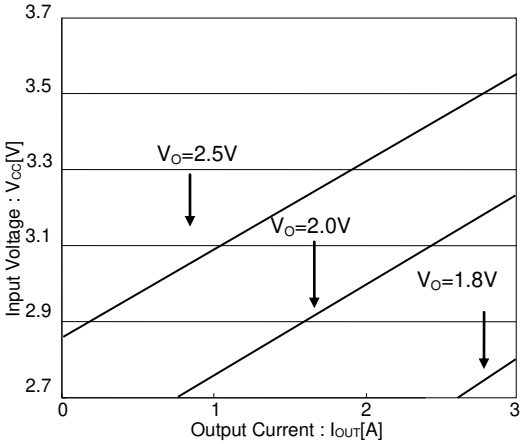


Figure 33. Minimum Input Voltage in each Output Voltage

7. BD8962MUV Cautions on PC Board Layout

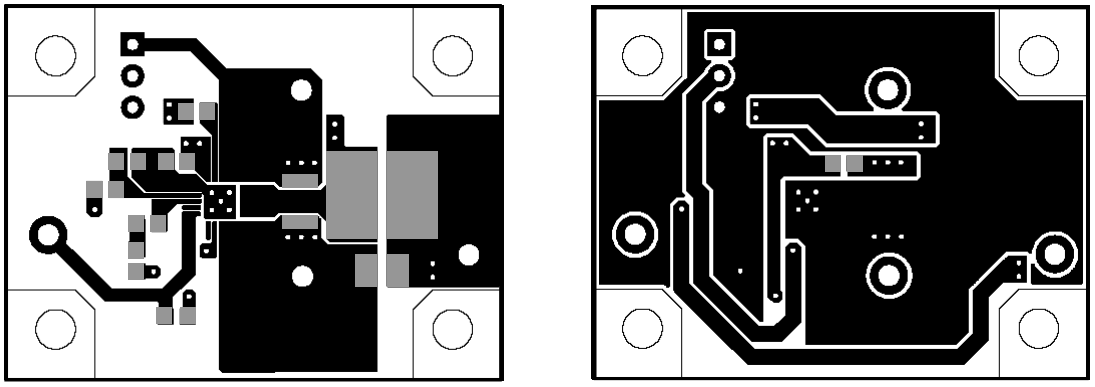


Figure 34. Layout Diagram

(1) Layout the input ceramic capacitor C_{IN} closer to the pins PVCC and PGND, and the output capacitor Co closer to the pin PGND.
(2) Layout C_{ITH} and R_{ITH} between the pins ITH and GND as near as possible with the least necessary wiring.

Note: VQFN020V4040 (BD8962MUV) has thermal PAD on the reverse of the package.
The package thermal performance may be enhanced by bonding the PAD to GND plane, which occupies a large area of the PCB.

8. Recommended Components List for Above Application

Symbol	Part	Value		Manufacturer	Series
L	Coil	2.0µH		Sumida	CDR6D28MNP-2R0NC
		2.2µH		Sumida	CDR6D26NP-2R2NC
C_{IN}	Ceramic Capacitor	22µF		Murata	GRM32EB11A226KE20
C_O	Ceramic Capacitor	22µF		Murata	GRM31CB30J226KE18
C_{ITH}	Ceramic Capacitor	V_{OUT}=1.0V	1500pF	Murata	CRM18 Series
		V_{OUT}=1.2V	1000pF	Murata	GRM18 Series
		V_{OUT}=1.5V	1000pF	Murata	GRM18 Series
		V_{OUT}=1.8V	560pF	Murata	GRM18 Series
		V_{OUT}=2.5V	560pF	Murata	GRM18 Series
R_{ITH}	Resistance	V_{OUT}=1.0V	5.6kΩ	Rohm	MCR03 Series
		V_{OUT}=1.2V	6.8kΩ	Rohm	MCR03 Series
		V_{OUT}=1.5V	6.8kΩ	Rohm	MCR03 Series
		V_{OUT}=1.8V	8.2kΩ	Rohm	MCR03 Series
		V_{OUT}=2.5V	12kΩ	Rohm	MCR03 Series
Cf	Ceramic Capacitor	1000 pF		Murata	GRM18 Series
Rf	Resistance	10Ω		Rohm	MCR03 Series
C_{BST}	Ceramic Capacitor	0.1 µF		Murata	GRM18 Series

Note: The parts list presented above is an example of the recommended parts. Although the parts are standard, actual circuit characteristics should be checked in your application carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is significant and may affect the system, a low pass filter should be inserted between the VCC and PVCC pins, and a schottky barrier diode or snubber established between the SW and PGND pins.

I/O Equivalent Circuit

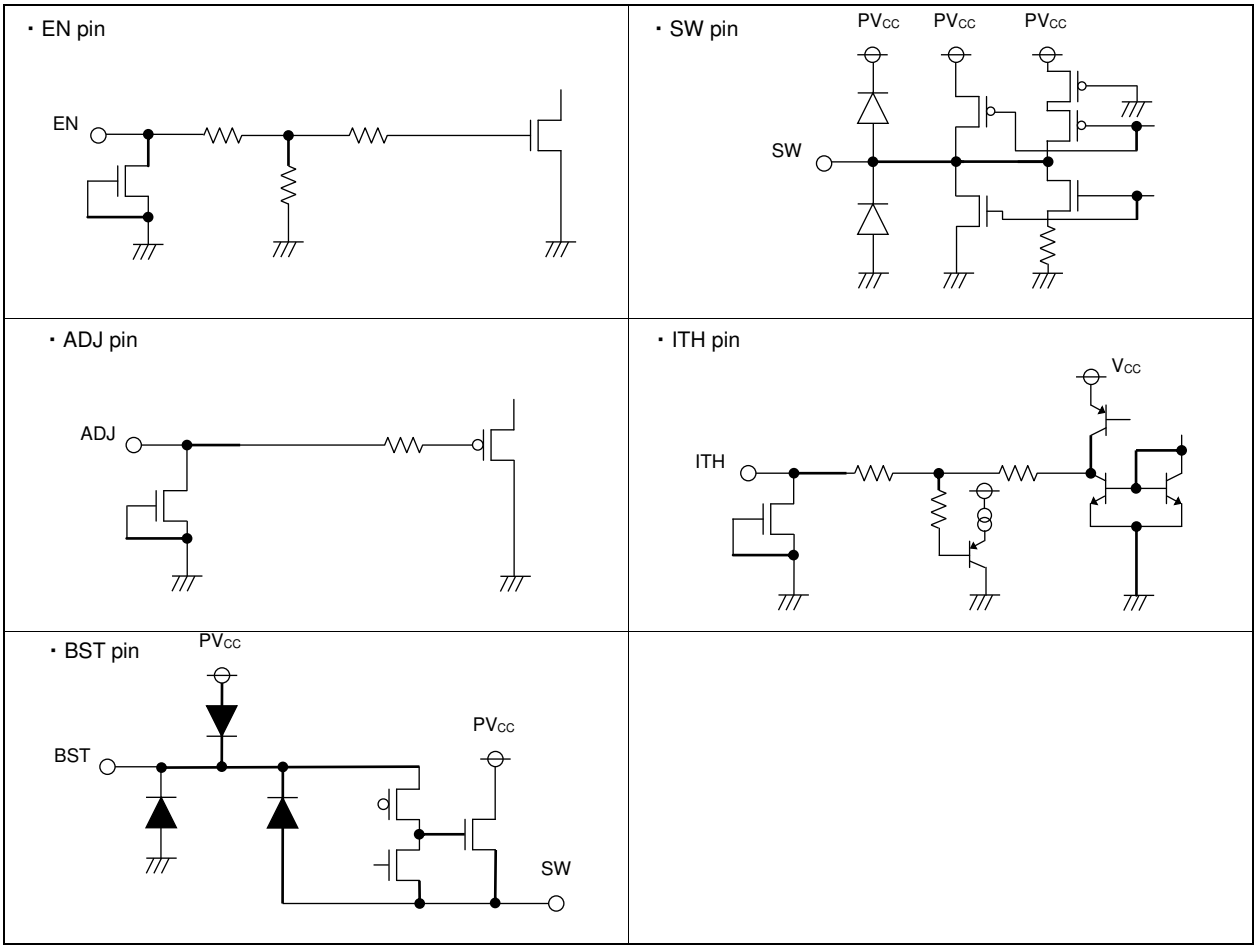


Figure 35. I/O Equivalent Circuit

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

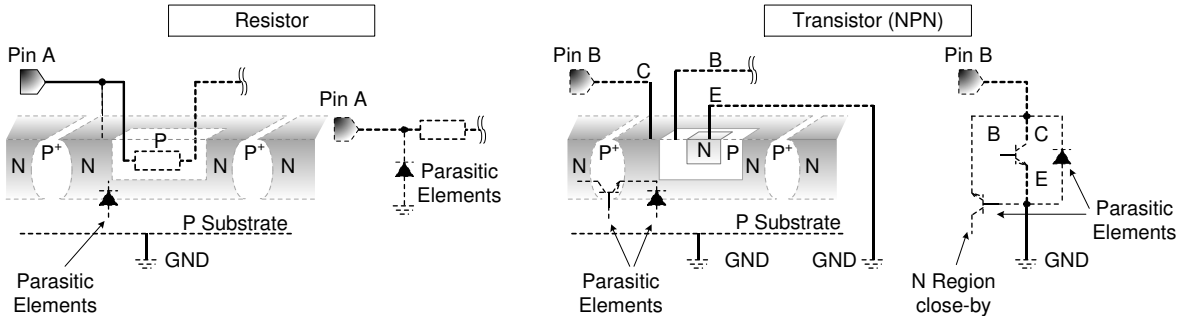


Figure 36. Example of monolithic IC structure

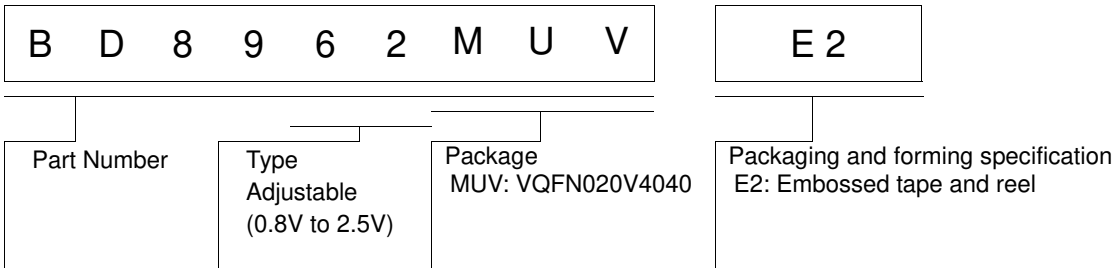
13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

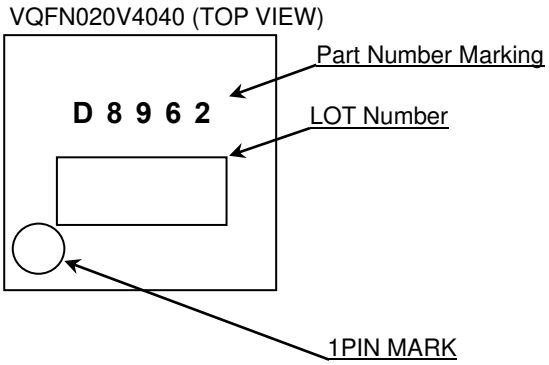
14. Selection of Inductor

It is recommended to use an inductor with a series resistance element (DCR) 0.1Ω or less. Especially, note that use of a high DCR inductor will cause an inductor loss, resulting in decreased output voltage. Should this condition continue for a specified period (soft start time + timer latch time), output short circuit protection will be activated and output will be latched OFF. When using an inductor over 0.1Ω, be careful to ensure adequate margins for variation between external devices and this IC, including transient as well as static characteristics. Furthermore, in any case, it is recommended to start up the output with EN after supply voltage is within.

Ordering Information

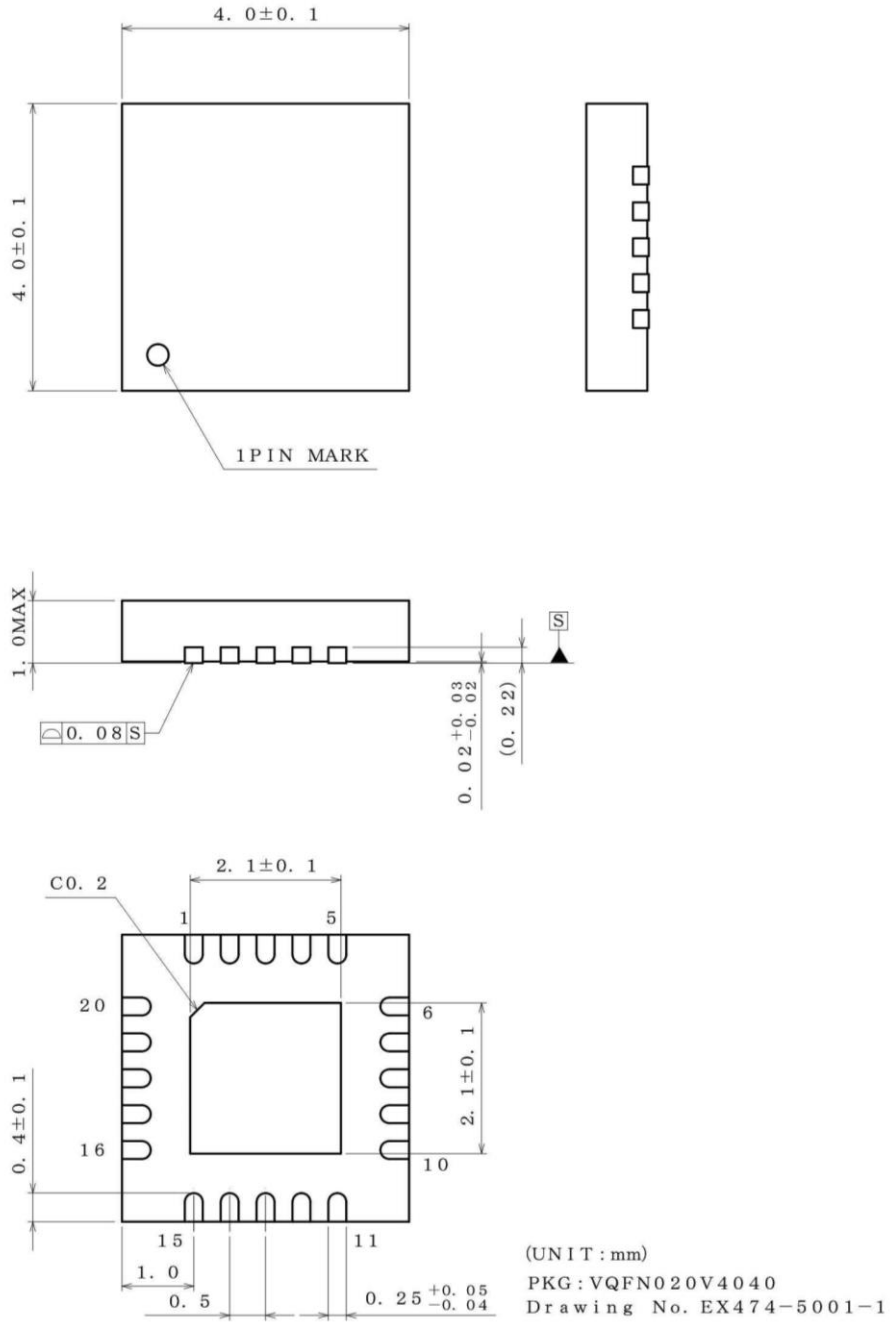


Marking Diagram



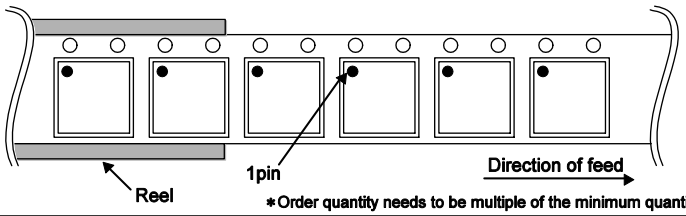
Physical Dimension Tape and Reel Information

Package Name	VQFN020V4040



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
02.Mar.2012	001	New Release
02.Oct.2014	002	Applied the ROHM Standard Style and improved understandability.

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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