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74VHC595 8-Bit Shift Register with Output Latches

Features

- High Speed: t_{PD} = 5.4ns (Typ.) at V_{CC} = 5V
- Low power dissipation: $I_{CC} = 4\mu A$ (Max.) at $T_A = 25$ °C
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- Power down protection is provided on all inputs
- Low noise: V_{OLP} = 0.9V (Typ.)
- Pin and function compatible with 74HC595

General Description

The VHC595 is an advanced high-speed CMOS Shift Register fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has eight 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

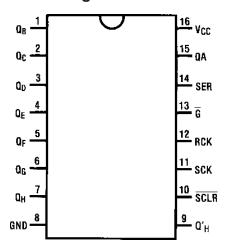
An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Ordering Information

Order Number	Package Number	Package Description
74VHC595M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC595SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC595MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

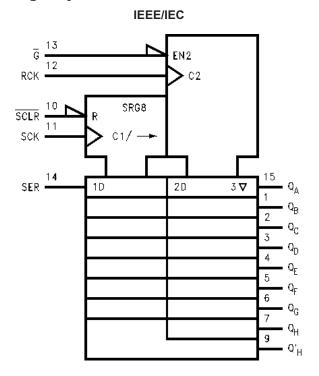
Connection Diagram



Pin Description

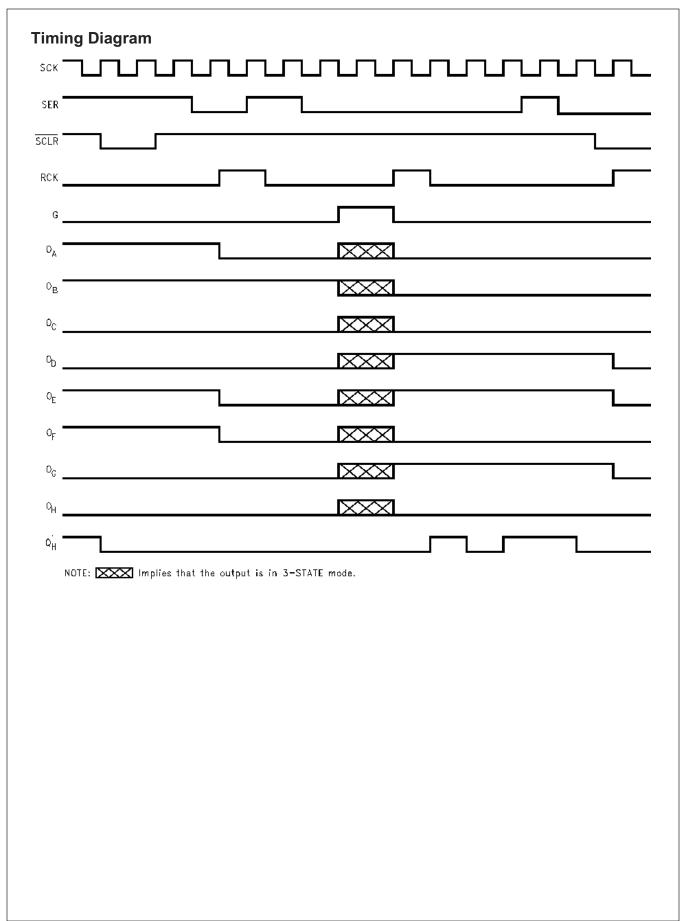
Pin Names	Description
SER	Serial Data Input
SCK	Shift Register Clock Input (Active rising edge)
RCK	Storage Register Clock Input (Active rising edge)
SCLR	Reset Input
G	3-STATE Output Enable Input (Active LOW)
$Q_A - Q_H$	Parallel Data Outputs
Q' _H	Serial Data Output

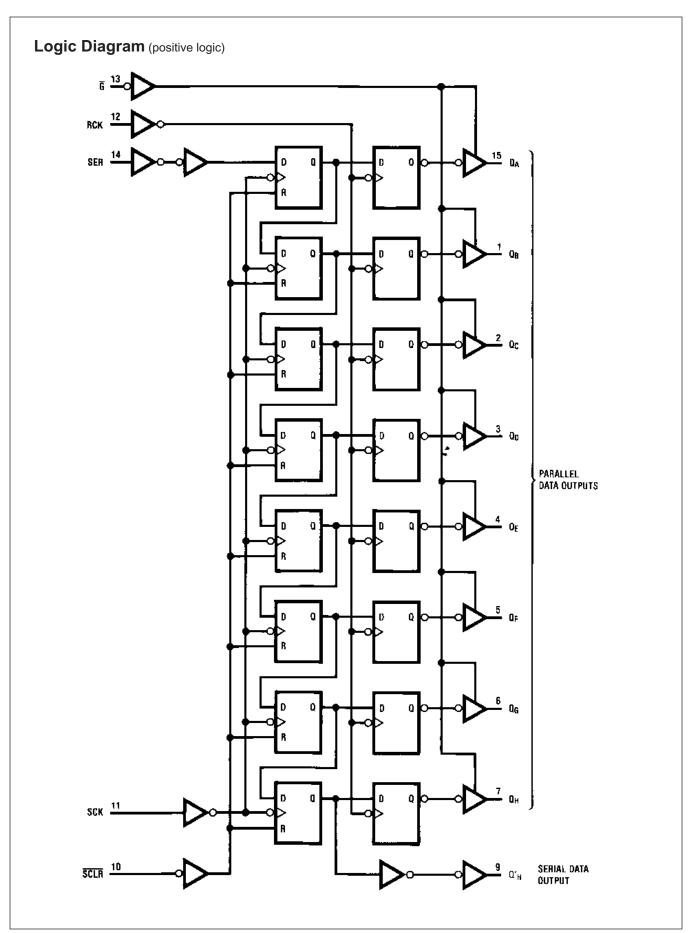
Logic Symbol



Truth Table

Inputs									
SER	RCK SCK SCLR G				Function				
Х	Х	Х	Х	Н	Q _A thru Q _H 3-STATE				
Х	Х	Х	Х	L	Q _A thru Q _H outputs enabled				
Х	Х	Х	L	L	Shift Register cleared: Q' _H = 0				
L	Х	1	Н	L	Shift Register clocked: $Q_N = Q_{n-1}$, $Q_0 = SER = L$				
Н	Х	1	Н	L	Shift Register clocked: $Q_N = Q_{n-1}$, $Q_0 = SER = H$				
Х	1	Х	Н	L	Contents of Shift Register transferred to output latches				





Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	-0.5V to +7.0V
V _{IN}	DC Input Voltage	-0.5V to +7.0V
V _{OUT}	DC Output Voltage	–0.5V to V _{CC} + 0.5V
I _{IK}	Input Diode Current	–20mA
I _{OK}	Output Diode Current	±20mA
I _{OUT}	DC Output Current	±25mA
I _{CC}	DC V _{CC} /GND Current	±75mA
T _{STG}	Storage Temperature	−65°C to +150°C
T _L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions⁽¹⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	2.0V to +5.5V
V _{IN}	Input Voltage	0V to +5.5V
V _{OUT}	Output Voltage	0V to V _{CC}
T _{OPR}	Operating Temperature	-40°C to +85°C
t _r , t _f	Input Rise and Fall Time	
	$V_{CC} = 3.3V \pm 0.3V$	0 ~ 100ns/V
	$V_{CC} = 5.0V \pm 0.5V$	0 ~ 20ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

					T,	T _A = 25°C		T _A = -40°C to +85°C		
Symbol	Parameter	V _{CC} (V)	Conditions		Min.	Тур.	Max.	Min.	Max.	Units
V _{IH}	HIGH Level Input	2.0			1.50			1.50		V
	Voltage	3.0 – 5.5			0.7 x V _{CC}			0.7 x V _{CC}		
V _{IL}	LOW Level Input	2.0					0.50		0.50	V
	Voltage	3.0 – 5.5					0.3 x V _{CC}		0.3 x V _{CC}	
V _{OH}	HIGH Level Output	2.0	$V_{IN} = V_{IH}$	$I_{OH} = -50\mu A$	1.9	2.0		1.9		V
Voltage	Voltage	3.0	or V _{IL}		2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		$I_{OH} = -4mA$	2.58			2.48		
		4.5		$I_{OH} = -8mA$	3.94			3.80		
V _{OL}	LOW Level Output	2.0		$I_{OL} = 50\mu A$		0.0	0.1		0.1	V
	Voltage	3.0	or V _{IL}			0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		I _{OL} = 4mA			0.36		0.44	
		4.5		I _{OL} = 8mA			0.36		0.44	
l _{OZ}	3-STATE Output Off-State Current	5.5	$V_{IN} = V_{CC}$ or GND, $V_{OUT} = V_{CC}$ or GND, $V_{IN}\overline{G} = V_{IH}$ or V_{IL}				±0.25		±2.5	μA
I _{IN}	Input Leakage Current	0 – 5.5	V _{IN} = 5.5V	or GND			±0.1		±1.0	μA
I _{CC}	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$	or GND			4.0		40.0	μA

Noise Characteristics

				$T_A = 25^{\circ}C$		
Symbol	Parameter	V _{CC} (V)	Conditions	Тур.	Limits	Units
V _{OLP} ⁽²⁾	Quiet Output Maximum Dynamic V _{OL}	5.0	C _L = 50pF	0.9	1.2	V
V _{OLV} ⁽²⁾	Quiet Output Minimum Dynamic V _{OL}	5.0	C _L = 50pF	-0.9	-1.2	V
V _{IHD} ⁽²⁾	Minimum HIGH Level Dynamic Input Voltage	5.0	C _L = 50pF		3.5	V
V _{ILD} ⁽²⁾	Maximum LOW Level Dynamic Input Voltage	5.0	C _L = 50pF		1.5	V

Note:

2. Parameter guaranteed by design.

AC Electrical Characteristics

					Т,	_λ = +25 ′	°C		–40°C 85°C	
Symbol	Parameter	V _{CC} (V)	Cond	itions	Min.	Тур.	Max.	Min.	Max.	Units
t _{PLH} , t _{PHL}	Propagation Delay Time,	3.3 ± 0.3		C _L = 15pF		7.7	11.9	1.0	13.5	ns
	RCK to Q _A –Q _H			$C_L = 50pF$		10.2	15.4	1.0	17.0	
		5.0 ± 0.5	1	C _L = 15pF		5.4	7.4	1.0	8.5	ns
				C _L = 50pF		6.9	9.4	1.0	10.5	
t _{PLH} , t _{PHL}	Propagation Delay Time,	3.3 ± 0.3		C _L = 15pF		8.8	13.0	1.0	15.0	ns
	SCK-Q'H			$C_L = 50pF$		11.3	16.5	1.0	18.5	
		5.0 ± 0.5	1	C _L = 15pF		6.2	8.2	1.0	9.4	ns
				C _L = 50pF		7.7	10.2	1.0	11.4	
t _{PHL}	Propagation Delay Time,	3.3 ± 0.3		C _L = 15pF		8.4	12.8	1.0	13.7	ns
	SCLR –Q'H			$C_L = 50pF$		10.9	16.3	1.0	17.2	
		5.0 ± 0.5		C _L = 15pF		5.9	8.0	1.0	9.1	ns
				C _L = 50pF		7.4	10.0	1.0	11.1	
t _{PZL} , t _{PZH}	Output Enable Time, G to Q _A –Q _H	3.3 ± 0.3	$R_L = 1k\Omega$	C _L = 15pF		7.5	11.5	1.0	13.5	ns
				C _L = 50pF		9.0	15.0	1.0	17.0	
		5.0 ± 0.5]	C _L = 15pF		4.8	8.6	1.0	10.0	ns
				C _L = 50pF		8.3	10.6	1.0	12.0	
t _{PLZ} , t _{PHZ}	Output Disable Time,	3.3 ± 0.3	$R_L = 1k\Omega$	$C_L = 50pF$		12.1	15.7	1.0	16.2	ns
	G to Q _A –Q _H	5.0 ± 0.5		$C_L = 50pF$		7.6	10.3	1.0	11.0	
f _{MAX}	Maximum Clock	3.3 ± 0.3		C _L = 15pF	80	150		70		MHz
	Frequency			$C_L = 50pF$	55	130		50		
		5.0 ± 0.5		$C_L = 15pF$	135	185		115		MHz
				$C_L = 50pF$	95	155		85		
tosch, toshc	Output to Output Skew	3.3 ± 0.3	(3)	$C_L = 50pF$			1.5		1.5	ns
		5.0 ± 0.5		C _L = 50pF			1.0		1.0	
C _{IN}	Input Capacitance		V _{CC} = Open			5.0	10		10	pF
C _{OUT}	Output Capacitance		V _{CC} = 5.0V			6.0				pF
C _{PD}	Power Dissipation Capacitance		(4)			87				pF

Notes:

- 3. Parameter guaranteed by design. $t_{OSLH} = |t_{PLH} max t_{PLH} min|$; $t_{OSHL} = |t_{PHL} max t_{PHL} min|$
- 4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (Opr.) = C_{PD} V_{CC} f_{IN} + I_{CC}

AC Operating Requirements

			T _A =	T _A = 25°C		
Symbol	Parameter	V _{CC} (V)	Тур.	Guaranteed Minimum		Units
t _S	Minimum Setup Time (SER-SCK)	3.3 ± 0.3		3.5	3.5	ns
		5.0 ± 0.5		3.0	3.0	
t _S	Minimum Setup Time (SCK–RCK)	3.3 ± 0.3		8.0	8.5	ns
		5.0 ± 0.5		5.0	5.0	
t _S	Minimum Setup Time (SCLR-RCK)	3.3 ± 0.3		8.0	9.0	ns
		5.0 ± 0.5		5.0	5.0	
t _H	Minimum Hold Time (SER-SCK)	3.3 ± 0.3		1.5	1.5	ns
		5.0 ± 0.5		2.0	2.0	
t _H	Minimum Hold Time (SCK-RCK)	3.3 ± 0.3		0.0	0.0	ns
		5.0 ± 0.5		0.0	0.0	
t _H	Minimum Hold Time (SCLR-RCK)	3.3 ± 0.3		0.0	0.0	ns
		5.0 ± 0.5		0.0	0.0	
t _{W(L)}	Minimum Pulse Width (SCLR)	3.3 ± 0.3		5.0	5.0	ns
		5.0 ± 0.5		5.0	5.0	
t _{W(L)} , t _{W(H)}	Minimum Pulse Width (SCK)	3.3 ± 0.3		5.0	5.0	ns
		5.0 ± 0.5		5.0	5.0	
$t_{W(L)}, t_{W}(H)$	Minimum Pulse Width (RCK)	3.3 ± 0.3		5.0	5.0	ns
		5.0 ± 0.5		5.0	5.0	
t _{rem}	Minimum Removal Time (SCLR-SCK)	3.3 ± 0.3		3.0	3.0	ns
		5.0 ± 0.5		2.5	2.5	

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

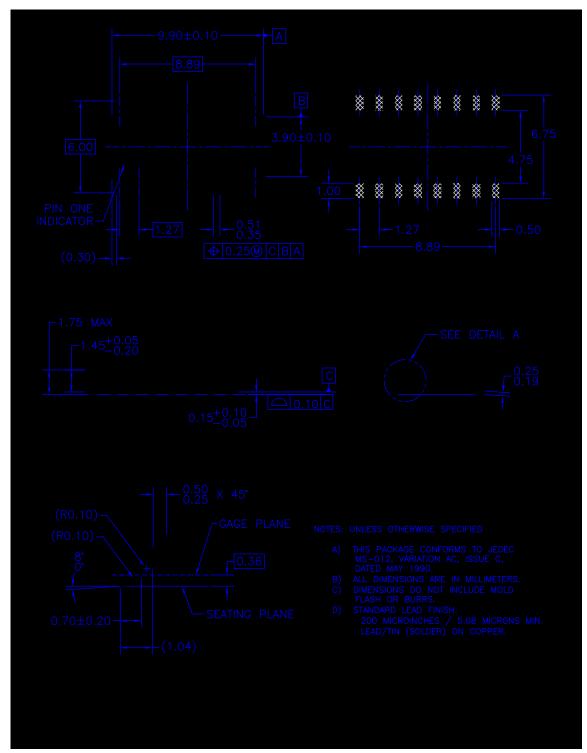


Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Physical Dimensions (Continued) Dimensions are in millimeters unless otherwise noted.

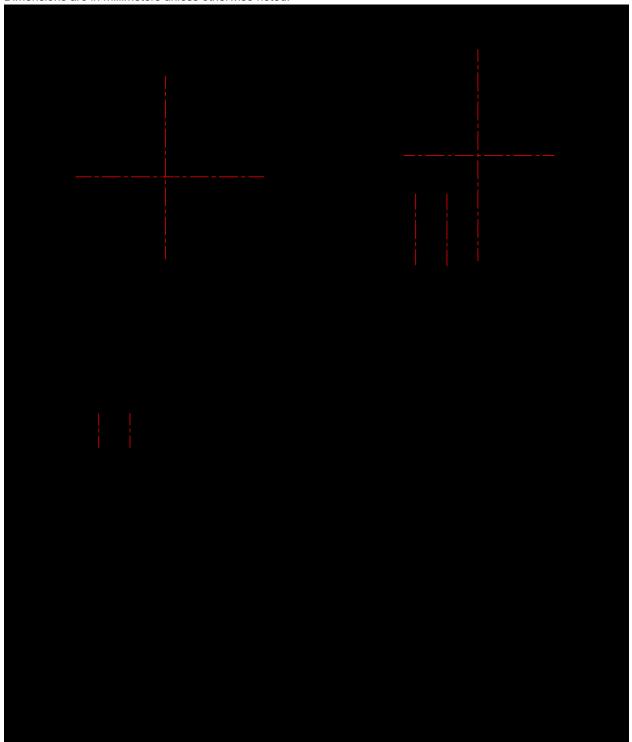


Figure 2. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.

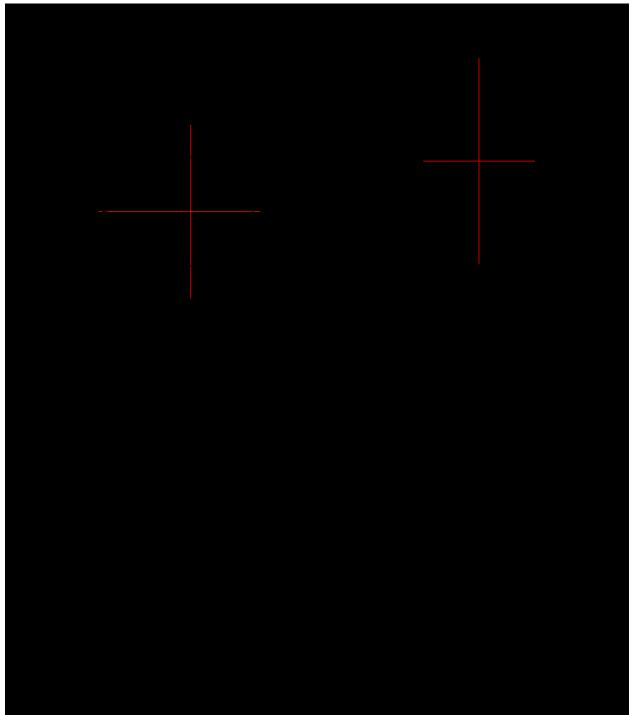
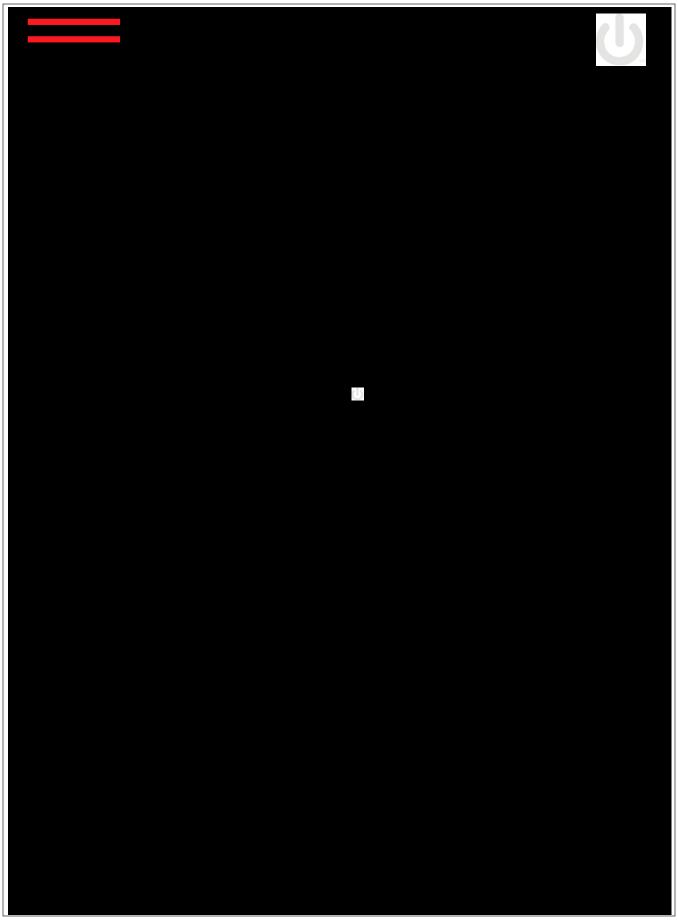


Figure 3. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16



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