

Vishay Siliconix

P-Channel 60 V (D-S) MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	-60			
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.024			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5 \text{ V}$	0.046			
Q _g typ. (nC)	10.1			
I _D (A)	-37.1 ^a			
Configuration	Single			

FEATURES

- New generation p-channel power MOSFET
- Ultra low R_{DS} x Q_g FOM product
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912

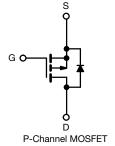


COMPLIANT HALOGEN

FREE

APPLICATIONS

- · Battery and circuit protection
- · Load switch
- Motor drive control



ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiR5623DP-T1-RE3

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-60	V
Gate-source voltage		V_{GS}	± 20	V
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		-37.1	
	T _C = 70 °C	1 . Г	-29.6	
	T _A = 25 °C	l _D	-10.5 ^{b, c}	
	T _A = 70 °C		-8.4 b, c	
Pulsed drain current (t = 100 μs)		I _{DM}	-80	A
Continuous source-drain diode current	T _C = 25 °C		-49.6	
	T _A = 25 °C	I _S	-4.0 ^{b, c}	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	-20	
Single pulse avalanche energy	L = U. I MIH	E _{AS}	20	mJ
Maximum power dissipation	T _C = 25 °C		59.5	
	T _C = 70 °C	1 , [38.0	147
	T _A = 25 °C	P _D	4.8 ^{b, c}	W
	T _A = 70 °C		3.0 b, c	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	-°C
Soldering recommendations (peak temperature) d			260	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^b	t ≤ 10 s	R _{thJA}	21	26	°C/W	
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.7	2.1	7 °C/W	

Notes

- a. $T_C = 25$ °C
- b. Surface mounted on 1" x 1" FR4 board
- t = 10 s
 See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
 Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
 Maximum under steady state conditions is 70 °C/W

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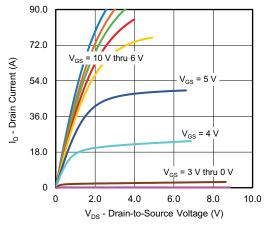
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			•				
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-60	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = -10 mA	-	-26	-	mV/°C	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	4.8	-		
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1.4	-	-2.6	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = +20 \text{ / } -20 \text{ V}$	-	-	100	nA	
Zero gate voltage drain current		V _{DS} = -60 V, V _{GS} = 0 V	-	-	-10	μА	
	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V, T _J = 70 °C	-	-	-50		
Data and a state and a same		$V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}$	-	0.0195	0.024	Ω	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -10 A	-	0.0375	0.046		
Forward transconductance a	9 _{fs}	$V_{DS} = -15 \text{ V}, I_{D} = -10 \text{ A}$	-	23	-	S	
Dynamic ^b			•				
Input capacitance	C _{iss}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	1575	-	pF	
Output capacitance	C _{oss}		-	800	-		
Reverse transfer capacitance	C _{rss}		-	36	-		
Total colorado o co	0	$V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}$ $V_{DS} = -30 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -10 \text{ A}$	-	21.8	33	nC	
Total gate charge	Q_g		-	10.1	15.5		
Gate-source charge	Q _{gs}		-	6.4	-		
Gate-drain charge	Q _{gd}		-	2.7	-		
Gate resistance	R_{g}	f = 1 MHz	0.4	1.0	1.7	Ω	
Turn-on delay time	t _{d(on)}		-	12	24	-	
Rise time	t _r	$\begin{aligned} V_{DD} = -30 \text{ V}, \text{ R}_L = 3 \Omega, \text{ I}_D &\cong -10 \text{ A}, \\ V_{GEN} = -10 \text{ V}, \text{ R}_g = 1 \Omega \end{aligned}$	-	5	10		
Turn-off delay time	t _{d(off)}		-	21	42		
Fall time	t _f		-	5	10	1	
Turn-on delay time	t _{d(on)}		-	24	48	ns -	
Rise time	t _r	$V_{DD} = -30 \text{ V}, R_1 = 3 \Omega, I_D \cong -10 \text{ A},$	-	181	360		
Turn-off delay time	t _{d(off)}	$V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	-	14	28		
Fall time	t _f		-	9	18		
Drain-Source Body Diode Characteristi	cs		•			•	
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	-49.6	A	
Pulse diode forward current	I _{SM}		-	-	-80		
Body diode voltage	V_{SD}	$I_{S} = -5 \text{ A}, V_{GS} = 0 \text{ V}$	-	-0.81	-1.2	V	
Body diode reverse recovery time	t _{rr}		-	42	84	ns	
Body diode reverse recovery charge	Q _{rr}	$I_F = -10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	37	74	nC	
Reverse recovery fall time	t _a	$T_J = 25 ^{\circ}C$	-	15	-		
Reverse recovery rise time	t _b		-	27	-	ns	

Notes

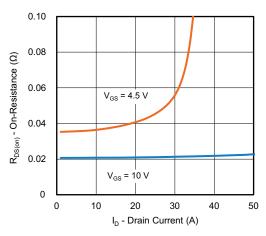
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

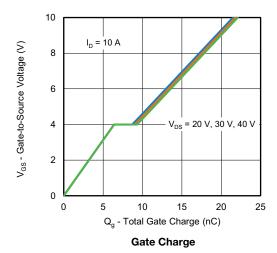


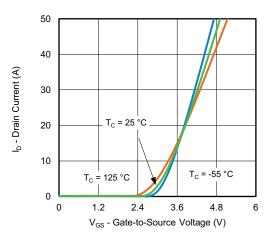


Output Characteristics

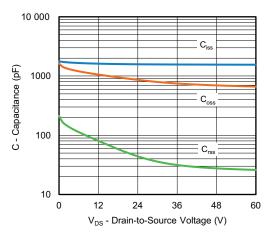


On-Resistance vs. Drain Current and Gate Voltage

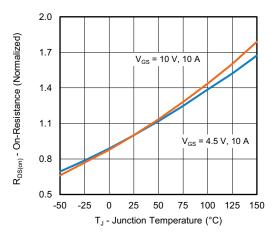




Transfer Characteristics

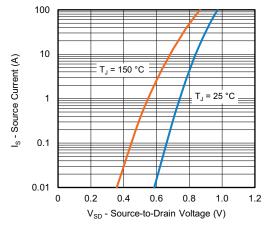


Capacitance

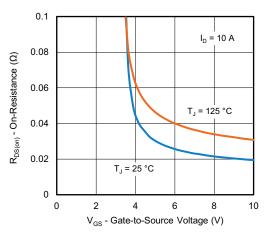


On-Resistance vs. Junction Temperature

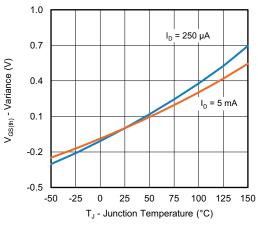




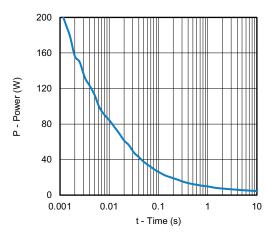
Source-Drain Diode Forward Voltage



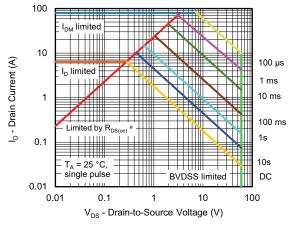
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



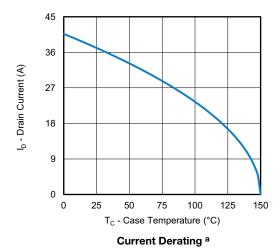
Safe Operating Area, Junction-to-Ambient

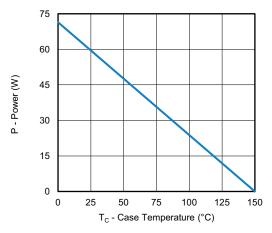
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

S23-0036-Rev. A, 30-Jan-2023





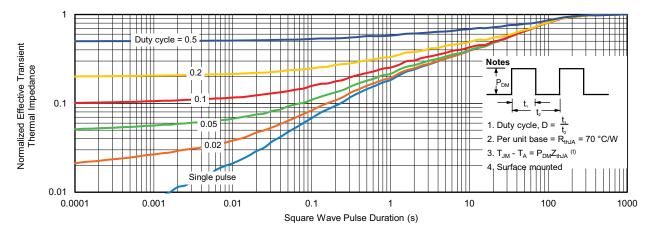


Power, Junction-to-Case

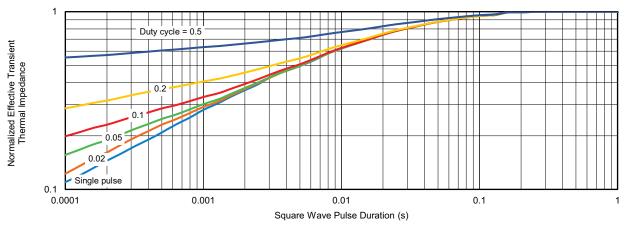
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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