

# TLV8544 500-nA, RRIO, Nanopower Operational Amplifiers for Cost-Optimized Systems

## 1 Features

- For Cost-Optimized Systems
- Nanopower Supply Current: 500 nA per Channel
- Offset Voltage: 3.1 mV (maximum)
- $T_C V_{OS}$ : 0.8  $\mu\text{V}/^\circ\text{C}$
- Gain Bandwidth: 8 kHz
- Unity-Gain Stable
- Low Input-Bias Current: 100 fA
- Wide Supply Range: 1.7 V to 3.6 V
- Rail-to-Rail Input and Output (RRIO)
- Temperature Range  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Industry Standard Package
  - Quad in 14-pin TSSOP

## 2 Applications

- Motion Detectors Using PIR Sensors [SNA301](#)
- Motion Detectors Using Microwave Sensors
- Gas Detectors
- Ionization Smoke Alarms
- Thermostats
- Remote Sensors, IoT (Internet of Things)
- Active RFID Readers and Tags
- Portable Medical Equipment
- Glucose Monitoring

## 3 Description

The TLV8544 ultra-low-power operational amplifier (op amps) is intended for cost-optimized sensing applications in wireless and low-power wired equipment. The TLV8544 op amp minimizes power consumption in equipment such as motion detecting security systems (like microwave and PIR motion sensing) where operational battery life is critical. It also has a carefully designed CMOS input stage, enabling very low, femto-ampere bias currents, thereby reducing  $I_{BIAS}$  and  $I_{OS}$  errors that would otherwise impact sensitive applications. Examples of these include transimpedance amplifier (TIA) configurations with megaohm feedback resistors, and high source impedance sensing applications. Additionally, built-in EMI protection reduces sensitivity to unwanted RF signals from sources such as mobile phones, WiFi, radio transmitters and tab readers.

The TLV8544 op amp operates with a single supply voltage down to 1.7 V supply, providing continuous performance in low battery situations over the extended temperature range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . The 4-channel TLV8544 is available in the industry standard 14-pin TSSOP package.

### Device Information<sup>(1)</sup>

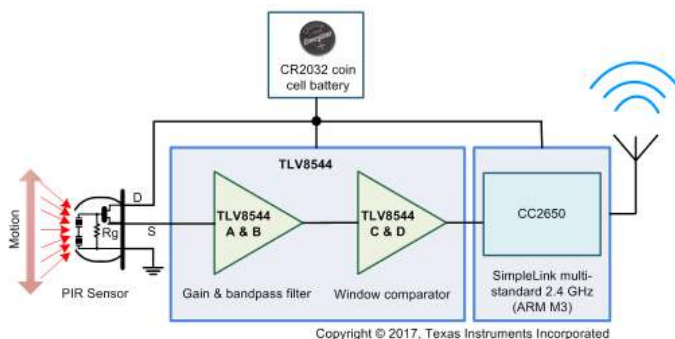
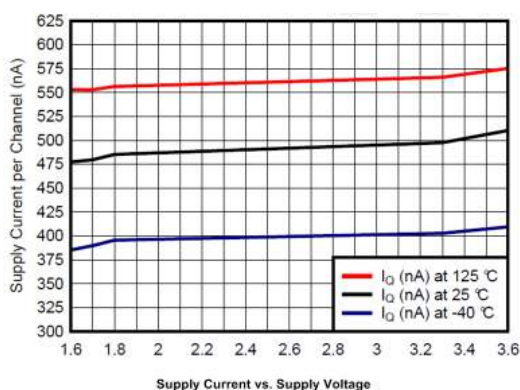
PART NUMBER	PACKAGE	BODY SIZE
TLV8544	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Nanopower Amplifiers Family

FAMILY	CHANNEL COUNT	$I_O$ PER CHANNEL	$V_{OS}$ (maximum)	$V_{SUPPLY}$
TLV8544	4	500 nA	3.1 mV	1.7 to 3.6 V
TLV880x	1, 2	320 nA	4.5 mV	1.7 to 5.5 V
LPV81x	1, 2	425 nA	0.3 mV	1.6 to 5.5 V

### Low Power PIR Motion Detector



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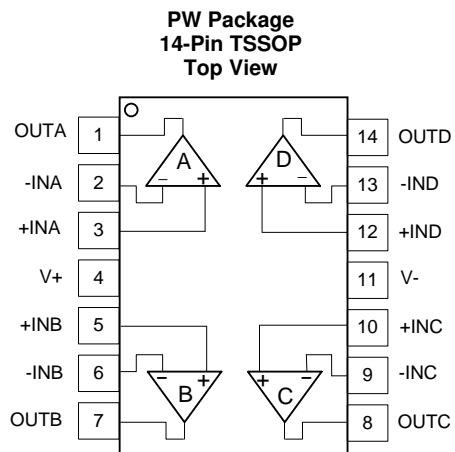
## Table of Contents

<b>1</b>	<b>Features</b> .....	<b>1</b>	<b>8</b>	<b>Application and Implementation</b> .....	<b>13</b>
<b>2</b>	<b>Applications</b> .....	<b>1</b>	8.1	Application Information.....	13
<b>3</b>	<b>Description</b> .....	<b>1</b>	8.2	Dos and Don'ts .....	19
<b>4</b>	<b>Revision History</b> .....	<b>2</b>	<b>9</b>	<b>Power Supply Recommendations</b> .....	<b>19</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	<b>10</b>	<b>Layout</b> .....	<b>20</b>
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	10.1	Layout Guidelines .....	20
6.1	Absolute Maximum Ratings .....	4	10.2	Layout Example .....	20
6.2	ESD Ratings.....	4	<b>11</b>	<b>Device and Documentation Support</b> .....	<b>21</b>
6.3	Recommended Operating Conditions .....	4	11.1	Device Support .....	21
6.4	Thermal Information .....	4	11.2	Documentation Support .....	21
6.5	Electrical Characteristics.....	5	11.3	Receiving Notification of Documentation Updates	21
6.6	Typical Characteristics.....	6	11.4	Community Resources.....	21
<b>7</b>	<b>Detailed Description</b> .....	<b>11</b>	11.5	Trademarks .....	21
7.1	Overview .....	11	11.6	Electrostatic Discharge Caution.....	21
7.2	Functional Block Diagram .....	11	11.7	Glossary .....	21
7.3	Feature Description.....	11	<b>12</b>	<b>Mechanical, Packaging, and Orderable Information</b> .....	<b>22</b>
7.4	Device Functional Modes.....	11			

## 4 Revision History

Changes from Original (December 2016) to Revision A	Page
• Changed Product Preview to Production Data release. ....	1

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUTA	O	Channel A output
2	-INA	I	Channel A inverting input
3	+INA	I	Channel A non-inverting input
4	V+	P	Positive (highest) power supply
5	+INB	I	Channel B non-inverting input
6	-INB	I	Channel B inverting input
7	OUTB	O	Channel B output
8	OUTC	O	Channel C output
9	-INC	I	Channel C inverting input
10	+INC	I	Channel C non-inverting input
11	V-	P	Negative (lowest) power supply
12	+IND	I	Channel D non-inverting input
13	-IND	I	Channel D inverting input
14	OUTD	O	Channel D output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>

		MIN	MAX	UNIT
Supply voltage, $V_s = (V+) - (V-)$		-0.3	4	V
Input pins	Voltage	Common mode		V
		(V-) - 0.3	(V+) + 0.3	
		Differential		V
		(V-) - 0.3	(V+) + 0.3	V
Input pins	Current	-10	10	mA
Output short current <sup>(4)</sup>		Continuous	Continuous	
Operating ambient temperature		-40	125	°C
Storage temperature, $T_{stg}$		-65	150	°C
Junction temperature			150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
- (3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) Short-circuit to ground.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	
		±1000	
		±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage ( $V+ - V-$ )	1.7		3.6	V
Specified ambient temperature	-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLV8544	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.2	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	7.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	65.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ ,  $V_S = 1.8\text{ V to }3.3\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L \geq 10\text{ M}\Omega$  to  $V_S / 2$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$V_{CM} = V^-$ , $V_S = 1.8\text{ V and }3.3\text{ V}$	-3.1	See Plots	3.1	mV
		$V_{CM} = V^+$ , $V_S = 1.8\text{ V and }3.3\text{ V}$	-3.4	See Plots	3.4	
$dV_{OS}/dT$	Input offset drift	$V_{CM} = V^-$ , $T_A = -40^\circ\text{C to }125^\circ\text{C}$		0.8		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_{CM} = V^-$ , $V_S = 1.8\text{ V and }3.3\text{ V}$	66	90		dB
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range	$V_S = 3.3\text{ V}$	0		3.3	V
CMRR	Common-mode rejection ratio	$(V^-) \leq V_{CM} \leq (V^+)$ , $V_S = 3.3\text{ V}$	60	80		dB
		$(V^-) \leq V_{CM} \leq (V^+) - 1.2\text{ V}$		90		
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current			100		fA
$I_{OS}$	Input offset current			100		fA
<b>INPUT IMPEDANCE</b>						
	Differential			2		pF
	Common mode			4		pF
<b>NOISE</b>						
$E_n$	Input voltage noise	$f = 0.1\text{ Hz to }10\text{ Hz}$		8.6		$\mu\text{Vp-p}$
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$		264		$\text{nV}/\sqrt{\text{Hz}}$
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$(V^-) + 0.3\text{ V} \leq V_O \leq (V^+) - 0.3\text{ V}$ , $R_L = 100\text{ k}\Omega$ to $V^+/2$		120		dB
<b>OUTPUT</b>						
$V_{OH}$	Voltage output swing from positive rail	$R_L = 100\text{ k}\Omega$ to $V^+/2$ , $V_S = 3.3\text{ V}$	12			mV
$V_{OL}$	Voltage output swing from negative rail	$R_L = 100\text{ k}\Omega$ to $V^+/2$ , $V_S = 3.3\text{ V}$			12	mV
$I_{SC}$	Short-circuit current	Sourcing, $V_O$ to $V^-$ , $V_{IN(\text{diff})} = 100\text{ mV}$ , $V_S = 3.3\text{ V}$		15		mA
		Sinking, $V_O$ to $V^+$ , $V_{IN(\text{diff})} = -100\text{ mV}$ , $V_S = 3.3\text{ V}$		30		
$Z_O$	Open loop output impedance	$f = 1\text{ kHz}$ , $I_O = 0\text{ mA}$		8		k $\Omega$
<b>FREQUENCY RESPONSE</b>						
GBP	Gain-bandwidth product	$C_L = 20\text{ pF}$ , $R_L = 10\text{ M}\Omega$		8		kHz
SR	Slew rate (10% to 90%)	$G = 1$ , rising edge, $C_L = 20\text{ pF}$		3.5		V/ms
		$G = 1$ , falling edge, $C_L = 20\text{ pF}$		4.5		
<b>POWER SUPPLY</b>						
$I_{Q-TLV8544}$	Quiescent current, per channel	$V_{CM} = V^-$ , $I_O = 0\text{ mA}$ , $V_S = 3.3\text{ V}$		500	640	nA

## 6.6 Typical Characteristics

$T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{ pF}$ ,  $V_{CM} = V_S / 2\text{ V}$  unless otherwise specified.

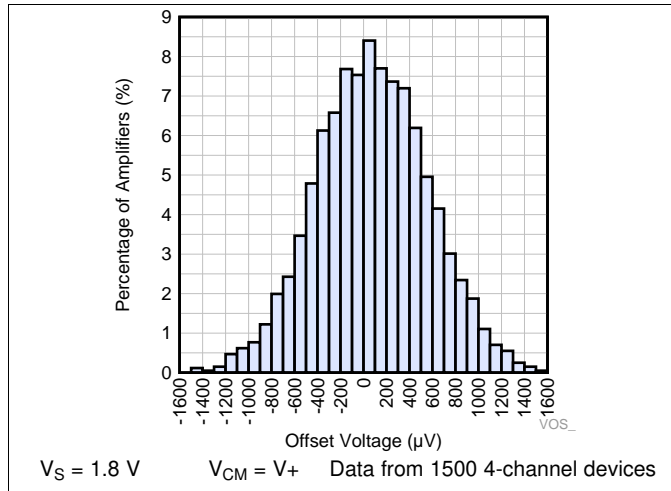


Figure 1. Offset Voltage Production Distribution

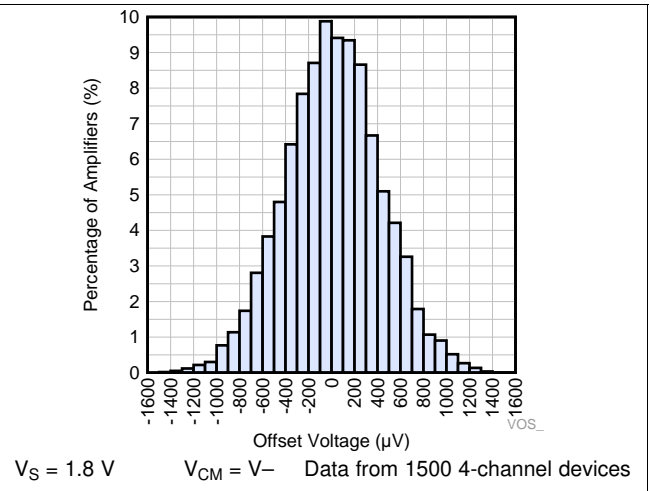


Figure 2. Offset Voltage Production Distribution

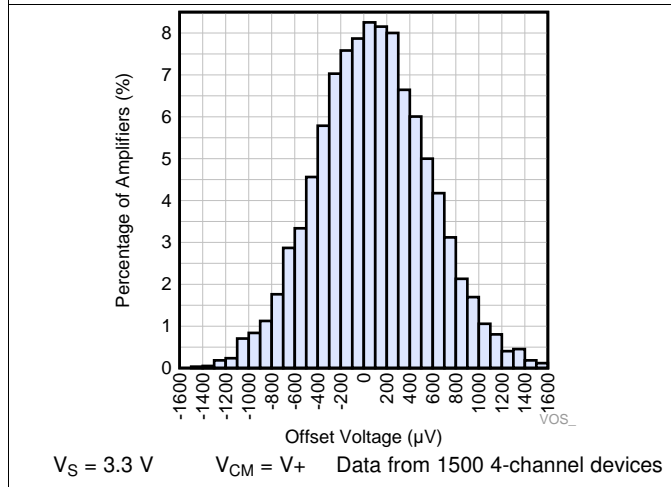


Figure 3. Offset Voltage Production Distribution

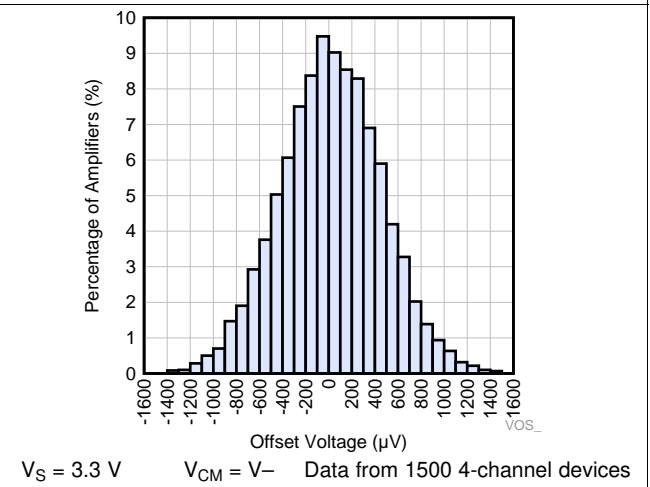


Figure 4. Offset Voltage Production Distribution

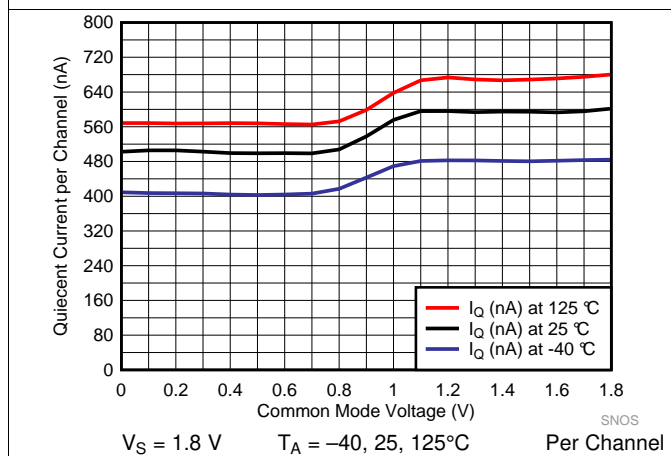


Figure 5. Supply Current vs Common Mode Voltage

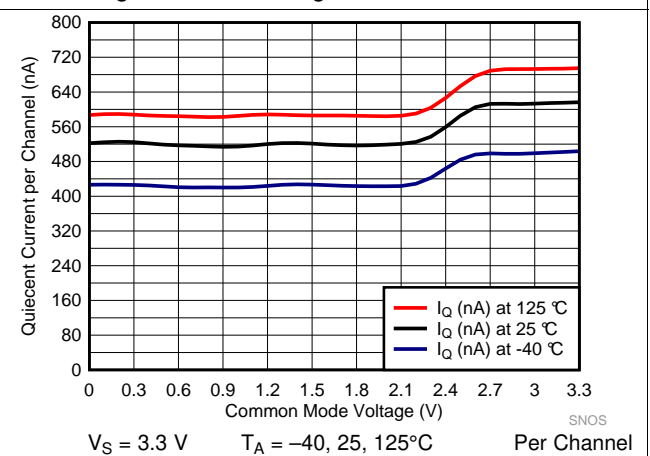


Figure 6. Supply Current vs Common Mode Voltage

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{ pF}$ ,  $V_{CM} = V_S / 2\text{ V}$  unless otherwise specified.

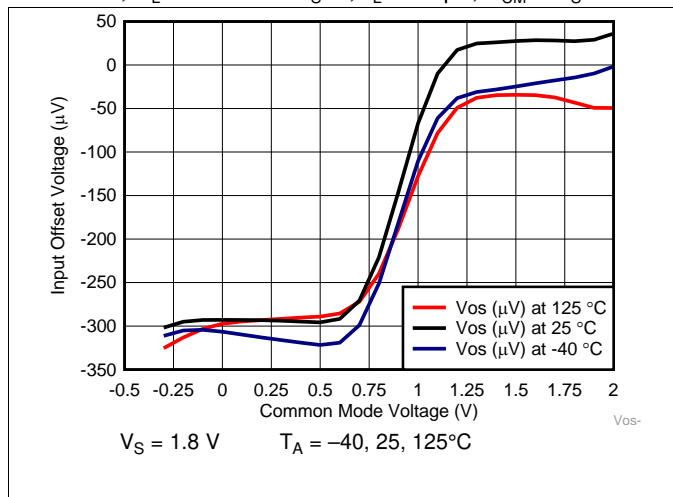


Figure 7. Typical Offset Voltage vs Common Mode Voltage

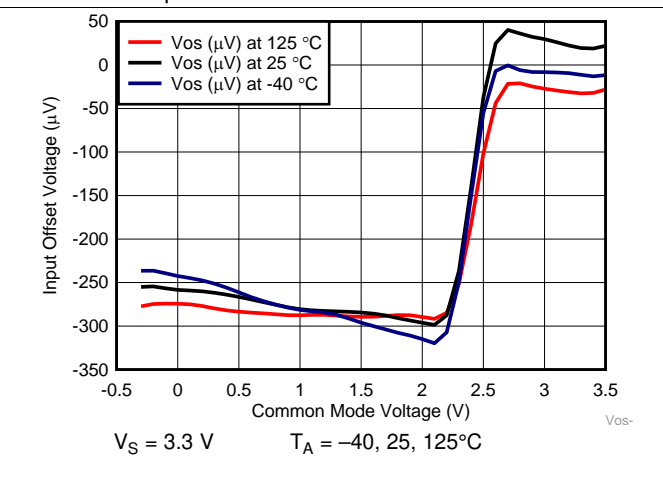


Figure 8. Typical Offset Voltage vs Common Mode Voltage

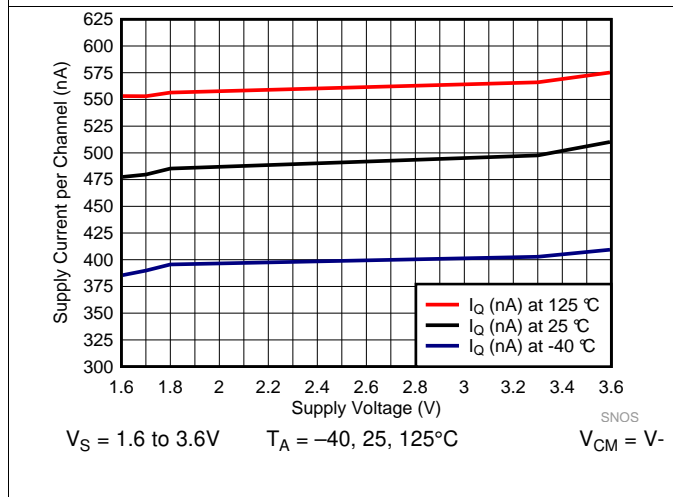


Figure 9. Supply Current vs Supply Voltage, Low VCM

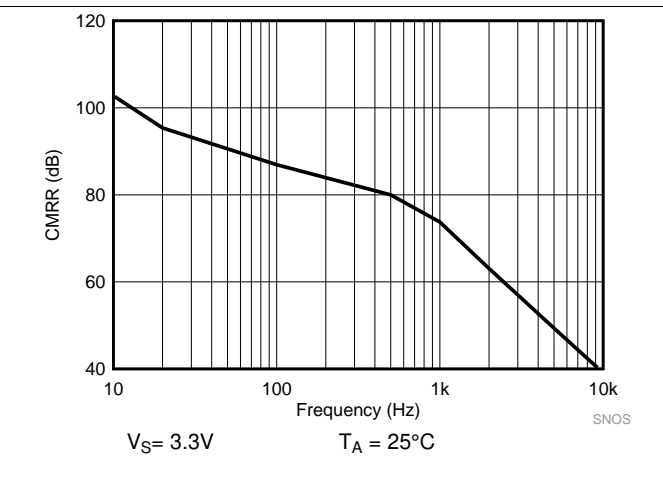


Figure 10. CMRR vs Frequency

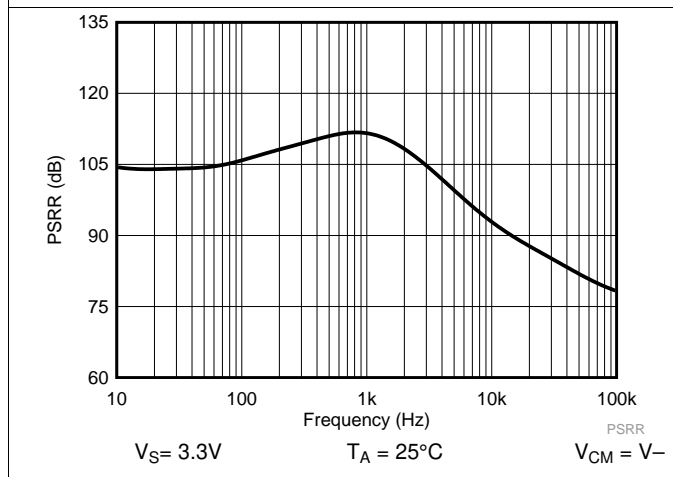


Figure 11. PSRR vs Frequency

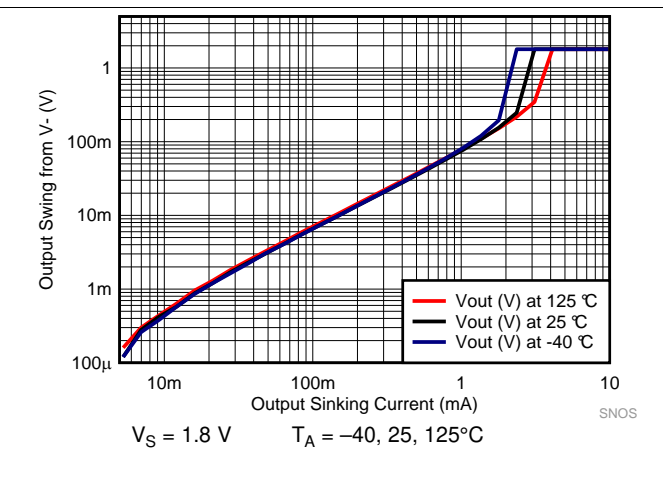


Figure 12. Output Swing vs Sinking Current

Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{ pF}$ ,  $V_{CM} = V_S / 2\text{ V}$  unless otherwise specified.

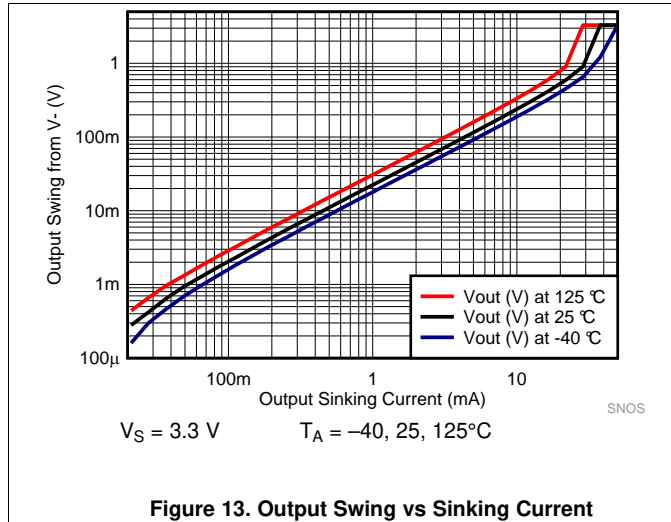


Figure 13. Output Swing vs Sinking Current

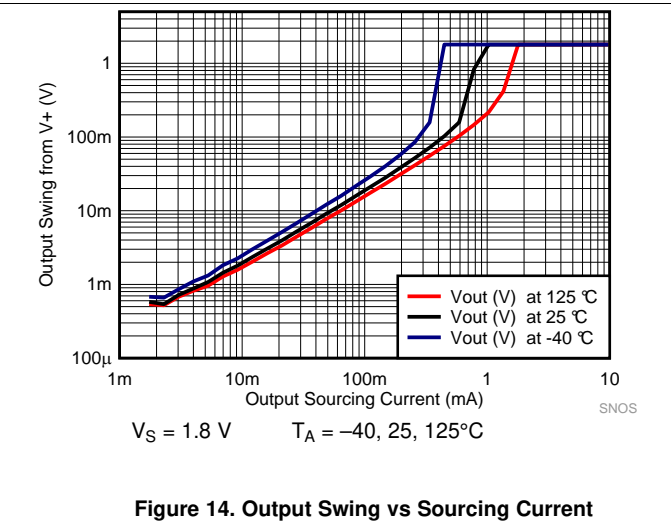


Figure 14. Output Swing vs Sourcing Current

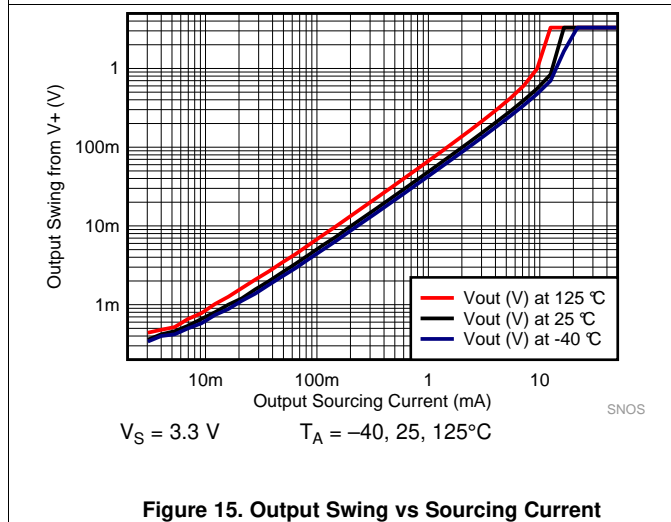


Figure 15. Output Swing vs Sourcing Current

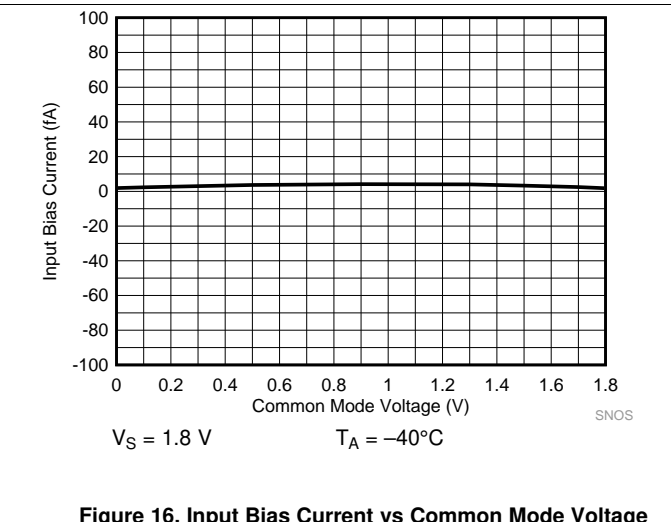


Figure 16. Input Bias Current vs Common Mode Voltage

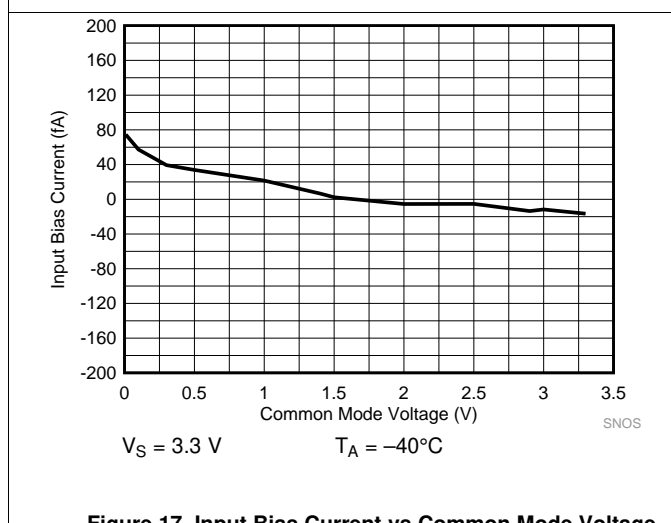


Figure 17. Input Bias Current vs Common Mode Voltage

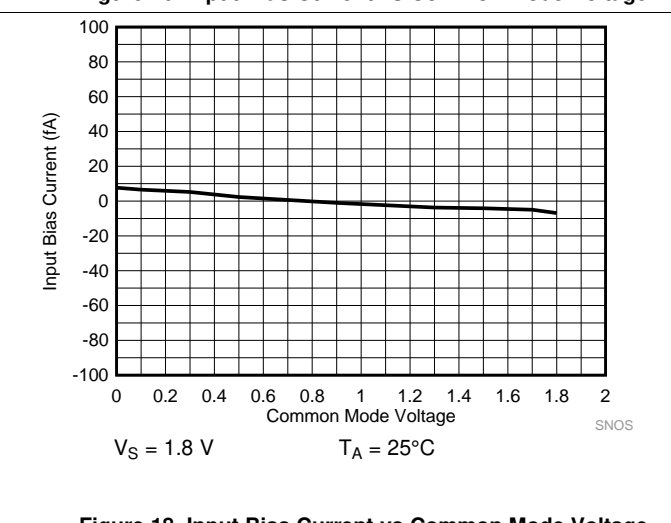
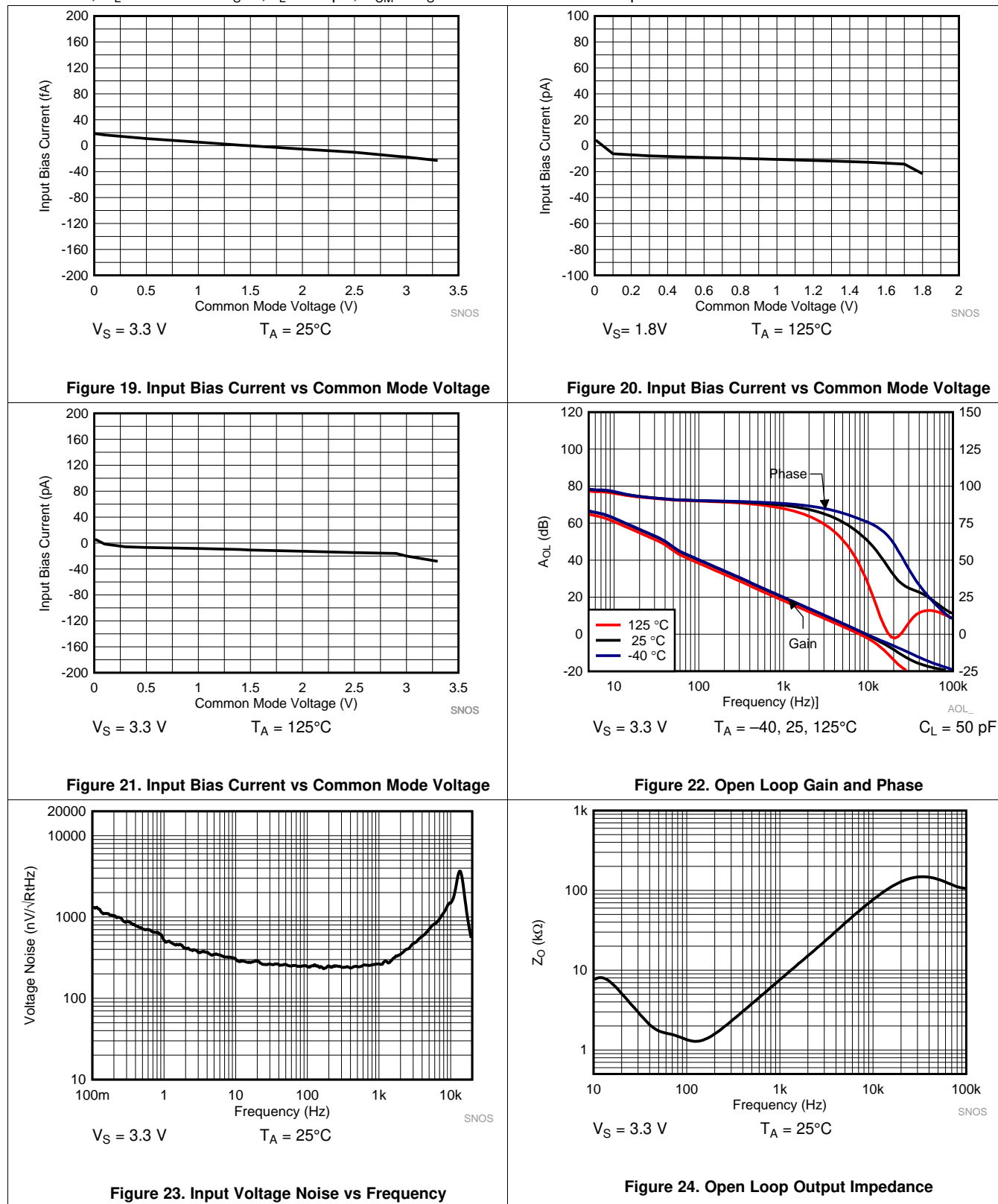


Figure 18. Input Bias Current vs Common Mode Voltage



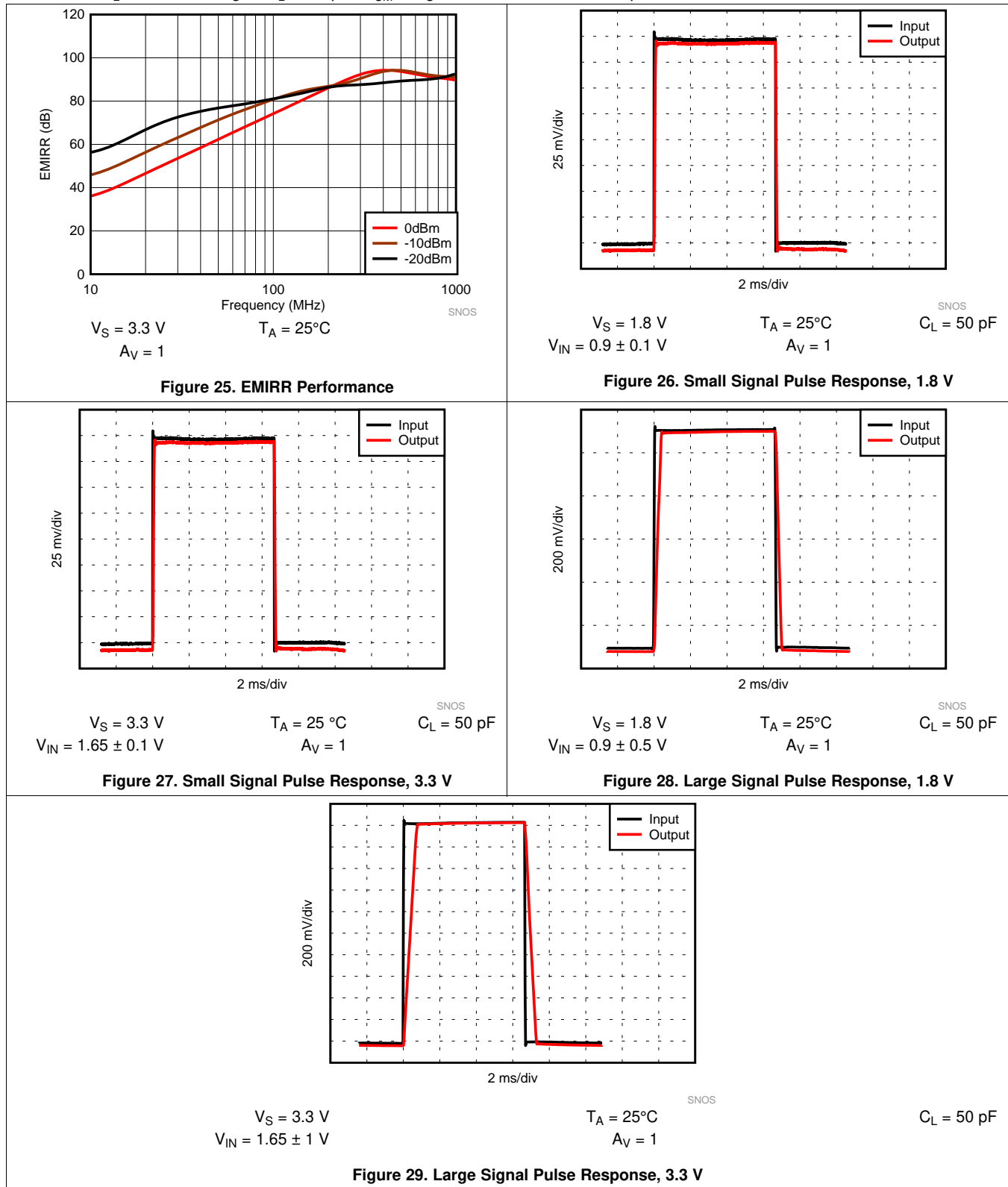
Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{ pF}$ ,  $V_{CM} = V_S / 2\text{ V}$  unless otherwise specified.



Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ M}\Omega$  to  $V_S/2$ ,  $C_L = 20\text{ pF}$ ,  $V_{CM} = V_S / 2\text{ V}$  unless otherwise specified.



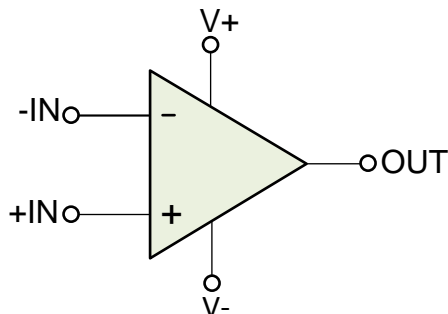
## 7 Detailed Description

### 7.1 Overview

The TLV8544 amplifier is unity-gain stable and can operate on a single supply, making it highly versatile and easy to use.

Parameters that vary significantly with operating voltages or temperature are shown in the [Typical Characteristics](#) curves.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The differential inputs of the amplifier consist of a non-inverting input (+IN) and an inverting input (–IN). The device amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp  $V_{OUT}$  is given by [Equation 1](#):

$$V_{OUT} = A_{OL} [(+IN) - (-IN)]$$

where

- $A_{OL}$  is the open-loop gain of the amplifier, typically around 100 dB. (1)

### 7.4 Device Functional Modes

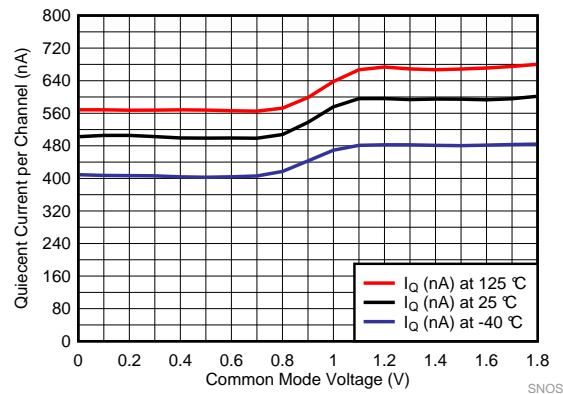
#### 7.4.1 Rail-To-Rail Input

The input common-mode voltage range of the TLV8544 extends to the supply rails. This is achieved with a complementary input stage — an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 800\text{ mV}$  to  $200\text{ mV}$  above the positive supply, while the P-channel pair is on for inputs from  $300\text{ mV}$  below the negative supply to approximately  $(V+) - 800\text{ mV}$ . There is a small transition region, typically  $(V+) - 1.2\text{ V}$  to  $(V+) - 0.8\text{ V}$ , in which both pairs are on. This 400-mV transition region can vary 200 mV with process variation. Within the 400-mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

#### 7.4.2 Supply Current Changes Over Common Mode

Because of the ultra-low supply current, changes in common mode voltages cause a noticeable change in the supply current as the input stages transition through the transition region, as shown in [Figure 30](#).

## Device Functional Modes (continued)



**Figure 30. Supply Current Change Over Common Mode at 1.8 V**

For the lowest supply current operation, keep the input common mode range between  $V_-$  and 1 V below  $V_+$ .

### 7.4.3 Design Optimization With Rail-To-Rail Input

In most applications, operation is within the range of only one differential pair. However, some applications can subject the amplifier to a common-mode signal in the transition region. Under this condition, the inherent mismatch between the two differential pairs may lead to degradation of the CMRR and THD. The unity-gain buffer configuration is the most problematic as it traverses through the transition region if a sufficiently wide input swing is required.

### 7.4.4 Design Optimization for Nanopower Operation

When designing for ultra-low power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors react with stray capacitance in the circuit and the input capacitance of the operational amplifier (op amp). These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

When possible, use AC coupling and AC feedback to reduce static current draw through the feedback elements. Use film or ceramic capacitors because large electrolytics may have static leakage currents in the tens to hundreds of nanoamps.

### 7.4.5 Common-Mode Rejection

The CMRR for the TLV8544 is specified in two ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region ( $V_{CM} < (V_+) - 1.2$  V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at  $V_S = 3.3$  V over the entire common-mode range is specified.

### 7.4.6 Output Stage

The TLV8544 output voltage swings 20 mV from rails at a 3.3-V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

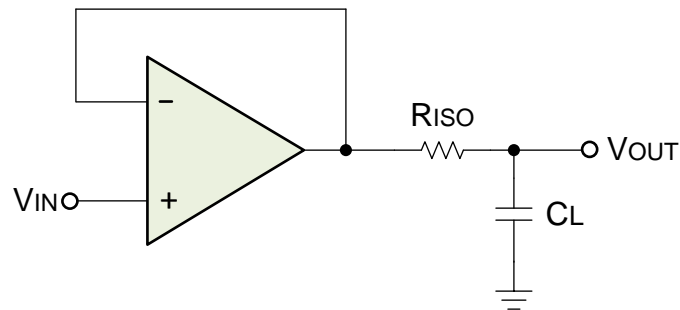
The TLV8544 maximum output voltage swing defines the maximum swing possible under a particular output load.

## Device Functional Modes (continued)

### 7.4.7 Driving Capacitive Load

The TLV8544 is internally compensated for stable unity-gain operation, with a 8-kHz typical gain bandwidth. However, the unity-gain follower is the most sensitive configuration-to-capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response is under-damped, which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy ( $> 50$  pF) capacitive loads, use an isolation resistor,  $R_{ISO}$ , as shown in Figure 31. By using this isolation resistor, the capacitive load is isolated from the output of the amplifier. The larger the value of  $R_{ISO}$ , the more stable the amplifier will be. If the value of  $R_{ISO}$  is sufficiently large, the feedback loop is stable, independent of the value of  $C_L$ . However, larger values of  $R_{ISO}$  (e.g. 50 k $\Omega$ ) result in reduced output swing and reduced output current drive.



**Figure 31. Resistive Isolation of Capacitive Load**

## 8 Application and Implementation

### NOTE

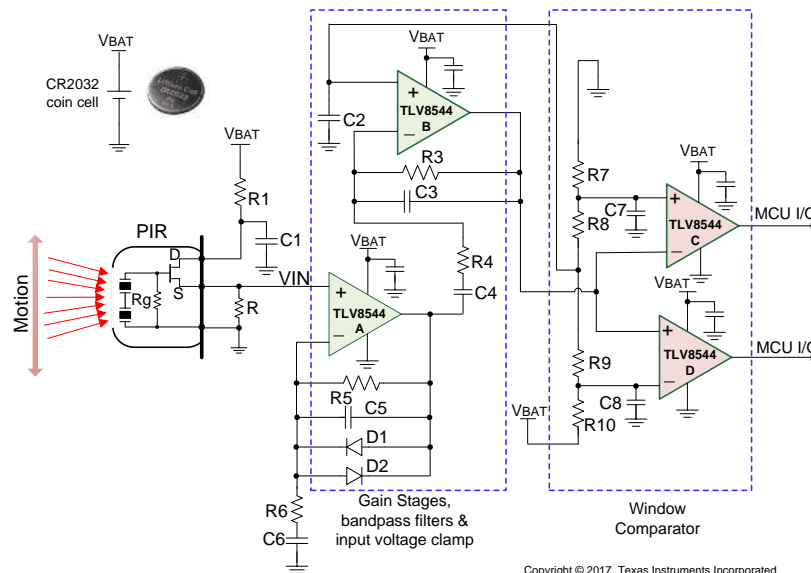
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TLV8544 is a nanopower op amp that provides 8-kHz bandwidth with only 500-nA typical quiescent current per channel and near precision drift specifications at a low cost. These rail-to-rail input and output amplifier are specifically designed for battery-powered applications. The input common-mode voltage range extends to the power-supply rails and the output swings to within millivolts of the rails, maintaining a wide dynamic range.

## Application Information (continued)

### 8.1.1 Typical Application: Battery-Powered Wireless PIR Motion Detectors



**Figure 32. PIR Motion Detector Circuit**

#### 8.1.1.1 Design Requirements

Smart building automation systems employ a large number of various sensing nodes distributed throughout small, medium, and large infrastructures. The sensing nodes measure motion, temperature, vibration, and other parameters of interest. Wireless nodes are monitored in a central location. Because of the large number of distributed nodes, battery-operation and cost-optimized electronic components are required. Typically, the wireless nodes need to run on a single CR2032 coin battery for eight to ten years.

For more information see [Design of Ultra-Low Power Discrete Signal Conditioning Circuit for Battery-Power, Ultra-Low-Power Wireless PIR Motion Detector Reference Design](#) and [BOOSTXL-TLV8544PIR User's Guide](#). The BOOSTXL-TLV8544PIR along with the companion CC2650 LaunchPad, [LAUNCHXL-CC2650](#) can be obtained from the TI website for hands-on experiments.

#### 8.1.1.2 Detailed Design Procedure

Referring to [Figure 32](#), the TLV8544 4-channel op amp is powered directly by a 3.3-V CR2032 coin battery. The first two amplifier stages of the TLV8544 implement active filter functionality. The remaining two amplifiers of the TLV8544 are used for building a window comparator. The comparator flags the detection of a motion event to an ultra-low-power wireless microcontroller on the same board. Due to the higher gain in the filter stages and higher output noise from the sensor, it is necessary to optimize the placement of the high-frequency filter pole and the window comparator thresholds to avoid false detection.

The first two amplifiers (A and B) in the circuit are used in identical active bandpass filters with corner frequencies of 0.7 and 10.6 Hz. Each filter stage has a gain of about 220 V/V to account for the reduced sensitivity of the sensor due to the low current biasing of the PIR sensor. Considering the 8-kHz unity gain bandwidth (UGBW) product of the TLV8544, the bandwidth of each stage is limited to approximately 36 Hz. The above choice of cutoff frequencies give a relatively wide bandwidth to detect a person running in the field of view, yet narrow enough to limit the peak-to-peak noise at the output of the filters.

Amplifier A is a noninverting gain/filter stage providing the high input impedance needed to prevent loading of the sensor. The DC gain of the stage due to the presence of C6 is unity. Therefore, the sensor output provides the bias voltage needed at the A stage to avoid clipping of the lower cycle of the input signal. Diodes D1 and D2 limit the output signal, avoiding overdriving of the second stage and consequently placing a large charge on coupling capacitor C4, which helps with the recovery time.

## Application Information (continued)

### 8.1.1.2.1 Calculation of the Cutoff Frequencies and Gain of Stage A:

The low cutoff frequency of the bandpass filter in stage A is:

$$f_{\text{Clow}} = \frac{1}{2\pi \times R_6 \times C_6} \quad (2)$$

Choosing  $R_6 = 6.81 \text{ k}\Omega$  and  $C_6 = 33 \text{ }\mu\text{F}$ , the low cutoff frequency is  $f_{\text{Clow}} = 0.71 \text{ Hz}$ . The high cutoff frequency of the filter is:

$$f_{\text{Chigh}} = \frac{1}{2\pi \times R_5 \times C_5} \quad (3)$$

For  $R_5 = 1.5 \text{ M}\Omega$  and  $C_5 = 0.01 \text{ }\mu\text{F}$ , the high cutoff frequency is  $f_{\text{Chigh}} = 10.6 \text{ Hz}$ . The gain of the stage is:

$$G = 1 + \frac{R_5}{R_6} \quad (4)$$

Choosing  $R_5 = 1.5 \text{ M}\Omega$  and  $R_6 = 6.81 \text{ k}\Omega$ , the gain of the stage A is  $G = 221.26 \text{ V/V}$  (46.9 dB).

### 8.1.1.2.2 Calculation of the Cutoff Frequencies and Gain of Stage B

As shown in [Figure 32](#), amplifier B is an inverting bandpass filter and gain stage. Capacitor C4 creates an AC coupled path between the A and the B stages. Thus the signal level must be shifted at the input of the amplifier B. This is done by connecting a midpoint voltage of the reference voltage dividers comprising R10, R9, R8 and R7 to the non-inverting input of amplifier B, biasing the input signal to the mid-rail (1.65 V). A very large feedback resistor R3 is chosen to minimize the dynamic current due to presence of peak-to-peak noise voltage at the output of this stage.

The low cutoff frequency of the filter of the stage B is:

$$f_{\text{Clow}} = \frac{1}{2\pi \times R_4 \times C_4} \quad (5)$$

Choosing  $R_4 = 68.1 \text{ k}\Omega$  and  $C_4 = 3.3 \text{ }\mu\text{F}$ , the low cutoff frequency is  $f_{\text{Clow}} = 0.71 \text{ Hz}$ . The high cutoff frequency of the filter is:

$$f_{\text{Chigh}} = \frac{1}{2\pi \times R_3 \times C_3} \quad (6)$$

For  $R_3 = 15 \text{ M}\Omega$  and  $C_3 = 1000 \text{ pF}$ , the high cutoff frequency is  $f_{\text{Chigh}} = 10.6 \text{ Hz}$ . The gain of the stage is:

$$G = -\frac{R_3}{R_4} \quad (7)$$

For  $R_3 = 15 \text{ M}\Omega$  and  $R_4 = 68.1 \text{ k}\Omega$ , the gain is calculated  $|G| = 220.26 \text{ V/V}$  (46.9 dB).

### 8.1.1.2.3 Calculation of the Total Gain of Stages A and B

The overall gain of the two stages A and B is:  $G_{\text{Total}} = G_A \times G_B = 221.26 \times 220.26 = 48810 \text{ V/V} = 93.77 \text{ dB}$ .

### 8.1.1.2.4 Window Comparator Stage

The signal from a moving object in front of the PIR sensor, after amplification and filtering, is connected to a window comparator. The comparator converts the analog signal to digital pulses for interrupting an on-board microcontroller unit (MCU), flagging detection of motion. A different approach is to digitize the analog signal continuously by an analog-to-digital converter (ADC) and implement the comparator functionality in the digital domain. This method has the advantage of enabling the post processing of the data to reduce the chance of false detection. However, continuous conversion and processing of data by the MCU increases the power consumption, lowering the lifetime of the battery substantially.

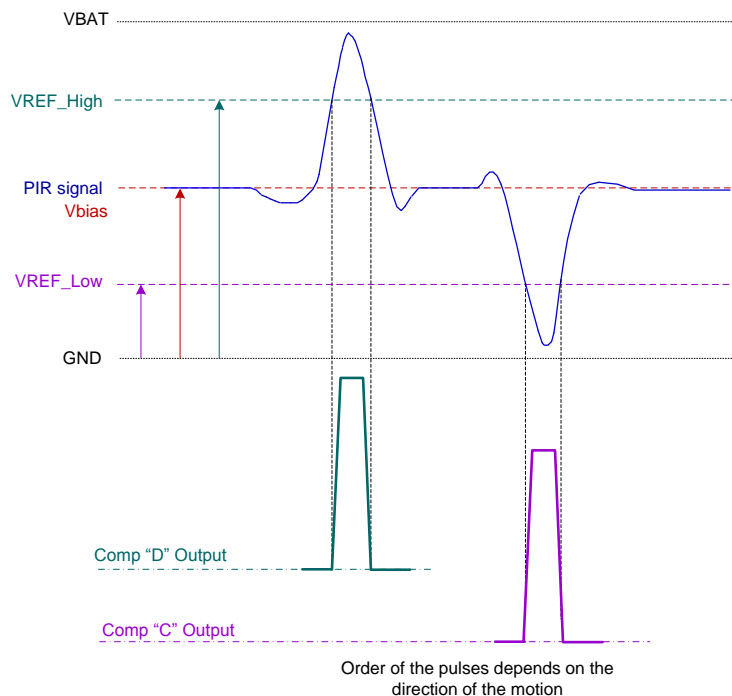
Rather than using a separate low-power comparator integrated circuits to implement the window comparator section of the circuit, the remaining op amps in the TLV8544 package are used to implement the comparator stage. Benefits of this approach include fewer components and thus reduced system cost.

## Application Information (continued)

Although an op amp can sometimes be used as a comparator, an amplifier cannot be used as a comparator interchangeably in all applications because of relatively long recovery time of the amplifier from output saturation and relatively long propagation delay due to internal compensation. Particularly, the nanopower op amps have very slow slew rate, limiting their usage as a comparator in only applications with very low frequency input signal. Fortunately, PIR sensor signals are relatively slow and this should not be an issue.

The new TLV8544 device is particularly suitable for implementing a window comparator in a battery operated PIR motion detector application because of its rail-to-rail operation capability, relatively low offset voltage, low offset voltage drift, very low bias current, and nanopower consumption, all at an optimal cost. The input signal of the comparator stage in the presence of moving heat source across the sensor is shown in [Figure 33](#). The signal is centered at mid-rail and can swing up or down from the center.

The window comparator is a combination of a non-inverting comparator implemented with amplifier *D* and an inverting comparator implemented with amplifier *C*, as shown in [Figure 32](#).



**Figure 33. Ideal Amplified PIR Signal and the Output of the Window Comparator Circuit**

### 8.1.1.2.5 Reference Voltages

Referring to [Figure 32](#), the divider networks comprising R7, R8, R9, and R10, generate the reference voltages *VREF\_High* and *VREF\_Low* of the window comparator. The center point of the divider provides the bias voltage of the gain in the stage *B* through the connection to the noninverting input of the amplifier.

Due to the very low bias current of the TLV8544 device, it is possible to use very large values of resistors in the divider networks to minimize the current to ground through the resistors to a negligible amount. For  $R7 = R8 = R9 = R10 = 15\text{ M}\Omega$ :

$$V_{REF\_High} = \left( \frac{R7 + R8 + R9}{R7 + R8 + R9 + R10} \right) V_{CC} = \frac{4.5 \times 10^6}{6 \times 10^6} \times V_{CC} = 0.75 \times V_{CC} \quad (8)$$

$$V_{REF\_Low} = \left( \frac{R7}{R8 + R9 + R10 + R7} \right) V_{CC} = \frac{1.5 \times 10^6}{6 \times 10^6} \times V_{CC} = 0.25 \times V_{CC} \quad (9)$$



### Application Information (continued)

Low leakage ceramic capacitors C7, and C8, maintain constant threshold voltages, preventing potential chatter at the output of the comparators. It should be noted that using cheap electrolytic capacitors must be avoided as they have high (many  $\mu\text{A}$ ) leakage current. The comparator outputs stay low in the absence of motion across the sensor. In the presence of motion, comparators C and D generate *high* output pulses as shown in Figure 33. The order of the pulses depends on the direction of the motion in front of the sensor.

#### 8.1.1.3 Application Curve

Scope plots of the amplified PIR signal at the input of the noninverting comparator and the corresponding output signal are shown in Figure 34 and Figure 35. As the PIR signal (blue line) crosses the VREF\_High threshold, the output of the comparator switches from the cutoff (slightly higher than ground) state to the saturation state (slightly lower than  $V_{\text{BAT}} = 3.3\text{ V}$ ). Depending on the speed of the object, the PIR signal peaks to its maximum and roles off within several seconds. When the signal crosses the VREF\_High threshold on the way down, the output of the noninverting amplifier toggles back to the cutoff region (low).

The data for plot of Figure 34 was captured using the BOOSTXL-TLV8544PIR board. Because the motion was created at very close proximity of the sensor on the booster board used to collect the data, the signal was limited by the diode in the first stage as shown in the plot.

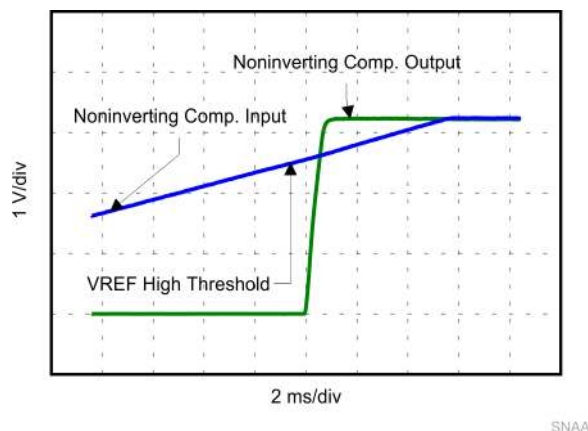


Figure 34. Noninverting Comparator Input and Output Signals

Referring to Figure 34, the output of the inverting comparator during the lower cycle of the PIR signal switches from the cutoff region to the saturation region as the input signal crosses the VREF\_Low threshold.

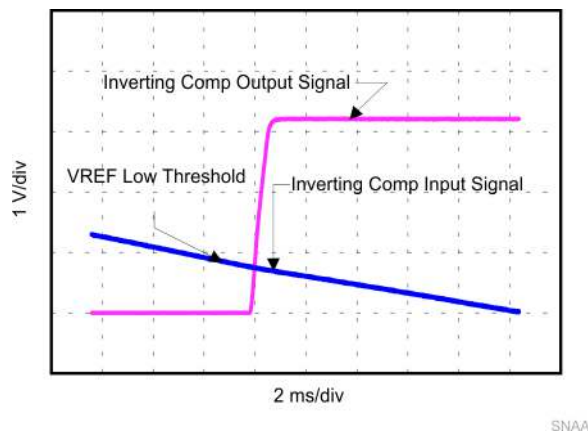
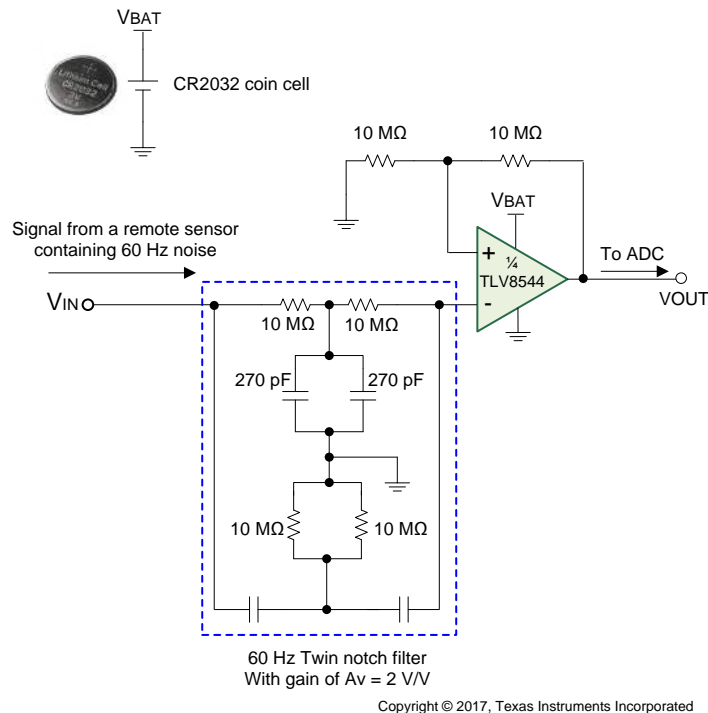


Figure 35. Noninverting Comparator Input and Output Signals

## Application Information (continued)

### 8.1.2 Typical Application: 60-Hz Twin T Notch Filter



**Figure 36. 60 Hz-Notch Filter**

#### 8.1.2.1 Design Requirements

Small signals from transducers in remote and distributed sensing applications commonly suffer strong 60-Hz interference from AC power lines. The circuit of [Figure 36](#) filters out (notches out) the 60 Hz and provides a system gain of  $A_V = 2$  V/V for the sensor signal represented by a 1-kHz sine wave. Similar stages may be cascaded to remove 2<sup>nd</sup> and 3<sup>rd</sup> harmonics of 60 Hz. Thanks to the nanopower consumption of the TLV8544, even five such circuits can run for 9.5 years from a small CR2032 lithium cell. These batteries have a nominal voltage of 3 V and an end of life voltage of 2 V. With an operating voltage from 1.7 V to 3.6 V the TLV8544 device can function over this voltage range.

#### 8.1.2.2 Detailed Design Procedure

The notch frequency is set by:

$$F_0 = 1 / 2\pi RC. \quad (10)$$

To achieve a 60-Hz notch use  $R = 10$  MΩ and  $C = 270$  pF. If eliminating 50-Hz noise, use  $R = 11.8$  MΩ and  $C = 270$  pF.

The twin T notch filter works by having two separate paths from  $V_{IN}$  to the input of the amplifier. A low-frequency path through the series input resistors and another separate high-frequency path through the series input capacitors. However, at frequencies around the notch frequency, the two paths have opposing phase angles, and the two signals tend to cancel at the input of the amplifier.

To ensure that the target center frequency is achieved and to maximize the notch depth (Q factor) the filter must be as balanced as possible. To obtain circuit balance, while overcoming limitations of available standard resistor and capacitor values, use passives in parallel to achieve the  $2C$  and  $R/2$  circuit requirements for the filter components that connect to ground.

To make sure passive component values stay as expected, clean the board with alcohol, rinse with deionized water, and air dry. Make sure board remains in a relatively low humidity environment to minimize moisture which may increase the conductivity of board components. Also large resistors come with considerable parasitic stray capacitance which effects can be reduced by cutting out the ground plane below components of concern.

## Application Information (continued)

Large resistors are used in the feedback network to minimize battery drain. When designing with large resistors, resistor thermal noise, op amp current noise, as well as op-amp voltage noise, must be considered in the noise analysis of the circuit. The noise analysis for the circuit in [Figure 36](#) can be done over a bandwidth of 2 kHz, which takes the conservative approach of overestimating the bandwidth (TLV8544 typical  $GBW/A_V$  is lower, where  $A_V$  is the gain of the system). The total noise at the output is approximately 800  $\mu$ Vpp, which is excellent considering the total consumption of the circuit is only 500 nA per channel. The dominant noise terms are op-amp voltage noise, current noise through the feedback network (430  $\mu$ Vp-p), and current noise through the notch filter network (280  $\mu$ Vp-p). Thus the total noise of the circuit is below 1/2 LSB of a 10-bit system with a 2-V reference, which is 1 mV.

### 8.1.2.3 Application Curve

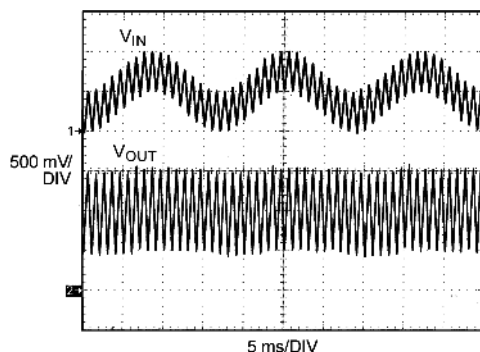


Figure 37. 60-Hz Notch Filter Waveform

## 8.2 Dos and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, particularly cables, multiplexers, and ADC inputs.

Do add series current limiting resistors and external Schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1 mA or less (1 K $\Omega$  per volt).

## 9 Power Supply Recommendations

The TLV8544 is specified for operation from 1.7 V to 3.6 V ( $\pm 0.85$  V to  $\pm 1.8$  V) over a  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

### CAUTION

Supply voltages larger than 3.6 V can permanently damage the device.

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 100-nF capacitors be placed as close as possible to the op-amp power supply pins. For single supply, place a capacitor between  $V+$  and  $V-$  supply leads. For dual supplies, place one capacitor between  $V+$  and ground and one capacitor between  $V-$  and ground.

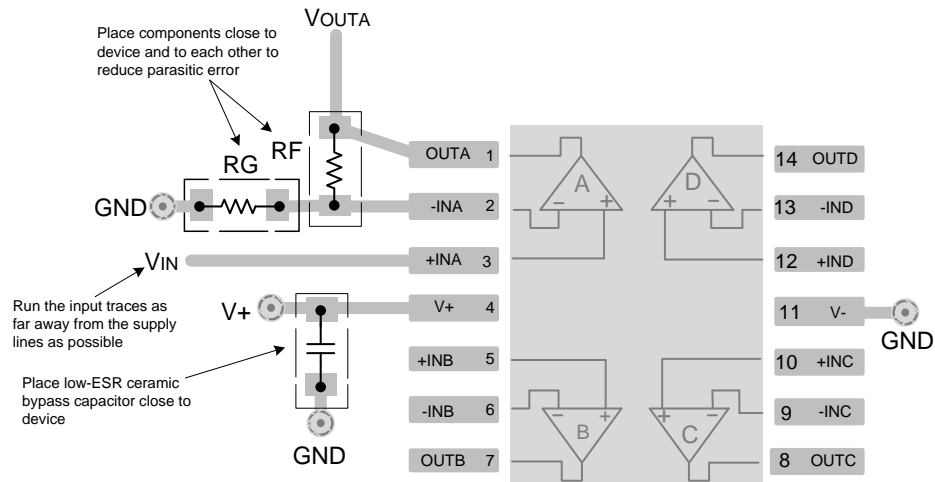
Low bandwidth nanopower devices do not have good high frequency ( $> 1$  kHz) AC PSRR rejection against high-frequency switching supplies and other 1-kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

## 10 Layout

### 10.1 Layout Guidelines

- The  $V+$  pin must be bypassed to ground with a low ESR capacitor.
- The optimum placement is closest to the  $V+$  and ground pins.
- Take care to minimize the loop area formed by the bypass capacitor connection between  $V+$  and ground.
- Connect the ground pin to the PCB ground plane at the pin of the device.
- Place the feedback components as close as possible to the device to minimize stray impedance.

### 10.2 Layout Example



**Figure 38. Layout Example of a Typical Dual Channel Package (Top View)**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

[TINA-TI SPICE-Based Analog Simulation Program](#)

[DIP Adapter Evaluation Module](#)

[TI Universal Operational Amplifier Evaluation Module](#)

[TI FilterPro Filter Design Software](#)

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation, see the following:

- [AN-1798 Designing with Electro-Chemical Sensors](#)
- [AN-1803 Design Considerations for a Transimpedance Amplifier](#)
- [AN-1852 Designing With pH Electrodes](#)
- [Compensate Transimpedance Amplifiers Intuitively](#)
- [Transimpedance Considerations for High-Speed Operational Amplifiers](#)
- [Noise Analysis of FET Transimpedance Amplifiers](#)
- [Circuit Board Layout Techniques](#)
- [Handbook of Operational Amplifier Applications](#)

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.7 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV8544PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL8544	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV8544PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

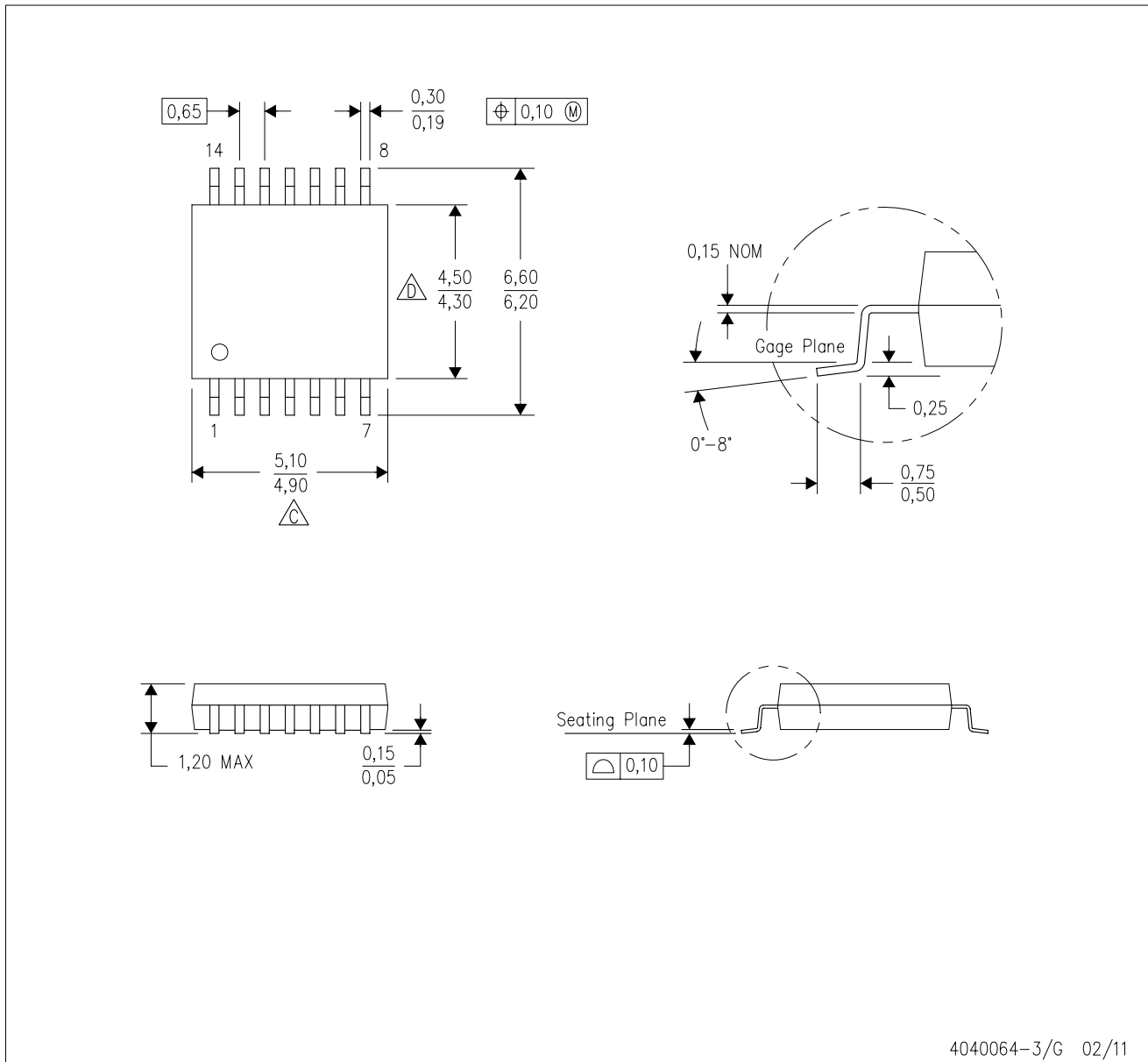


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV8544PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

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