DSA557-03/04/05

Multiple Output MEMS PCIe Gen1/2/3/4 Clocks for Automotive

Features

- Automotive AEC-Q100 Qualified
- Complies with PCIe Gen1/2/3/4 Common Clock Spec
- Integrated MEMS Resonator Eliminates the Need for External 25 MHz Crystal
- Wide Temperature Range:
  - Automotive Grade 2: –40°C to +105°C
  - Automotive Grade 3: –40°C to +85°C
- 100 MHz HCSL/LVDS/LVCMOS Options Available
- Dedicated Output Enable (OE) Pins for Clock Outputs
- Small Footprints:
  - 14-Lead QFN (DSA557-03, Two Outputs)
  - 20-Lead VQFN (DSA557-04, Three Outputs; DSA557-05, Four Outputs)
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x Better MTF than Quartz Oscillators
- Low Current Consumption: 30% Lower than Competing Devices
- Supply Range of 2.25V to 3.63V
- Lead-Free and RoHS Compliant

Applications

- Automotive Infotainment
- Automotive ADAS
- Autonomous Driving
- In-Vehicle Network

General Description

The DSA557 series of high performance PCI Express clock generators use a proven silicon MEMS technology to provide 100 MHz differential output clocks with excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

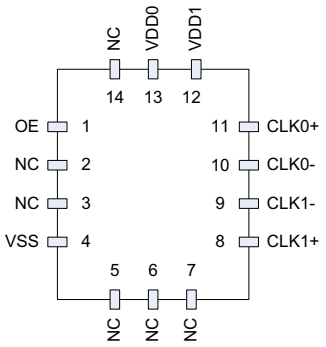
The DSA557-03/04/05 have two, three, and four 100 MHz outputs, respectively. All have output enable/disable features.

The DSA557-03 is available in a space-saving 14-lead QFN package. The DSA557-04 and DSA557-05 are available in a 20-lead VQFN.

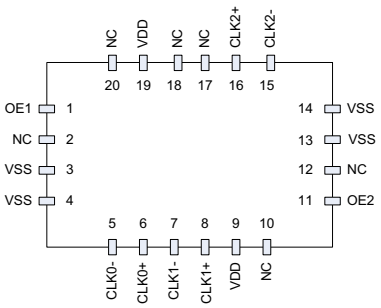
Additional LVDS and LVCMOS output formats are available in addition to the default HCSL output format.

Package Types

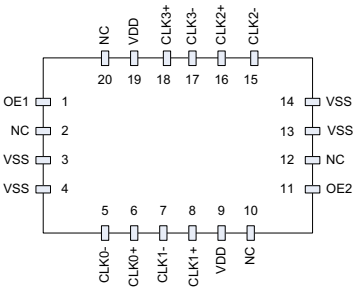
DSA557-03
14-Lead QFN
(Top View)



DSA557-04
20-Lead VQFN
(Top View)

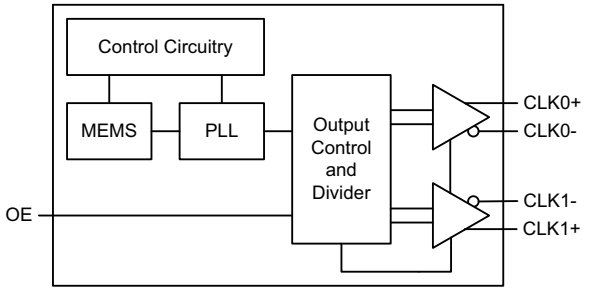


DSA557-05
20-Lead VQFN
(Top View)

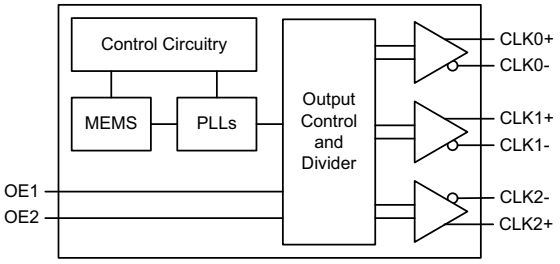


Block Diagrams

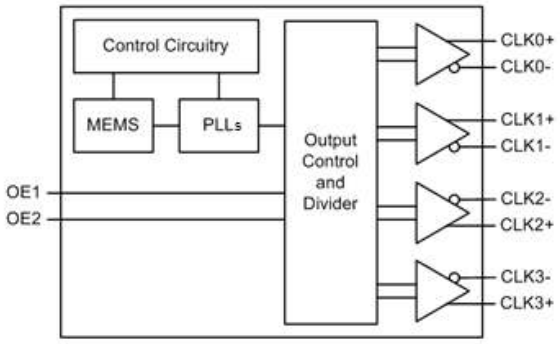
DSA557-03



DSA557-04



DSA557-05



Note: CLK0+/–, CLK1+/–, CLK2+/–, and CLK3+/– are 100 MHz, per PCIe standards.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage ..... –0.3V to V_{DD} + 0.3V
Supply Voltage ..... –0.3V to +4.0V
ESD Protection on All Pins (HBM) ..... 4 kV
ESD Protection on All Pins (CDM) ..... 1.5 kV

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, T = +25°C, V_{DD} = 3.3V.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage	V_{DD}	2.25	—	3.63	V	Note 1
Supply Current, DSA557-03	I_{DD}	—	21	23	mA	HCSL output, EN pin low, output disabled
		—	60	—		HCSL output, EN pin high, output enabled
Supply Current, DSA557-04	I_{DD}	—	42	46	mA	HCSL output, EN pin low, output disabled
		—	100	—		HCSL output, EN pin high, output enabled
Supply Current, DSA557-05	I_{DD}	—	42	46	mA	HCSL output, EN pin low, output disabled
		—	120	—		HCSL output, EN pin high, output enabled
Frequency Stability (including frequency variations due to initial tolerance, temp., and power supply voltage)	Δf	—	—	±100	ppm	All temperature ranges
		—	—	±50		
Aging - 1st Year	Δf	—	—	±5	ppm	±1 ppm each subsequent year
Startup Time (Note 2)	t_{SU}	—	—	5	ms	T = +25°C
Input Logic Levels						
Input Logic High	V_{IH}	0.75 x V_{DD}	—	—	V	—
Input Logic Low	V_{IL}	—	—	0.25 x V_{DD}	V	—
Output Disable Time (Note 3)	t_{DS}	—	—	5	ns	—
Output Enable Time	t_{EN}	—	—	20	ns	—
Enable Pull-Up Resistor (Note 4)	—	—	40	—	kΩ	Internally pulled up
HCSL Outputs (Note 5)						
Output Logic High	V_{OH}	0.725	—	—	V	R_L = 50Ω
Output Logic Low	V_{OL}	—	—	0.1	V	R_L = 50Ω
Peak-to-Peak Output Swing	—	—	750	—	mV	Single-Ended
Output Frequency	f_{OUT}	—	100	—	MHz	—

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, T = +25°C, V_{DD} = 3.3V.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Transition Time (Note 6)	t_r/t_f	200	—	400	ps	20% to 80%, R_L = 50Ω, C_L = 2 pF
Output Duty Cycle	SYM	48	—	52	%	Differential
Period Jitter (Note 7)	J_{PER}	—	2.5	—	ps_{RMS}	$f_{01} = f_{02}$ = 100 MHz
Jitter, Phase (Common Clock Architecture)	T_J	—	17	86	ps_{PP}	PCIe Gen 1.1, (Note 8) $T_J = D_J + 14.069 \times R_J$ (BER 10^{-12})
	$J_{RMS-CCHF}$	—	1.46	3.1	ps_{RMS}	PCIe Gen 2.1, 1.5 MHz to Nyquist, (Note 8)
	$J_{RMS-CCLF}$	—	0.08	3.0	ps_{RMS}	PCIe Gen 2.1, 10 kHz to 1.5 MHz, (Note 8)
	J_{RMS-CC}	—	0.313	1.0	ps_{RMS}	PCIe Gen 3.0, (Note 8)
	J_{RMS-CC}	—	0.313	0.5	ps_{RMS}	PCIe Gen 4.0, 16 GHz, (Note 8)
Integrated Phase Noise (Data Clock Architecture)	$J_{RMS-DCHF}$	—	2.15	4.0	ps_{RMS}	PCIe Gen 2.1, 1.5 MHz to Nyquist, (Note 8)
	$J_{RMS-DCLF}$	—	0.06	7.5	ps_{RMS}	PCIe Gen 2.1, 10 kHz to 1.5 MHz, (Note 8)
	J_{RMS-DC}	—	0.32	1.0	ps_{RMS}	PCIe Gen 3.0, (Note 8)
LVDS Output						
Offset Voltage	V_{OS}	1.125	1.25	1.40	V	V_{DD} = 2.5V/3.3V
V_{OS} Magnitude Change	ΔV_{OS}	—	—	50	mV	—
Output High Voltage	V_{OH}	$0.9xV_{DD}$	—	—	V	—
Output Low Voltage	V_{OL}	—	—	$0.1xV_{DD}$	V	—
Output Frequency	f_{OUT}	—	100	—	MHz	—
Differential Output Voltage	V_{OD}	275	350	475	mV_{PP}	—
V_{OD} Magnitude Change	ΔV_{OD}	—	—	40	mV	—
LVDS Output Rise/Fall Time	t_r/t_f	—	200	—	ps	20% – 80%
Output Duty Cycle	ODC	48	50	52	%	20% – 80%, R_L = 50Ω, C_L = 2 pF
Period Jitter, Peak to Peak	J_{PTP}	—	2.5	—	ps	f_{OUT} = 100 MHz, Standard Drive
Integrated Phase Noise	J_{PH}	—	0.28	—	ps_{RMS}	200 kHz to 20 MHz @ 100 MHz, T_A = +105°C
		—	0.4	—		100 kHz to 80 MHz @ 100 MHz
		—	1.7	2.0		12 kHz to 10 MHz @ 100 MHz

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, T = +25°C, V_{DD} = 3.3V.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
LVCMOS Output						
Output High Voltage	V_{OH}	0.8xV_{DD}	—	—	V	±10 mA drive current
Output Low Voltage	V_{OL}	—	—	0.2xV_{DD}	V	±10 mA drive current
Output Frequency	f_{OUT}	—	100	—	MHz	—
Output Rise/Fall Time	t_r/t_f	—	1.2	—	ns	20% – 80%, C_L = 15 pF
Output Duty Cycle	ODC	48	50	52	%	f_{OUT} = 100 MHz, Standard Drive
Period Jitter	J_{PTP}	—	3	—	ps_{RMS}	f_{OUT} = 100 MHz, Standard Drive
Integrated Phase Noise	J_{PH}	—	0.3	—	ps_{RMS}	200 kHz to 20 MHz @ 100 MHz
		—	0.38	—		100 kHz to 20 MHz @ 100 MHz
		—	1.7	2.0		12 kHz to 20 MHz @ 100 MHz

Note 1: Each pin V_{DD} should be filtered with a 0.1 µF capacitor.

2: t_{SU} is time to 100 ppm of output frequency after V_{DD} is applied and outputs are enabled.

3: Output Waveform and Test Circuit figures define the parameters.

4: Output is enabled if pad is floated or not connected.

5: Contact Microchip for alternate output options (LVDS, LVCMOS).

6: Output Waveform and Connection Diagram define the parameters.

7: Period Jitter includes crosstalk from adjacent output.

8: Jitter limits established by Gen 1.1, Gen 2.1, Gen 3.0, and Gen 4.0 PCIe standards.

TEMPERATURE SPECIFICATIONS

Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	–40	—	+85	°C	Ordering Option I
		–40	—	+105	°C	Ordering Option L
Junction Operating Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–55	—	+150	°C	—
Lead Temperature	—	—	+260	—	°C	Soldering, 40s

2.0 PIN DESCRIPTIONS AND CONNECTION DIAGRAMS

The descriptions of the pins are listed in Table 2-1, Table 2-2, and Table 2-3.

TABLE 2-1: DSA557-03 QFN-14 PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Description
1	OE	I	Output enable, active-high.
2	NC	N/A	Ground recommended or leave as a NC.
3	NC	N/A	Ground recommended or leave as a NC.
4	VSS	P	Ground.
5	NC	N/A	Ground recommended or leave as a NC.
6	NC	N/A	Ground recommended or leave as a NC.
7	NC	N/A	Ground recommended or leave as a NC.
8	CLK1+	O	True output of differential pair.
9	CLK1–	O	Complement output of differential pair.
10	CLK0–	O	Complement output of differential pair.
11	CLK0+	O	True output of differential pair.
12	VDD1	P	Power supply for core and output 1 (CLK1+/CLK1–)
13	VDD0	P	Power supply for output 0 (CLK0+/CLK0–)
14	NC	N/A	Ground recommended or leave as a NC.

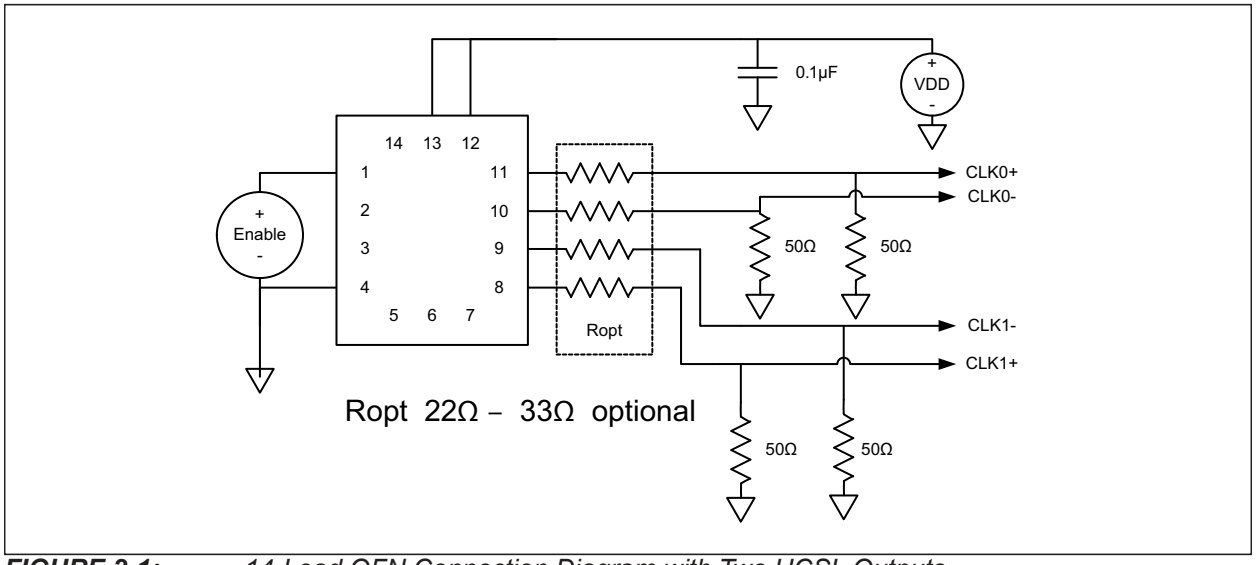


FIGURE 2-1: *14-Lead QFN Connection Diagram with Two HCSL Outputs.*

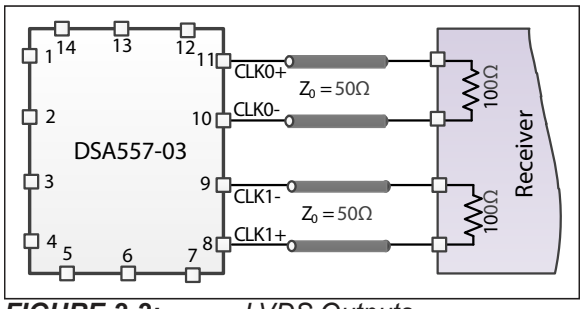


FIGURE 2-2: *LVDS Outputs.*

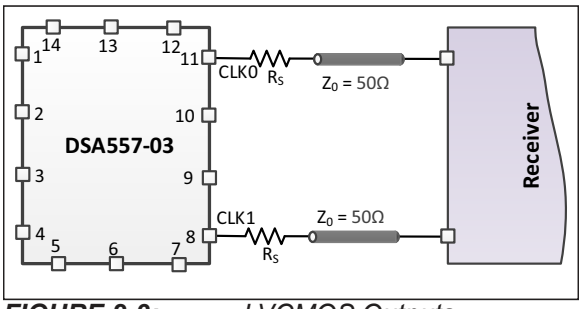


FIGURE 2-3: *LVCMOS Outputs.*

TABLE 2-2: DSA557-04 QFN-20 PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Description
1	OE1	I	Output enable, active-high. Controls CLK0.
2	NC	N/A	Leave unconnected or grounded.
3	VSS	P	Ground.
4	VSS	P	Ground.
5	CLK0–	O	Complement output of differential pair.
6	CLK0+	O	True output of differential pair.
7	CLK1–	O	Complement output of differential pair.
8	CLK1+	O	True output of differential pair.
9	VDD	P	Power supply.
10	NC	N/A	Leave unconnected or grounded.
11	OE2	I	Output enable, active-high. Controls CLK1 and CLK2.
12	NC	N/A	Leave unconnected or grounded.
13	VSS	P	Ground.
14	VSS	P	Ground.
15	CLK2–	O	Complement output of differential pair.
16	CLK2+	O	True output of differential pair.
17	NC	N/A	Leave unconnected or grounded.
18	NC	N/A	Leave unconnected or grounded.
19	VDD	P	Power supply.
20	NC	N/A	Leave unconnected or grounded.

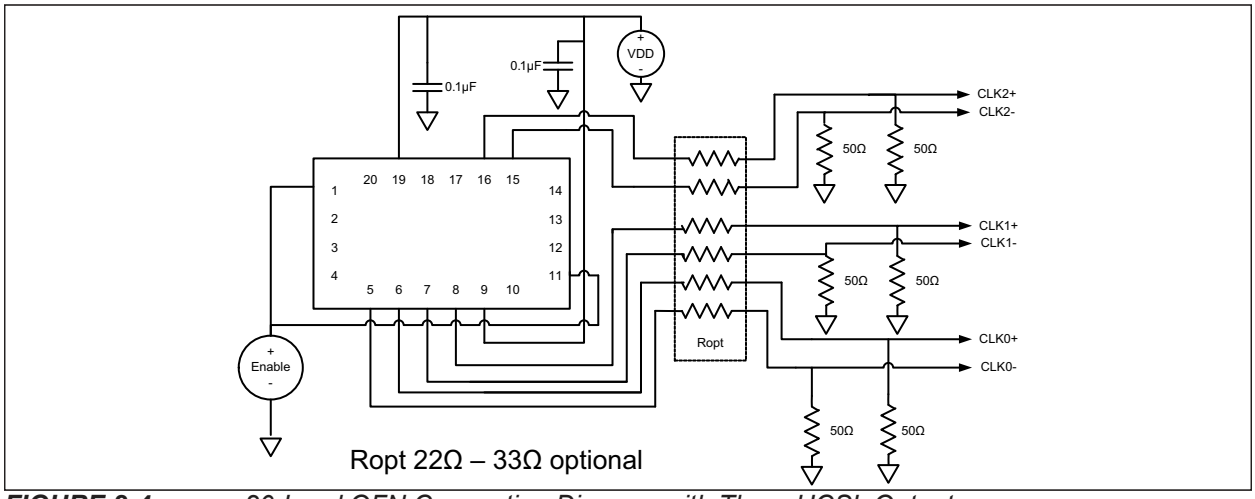


FIGURE 2-4: *20-Lead QFN Connection Diagram with Three HCSL Outputs.*

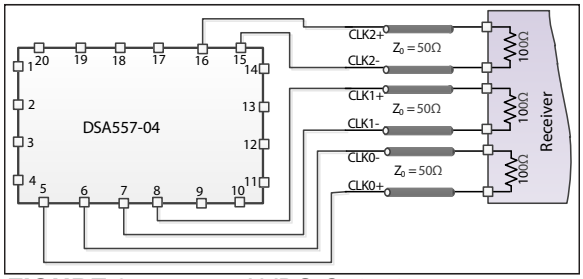


FIGURE 2-5: *LVDS Outputs.*

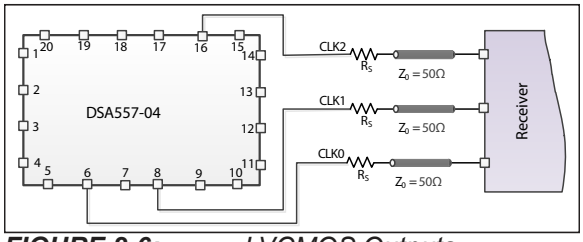


FIGURE 2-6: *LVCMOS Outputs.*

TABLE 2-3: DSA557-05 QFN-20 PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Description
1	OE1	I	Output enable, active-high. Controls CLK0 and CLK3.
2	NC	N/A	Leave unconnected or grounded.
3	VSS	P	Ground.
4	VSS	P	Ground.
5	CLK0–	O	Complement output of differential pair.
6	CLK0+	O	True output of differential pair.
7	CLK1–	O	Complement output of differential pair.
8	CLK1+	O	True output of differential pair.
9	VDD	P	Power supply.
10	NC	N/A	Leave unconnected or grounded.
11	OE2	I	Output enable, active-high. Controls CLK1 and CLK2.
12	NC	N/A	Leave unconnected or grounded.
13	VSS	P	Ground.
14	VSS	P	Ground.
15	CLK2–	O	Complement output of differential pair.
16	CLK2+	O	True output of differential pair.
17	CLK3–	O	Complement output of differential pair.
18	CLK3+	O	True output of differential pair.
19	VDD	P	Power supply.
20	NC	N/A	Leave unconnected or grounded.

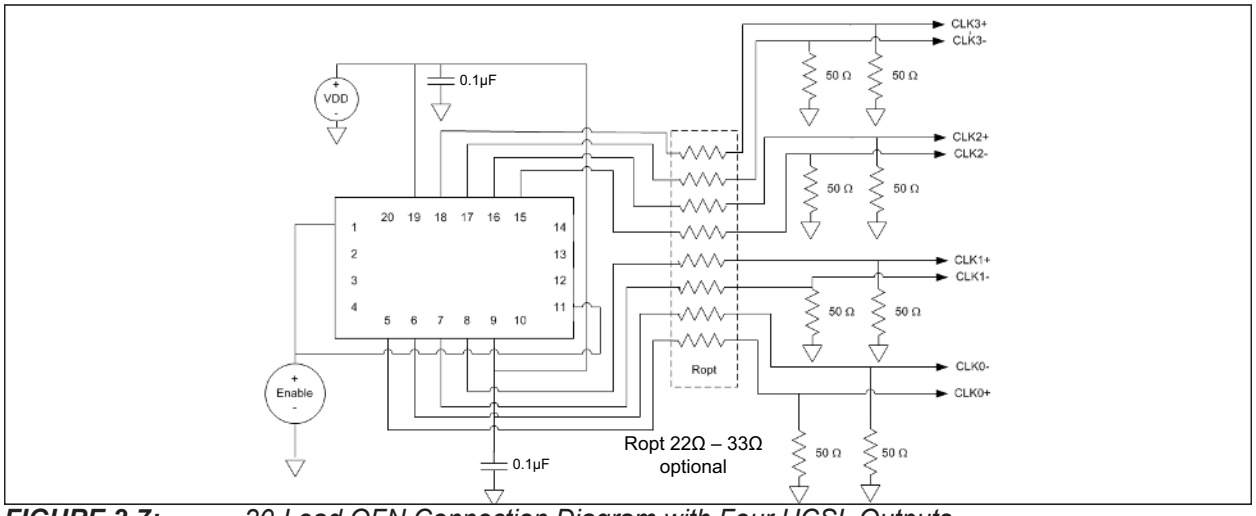


FIGURE 2-7: *20-Lead QFN Connection Diagram with Four HCSL Outputs.*

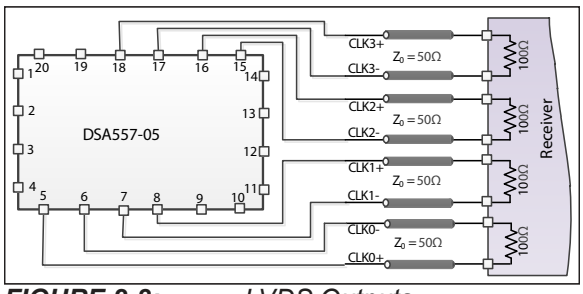


FIGURE 2-8: *LVDS Outputs.*

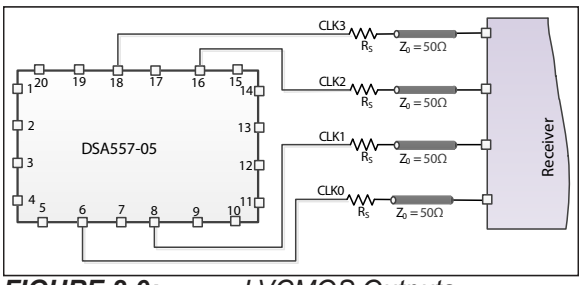


FIGURE 2-9: *LVCMOS Outputs.*

3.0 OUTPUT WAVEFORM

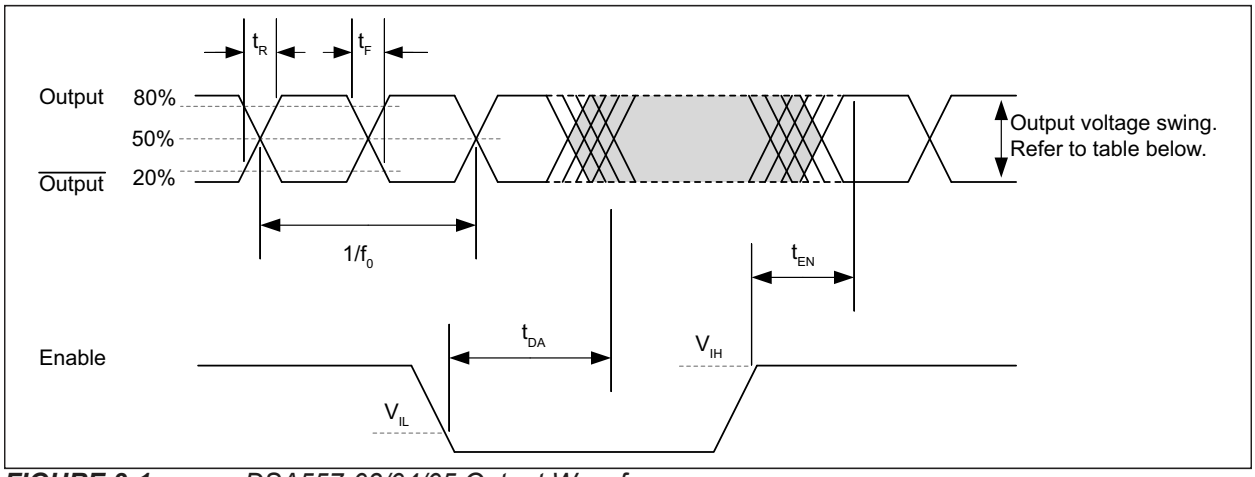


FIGURE 3-1: *DSA557-03/04/05 Output Waveform.*

TABLE 3-1: OUTPUT VOLTAGE SWING

Specification	V_{CM}	V_{SWING_SE} (typ.)
LVDS	1.2V	350 mV
HCSL	350 mV	675 mV

4.0 SOLDER REFLOW PROFILE

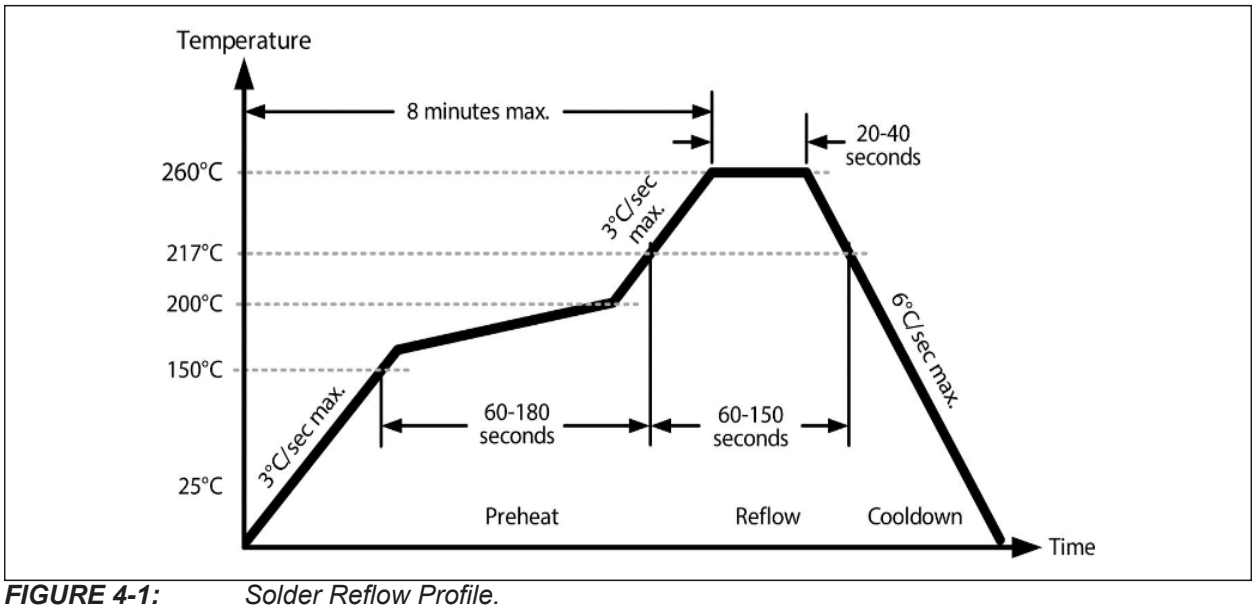


FIGURE 4-1: *Solder Reflow Profile.*

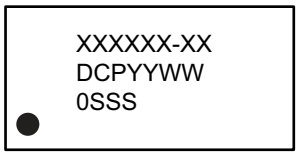
TABLE 4-1: SOLDER REFLOW

QFN-14 MSL 1 @ 260°C Refer to JSTD-020C TSSOP-16 MSL 3 @ 260°C Refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp.)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time Maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20 to 40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

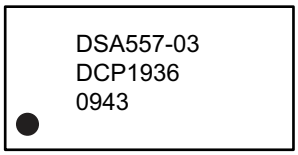
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

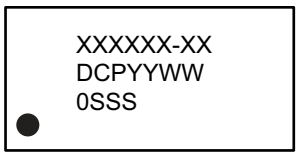
14-Lead QFN*



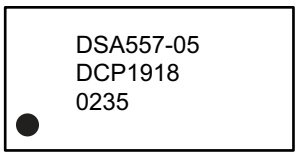
Example



20-Lead QFN*



Example



Legend:	XX...X	Product code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	SSS	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

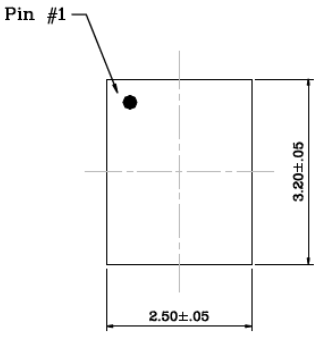
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

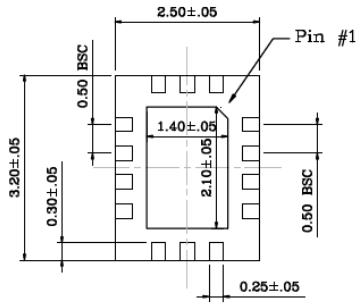
TITLE

14 LEAD QFN 2.5x3.2mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN2532-14LD-PL-1	UNIT	MM

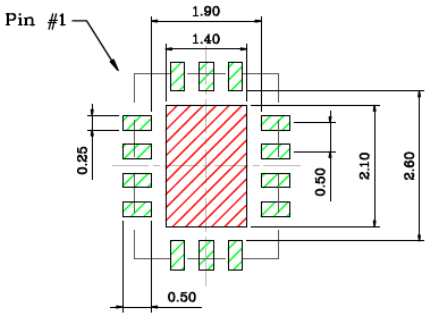


Top View



Bottom View

Side View



Recommended Land Pattern

NOTE:

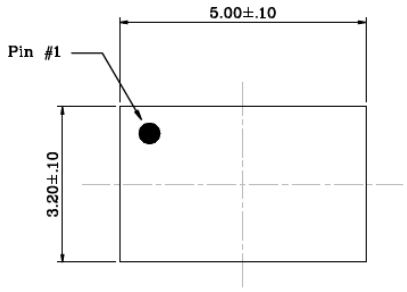
1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
2. Red shaded rectangle in Recommended Land Pattern is keep out area.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

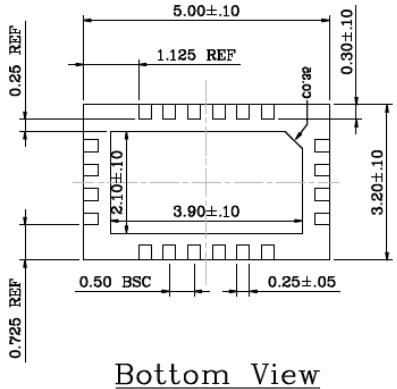
TITLE

20 LEAD QFN 5.0x3.2mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

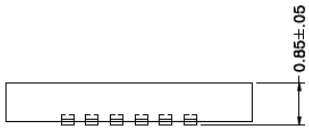
DRAWING #	QFN5032-20LD-PL-1	UNIT	MM



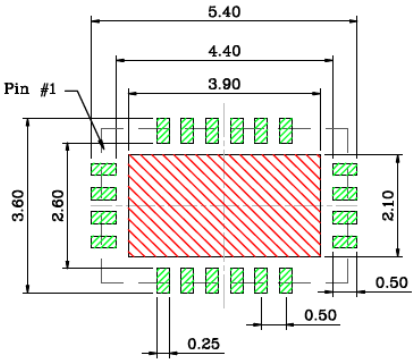
Top View



Bottom View



Side View



Recommended Land Pattern

NOTE:

1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
2. Red shaded rectangle in Recommended Land Pattern is keep-out area.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2019)

- Initial release of DSA557-03/04/05 as Microchip data sheet DS20006175A.

Revision B (May 2020)

- Updated Product Identification System section to add the Automotive Suffix to the full part number.
- Removed LVPECL option throughout data sheet.
- Added LVDS and LVCMOS information to Electrical Characteristics section.
- Added Figure 2-2, Figure 2-3, Figure 2-5, Figure 2-6, Figure 2-8, and Figure 2-9.

Revision C (June 2020)

- Updated Phase Jitter values in the Electrical Characteristics table.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	XXXX	X	X	X	X	XXX
Device	Output Format	Package	Temp. Range	Stability	Packing Option	Automotive Suffix

Device:	DSA557-03:	Two Output PCIe Clock Generator for Automotive	
	DSA557-04:	Three Output PCIe Clock Generator for Automotive	
	DSA557-05:	Four Output PCIe Clock Generator for Automotive	
Output Format: (Note 1)	1	=	LVCMOS
	3	=	LVDS
	4	=	HCSL
Package:	F	=	14-Lead QFN (DSA557-03 Only)
	K	=	20-Lead QFN (DSA557-04/05 Only)
Temperature Range:	L	=	–40°C to +105°C (Automotive Grade 2)
	I	=	–40°C to +85°C (Automotive Grade 3)
Stability:	0	=	±100 ppm
	1	=	±50 ppm
Packing Option:	<blank>=		72/Tube (DSA557-04/05)
	<blank>=		96/Tube (DSA557-03)
	T	=	1000/Reel (All Package Options)
Automotive Suffix:	Vxx	=	Automotive suffix in which “xx” is assigned by Microchip. Default value is “AO” for standard automotive part.

Note 1: The Output Format’s arrangement is CLK3 to CLK0 (left-to-right) and may only have as many digits as that particular part allows. For example, DSA557-03 has two outputs; the part number example can only have two digits in that location. DSA557-04 can only have three and DSA557-05 can only have four.

Examples:

a) DSA557-0344FL0VAO:
Two HCSL Outputs PCIe Clock Generator for Automotive, 14-Lead QFN, –40°C to +105°C Temperature Range, ±100 ppm Stability, 96/Tube, Standard Automotive

b) DSA557-04111KI1TVAO:
Three LVCMOS Outputs PCIe Clock Generator for Automotive, 20-Lead QFN, –40°C to +85°C Temperature Range, ±50 ppm Stability, 1000/Reel, Standard Automotive

c) DSA557-053344KL0VAO:
Four Output PCIe Clock Generator for Automotive, (CLK3/CLK2: LVDS, CLK1/CLK0: HCSL), 20-Lead QFN, –40°C to +105°C Temperature Range, ±100 ppm Stability, 96/Tube, Standard Automotive

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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