# TimerBlox: Voltage Controlled Silicon Oscillator

## FEATURES

- **Fixed-Frequency or Voltage-Controlled Operation**
  - **Fixed: Single Resistor Programs Frequency with <1.5% Max Error**
  - **VCO: Two Resistors Set VCO Center Frequency and Tuning Range**
- **Frequency Range: 488Hz to 2MHz**
- 2.25V to 5.5V Single Supply Operation
- 72µA Supply Current at 100kHz
- 500µs Start-Up Time
- VCO Bandwidth >300kHz at 1MHz
- CMOS Logic Output Sources/Sinks 20mA
- 50% Duty Cycle Square Wave Output
- Output Enable (Selectable Low or Hi-Z When Disabled)
- 55°C to 125°C Operating Temperature Range
- Available in Low Profile (1mm) SOT-23 (ThinSOT™) and 2mm × 3mm DFN Package
- AEC-Q100 Qualified for Automotive Applications

## APPLICATIONS

- Low Cost Precision Programmable Oscillator
- Voltage-Controlled Oscillator
- High Vibration, High Acceleration Environments
- Replacement for Fixed Crystal and Ceramic Oscillators
- Portable and Battery-Powered Equipment

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## DESCRIPTION

The LTC®6990 is a precision silicon oscillator with a programmable frequency range of 488Hz to 2MHz. It can be used as a fixed-frequency or voltage-controlled oscillator (VCO). The LTC6990 is part of the TimerBlox® family of versatile silicon timing devices.

A single resistor, $R_{SET}$, programs the LTC6990's internal master oscillator frequency. The output frequency is determined by this master oscillator and an internal frequency divider, $N_{DIV}$, programmable to eight settings from 1 to 128.

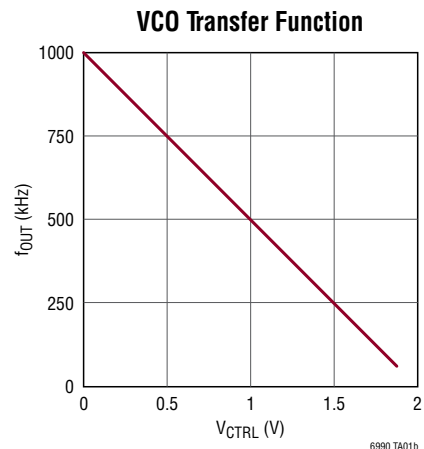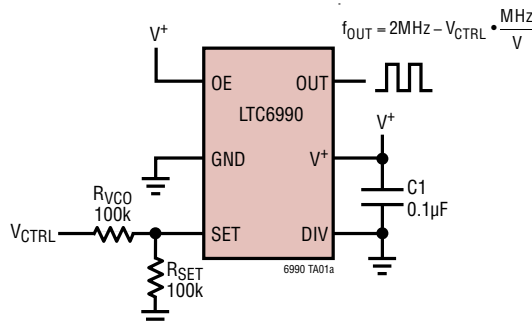$$f_{OUT} = \frac{1\text{MHz}}{N_{DIV}} \cdot \frac{50\text{k}\Omega}{R_{SET}}, N_{DIV} = 1, 2, 4 \dots 128$$

Optionally, a second resistor at the SET input provides linear voltage control of the output frequency and can be used for frequency modulation. A narrow or wide VCO tuning range can be configured by the appropriate selection of the two resistors.

The LTC6990 includes an enable function that is synchronized with the master oscillator to ensure clean, glitch-free output pulses. The disabled output can be configured to be high impedance or forced low.

For easy configuration of the LTC6990, use the TimerBlox LTC6990: Voltage Controlled Oscillator Web-Based Design Tool.

## TYPICAL APPLICATION
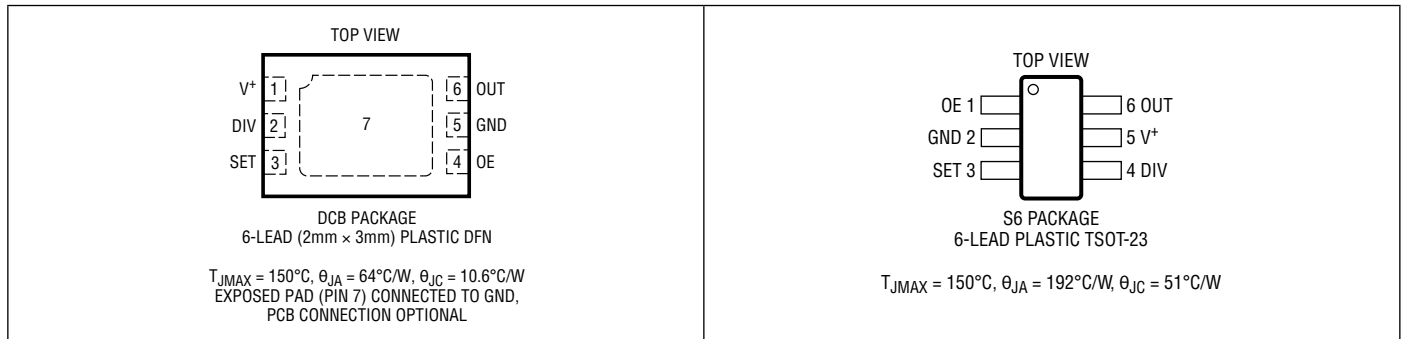
**Voltage Controlled Oscillator with 16:1 Frequency Range**



$$f_{OUT} = 2\text{MHz} - V_{CTRL} \cdot \frac{\text{MHz}}{\text{V}}$$

6990 TA01a

**VCO Transfer Function**



6990 TA01b

Rev. D

1

# ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V⁺) to GND ........................................6V

Maximum Voltage on Any Pin
........................... (GND − 0.3V) ≤ $V_{PIN}$ ≤ (V⁺ + 0.3V)

Operating Temperature Range (Note 2)
LTC6990C...........................................−40°C to 85°C
LTC6990I............................................−40°C to 85°C
LTC6990H...........................................−40°C to 125°C
LTC6990MP........................................−55°C to 125°C

Specified Temperature Range (Note 3)
LTC6990C.................................................0°C to 70°C
LTC6990I.............................................−40°C to 85°C
LTC6990H............................................−40°C to 125°C
LTC6990MP.........................................−55°C to 125°C
Junction Temperature .......................................... 150°C
Storage Temperature Range .................−65°C to 150°C
Lead Temperature (Soldering, 10sec)...................300°C

# PIN CONFIGURATION

TOP VIEW

V⁺  1  | 6  OUT
DIV 2  | 5  GND
SET 3  | 4  OE

7

DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 64°C/W, $\theta_{JC}$ = 10.6°C/W
EXPOSED PAD (PIN 7) CONNECTED TO GND,
PCB CONNECTION OPTIONAL

TOP VIEW

OE 1 | 6 OUT
GND 2 | 5 V⁺
SET 3 | 4 DIV

S6 PACKAGE
6-LEAD PLASTIC TSOT-23

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 192°C/W, $\theta_{JC}$ = 51°C/W

# ORDER INFORMATION

**Lead Free Finish**

| TAPE AND REEL (MINI) | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC6990CDCB#TRMPBF | LTC6990CDCB#TRPBF | LDWX | 6-Lead (2mm × 3mm) Plastic DFN | 0°C to 70°C |
| LTC6990IDCB#TRMPBF | LTC6990IDCB#TRPBF | LDWX | 6-Lead (2mm × 3mm) Plastic DFN | −40°C to 85°C |
| LTC6990HDCB#TRMPBF | LTC6990HDCB#TRPBF | LDWX | 6-Lead (2mm × 3mm) Plastic DFN | −40°C to 125°C |
| LTC6990CS6#TRMPBF | LTC6990CS6#TRPBF | LTDWW | 6-Lead Plastic TSOT-23 | 0°C to 70°C |
| LTC6990IS6#TRMPBF | LTC6990IS6#TRPBF | LTDWW | 6-Lead Plastic TSOT-23 | −40°C to 85°C |
| LTC6990HS6#TRMPBF | LTC6990HS6#TRPBF | LTDWW | 6-Lead Plastic TSOT-23 | −40°C to 125°C |
| LTC6990MPS6#TRMPBF | LTC6990MPS6#TRPBF | LTDWW | 6-Lead Plastic TSOT-23 | −55°C to 125°C |
| **AUTOMOTIVE PRODUCTS**\*\* | | | | |
| LTC6990IS6#WTRMPBF | LTC6990IS6#WTRPBF | LTDWW | 6-Lead Plastic TSOT-23 | −40°C to 85°C |
| LTC6990HS6#WTRMPBF | LTC6990HS6#WTRPBF | LTDWW | 6-Lead Plastic TSOT-23 | −40°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Rev. D

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. Test conditions are $V^+ = 2.25V$ to $5.5V$, OE = $V^+$, DIVCODE = 0 to 15 ($N_{DIV}$ = 1 to 128), $R_{SET}$ = 50k to 800k, $R_{LOAD}$ = 5k, $C_{LOAD}$ = 5pF unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | Recommended Range: $R_{SET}$ = 50k to 800k<br>Extended Range: $R_{SET}$ = 25k to 800k | | 0.488<br>0.488 | | 1000<br>2000 | kHz<br>kHz |
| $\Delta f_{OUT}$ | Frequency Accuracy (Note 4) | Recommended Range<br>$R_{SET}$ = 50k to 800k | ● | | ±0.8 | ±1.5<br>±2.2 | %<br>% |
| | | Extended Range<br>$R_{SET}$ = 25k to 800k | ● | | | ±2.4<br>±3.2 | %<br>% |
| $\Delta f_{OUT}/\Delta T$ | Frequency Drift Over Temperature | | ● | | ±0.005 | | %/°C |
| $\Delta f_{OUT}/\Delta V^+$ | Frequency Drift Over Supply | $V^+$ = 4.5V to 5.5V<br>$V^+$ = 2.25V to 4.5V | ●<br>● | | 0.23<br>0.06 | 0.55<br>0.16 | %/V<br>%/V |
| | Long-Term Frequency Stability | (Note 11) | | | 90 | | ppm/√kHr |
| | Period Jitter (Note 10) | $N_{DIV}$ = 1 | | | 0.38 | | $\%_{P-P}$ |
| | | $N_{DIV}$ = 2 | | | 0.22<br>0.027 | | $\%_{P-P}$<br>$\%_{RMS}$ |
| | | $N_{DIV}$ = 128 | | | 0.022<br>0.004 | | $\%_{P-P}$<br>$\%_{RMS}$ |
| | Duty Cycle | $N_{DIV}$ = 1, $R_{SET}$ = 25k to 800k<br>$N_{DIV}$ > 1, $R_{SET}$ = 25k to 800k | ●<br>● | 47<br>48 | 50<br>50 | 53<br>52 | %<br>% |
| BW | Frequency Modulation Bandwidth | | | | 0.4•$f_{OUT}$ | | kHz |
| $t_S$ | Frequency Change Settling Time (Note 9) | $t_{MASTER} = t_{OUT}/N_{DIV}$ | | | 6•$t_{MASTER}$ | | µs |
| **Analog Inputs** | | | | | | | |
| $V_{SET}$ | Voltage at SET Pin | | ● | 0.97 | 1.00 | 1.03 | V |
| $\Delta V_{SET}/\Delta T$ | $V_{SET}$ Drift Over Temperature | | ● | | ±75 | | µV/°C |
| $\Delta V_{SET}/\Delta V^+$ | $V_{SET}$ Drift Over Supply | | | | −150 | | µV/V |
| $\Delta V_{SET}/\Delta I_{SET}$ | $V_{SET}$ Droop with $I_{SET}$ | | | | −7 | | Ω |
| $R_{SET}$ | Frequency-Setting Resistor | Recommended Range<br>Extended Range | ●<br>● | 50<br>25 | | 800<br>800 | kΩ<br>kΩ |
| $V_{DIV}$ | DIV Pin Voltage | | ● | 0 | | $V^+$ | V |
| $\Delta V_{DIV}/V^+$ | DIV Pin Valid Code Range (Note 5) | Deviation from Ideal $V_{DIV}/V^+$ = (DIVCODE + 0.5)/16 | ● | | | ±1.5 | % |
| | DIV Pin Input Current | | ● | | | ±10 | nA |
| **Power Supply** | | | | | | | |
| $V^+$ | Operating Supply Voltage Range | | ● | 2.25 | | 5.5 | V |
| | Power-On Reset Voltage | $R_{SET}$ = 25k to 800k | ● | | | 1.95 | V |
| $I_S$ | Supply Current | $R_L = ∞$, $N_{DIV}$ = 1, $R_{SET}$ = 50k    $V^+$ = 5.5V<br>$V^+$ = 2.25V | ●<br>● | | 235<br>145 | 283<br>183 | µA<br>µA |
| | | $R_L = ∞$, $N_{DIV}$ = 1 $R_{SET}$ = 800k    $V^+$ = 5.5V<br>$V^+$ = 2.25V | ●<br>● | | 71<br>59 | 105<br>92 | µA<br>µA |
| | | $R_L = ∞$, $N_{DIV}$ = 128, $R_{SET}$ = 50k    $V^+$ = 5.5V<br>$V^+$ = 2.25V | ●<br>● | | 137<br>106 | 180<br>145 | µA<br>µA |
| | | $R_L = ∞$, $N_{DIV}$ = 128, $R_{SET}$ = 800k    $V^+$ = 5.5V<br>$V^+$ = 2.25V | ●<br>● | | 66<br>56 | 100<br>90 | µA<br>µA |

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. Test conditions are $V^+$ = 2.25V to 5.5V, OE = $V^+$, DIVCODE = 0 to 15 ($N_{DIV}$ = 1 to 128), $R_{SET}$ = 25k to 800k, $R_{LOAD}$ = ∞, $C_{LOAD}$ = 5pF unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Digital I/O** | | | | | | | |
| | OE Pin Input Capacitance | | | | 2.5 | | pF |
| | OE Pin Input Current | OE = 0V to $V^+$ | ● | | | ±10 | nA |
| $V_{IH}$ | High Level OE Pin Input Voltage | (Note 6) | ● | 0.7•$V^+$ | | | V |
| $V_{IL}$ | Low Level OE Pin Input Voltage | (Note 6) | ● | | | 0.3•$V^+$ | V |
| | OUT Pin Hi-Z Leakage | OE = 0V, DIVCODE ≥ 8, OUT = 0V to $V^+$ | | | | ±10 | µA |
| $I_{OUT(MAX)}$ | Maximum Output Current | | | | ±20 | | mA |
| $V_{OH}$ | High Level Output Voltage (Note 7) | $V^+$ = 5.5V | $I_{OH}$ = –1mA | ● | 5.45 | 5.48 | | V |
| | | | $I_{OH}$ = –16mA | ● | 4.84 | 5.15 | | V |
| | | $V^+$ = 3.3V | $I_{OH}$ = –1mA | ● | 3.24 | 3.27 | | V |
| | | | $I_{OH}$ = –10mA | ● | 2.75 | 2.99 | | V |
| | | $V^+$ = 2.25V | $I_{OH}$ = –1mA | ● | 2.17 | 2.21 | | V |
| | | | $I_{OH}$ = –8mA | ● | 1.58 | 1.88 | | V |
| $V_{OL}$ | Low Level Output Voltage (Note 7) | $V^+$ = 5.5V | $I_{OL}$ = 1mA | ● | | 0.02 | 0.04 | V |
| | | | $I_{OL}$ = 16mA | ● | | 0.26 | 0.54 | V |
| | | $V^+$ = 3.3V | $I_{OL}$ = 1mA | ● | | 0.03 | 0.05 | V |
| | | | $I_{OL}$ = 10mA | ● | | 0.22 | 0.46 | V |
| | | $V^+$ = 2.25V | $I_{OL}$ = 1mA | ● | | 0.03 | 0.07 | V |
| | | | $I_{OL}$ = 8mA | ● | | 0.26 | 0.54 | V |
| $t_{PD}$ | Output Disable Propagation Delay | $V^+$ = 5.5V | | | | 17 | | ns |
| | | $V^+$ = 3.3V | | | | 26 | | ns |
| | | $V^+$ = 2.25V | | | | 44 | | ns |
| $t_{ENABLE}$ | Output Enable Time | $N_{DIV}$ ≤ 2, $t_{OUT}$ = 1/$f_{OUT}$ | | | $t_{PD}$ to $t_{OUT}$ | | µs |
| | | $N_{DIV}$ ≥ 4, $t_{MASTER}$ = $t_{OUT}$/$N_{DIV}$ | | | $t_{PD}$ to 2•$t_{MASTER}$ | | µs |
| $t_r$ | Output Rise Time (Note 8) | $V^+$ = 5.5V | | | | 1.1 | | ns |
| | | $V^+$ = 3.3V | | | | 1.7 | | ns |
| | | $V^+$ = 2.25V | | | | 2.7 | | ns |
| $t_f$ | Output Fall Time (Note 8) | $V^+$ = 5.5V | | | | 1.0 | | ns |
| | | $V^+$ = 3.3V | | | | 1.6 | | ns |
| | | $V^+$ = 2.25V | | | | 2.4 | | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC6990C is guaranteed functional over the operating temperature range of –40°C to 85°C.

**Note 3:** The LTC6990C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6990C is designed, characterized and expected to meet specified performance from –40°C to 85°C but it is not tested or QA sampled at these temperatures. The LTC6990I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6990H is guaranteed to meet specified performance from –40°C to 125°C. The LTC6990MP is guaranteed to meet specified performance from –55°C to 125°C.

**Note 4:** Frequency accuracy is defined as the deviation from the $f_{OUT}$ equation, assuming $R_{SET}$ is used to program the frequency.

**Note 5:** See Operation section, Table 1 and Figure 2 for a full explanation of how the DIV pin voltage selects the value of DIVCODE.

**Note 6:** The OE pin has hysteresis to accommodate slow rising or falling signals. The threshold voltages are proportional to $V^+$. Typical values can be estimated at any supply voltage using $V_{OE(RISING)}$ ≈ 0.55 • $V^+$ + 185mV and $V_{OE(FALLING)}$ ≈ 0.48 • $V^+$ – 155mV.

**Note 7:** To conform to the Logic IC Standard, current out of a pin is arbitrarily given a negative value.

**Note 8:** Output rise and fall times are measured between the 10% and the 90% power supply levels with 5pF output load. These specifications are based on characterization.

**Note 9:** Settling time is the amount of time required for the output to settle within ±1% of the final frequency after a 0.5x or 2x change in $I_{SET}$.
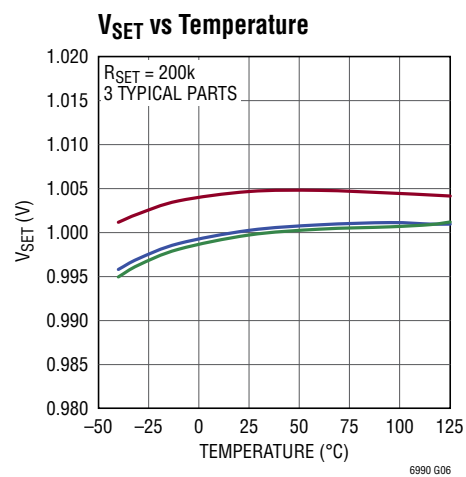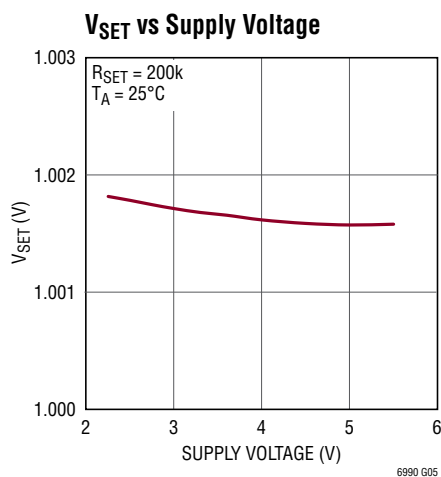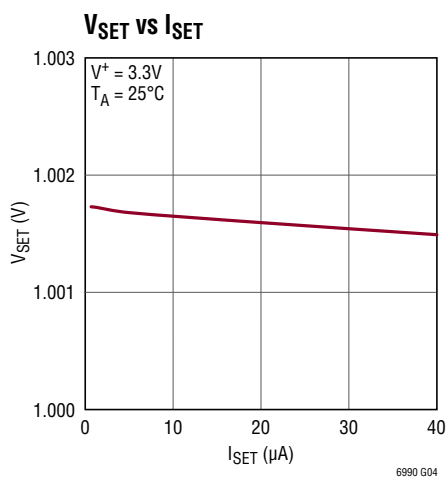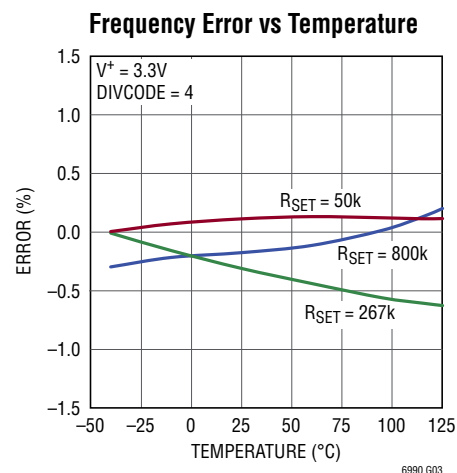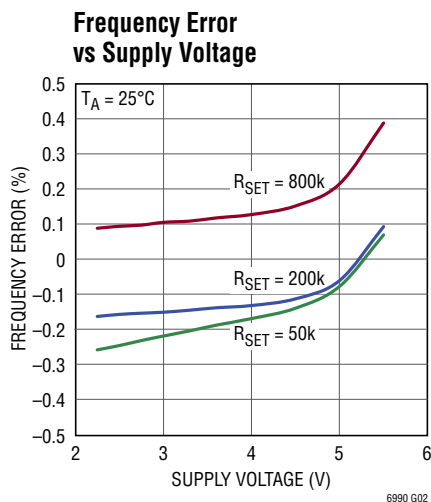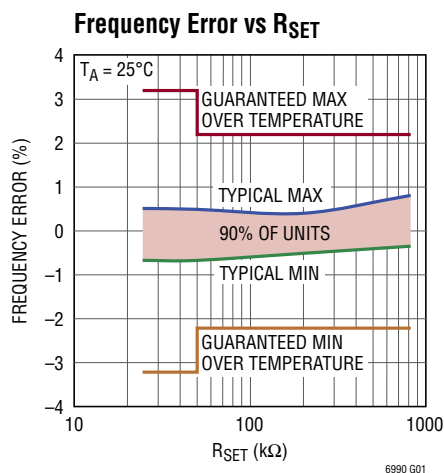
**Note 10:** Jitter is the ratio of the deviation of the period to the mean of the period. This specification is based on characterization and is not 100% tested.
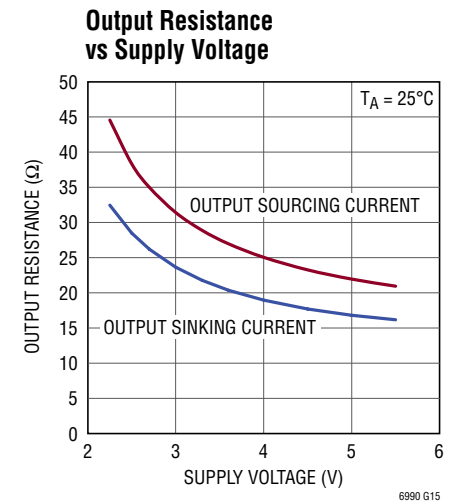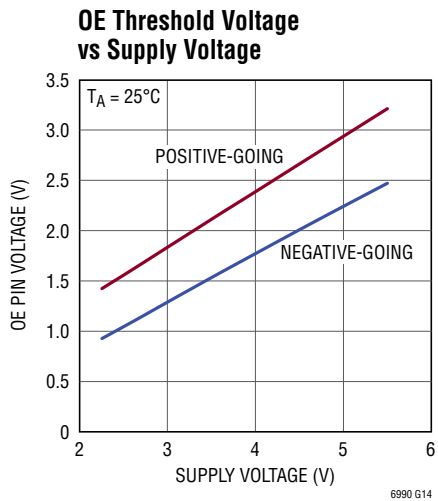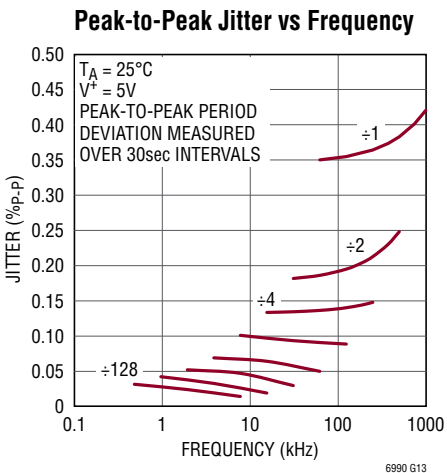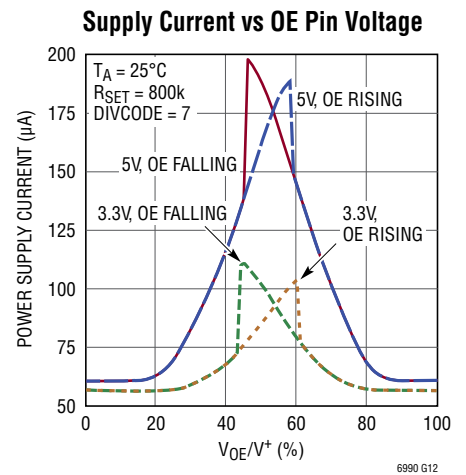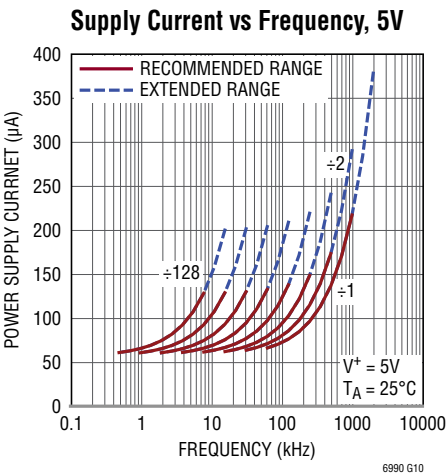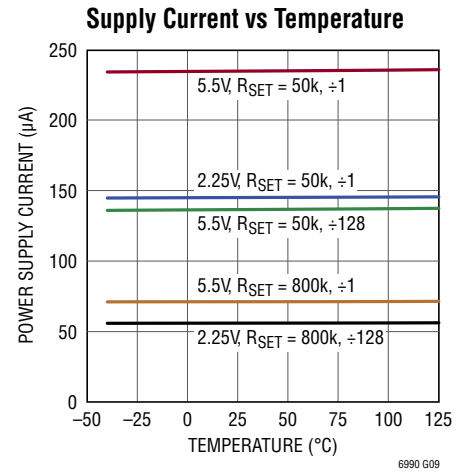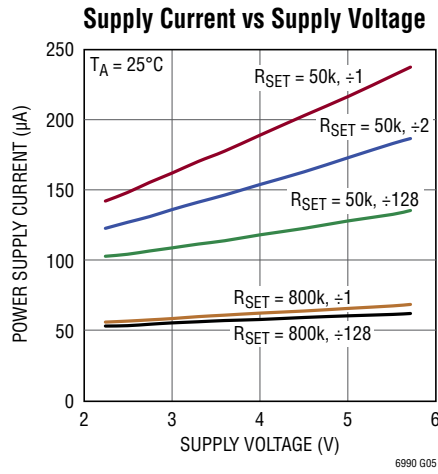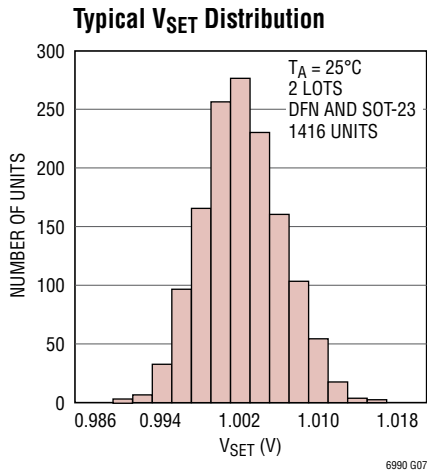
# ELECTRICAL CHARACTERISTICS

**Note 11:** Long-term drift of silicon oscillators is primarily due to the movement of ions and impurities within the silicon and is tested at 30°C under otherwise nominal operating conditions. Long-term drift is specified as ppm/√kHr due to the typically nonlinear nature of the drift. To calculate drift for a set time period, translate that time into thousands of hours, take the square root and multiply by the typical drift number. For instance, a year is 8.77kHr and would yield a drift of 266ppm at 90ppm/√kHr. Drift without power applied to the device may be approximated as 1/10th of the drift with power, or 9ppm/√kHr for a 90ppm/√kHr device.

# TYPICAL PERFORMANCE CHARACTERISTICS $V^+ = 3.3V$, unless otherwise noted.

**Frequency Error vs $R_{SET}$**

6990 G01

**Frequency Error vs Supply Voltage**

6990 G02

**Frequency Error vs Temperature**

6990 G03

**$V_{SET}$ vs $I_{SET}$**

6990 G04

**$V_{SET}$ vs Supply Voltage**

6990 G05

**$V_{SET}$ vs Temperature**

6990 G06

Rev. D

# TYPICAL PERFORMANCE CHARACTERISTICS $V^+ = 3V$, unless otherwise noted.

### Typical $V_{SET}$ Distribution



$T_A = 25°C$
2 LOTS
DFN AND SOT-23
1416 UNITS

NUMBER OF UNITS / $V_{SET}$ (V)

6990 G07

### Supply Current vs Supply Voltage



$T_A = 25°C$

$R_{SET} = 50k, \div1$
$R_{SET} = 50k, \div2$
$R_{SET} = 50k, \div128$
$R_{SET} = 800k, \div1$
$R_{SET} = 800k, \div128$

POWER SUPPLY CURRENT (µA) / SUPPLY VOLTAGE (V)

6990 G05

### Supply Current vs Temperature



5.5V, $R_{SET} = 50k, \div1$
2.25V, $R_{SET} = 50k, \div1$
5.5V, $R_{SET} = 50k, \div128$
5.5V, $R_{SET} = 800k, \div1$
2.25V, $R_{SET} = 800k, \div128$

POWER SUPPLY CURRENT (µA) / TEMPERATURE (°C)

6990 G09

### Supply Current vs Frequency, 5V



RECOMMENDED RANGE
EXTENDED RANGE

$\div2$
$\div128$
$\div1$

$V^+ = 5V$
$T_A = 25°C$

POWER SUPPLY CURRNET (µA) / FREQUENCY (kHz)

6990 G10

### Supply Current vs Frequency, 2.5V



RECOMMENDED RANGE
EXTENDED RANGE

$\div1$
$\div2$
$\div128$

$V^+ = 2.5V$
$T_A = 25°C$

POWER SUPPLY CURRNET (µA) / FREQUENCY (kHz)

6990 G11

### Supply Current vs OE Pin Voltage



$T_A = 25°C$
$R_{SET} = 800k$
DIVCODE = 7

5V, OE RISING
5V, OE FALLING
3.3V, OE FALLING
3.3V, OE RISING

POWER SUPPLY CURRENT (µA) / $V_{OE}/V^+$ (%)

6990 G12

### Peak-to-Peak Jitter vs Frequency



$T_A = 25°C$
$V^+ = 5V$
PEAK-TO-PEAK PERIOD
DEVIATION MEASURED
OVER 30sec INTERVALS

$\div1$
$\div2$
$\div4$
$\div128$

JITTER (%P-P) / FREQUENCY (kHz)

6990 G13

### OE Threshold Voltage vs Supply Voltage



$T_A = 25°C$

POSITIVE-GOING
NEGATIVE-GOING

OE PIN VOLTAGE (V) / SUPPLY VOLTAGE (V)

6990 G14

### Output Resistance vs Supply Voltage



$T_A = 25°C$

OUTPUT SOURCING CURRENT
OUTPUT SINKING CURRENT

OUTPUT RESISTANCE (Ω) / SUPPLY VOLTAGE (V)

6990 G15

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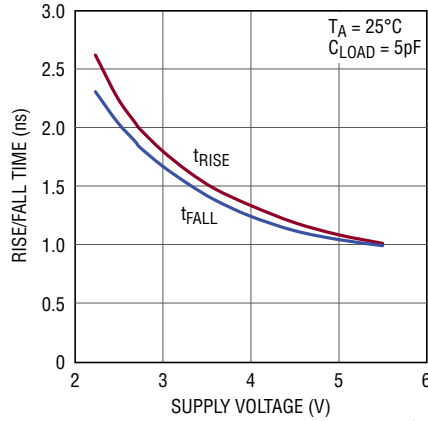# TYPICAL PERFORMANCE CHARACTERISTICS $V^+ = 3V$, unless otherwise noted.

**Typical Frequency Error vs Time (Long-Term Drift)**

65 UNITS
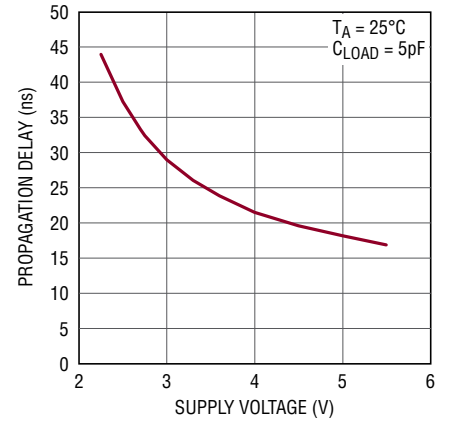SOT-23 AND DFN PARTS
$T_A = 30°C$
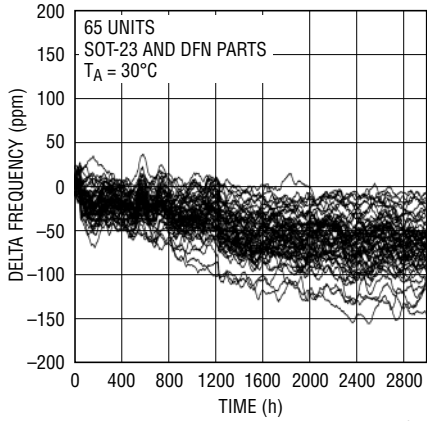
6990 G15a

**Rise and Fall Time vs Supply Voltage**

$T_A = 25°C$
$C_{LOAD} = 5pF$

$t_{RISE}$
$t_{FALL}$

6990 G16

**Output Disable Propagation Delay ($t_{PD}$) vs Supply Voltage**

$T_A = 25°C$
$C_{LOAD} = 5pF$

6990 G17

**Typical $I_{SET}$ Current Limit vs $V^+$**

$T_A = 25°C$
SET PIN SHORTED TO GND
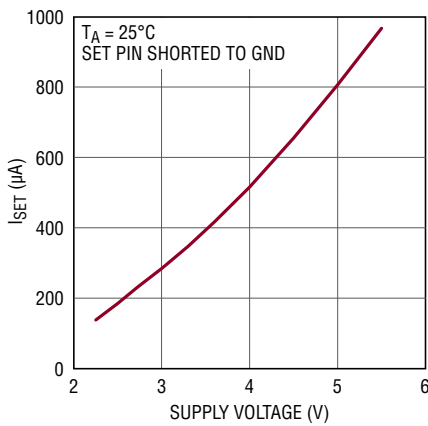
6990 G18

**Typical Output Waveform**

$V^+ = 3.3V$
DIVCODE = 2
$R_{SET} = 200k$

OE
2V/DIV

OUT
2V/DIV
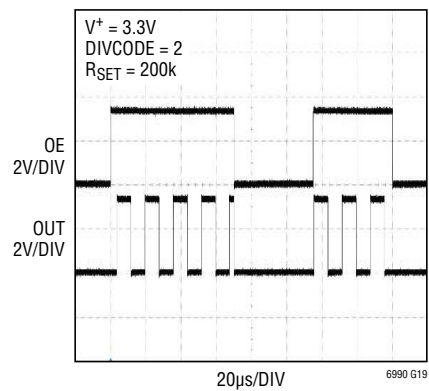
6990 G19

**Frequency Modulation**

$V_{CTRL}$
2V/DIV

OUT
2V/DIV

$f_{OUT}$
50kHz/DIV

20µs/DIV
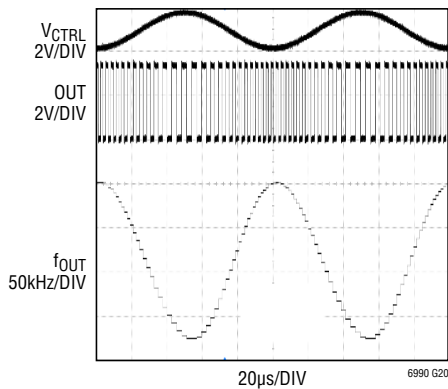
6990 G20

$V^+ = 3.3V$, DIVCODE = 0
$R_{SET} = 200k$, $R_{VCO} = 464k$
$f_{OUT} = 175kHz$ to $350kHz$

**Frequency Modulation**

$V_{CTRL}$
2V/DIV

OUT
2V/DIV

$f_{OUT}$
50kHz/DIV

20µs/DIV
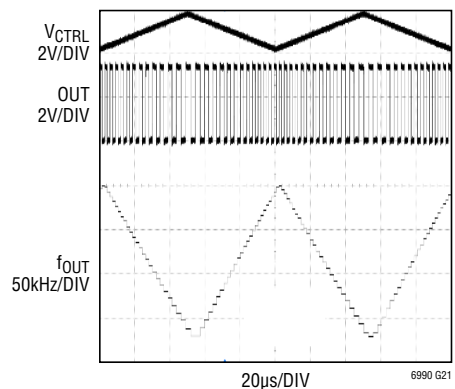
6990 G21

$V^+ = 3.3V$, DIVCODE = 0
$R_{SET} = 200k$, $R_{VCO} = 464k$
$f_{OUT} = 175kHz$ to $350kHz$

Rev. D

# PIN FUNCTIONS (DCB/S6)

**V⁺ (Pin 1/Pin 5):** Supply Voltage (2.25V to 5.5V). This supply must be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1µF capacitor.

**DIV (Pin 2/Pin 4):** Programmable Divider and Hi-Z Mode Input. A V⁺ referenced A/D converter monitors the DIV pin voltage ($V_{DIV}$) to determine a 4-bit result (DIVCODE). $V_{DIV}$ may be generated by a resistor divider between V⁺ and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that $V_{DIV}$ settles quickly. The MSB of DIVCODE (Hi-Z) determines the behavior of the output when OE is driven low. If Hi-Z = 0 the output is pulled low when disabled. If Hi-Z = 1 the output is placed in a high impedance condition when disabled.

**SET (Pin 3/Pin 3):** Frequency-Setting Input. The voltage on the SET pin ($V_{SET}$) is regulated to 1V above GND. The amount of current sourced from the SET pin ($I_{SET}$) programs the master oscillator frequency. The $I_{SET}$ current range is 1.25µA to 40µA. The output oscillation will stop if $I_{SET}$ drops below approximately 500nA. A resistor connected between SET and GND is the most accurate way to set the frequency. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less than 100pF maintains the stability of the feedback circuit regulating the $V_{SET}$ voltage.
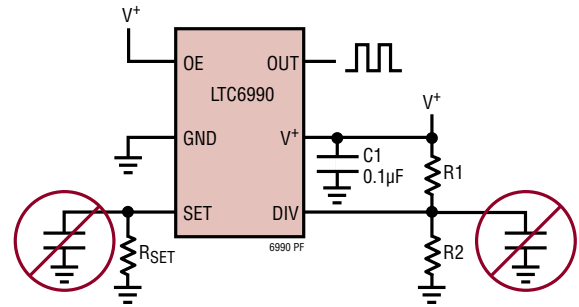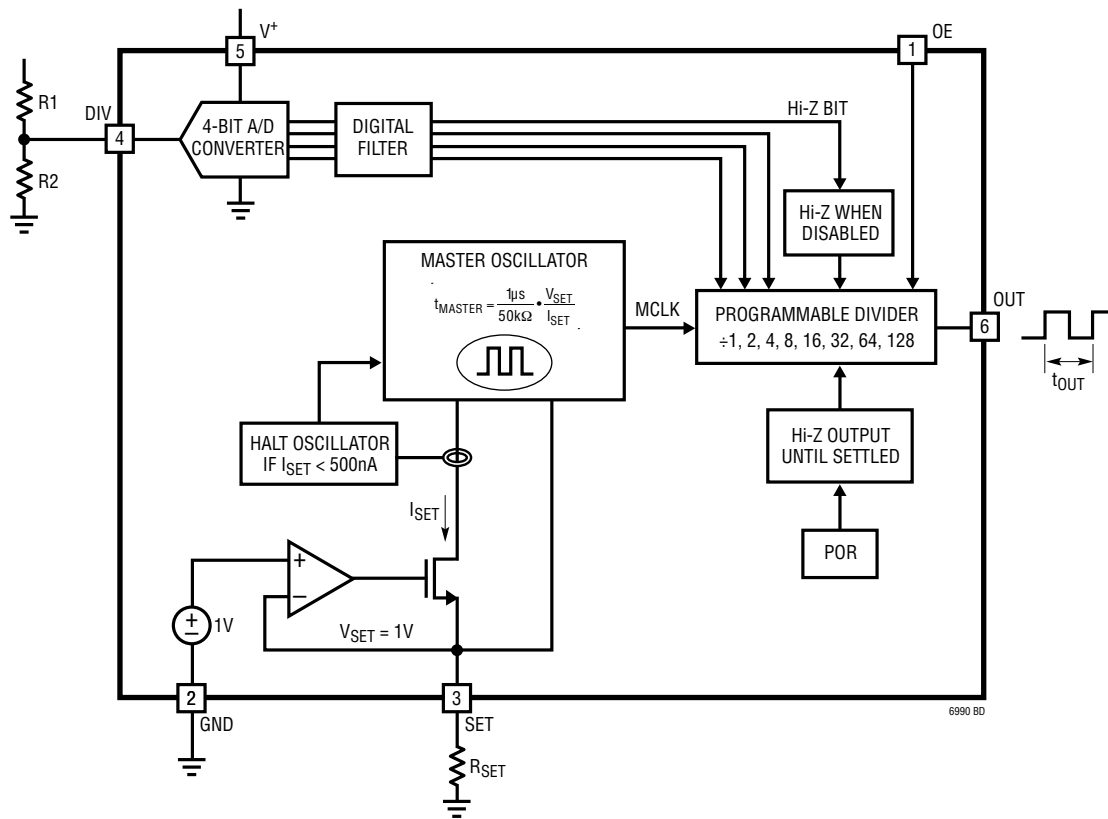


**OE (Pin 4/Pin 1):** Output Enable. Drive high to enable the output driver (Pin 6). Driving OE low disables the output asynchronously, so that the output is immediately forced low (Hi-Z = 0) or floated (Hi-Z = 1). When enabled, the output may temporarily remain low to synchronize with the internal oscillator in order to eliminate pulse slivers.

**GND (Pin 5/Pin 2):** Ground. Tie to a low inductance ground plane for best performance.

**OUT (Pin 6/Pin 6):** Oscillator Output. The OUT pin swings from GND to V⁺ with an output resistance of approximately 30Ω. When driving an LED or other low-impedance load a series output resistor should be used to limit source/sink current to 20mA.

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# BLOCK DIAGRAM  (S6 Package Pin Numbers Shown)



The master oscillator period is given by:

$$t_{MASTER} = \frac{1\mu s}{50k\Omega} \cdot \frac{V_{SET}}{I_{SET}}$$

$V_{SET} = 1V$

PROGRAMMABLE DIVIDER ÷1, 2, 4, 8, 16, 32, 64, 128

HALT OSCILLATOR IF $I_{SET}$ < 500nA

6990 BD

# OPERATION

The LTC6990 is built around a master oscillator with a 1MHz maximum frequency. The oscillator is controlled by the SET pin current ($I_{SET}$) and voltage ($V_{SET}$), with a 1MHz • 50k conversion factor that is accurate to ±0.8% under typical conditions.

$$f_{MASTER} = \frac{1}{t_{MASTER}} = 1MHz • 50k • \frac{I_{SET}}{V_{SET}}$$

A feedback loop maintains $V_{SET}$ at 1V ±30mV, leaving $I_{SET}$ as the primary means of controlling the output frequency. The simplest way to generate $I_{SET}$ is to connect a resistor ($R_{SET}$) between SET and GND, such that $I_{SET} = V_{SET}/R_{SET}$. The master oscillator equation reduces to:

$$f_{MASTER} = \frac{1}{t_{MASTER}} = \frac{1MHz • 50k}{R_{SET}}$$

From this equation it is clear that $V_{SET}$ drift will not affect the output frequency when using a single program resistor ($R_{SET}$). Error sources are limited to $R_{SET}$ tolerance and the inherent frequency accuracy $\Delta f_{OUT}$ of the LTC6990.

$R_{SET}$ values between 50k and 800k (equivalent to $I_{SET}$ between 1.25µA and 20µA) produce the best results, although $R_{SET}$ may be reduced to 25k ($I_{SET} = 40µA$) with reduced accuracy.

The LTC6990 includes a programmable frequency divider which can further divide the frequency by 1, 2, 4, 8, 16, 32, 64 or 128 before driving the OUT pin. The divider ratio $N_{DIV}$ is set by a resistor divider attached to the DIV pin.

$$f_{OUT} = \frac{1}{t_{OUT}} = \frac{1MHz • 50k}{N_{DIV}} • \frac{I_{SET}}{V_{SET}}$$

With $R_{SET}$ in place of $V_{SET}/I_{SET}$ the equation reduces to:

$$f_{OUT} = \frac{1}{t_{OUT}} = \frac{1MHz • 50k}{N_{DIV} • R_{SET}}$$

## DIVCODE

The DIV pin connects to an internal, V$^+$ referenced 4-bit A/D converter that monitors the DIV pin voltage ($V_{DIV}$) to determine the DIVCODE value. DIVCODE programs two settings on the LTC6990:

1. DIVCODE determines the output frequency divider setting, $N_{DIV}$.

2. DIVCODE determines the state of the output when disabled, via the Hi-Z bit.

$V_{DIV}$ may be generated by a resistor divider between V$^+$ and GND as shown in Figure 1.
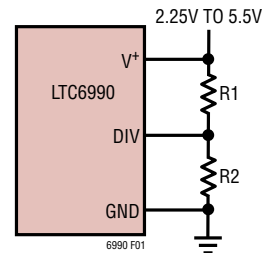


**Figure 1. Simple Technique for Setting DIVCODE**

# OPERATION

**Table 1. DIVCODE Programming**

| DIVCODE | Hi-Z | $N_{DIV}$ | Recommended $f_{OUT}$ | R1 (k) | R2 (k) | $V_{DIV}/V^+$ |
|---------|------|-----------|----------------------|--------|--------|---------------|
| 0 | 0 | 1 | 62.5kHz to 1MHz | Open | Short | $\leq 0.03125 \pm 0.015$ |
| 1 | 0 | 2 | 31.25kHz to 500kHz | 976 | 102 | $0.09375 \pm 0.015$ |
| 2 | 0 | 4 | 15.63kHz to 250kHz | 976 | 182 | $0.15625 \pm 0.015$ |
| 3 | 0 | 8 | 7.813kHz to 125kHz | 1000 | 280 | $0.21875 \pm 0.015$ |
| 4 | 0 | 16 | 3.906kHz to 62.5kHz | 1000 | 392 | $0.28125 \pm 0.015$ |
| 5 | 0 | 32 | 1.953kHz to 31.25kHz | 1000 | 523 | $0.34375 \pm 0.015$ |
| 6 | 0 | 64 | 976.6Hz to 15.63kHz | 1000 | 681 | $0.40625 \pm 0.015$ |
| 7 | 0 | 128 | 488.3Hz to 7.813kHz | 1000 | 887 | $0.46875 \pm 0.015$ |
| 8 | 1 | 128 | 488.3Hz to 7.813kHz | 887 | 1000 | $0.53125 \pm 0.015$ |
| 9 | 1 | 64 | 976.6Hz to 15.63kHz | 681 | 1000 | $0.59375 \pm 0.015$ |
| 10 | 1 | 32 | 1.953kHz to 31.25kHz | 523 | 1000 | $0.65625 \pm 0.015$ |
| 11 | 1 | 16 | 3.906kHz to 62.5kHz | 392 | 1000 | $0.71875 \pm 0.015$ |
| 12 | 1 | 8 | 7.813kHz to 125kHz | 280 | 1000 | $0.78125 \pm 0.015$ |
| 13 | 1 | 4 | 15.63kHz to 250kHz | 182 | 976 | $0.84375 \pm 0.015$ |
| 14 | 1 | 2 | 31.25kHz to 500kHz | 102 | 976 | $0.90625 \pm 0.015$ |
| 15 | 1 | 1 | 62.5kHz to 1MHz | Short | Open | $\geq 0.96875 \pm 0.015$ |

Table 1 offers recommended 1% resistor values that accurately produce the correct voltage division as well as the corresponding $N_{DIV}$ and Hi-Z values for the recommended resistor pairs. Other values may be used as long as:

1. The $V_{DIV}/V^+$ ratio is accurate to ±1.5% (including resistor tolerances and temperature effects)

2. The driving impedance (R1||R2) does not exceed 500kΩ.

If the voltage is generated by other means (i.e. the output of a DAC) it must track the $V^+$ supply voltage. The last column in Table 1 shows the ideal ratio of $V_{DIV}$ to the supply voltage, which can also be calculated as:

$$\frac{V_{DIV}}{V^+} = \frac{DIVCODE + 0.5}{16} \pm 1.5\%$$

For example, if the supply is 3.3V and the desired DIVCODE is 4, $V_{DIV} = 0.281 \cdot 3.3V = 928mV \pm 50mV$.

Figure 2 illustrates the information in Table 1, showing that $N_{DIV}$ is symmetric around the DIVCODE midpoint.

On start-up, the DIV pin A/D converter must determine the correct DIVCODE before the output is enabled. If $V_{DIV}$
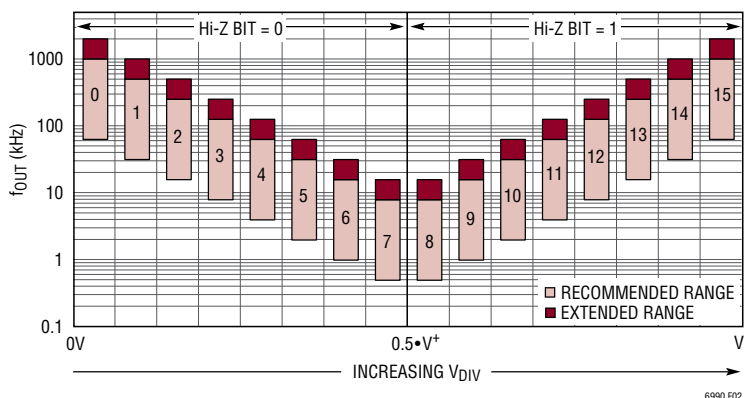


**Figure 2. Frequency Range and Hi-Z Bit vs DIVCODE**

# OPERATION

is not stable, it will increase the start-up time as the converter waits for a stable result. Therefore, capacitance on the DIV pin should be minimized so it will settle quickly. Less than 100pF will not affect performance.

## Output Enable

The OE pin controls the state of the LTC6990's output as seen on the OUT pin. Pulling the OE pin high enables the oscillator output. Pulling it low disables the output. When the output is disabled, it is either held low or placed in a high impedance state as dictated by the Hi-Z bit value (determined by the DIVCODE as described earlier). Table 2 summarizes the output control states.

**Table 2. Output States**

| OE Pin | Hi-Z | OUT |
|--------|------|-----|
| 1 | X | Enabled, Output is Active |
| 0 | 1 | Disabled, Output is Hi-Z |
| 0 | 0 | Disabled, Output is Held Low |

Figure 3 illustrates the timing for the OE function when Hi-Z = 0. When OE is low, the output is disabled and OUT is held low. Bringing OE high enables the output after a delay, $t_{ENABLE}$, which synchronizes the enable to eliminate sliver pulses and guarantee the correct width for the first pulse. If $N_{DIV}$ = 1 or 2 this delay will be no longer than the output period, $t_{OUT}$. If $N_{DIV}$ > 2 the delay is limited to twice the internal master oscillator period (or 2 • $t_{MASTER}$). Forcing OE low will bring OUT low after a propagation delay, $t_{PD}$. If the output is high when OE falls, the output pulse will be truncated.

As shown in Figure 4, setting Hi-Z = 1 places the output in a high-impedance state when OE = 0. This feature allows for "wired-OR" connections of multiple devices. Driving OE high enables the output. The output will usually be forced low during this time, although it is possible for OUT to transition directly from high-impedance to a high output, depending on the timing of the OE transition relative to the internal oscillator. Once high, the first output pulse will have the correct width (unless truncated by bringing OE low again).
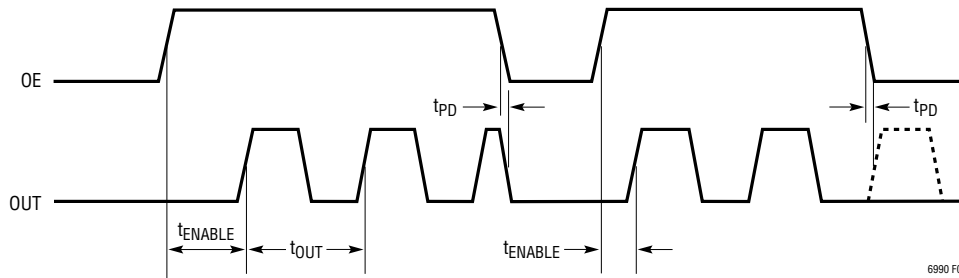


**Figure 3. OE Timing Diagram (Hi-Z = 0)**
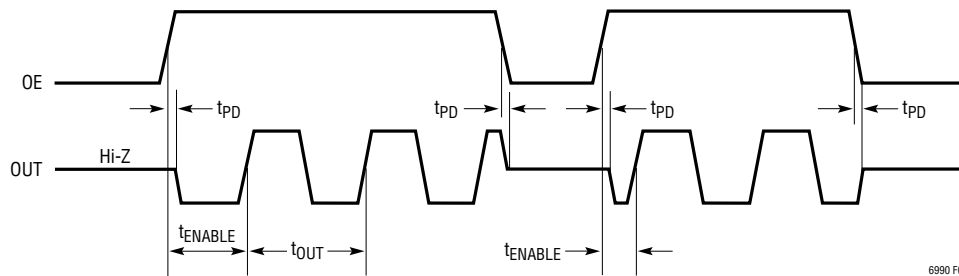


**Figure 4. OE Timing Diagram (Hi-Z = 1)**

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# OPERATION

### Changing DIVCODE After Start-Up

Following start-up, the A/D converter will continue monitoring $V_{DIV}$ for changes. Changes to DIVCODE will be recognized slowly, as the LTC6990 places a priority on eliminating any "wandering" in the DIVCODE. The typical delay depends on the difference between the old and new DIVCODE settings and is proportional to the master oscillator period.

$$t_{DIVCODE} = 16 \bullet (\Delta DIVCODE + 6) \bullet t_{MASTER}$$

A change in DIVCODE will not be recognized until it is stable, and will not pass through intermediate codes. A digital filter is used to guarantee the DIVCODE has settled to a new value before making changes to the output. Then the output will make a clean (glitchless) transition to the new divider setting.

### Start-Up Time

When power is first applied to the LTC6990 the power-on reset (POR) circuit will initiate the start-up time, $t_{START}$. The OUT pin is floated (high-impedance) during this time. The typical value for $t_{START}$ ranges from 0.5ms to 8ms depending on the master oscillator frequency (independent of $N_{DIV}$):

$$t_{START(TYP)} = 500 \bullet t_{MASTER}$$

The start-up time may be longer if the supply or DIV pin voltages are not stable. For this reason, it is recommended to minimize the capacitance on the DIV pin so it will properly track $V^+$.
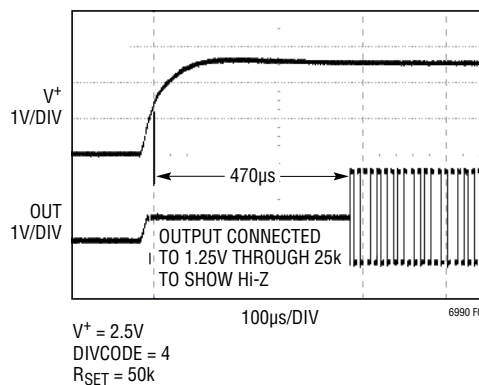
DIV
1V/DIV

576µs

OUT
1V/DIV

100µs/DIV

6990 F05

$V^+$ = 3.3V
$R_{SET}$ = 200k

**Figure 5. DIVCODE Change from 5 to 2**

$V^+$
1V/DIV

470µs

OUT
1V/DIV

OUTPUT CONNECTED
TO 1.25V THROUGH 25k
TO SHOW Hi-Z

100µs/DIV

6990 F06

$V^+$ = 2.5V
DIVCODE = 4
$R_{SET}$ = 50k

**Figure 6. Typical Start-Up**
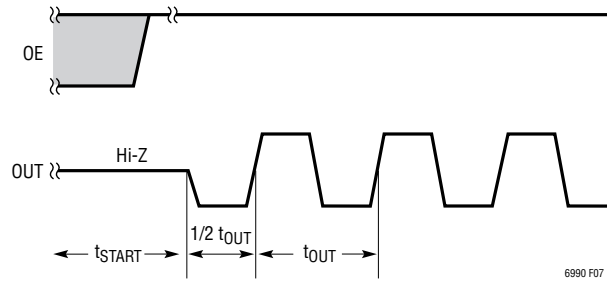
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# APPLICATIONS INFORMATION



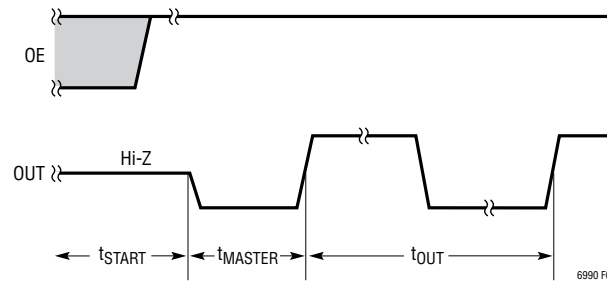**Figure 7. Start-Up Timing Diagram (OE = 1, $N_{DIV}$ = 1 or 2, Hi-Z = 0 or 1)**



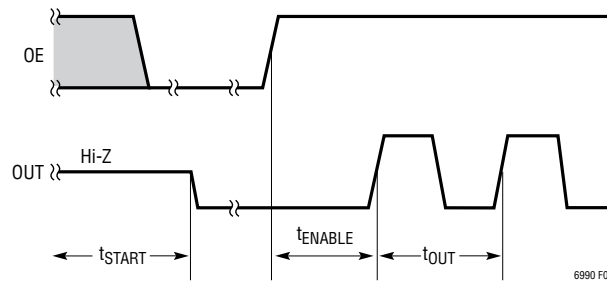**Figure 8. Start-Up Timing Diagram (OE = 1, $N_{DIV} \geq 4$, Hi-Z = 0 or 1)**



**Figure 9. Start-Up Timing Diagram (OE = 0, $N_{DIV}$ = Any, Hi-Z = 0)**
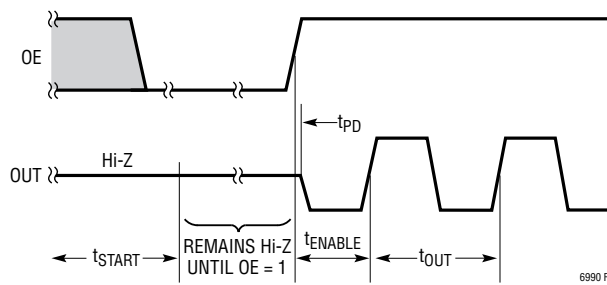


**Figure 10. Start-Up Timing Diagram (OE = 0, $N_{DIV}$ = Any, Hi-Z = 1)**

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# APPLICATIONS INFORMATION

### Start-Up Behavior

When first powered up, the output is high impedance. If the output is enabled (OE = 1) at the end of the start-up time, the output will go low for one $t_{MASTER}$ cycle (or half a $t_{OUT}$ cycle if $N_{DIV} < 4$) before the first rising edge. If the output is disabled (OE = 0) at the end of the start-up time, the output will drop to a low output if the Hi-Z bit = 0, or simply remain floating if Hi-Z = 1.

### Basic Fixed Frequency Operation

The simplest and most accurate method to program the LTC6990 for fixed frequency operation is to use a single resistor, $R_{SET}$, between the SET and GND pins. The design procedure is a simple two step process. First select the $N_{DIV}$ value and then calculate the value for the $R_{SET}$ resistor.

Alternatively, Analog Devices offers the easy to use TimerBlox Designer tool to quickly design any LTC6990 based circuit. Use the free TimerBlox LTC6990: Voltage Controlled Oscillator Web-Based Design Tool.

### Step 1: Selecting the $N_{DIV}$ Frequency Divider Value

As explained earlier, the voltage on the DIV pin sets the DIVCODE which determines both the Hi-Z bit and the $N_{DIV}$ value. For a given output frequency, $N_{DIV}$ should be selected to be within the following range.

$$\frac{62.5\,kHz}{f_{OUT}} \le N_{DIV} \le \frac{1MHz}{f_{OUT}} \tag{1a}$$

To minimize supply current, choose the lowest $N_{DIV}$ value (generally recommended). For faster start-up or decreased jitter, choose a higher $N_{DIV}$ setting. Alternatively, use Table 1 as a guide to select the best $N_{DIV}$ value for the given application. After choosing the value for $N_{DIV}$, use Table 1 to select the proper resistor divider or $V_{DIV}/V^+$ ratio to apply to the DIV pin.

### Step 2: Calculate and Select $R_{SET}$

The final step is to calculate the correct value for $R_{SET}$ using the following equation.

$$R_{SET} = \frac{1MHz \cdot 50k}{N_{DIV} \cdot f_{OUT}} \tag{1b}$$

Select the standard resistor value closest to the calculated value.

### Example: Design a 20kHz Oscillator with Minimum Power Consumption

### Step 1: Selecting the $N_{DIV}$ Frequency Divider Value

First, choose an $N_{DIV}$ value that meets the requirements of Equation (1a).

$$3.125 \le N_{DIV} \le 50$$

Potential settings for $N_{DIV}$ include 4, 8, 16, and 32. $N_{DIV}$ = 4 is the best choice, as it minimizes supply current by using a large $R_{SET}$ resistor. Using Table 1, choose the R1 and R2 values to program DIVCODE to either 2 or 13, depending on the desired behavior when the output is disabled.

### Step 2: Select $R_{SET}$

Calculate the correct value for $R_{SET}$ using Equation (1b).

$$R_{SET} = \frac{1MHz \cdot 50k}{4 \cdot 20kHz} = 625k$$

Since 625k is not available as a standard 1% resistor, substitute 619k if a 0.97% frequency shift is acceptable. Otherwise, select a parallel or series pair of resistors such as 309k and 316k to attain a more precise resistance.

# APPLICATIONS INFORMATION

**Frequency Modulated Operation (Voltage-Controlled Oscillator)**

Operating the LTC6990 as a voltage-controlled oscillator in its simplest form is achieved with one additional resistor. As shown in Figure 11, voltage $V_{CTRL}$ sources/sinks a current through $R_{VCO}$ to vary the $I_{SET}$ current, which in turn modulates the output frequency as described in Equation (2).

$$f_{OUT} = \frac{1MHz \cdot 50k}{N_{DIV} \cdot R_{VCO}} \cdot \left(1 + \frac{R_{VCO}}{R_{SET}} - \frac{V_{CTRL}}{V_{SET}}\right) \quad (2)$$
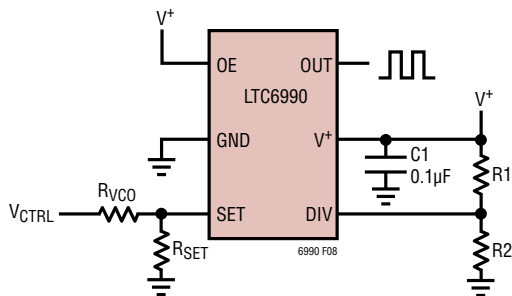


**Figure 11. Voltage Controlled Oscillator**

Equation (2) can be re-written as shown below, where $f_{(0V)}$ is the output frequency when $V_{CTRL} = 0V$, and $K_{VCO}$ is the frequency gain. Note that the gain is negative (the output frequency decreases as $V_{CTRL}$ increases).

$$f_{OUT} = f_{(0V)} - K_{VCO} \cdot V_{CTRL}$$

$$f_{(0V)} = \frac{1MHz \cdot 50k}{N_{DIV} \cdot (R_{SET} \| R_{VCO})}$$

$$K_{VCO} = \frac{1MHz \cdot 50k}{N_{DIV} \cdot V_{SET} \cdot R_{VCO}}$$

The design procedure for a VCO is a simple four step process. First select the $N_{DIV}$ value. Then calculate the intermediate values $K_{VCO}$ and $f_{(0V)}$. Next, calculate and select the $R_{VCO}$ resistor. Finally calculate and select the $R_{SET}$ resistor.

**Step 1: Select the $N_{DIV}$ Frequency Divider Value**

For best accuracy, the master oscillator frequency should fall between 62.5kHz and 1MHz. Since $f_{MASTER} = N_{DIV} \cdot$

$f_{OUT}$, choose a value for $N_{DIV}$ that meets the following conditions

$$\frac{62.5kHz}{f_{OUT(MIN)}} \leq N_{DIV} \leq \frac{1MHz}{f_{OUT(MAX)}} \quad (3a)$$

The 16:1 frequency range of the master oscillator and the 2:1 divider step-size provides several overlapping frequency spans to guarantee that any 8:1 modulation range can be covered by a single $N_{DIV}$ setting. $R_{VCO}$ allows the gain to be tailored to the application, mapping the $V_{CTRL}$ voltage range to the modulation range.

**Step 2: Calculate $K_{VCO}$ and $f_{(0V)}$**

$K_{VCO}$ and $f_{(0V)}$ define the VCO's transfer function and simplify the calculation of the the $R_{VCO}$ and $R_{SET}$ resistors. Calculate these parameters using the following equations.

$$K_{VCO} = \frac{f_{OUT(MAX)} - f_{OUT(MIN)}}{V_{CTRL(MAX)} - V_{CTRL(MIN)}} \quad (3b)$$

$$f_{(0V)} = f_{OUT(MAX)} + K_{VCO} \cdot V_{CTRL(MIN)} \quad (3c)$$

$K_{VCO}$ and $f_{(0V)}$ are not device settings or resistor values themselves. However, beyond their utility for the resistor calculations, these parameters provide a useful and intuitive way to look at the VCO application. The $f_{(0V)}$ parameter is the output frequency when $V_{CTRL}$ is at 0V. Viewed another way, it is the fixed output frequency when the $R_{VCO}$ and $R_{SET}$ resistors are in parallel. $K_{VCO}$ is actually the frequency gain of the circuit.

With $K_{VCO}$ and $f_{(0V)}$ determined, the $R_{VCO}$ and $R_{SET}$ values can now be calculated.

**Step 3: Calculate and Select $R_{VCO}$**

The next step is to calculate the correct value for $R_{VCO}$ using the following equation.

$$R_{VCO} = \frac{1MHz \cdot 50k}{N_{DIV} \cdot V_{SET} \cdot K_{VCO}} \quad (3d)$$

Select the standard resistor value closest to the calculated value.

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# APPLICATIONS INFORMATION

### Step 4: Calculate and Select $R_{SET}$

The final step is to calculate the correct value for $R_{SET}$ using the following equation:

$$R_{SET} = \frac{1MHz \cdot 50k}{N_{DIV} \cdot \left( f_{(0V)} - V_{SET} \cdot K_{VCO} \right)} \qquad (3e)$$

Select the standard resistor value closest to the calculated value.

Some applications require combinations of $f_{OUT(MIN)}$, $f_{OUT(MAX)}$, $V_{CTRL(MIN)}$ and $V_{CTRL(MAX)}$ that are not achievable. These applications result in unrealistic or unrealizable (e.g. negative value) resistors. These applications will require preconditioning of the $V_{CTRL}$ signal via range scaling and/or level shifting to place the $V_{CTRL}$ into a range that yields realistic resistor values.

### Frequency Error in VCO Applications Due to $V_{SET}$ Error

As stated earlier, $f_{(0V)}$ represents the frequency for $V_{CTRL}$ = 0V, which is the same value as would be generated by a single resistor between SET and GND with a value of $R_{SET} \| R_{VCO}$. Therefore, $f_{(0V)}$ is not affected by error or drift in $V_{SET}$ (i.e. $\Delta V_{SET}$ adds no frequency error when $V_{CTRL}$ = 0V).

The accuracy of $K_{VCO}$ *does* depend on $V_{SET}$ because the output frequency is controlled by the ratio of $V_{CTRL}$ to $V_{SET}$. The frequency error (in Hertz) due to $\Delta V_{SET}$ is approximated by:

$$\Delta f_{OUT} \cong K_{VCO} \cdot V_{CTRL} \cdot \frac{\Delta V_{SET}}{V_{SET}}$$

As the equation indicates, the potential for error in output frequency due to $V_{SET}$ error increases with $K_{VCO}$ and is at its largest when $V_{CTRL}$ is at its maximum. Recall that when $V_{CTRL}$ is at its maximum, the output frequency is at its minimum. With the maximum absolute frequency error (in Hertz) occurring at the lowest output frequency, the relative frequency error (in percent) can be significant.

$V_{SET}$ is nominally 1.0V with a maximum error of ±30mV for at most a ±3% error term. However, this ±3% potential error term is multiplied by both $V_{CTRL}$ and $K_{VCO}$. Wide

frequency range applications (high $K_{VCO}$) can have frequency errors greater than ±50% at the highest $V_{CTRL}$ voltage (lowest $f_{OUT}$). For this reason the simple, two resistor VCO circuit must be used with caution for applications where the frequency range is greater than 4:1. Restricting the range to 4:1 typically keeps the frequency error due to $V_{SET}$ variation below 10%.

For wide frequency range applications, the non-inverting VCO circuit shown in Figure 13 is preferred because the maximum frequency error occurs when the frequency is highest, keeping the relative error (in percent) much smaller.
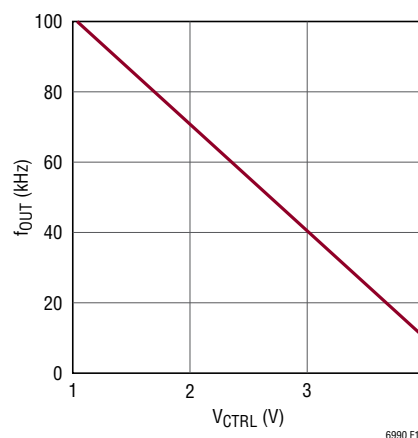


**Figure 12. VCO Transfer Function**

### Example: Design a VCO with the Following Parameters

$f_{OUT(MAX)}$ = 100kHz at $V_{CTRL(MIN)}$ = 1V

$f_{OUT(MIN)}$ = 10kHz at $V_{CTRL(MAX)}$ = 4V

### Step 1: Select the $N_{DIV}$ Value

First, choose an $N_{DIV}$ that meets the requirements of Equation (3a).

$6.25 \le N_{DIV} \le 10$

The application's desired frequency range is 10:1, which isn't always possible. However, in this case $N_{DIV}$ = 8 meets both requirements of Equation (3).

# APPLICATIONS INFORMATION

**Step 2: Calculate K$_{VCO}$ and f$_{(0V)}$**

Next, calculate the intermediate values K$_{VCO}$ and f$_{(0V)}$ using Equations (3b) and (3c).

$$K_{VCO} = \frac{100kHz - 10kHz}{4V - 1V} = 30kHz/V$$

$$f_{(0V)} = 100kHz + 30kHz/V \cdot 1V = 130kHz$$

**Step 3: Calculate and Select R$_{VCO}$**

The next step is to use Equation (3d) to calculate the correct value for R$_{VCO}$.

$$R_{VCO} = \frac{1MHz \cdot 50k}{8 \cdot 1V \cdot 30kHz/V} = 208.333k$$

Select R$_{VCO}$ = 210k.

**Step 4: Calculate and Select R$_{SET}$**

The final step is to calculate the correct value for R$_{SET}$ using Equation (3e).

$$R_{SET} = \frac{1MHz \cdot 50k}{8 \cdot (130kHz - 1V \cdot 30kHz/V)} = 62.5k$$

Select R$_{SET}$ = 61.9k

In this design example, with its wide 10:1 frequency range, the potential output frequency error due to V$_{SET}$ error alone ranges from less than ±1% when V$_{CTRL}$ is at its minimum up to ±36% when V$_{CTRL}$ is at its maximum. This error must be accounted for in the system design.

Depending on the application's requirements, the non-inverting VCO circuit in Figure 13 may be preferred for this wide of a frequency variation as its maximum inaccuracy due to V$_{SET}$ error is only ±9% and can be reduced to only ±3% with a small change to the voltage tuning range specification.

### Reducing V$_{SET}$ Error Effects in VCO Applications

Figure 13 shows a VCO that reduces the effect of $\Delta V_{SET}$ by adding an op-amp to make V$_{CTRL}$ dependent on V$_{SET}$. This circuit also has a positive transfer function (the output frequency increases as V$_{IN}$ increases). Furthermore, for positive V$_{IN}$ voltages, this circuit places the greatest absolute frequency error at the highest output frequency. Compared to the simple VCO circuit of Figure 11, the absolute frequency error is unchanged. However, with the maximum absolute frequency error (in Hertz) now occurring at the highest output frequency, the relative frequency error (in percent) is greatly improved.
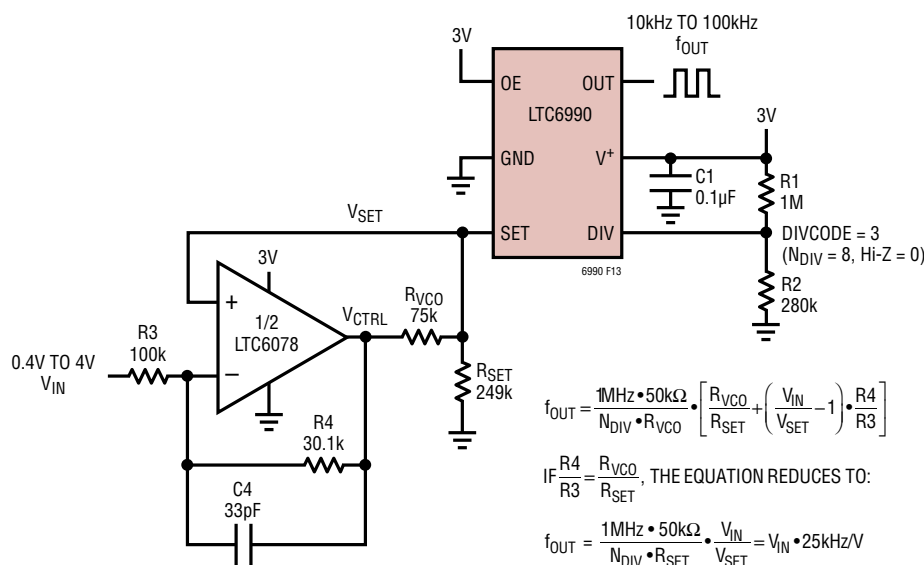


$$f_{OUT} = \frac{1MHz \cdot 50k\Omega}{N_{DIV} \cdot R_{VCO}} \cdot \left[ \frac{R_{VCO}}{R_{SET}} + \left( \frac{V_{IN}}{V_{SET}} - 1 \right) \cdot \frac{R4}{R3} \right]$$

IF $\frac{R4}{R3} = \frac{R_{VCO}}{R_{SET}}$, THE EQUATION REDUCES TO:

$$f_{OUT} = \frac{1MHz \cdot 50k\Omega}{N_{DIV} \cdot R_{SET}} \cdot \frac{V_{IN}}{V_{SET}} = V_{IN} \cdot 25kHz/V$$

**Figure 13. VCO with Reduced $\Delta$V$_{SET}$ Sensitivity**

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# APPLICATIONS INFORMATION

Additionally, by choosing the VCO's specifications shrewdly, the frequency error (in percent) due to $V_{SET}$ variation is reduced to $\Delta V_{SET}/V_{SET} = \pm 3\%$. To realize this improvement, the design must abide by three conditions. First, the $V_{IN}$ voltage must be positive throughout the range. Second, choose $V_{MAX}/V_{MIN} \geq f_{MAX}/f_{MIN}$. Last, choose $R_{VCO}/R_{SET} \geq R4/R3$.

Figure 13 shows a design similar to the previous design example where the $V_{MIN}$ voltage is now specified to be 0.4V. This satisfies the $V_{MAX}/V_{MIN} \geq f_{MAX}/f_{MIN}$ condition and the design assures that the output frequency error due to $V_{SET}$ variation is only $\pm 3\%$.

## Eliminating $V_{SET}$ Error Effects with DAC Frequency Control

Many DACs allow for the use of an external reference. If such a DAC is used to provide the $V_{CTRL}$ voltage, the $V_{SET}$ error is eliminated by buffering $V_{SET}$ and using it as the DAC's reference voltage, as shown in Figure 14. The DAC's output voltage now tracks any $V_{SET}$ variation and eliminates it as an error source. The SET pin cannot be tied directly to the reference input of the DAC because the current drawn by the DAC's REF input would affect the frequency.

## $I_{SET}$ Extremes (Master Oscillator Frequency Extremes)

Pushing $I_{SET}$ outside of the recommended 1.25µA to 20µA range forces the master oscillator to operate outside of the 62.5kHz to 1MHz range in which it is most accurate. The oscillator will still function with reduced accuracy in its extended range (see the Electrical Characteristics section).

The LTC6990 is designed to function normally for $I_{SET}$ as low as 1.25µA. At approximately 500nA, the oscillator output will be frozen in its current state. For $N_{DIV} = 1$ or 2, OUT will halt in a low state. But for larger divider ratios, it could halt in a high or low state. This avoids introducing short pulses while modulating a very low frequency output. Note that the output will not be *disabled* as when OE is low (e.g. the output will not enter a high impedance state if Hi-Z = 1).

At the other extreme, the master oscillator frequency can reach 2MHz for $I_{SET} = 40$µA ($R_{SET} = 25$k). It is not recommended to operate the master oscillator beyond 2MHz because the accuracy of the DIV pin ADC will suffer.



$$f_{OUT} = \frac{1\text{MHz} \cdot 50\text{k}\Omega}{N_{DIV} \cdot R_{VCO}} \cdot \left(1 + \frac{R_{VCO}}{R_{SET}} - \frac{D_{IN}}{4096}\right)$$
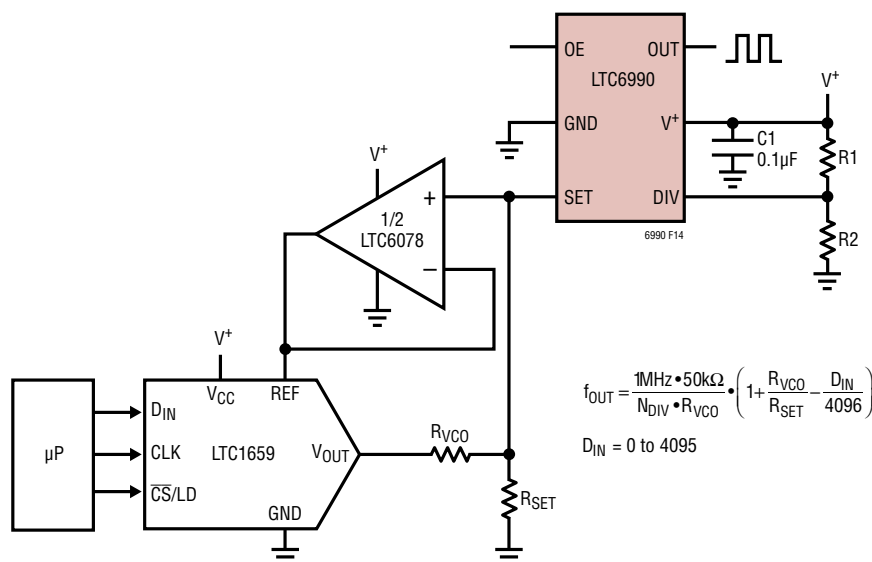
$D_{IN} = 0$ to 4095

**Figure 14. Digitally Controlled Oscillator with $V_{SET}$ Variation Eliminated**

# APPLICATIONS INFORMATION

### Modulation Bandwidth and Settling Time

The LTC6990 will respond to changes in $I_{SET}$ up to a −3dB bandwidth of $0.4 \cdot f_{OUT}$ (see Figure 15). This makes it easy to stabilize a feedback loop around the LTC6990, since it does not introduce a low-frequency pole.

Settling time depends on the master oscillator frequency. Following a 2x or 0.5x step change in $I_{SET}$, the output frequency takes approximately six master clock cycles ($6 \cdot t_{MASTER}$) to settle to within 1% of the final value. An example is shown in Figure 16.
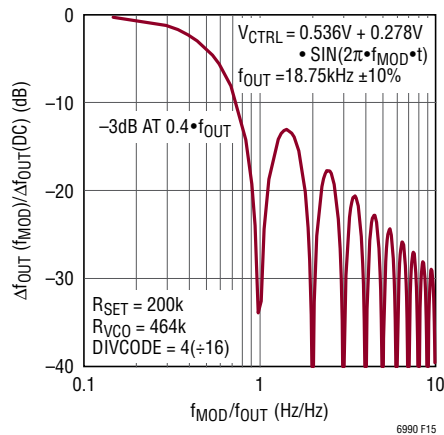


**Figure 15. Modulation Frequency Response**

### Power Supply Current

The power supply current varies with frequency, supply voltage and output loading. It can be estimated under any condition using the following equation:

$$I_{S(TYP)} \approx V^+ \bullet f_{MASTER} \bullet 7pF + V^+ \bullet f_{OUT} \bullet (13pF + C_{LOAD})$$

$$+ \frac{V^+}{480k\Omega} + \frac{V^+}{2 \bullet R_{LOAD}} + 1.75 \bullet I_{SET} + 50\mu A$$

The equation is also valid for OE = 0 (output disabled), with $f_{OUT} = 0Hz$.
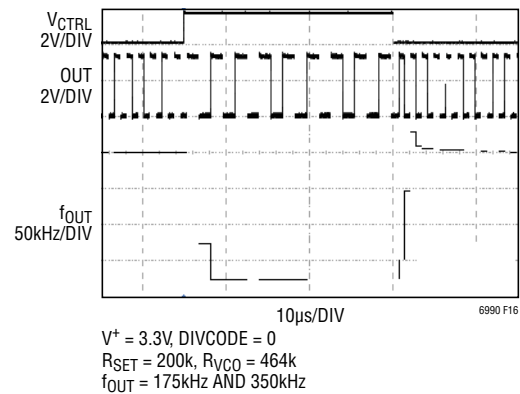


**Figure 16. Settling Time**

# APPLICATIONS INFORMATION

## SUPPLY BYPASSING AND PCB LAYOUT GUIDELINES

The LTC6990 is a 2.2% accurate silicon oscillator when used in the appropriate manner. The part is simple to use and by following a few rules, the expected performance is easily achieved. The most important use issues involve adequate supply bypassing and proper PCB layout.

Figure 17 shows example PCB layouts for both the SOT-23 and DCB packages using 0603 sized passive components. The layouts assume a two layer board with a ground plane layer beneath and around the LTC6990. These layouts are a guide and need not be followed exactly.

1. Connect the bypass capacitor, C1, directly to the V$^+$ and GND pins using a low inductance path. The connection from C1 to the V$^+$ pin is easily done directly on the top layer. For the DCB package, C1's connection to GND is also simply done on the top layer. For the SOT-23, OUT can be routed through the C1 pads to allow a good C1 GND connection. If the PCB design rules do not allow that, C1's GND connection can be accomplished through multiple vias to the ground plane. Multiple vias for both the GND pin connection to the ground

plane and the C1 connection to the ground plane are recommended to minimize the inductance. Capacitor C1 should be a 0.1µF ceramic capacitor.

2. Place all passive components on the top side of the board. This minimizes trace inductance.

3. Place R$_{SET}$ as close as possible to the SET pin and make a direct, short connection. The SET pin is a current summing node and currents injected into this pin directly modulate the operating frequency. Having a short connection minimizes the exposure to signal pickup.

4. Connect R$_{SET}$ directly to the GND pin. Using a long path or vias to the ground plane will not have a significant affect on accuracy, but the direct, short connection is recommended and easy to apply.

5. Use a ground trace to shield the SET pin. This provides another layer of protection from radiated signals.

6. Place R1 and R2 close to the DIV pin. A direct, short connection to the DIV pin minimizes the external signal coupling.
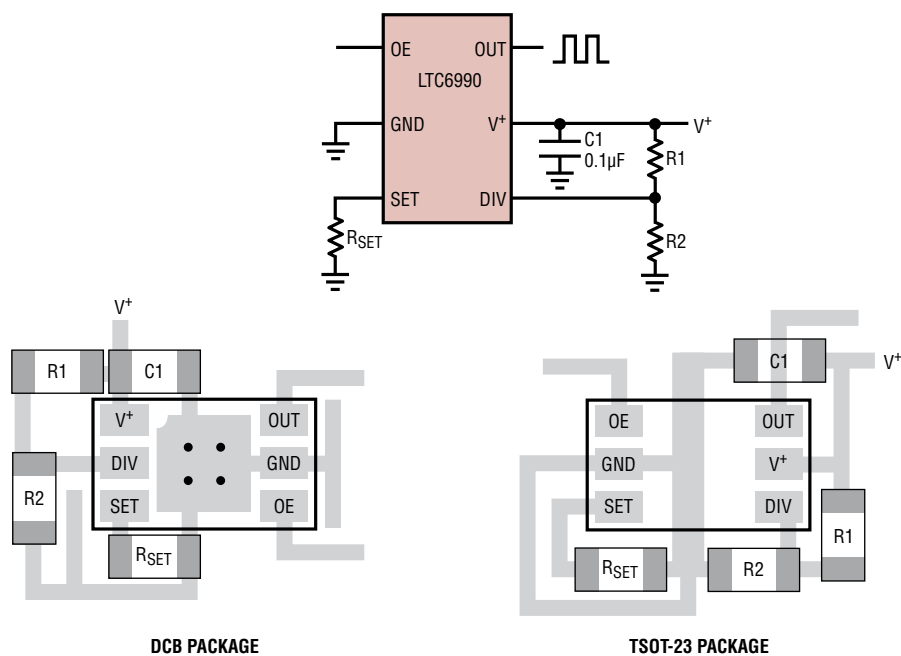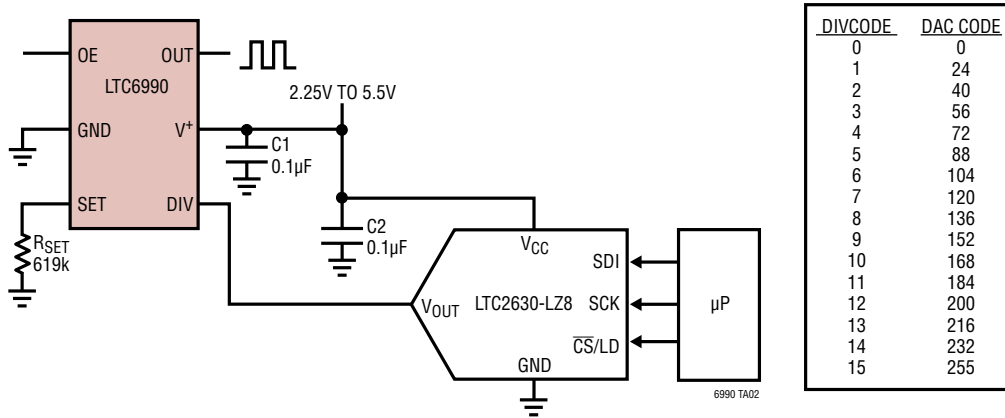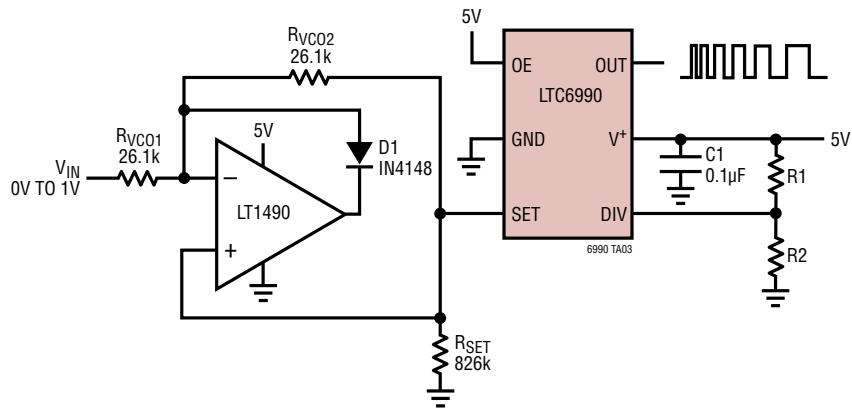


**Figure 17. Supply Bypassing and PCB Layout**

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# TYPICAL APPLICATIONS

**Programming $N_{DIV}$ Using an 8-Bit DAC**



| DIVCODE | DAC CODE |
|---------|----------|
| 0 | 0 |
| 1 | 24 |
| 2 | 40 |
| 3 | 56 |
| 4 | 72 |
| 5 | 88 |
| 6 | 104 |
| 7 | 120 |
| 8 | 136 |
| 9 | 152 |
| 10 | 168 |
| 11 | 184 |
| 12 | 200 |
| 13 | 216 |
| 14 | 232 |
| 15 | 255 |

**Full Range VCO with Any $N_{DIV}$ Setting ($f_{MAX}$ to $f_{MIN}$ for $V_{IN}$ = 0V to $V_{SET}$)**



**Full Range VCO with Any $N_{DIV}$ Setting (Positive Frequency Control, $f_{MIN}$ to $f_{MAX}$ for $V_{IN}$ = 0V to $V_{SET}$**



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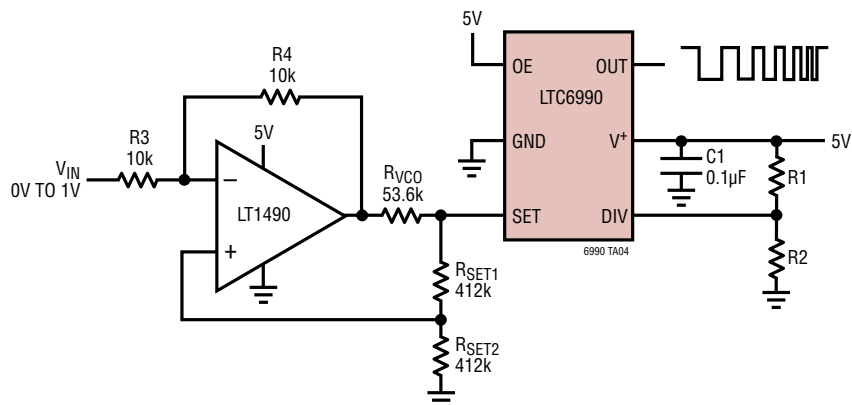
# TYPICAL APPLICATIONS

**Speaker Alarm. Modulate Tone with $R_{VCO}$ within 500Hz to 8kHz Span**
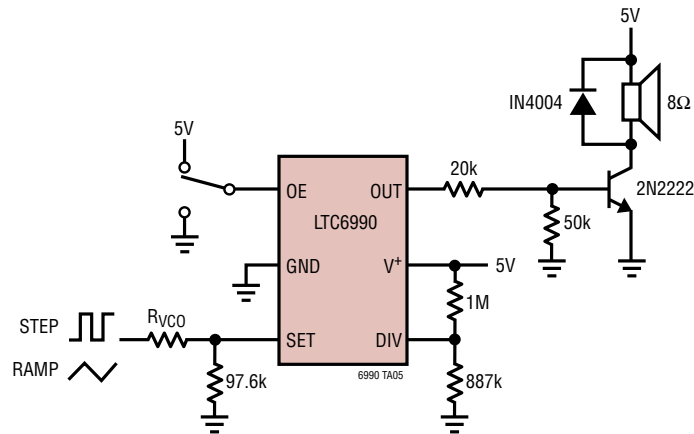


**Overvoltage Detector/Alarm. Direct Drive of Piezo Alarm**



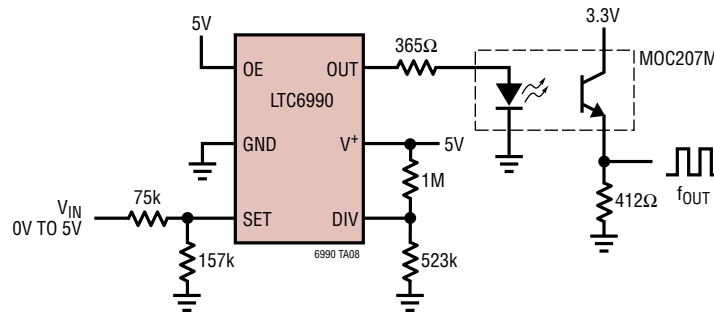$$V_{ALARM} = 400mV\left(1 + \frac{R_A}{R_B}\right) = 30V$$
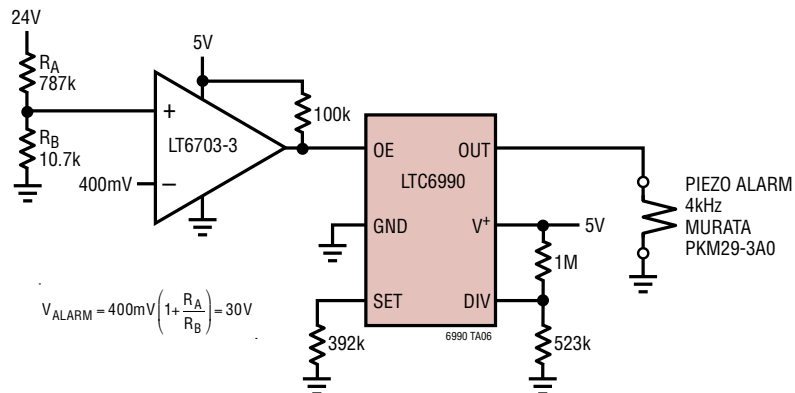
# TYPICAL APPLICATIONS

**Direct Piezo Alarm Driver. Adjust Frequency for Maximum Alarm Sound Pressure
(Maximum Annoyance for Best Effect)**
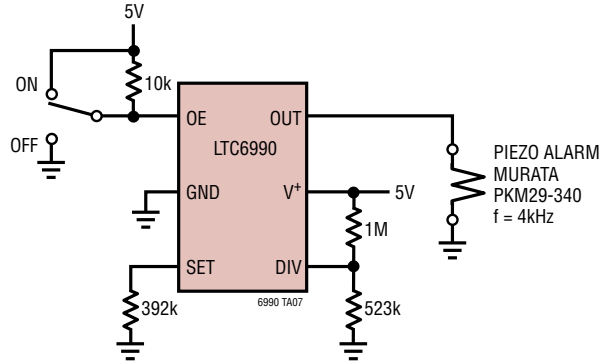


**Isolated V → F Converter. $V_{IN}$ Provided by Isolated Measurement Circuit.
5µs Rise/Fall Time of Isolator Limits $f_{MAX}$ to 60kHz**



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# TYPICAL APPLICATIONS

**Quadrature Sine Wave Oscillator. Voltage Controlled Frequency Range**
**from ~5Hz to ~20kHz with 1V$_{P-P}$ Constant Output Amplitude**



*1/2 OF AN LTC1060 FILTER CAN
BE USED IN PLACE OF THE LTC1059
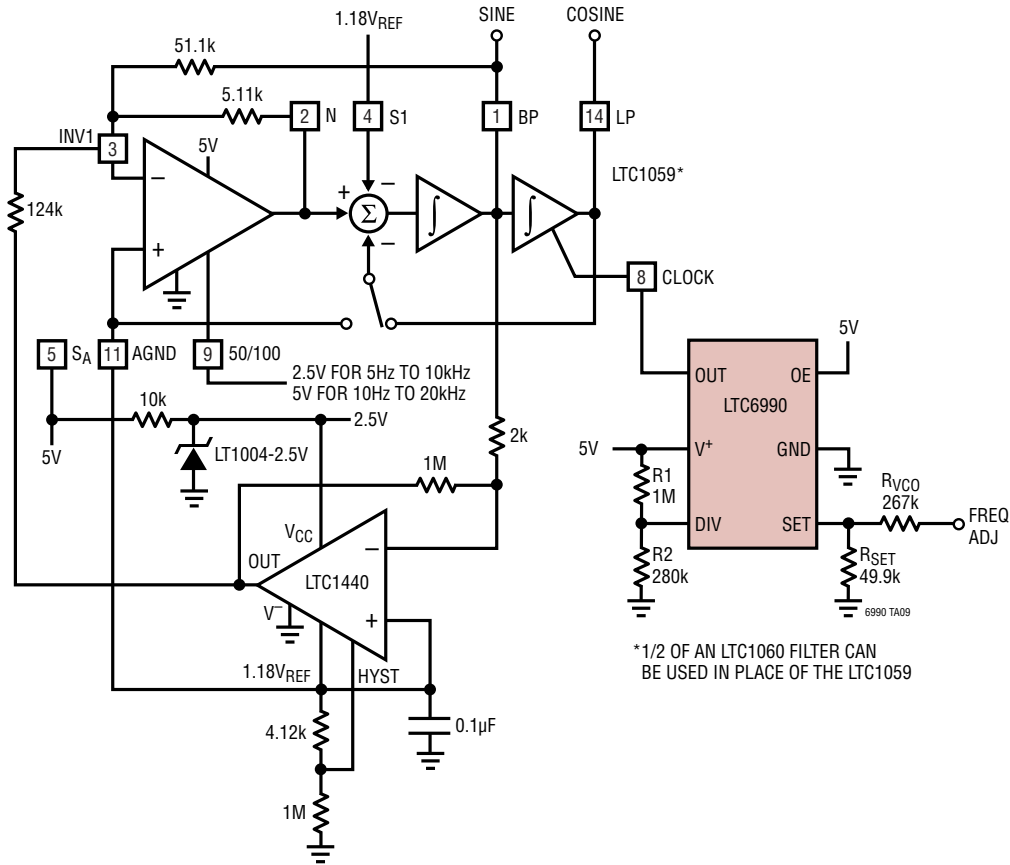
**Temperature to Frequency Converter.**
**3% Linearity from –20°C (f$_{OUT}$ ≈ 20kHz) to 75°C (f$_{OUT}$ ≈ 25kHz)**



THERMISTOR: VISHAY NTHS120601N2202J

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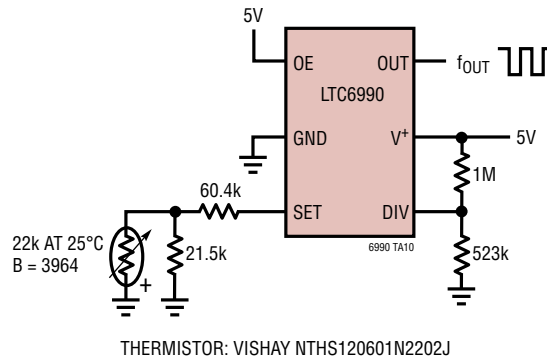
# TYPICAL APPLICATIONS

**Full Range Temperature to Frequency Converter. 16kHz to 1kHz from −20°C to 80°C**
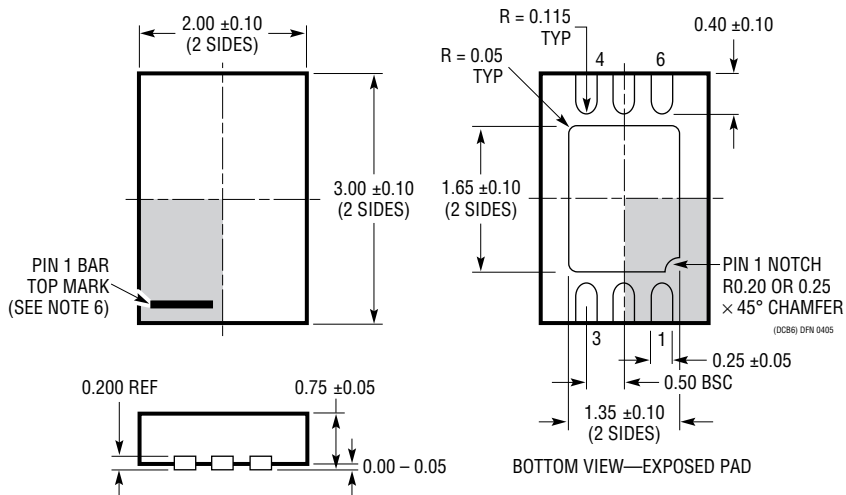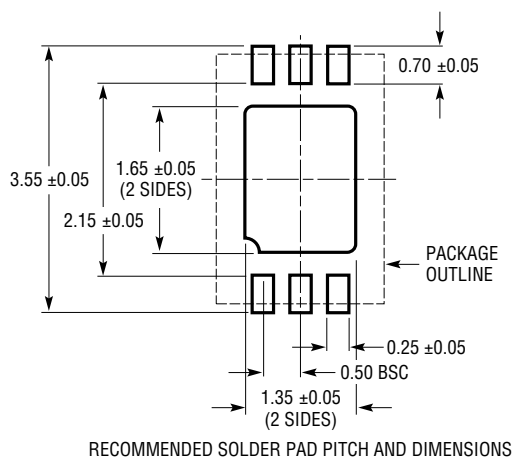
THERMISTOR: VISHAY NTHS120601N2202J
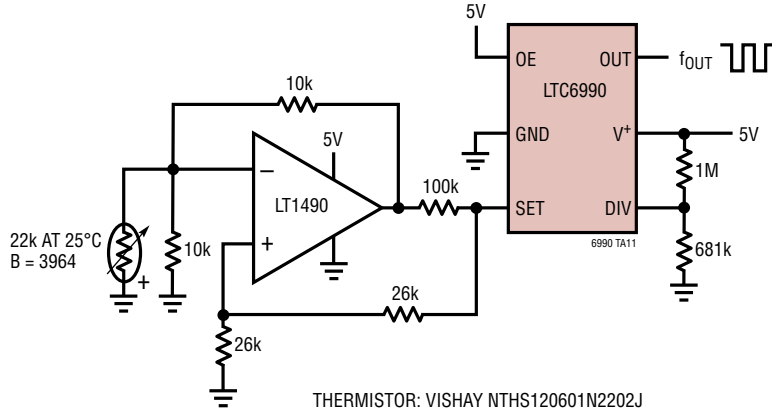
**Light to Frequency Converter. $f_{OUT} \approx$ −1.4kHz per Microampere of Photo Diode Current, $I_{PD}$**
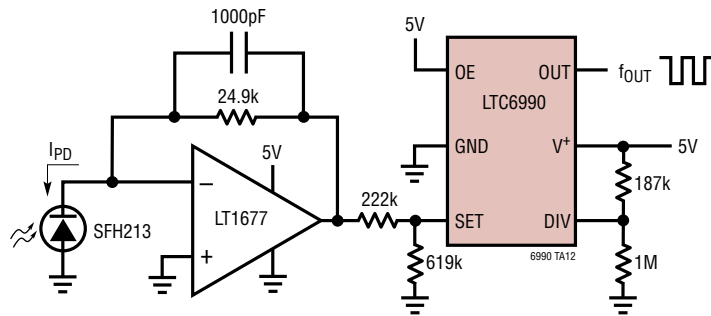
# PACKAGE DESCRIPTION

**DCB Package**
**6-Lead Plastic DFN (2mm × 3mm)**
(Reference LTC DWG # 05-08-1715 Rev A)
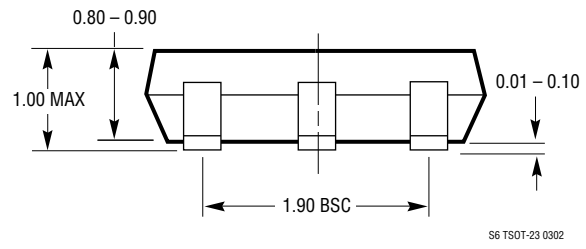


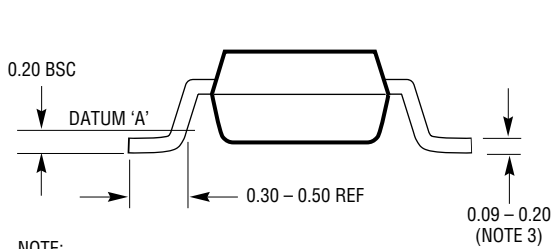RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD

NOTE:
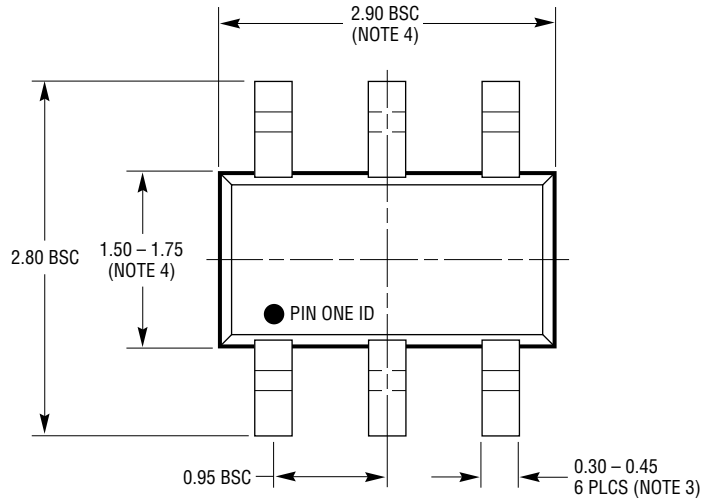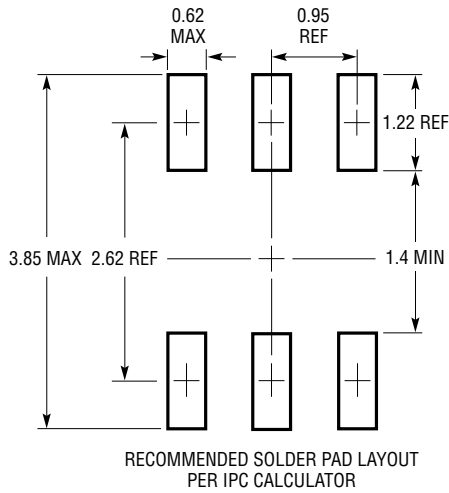1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MO-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**S6 Package**
**6-Lead Plastic TSOT-23**
(Reference LTC DWG # 05-08-1636)

0.62 MAX

0.95 REF

1.22 REF

3.85 MAX    2.62 REF

1.4 MIN

RECOMMENDED SOLDER PAD LAYOUT
PER IPC CALCULATOR

2.90 BSC
(NOTE 4)

2.80 BSC

1.50 – 1.75
(NOTE 4)

PIN ONE ID

0.95 BSC

0.30 – 0.45
6 PLCS (NOTE 3)

0.20 BSC

DATUM 'A'

0.30 – 0.50 REF

0.09 – 0.20
(NOTE 3)

0.80 – 0.90

1.00 MAX

0.01 – 0.10

1.90 BSC

S6 TSOT-23 0302

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
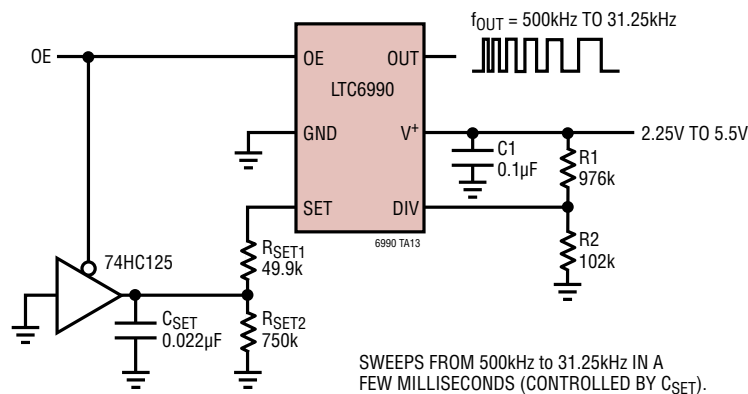5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

Rev. D

# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 7/11 | Updated Features, Description, Pin Configuration, and Order Information sections | 1, 2 |
| | | Added additional information to $\Delta f_{OUT}/\Delta V^+$ and included Note 11 in Electrical Characteristics section | 3, 4 |
| | | Added Typical Frequency Error vs Time curve to Typical Performance Characteristics section | 7 |
| | | Modified drawing in SET pin description in Pin Functions | 8 |
| | | Added text to Basic Fixed Frequency Operation paragraph in Applications Information section | 15 |
| | | Updated Related Parts list | 30 |
| B | 01/12 | Added MP-grade | 1, 2, 4 |
| C | 02/14 | Web links added | 1-30 |
| | | Schematic edits to Quadrature Sine Wave Oscillator circuit | 25 |
| | | Edits to description of LTC6906 and LTC6907 (Related Parts) | 30 |
| D | 01/20 | Added AEC-Q100 Qualified Note to Front Page | 1 |
| | | Added W-Grade Order Information | 2 |

# TYPICAL APPLICATION

**Ultrasonic Frequency Sweep Generator**



$f_{OUT}$ = 500kHz TO 31.25kHz

OE

OE    OUT

LTC6990

GND    V⁺

SET    DIV

6990 TA13

74HC125

$R_{SET1}$ 49.9k

$C_{SET}$ 0.022µF

$R_{SET2}$ 750k

C1 0.1µF

R1 976k

R2 102k

2.25V TO 5.5V

SWEEPS FROM 500kHz to 31.25kHz IN A FEW MILLISECONDS (CONTROLLED BY $C_{SET}$).

# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1799 | 1MHz to 33MHz ThinSOT Silicon Oscillator | Wide Frequency Range |
| LTC6900 | 1MHz to 20MHz ThinSOT Silicon Oscillator | Low Power, Wide Frequency Range |
| LTC6906 | 10kHz to 1MHz ThinSOT Silicon Oscillator | Micropower, $I_{SUPPLY}$ = 12µA at 100kHz |
| LTC6907 | 40kHz to 4MHz ThinSOT Silicon Oscillator | Micropower, $I_{SUPPLY}$ = 35µA at 400kHz |
| LTC6930 | Fixed Frequency Oscillator, 32.768kHz to 8.192MHz | 0.09% Accuracy, 110µs Start-Up Time, 105µA at 32kHz |
| LTC6991 | TimerBlox, Very Low Frequency Clock with Reset | Cycle Time from 2ms to 9.5 Hours, No Caps, 2.2% Accurate |
| LTC6992 | TimerBlox, Voltage-Controlled Pulse Width Modulator (PWM) | Simple PWM with Wide Frequency Range |
| LTC6993 | TimerBlox, Monostable Pulse Generator | Resistor Set Pulse Width from 1µs to 34sec, No Caps, 3% Accurate |
| LTC6994 | TimerBlox, Delay Block/Debouncer | Resistor Set Delay from 1µs to 34sec, No Caps Required, 3% Accurate |