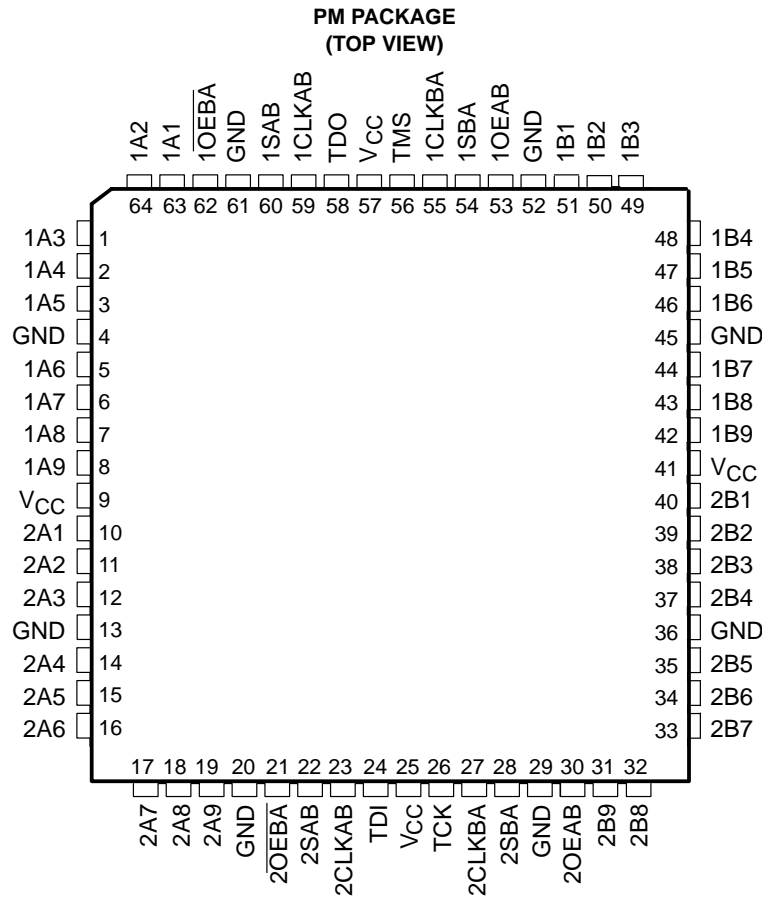


**SN74ABT18652**  
**SCAN TEST DEVICE**  
**WITH 18-BIT TRANSCEIVER AND REGISTER**  
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- **Member of the Texas Instruments Widebus™ Family**
- **Compatible With IEEE Std 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Includes D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data**
- **Two Boundary-Scan Cells Per I/O for Greater Flexibility**
- **SCOPE™ Instruction Set**
  - IEEE Std 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ
  - Parallel Signature Analysis at Inputs With Masking Option
  - Pseudorandom Pattern Generation From Outputs
  - Sample Inputs/Toggle Outputs
  - Binary Count From Outputs
  - Device Identification
  - Even-Parity Opcodes



**description**

This scan test device with an 18-bit bus transceiver and register is a member of the Texas Instruments SCOPE™ testability IC family. This device supports IEEE Std 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the four-wire test access port (TAP) interface.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SCOPE and Widebus are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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# SN74ABT18652 SCAN TEST DEVICE WITH 18-BIT TRANSCEIVER AND REGISTER

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## description (continued)

In the normal mode, this device is an 18-bit bus transceiver and register that allows for multiplexed transmission of data directly from the input bus or from the internal registers. It can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self-test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE bus transceivers and registers.

Data flow in each direction is controlled by clock (CLKAB and CLKBA), select (SAB and SBA), and output-enable (OEAB and OEBA) inputs. For A-to-B data flow, data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). When OEAB is high, the B outputs are active. When OEAB is low, the B outputs are in the high-impedance state. Control for B-to-A data flow is similar to that for A-to-B data flow but uses CLKBA, SBA, and OEBA inputs. Since the OEBA input is active-low, the A outputs are active when OEBA is low and are in the high-impedance state when OEBA is high. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ABT18652.

In the test mode, the normal operation of the SCOPE bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Std 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions, such as parallel signature analysis on data inputs and pseudorandom pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LQFP – PM	Tray	SN74ABT18652PM	ABT18652

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**FUNCTION TABLE**  
(normal mode, each 9-bit section)

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A9	B1–B9	
L	H	L	L	X	X	Input disabled	Input disabled	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified <sup>†</sup>	Store A, hold B
H	H	↑	↑	X <sup>‡</sup>	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified <sup>†</sup>	Input	Hold A, store B
L	L	↑	↑	X	X <sup>‡</sup>	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	X	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	X	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

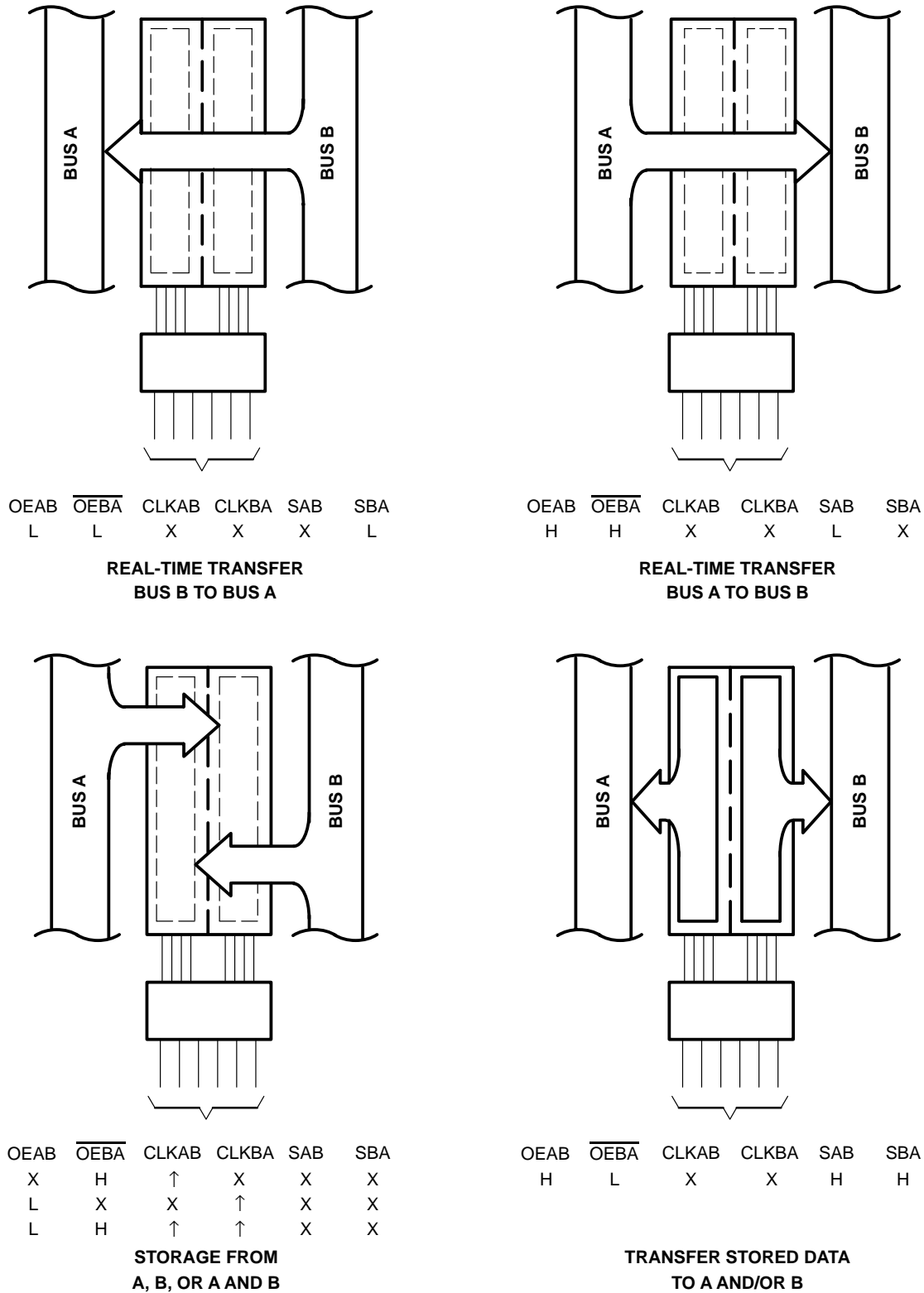
<sup>†</sup> The data output functions can be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

<sup>‡</sup> Select control = L: clocks can occur simultaneously.

Select control = H: clocks must be staggered in order to load both registers.

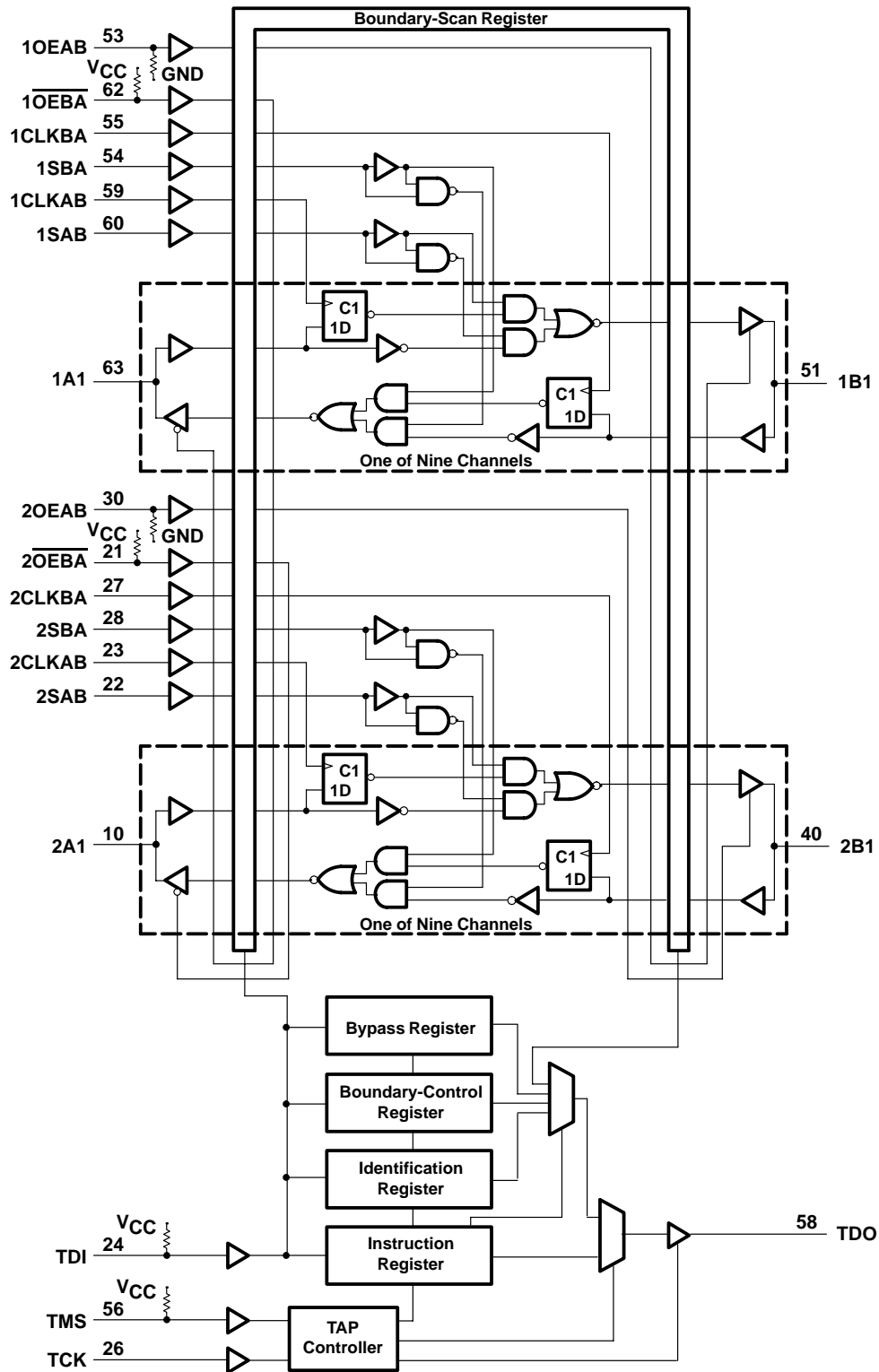
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**Figure 1. Bus-Management Functions**

**functional block diagram**



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1)	–0.5 V to 7 V
I/O ports (see Note 1)	–0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$	96 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2)	34°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		–32	mA
$I_{OL}$ Low-level output current		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		10	ns/V
$T_A$ Operating free-air temperature	–40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)**

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -3\text{ mA}$	2.5			V
	$V_{CC} = 5\text{ V}$ ,	$I_{OH} = -3\text{ mA}$	3			
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$				
$I_{OH} = -32\text{ mA}$		2				
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$				V
		$I_{OL} = 64\text{ mA}$			0.55	
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_{CC} = 5.5\text{ V}$	CLK, OEAB, OEBA, S, TCK		$\pm 1$	$\mu\text{A}$
			A or B ports		$\pm 100$	
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = V_{CC}$ ,	TDI, TMS		10	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = \text{GND}$ ,	TDI, TMS		-150	$\mu\text{A}$
$I_{OZH}^{\ddagger}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			50	$\mu\text{A}$
$I_{OZL}^{\ddagger}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.5\text{ V}$			-50	$\mu\text{A}$
$I_{off}$	$V_{CC} = 0$ ,	$V_I$ or $V_O \leq 5.5\text{ V}$			$\pm 100$	$\mu\text{A}$
$I_{CEX}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 5.5\text{ V}$	Outputs high		50	$\mu\text{A}$
$I_{O}^{\S}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.5\text{ V}$	-50		-200	$\text{mA}$
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or $\text{GND}$	A or B ports	Outputs high		5.5	$\text{mA}$
			Outputs low		38 $\uparrow$	
			Outputs disabled		5	
$\Delta I_{CC}^{\#}$	$V_{CC} = 5.5\text{ V}$ ,	One input at 3.4 V,	Other inputs at $V_{CC}$ or $\text{GND}$		2.5	$\text{mA}$
$C_i$	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$ ,		Control inputs		3	$\text{pF}$
$C_{io}$	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$ ,		A or B ports		10	$\text{pF}$
$C_o$	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$ ,		TDO		8	$\text{pF}$

NOTE 4: Preliminary specifications based on SPICE analysis

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

$\uparrow$  If both A and B ports are low,  $I_{CCL}$  is 76 mA.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or  $\text{GND}$ .

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)**

			MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency	CLKAB or CLKBA		100	MHz
$t_w$	Pulse duration	CLKAB or CLKBA high or low	4		ns
$t_{su}$	Setup time	A before CLKAB $\uparrow$ or B before CLKBA $\uparrow$	4.5		ns
$t_h$	Hold time	A after CLKAB $\uparrow$ or B after CLKBA $\uparrow$	0		ns

NOTE 4: Preliminary specifications based on SPICE analysis

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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)**

			MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency	TCK		50	MHz
$t_w$	Pulse duration	TCK high or low	8		ns
$t_{\text{su}}$	Setup time	A, B, CLK, OEAB, $\overline{\text{OEBA}}$ , or S before TCK $\uparrow$	4.5		ns
		TDI before TCK $\uparrow$	7.5		
		TMS before TCK $\uparrow$	3		
$t_{\text{h}}$	Hold time	A or B after TCK $\uparrow$	1		ns
		CLK, OEAB, $\overline{\text{OEBA}}$ , or S after TCK $\uparrow$	0		
		TDI after TCK $\uparrow$	0.5		
		TMS after TCK $\uparrow$	0.5		
$t_d$	Delay time	Power up to TCK $\uparrow$	50		ns
$t_r$	Rise time	V <sub>CC</sub> power up	1		$\mu$ s

NOTE 4: Preliminary specifications based on SPICE analysis

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$f_{\text{max}}$	CLKAB or CLKBA		100		MHz
$t_{\text{PLH}}$	A or B	B or A	2	5.4	ns
$t_{\text{PHL}}$			2	6.6	
$t_{\text{PLH}}$	CLKAB or CLKBA	B or A	2.5	8	ns
$t_{\text{PHL}}$			2.5	7.4	
$t_{\text{PLH}}$	SAB or SBA	B or A	2	7.5	ns
$t_{\text{PHL}}$			2	8	
$t_{\text{PZH}}$	OEAB	B	2.5	8.6	ns
$t_{\text{PZL}}$			3	9.3	
$t_{\text{PZH}}$	$\overline{\text{OEBA}}$	A	2	6.9	ns
$t_{\text{PZL}}$			2.5	7.9	
$t_{\text{PHZ}}$	OEAB	B	3	10.5	ns
$t_{\text{PLZ}}$			2	8.5	
$t_{\text{PHZ}}$	$\overline{\text{OEBA}}$	A	3	8.4	ns
$t_{\text{PLZ}}$			1.5	6.5	

NOTE 4: Preliminary specifications based on SPICE analysis





**SN74ABT18652**  
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

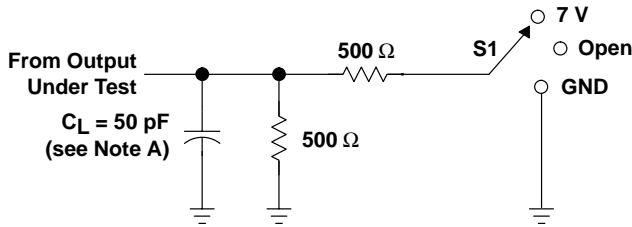
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f <sub>max</sub>	TCK		50		MHz
t <sub>PLH</sub>	TCK↓	A or B	2.5	13.5	ns
t <sub>PHL</sub>			2.5	12.5	
t <sub>PLH</sub>	TCK↓	TDO	2	6.5	ns
t <sub>PHL</sub>			2	6.5	
t <sub>PZH</sub>	TCK↓	A or B	4.5	14.2	ns
t <sub>PZL</sub>			5	15.5	
t <sub>PZH</sub>	TCK↓	TDO	2	7	ns
t <sub>PZL</sub>			3	7.5	
t <sub>PHZ</sub>	TCK↓	A or B	4	17	ns
t <sub>PLZ</sub>			3	16	
t <sub>PHZ</sub>	TCK↓	TDO	3	9	ns
t <sub>PLZ</sub>			3	7.5	

NOTE 4: Preliminary specifications based on SPICE analysis

**SN74ABT18652**  
**SCAN TEST DEVICE**  
**WITH 18-BIT TRANSCEIVER AND REGISTER**

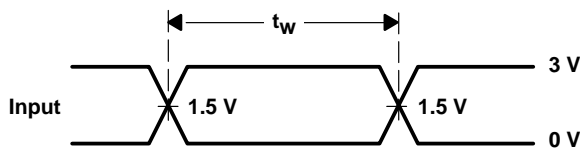
SCBS132B – AUGUST 1992 – REVISED JANUARY 2002

**PARAMETER MEASUREMENT INFORMATION**

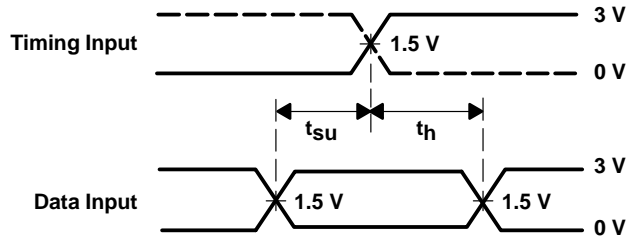


**LOAD CIRCUIT**

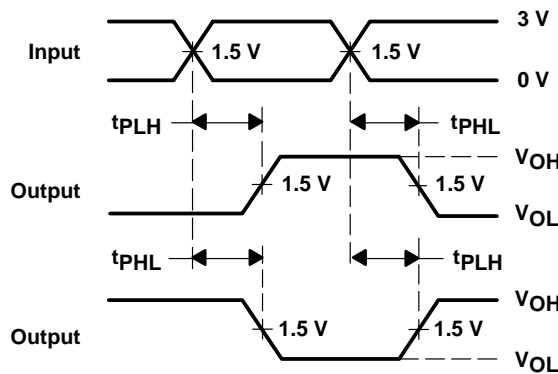
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



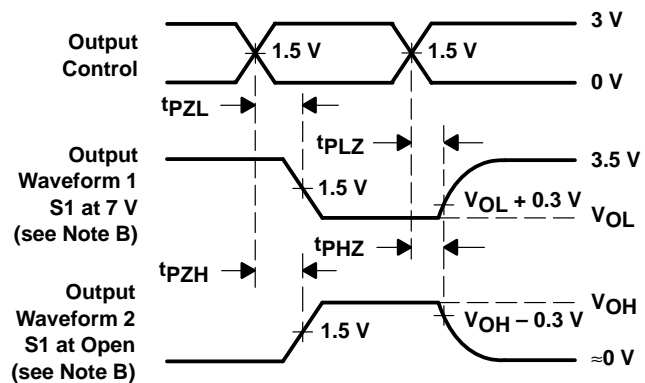
**VOLTAGE WAVEFORMS  
 PULSE DURATION**



**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT18652PM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABT18652	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

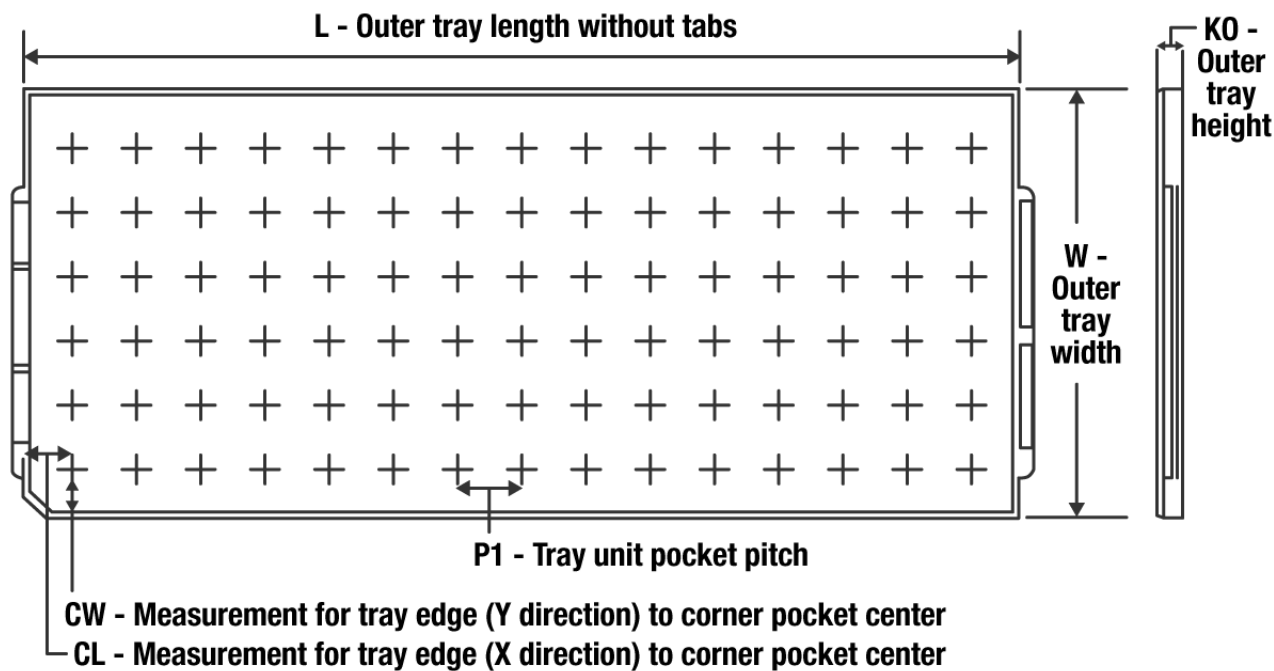
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TRAY**


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN74ABT18652PM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13

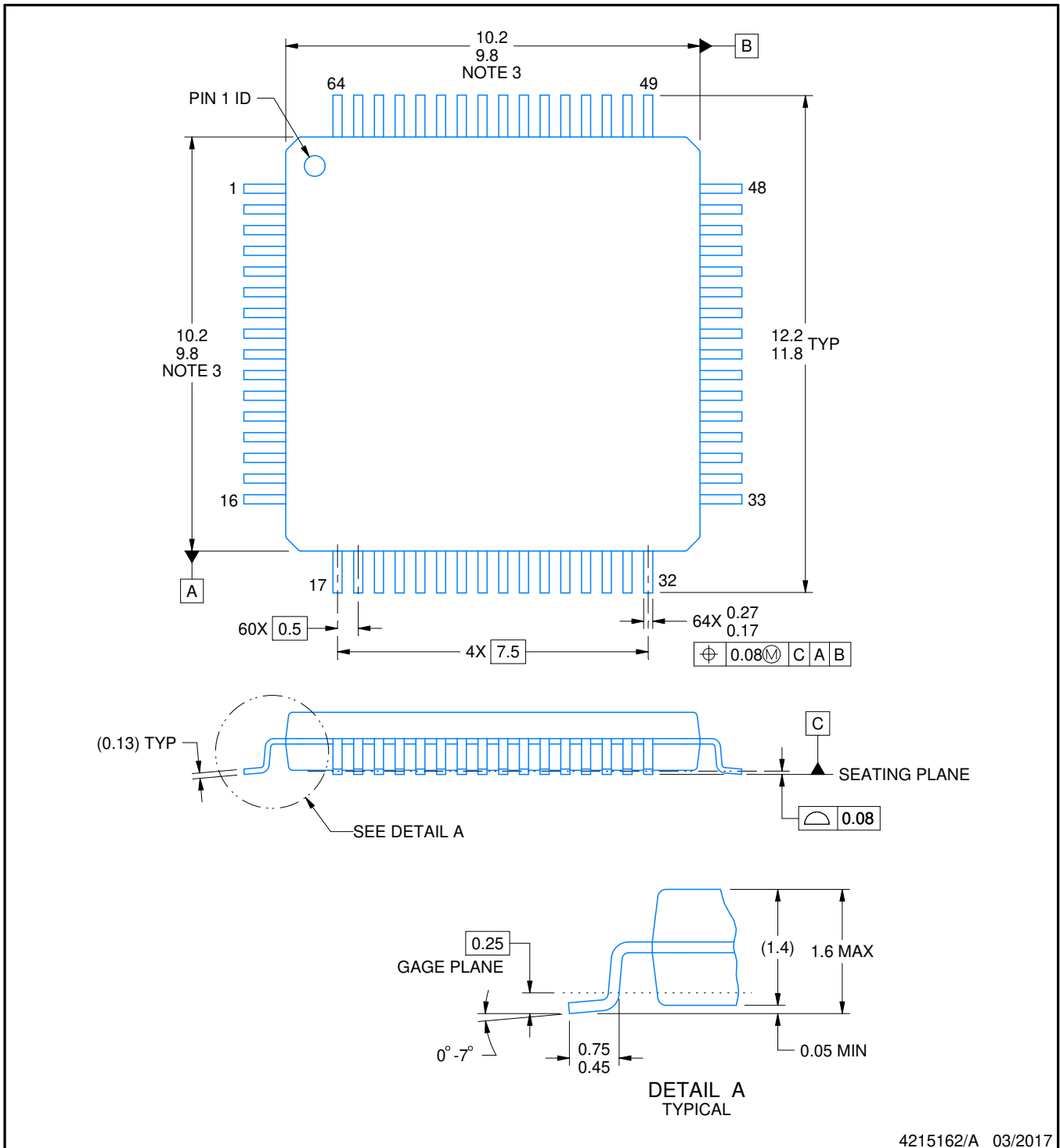
# PM0064A



# PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



4215162/A 03/2017

**NOTES:**

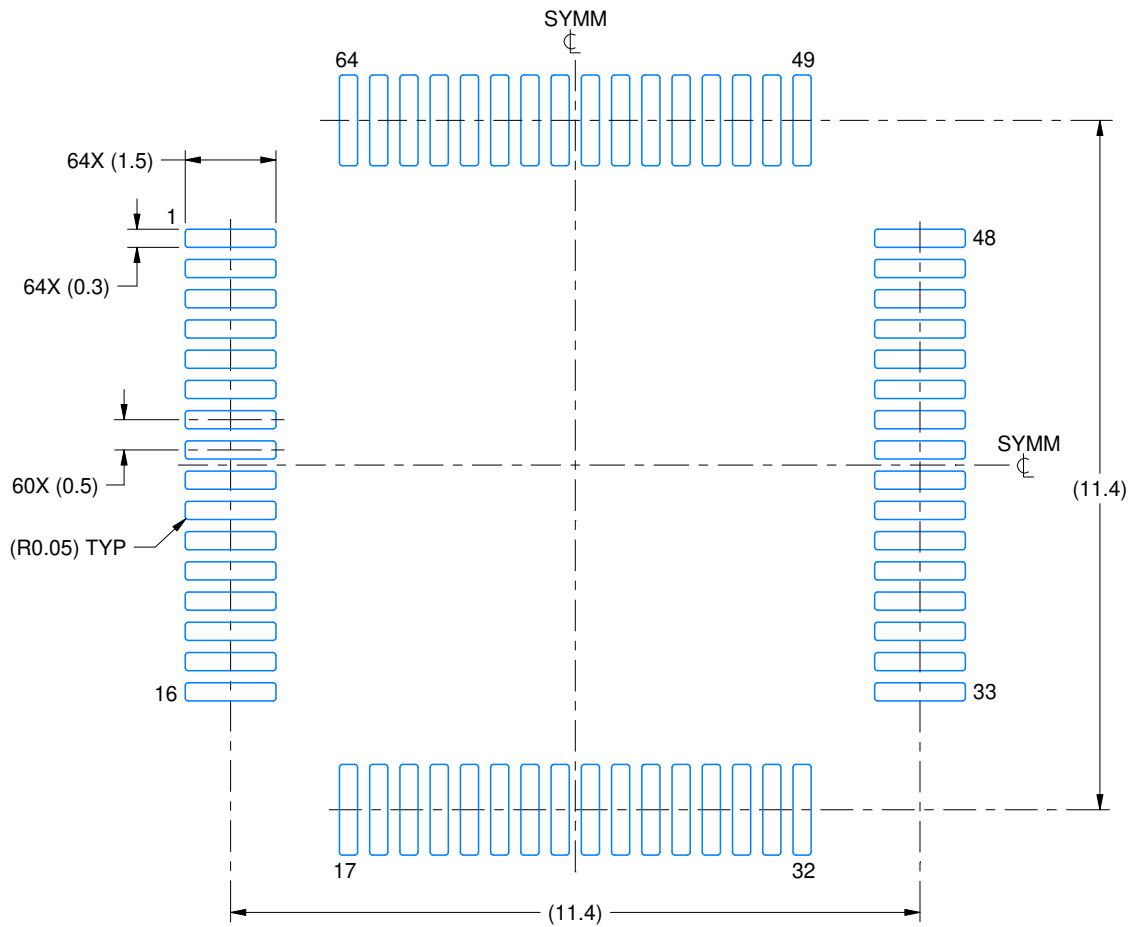
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

# EXAMPLE BOARD LAYOUT

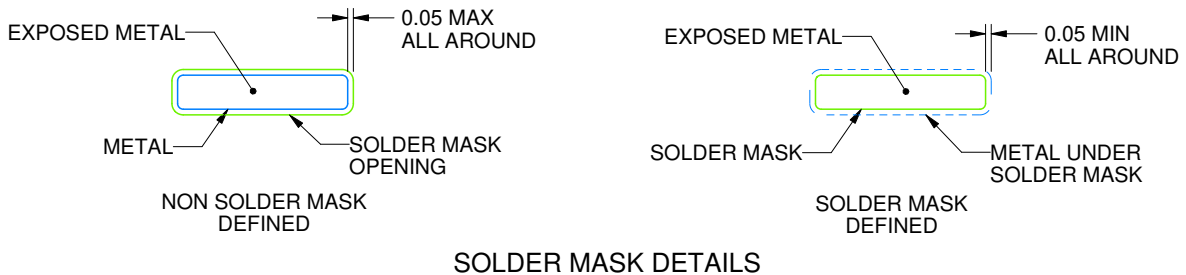
PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



4215162/A 03/2017

NOTES: (continued)

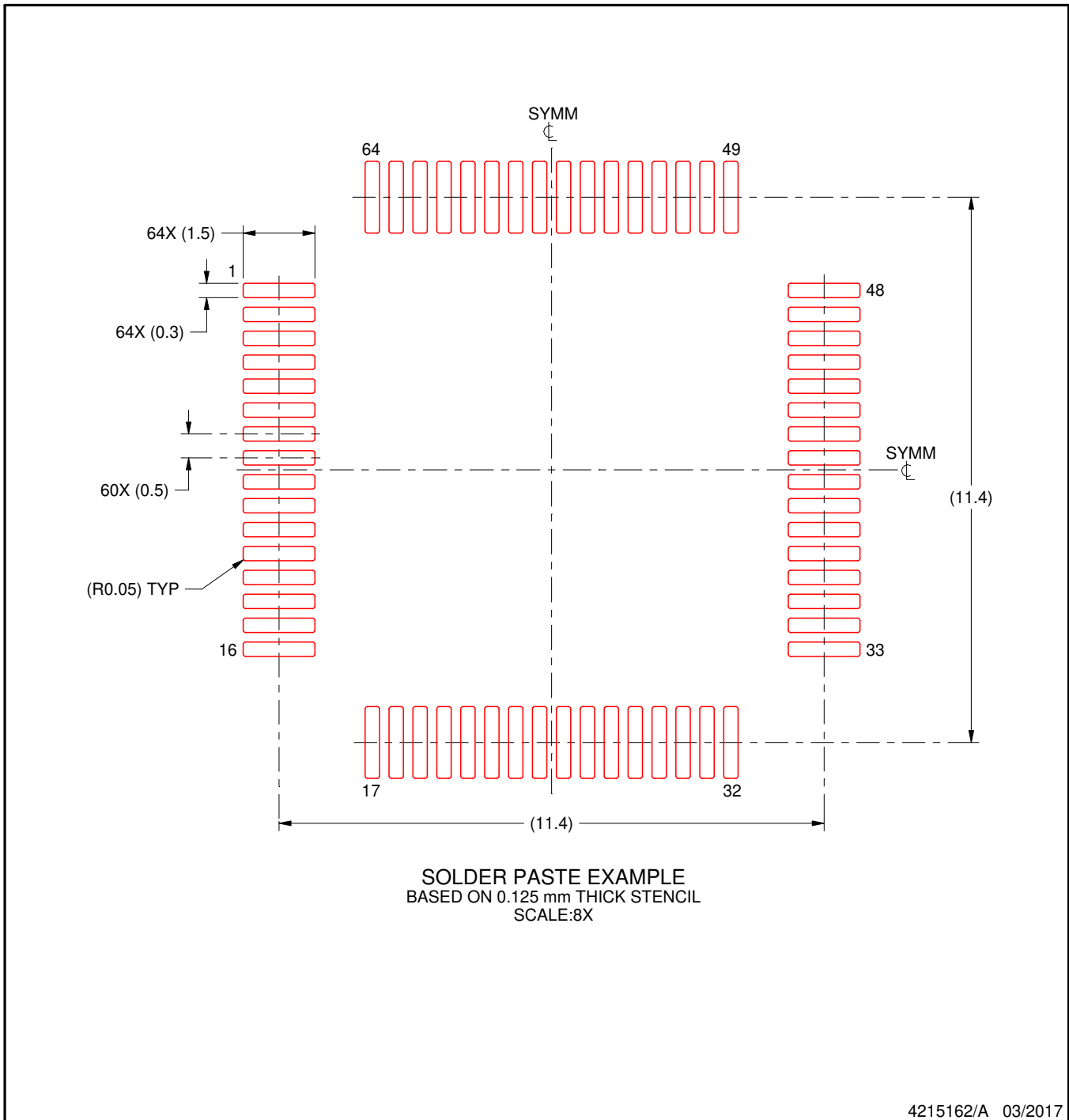
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).

# EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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