

3V-5.5V, 3.5A Step Down PWM Switching Regulator

Features

Description

LX7175 is a step-down PWM Switching Regulator IC with integrated high side P-CH and low side N-CH MOSFETs. The IC operates using a hysteretic control topology with a full load switching frequency of 1.4MHz allowing small output filter components while maintaining excellent dynamic load response.

The operational input voltage range of LX7175 is from 3V to 5.5V and it has two modes of operation selected externally by MODE pin. When MODE pin is high, it operates in continuous PWM operation and when it is tied low, it operates in Power Save Mode (PSM) with automatic transition between PWM and PSM mode depending on the load current. This allows the converter's efficiency to remain high when load current drops.

In the shutdown mode, the IC's current consumption is reduced to less than 1 μ A and the output capacitor is discharged.

Other features of the part are: a) cycle-by-cycle current limit followed by latch off, b) thermal protection with hysteresis, c) internal digital soft start, d) and Power Good function.

- 3.5A Step-down Regulator
- Operational Input Supply Voltage Range: 3V-5.5V
- Integrated PMOS and NMOS
- Load Current from zero to 3.5A
- 1.4MHz Switching Frequency
- SKIP Pulse to Improve Light Load Efficiency
- Open VReg Type 0 LV Compatible
- Input UVLO Protection
- Enable Pin
- Power Good
- Internal Soft-start
- Cycle-by-Cycle Over Current Protection
- Latch Off Operation Under Output Short.
- RoHS Compliant for Pb-free

Applications

- Small Battery Operated Devices
- HDD
- Set-Top Box
- LCD TV's
- Notebook/Netbook
- Routers
- Video Cards
- PC Peripherals
- PoE Powered Devices

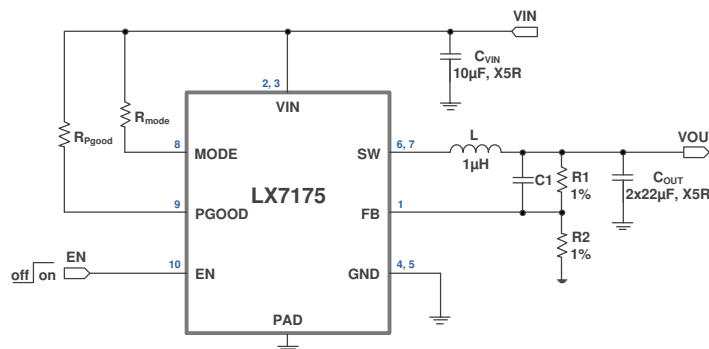


Figure 1 · Typical Application of LX7175

Pin Configuration and Pinout

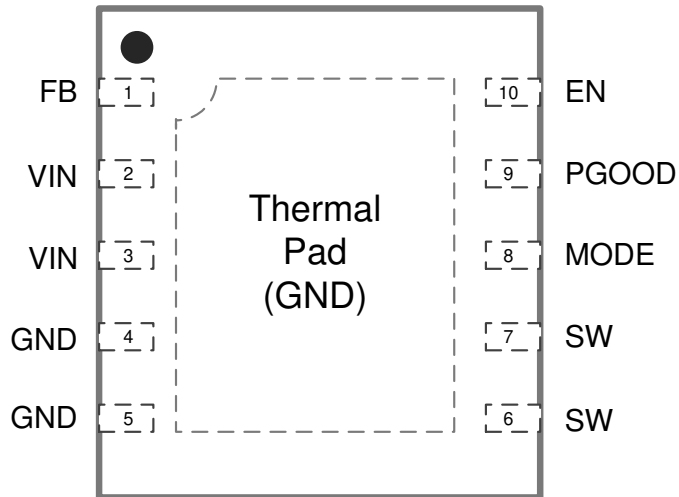


Figure 2 · Pinout DFN 3x3 10L Top View

Marking: Line1 7175
Line2 Date / Lot Code
Line3 * MSC (* is the pin 1 dot)

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-10°C to 85°C	RoHS Compliant, Pb-free	DFN 3X3 10L	LX7175CLD	Bulk / Tube
			LX7175CLD-TR	Tape and Reel

Pin Description

Pin Number	Pin Designator	Description
1	FB	Voltage feedback pin. Connect to the output terminal through a resistor divider network to set the output voltage of the regulator to the desired voltage.
2, 3	VIN	Input voltage terminal of the regulator. A minimum of 10 μ F, X5R type ceramic capacitor must be connected as close as possible from this pin to GND plane to insure proper operation.
4, 5	GND	Ground pins for the power stage.
6, 7	SW	Switch-node pin. Connect the output inductor between this pin and output capacitor.
8	MODE	When this pin is connected to GND, the chip will go into variable frequency hysteretic mode that gradually reduces switching frequency as the load is reduced. When it is connected to VIN, it operates in constant frequency hysteretic mode, and will remain in continuous conduction mode. In this mode the low side MOSFET is not turned off when the current in the inductor reverses direction to pull current from the load.
9	PGOOD	Power-good pin. This is an open-drain output and should be connected to a voltage rail (for example, VIN) with an external pull-up resistor. During the power on sequence, this pin switches from Low to High state when the FB voltage exceeds the power good threshold and the internal soft start has finished its operation. It will be pulled low, when the FB falls below the power good threshold minus the hysteresis. It will turn back on, when the pull FB rises again above the threshold.
10	EN	Pulling this pin higher than 2V will enable the regulator. When pulled low, the regulator will turn off.
	Thermal PAD	For good thermal connection, this PAD must be connected using thermal VIAs to the GND plane and to the LAND pattern of the IC.

Block Diagram

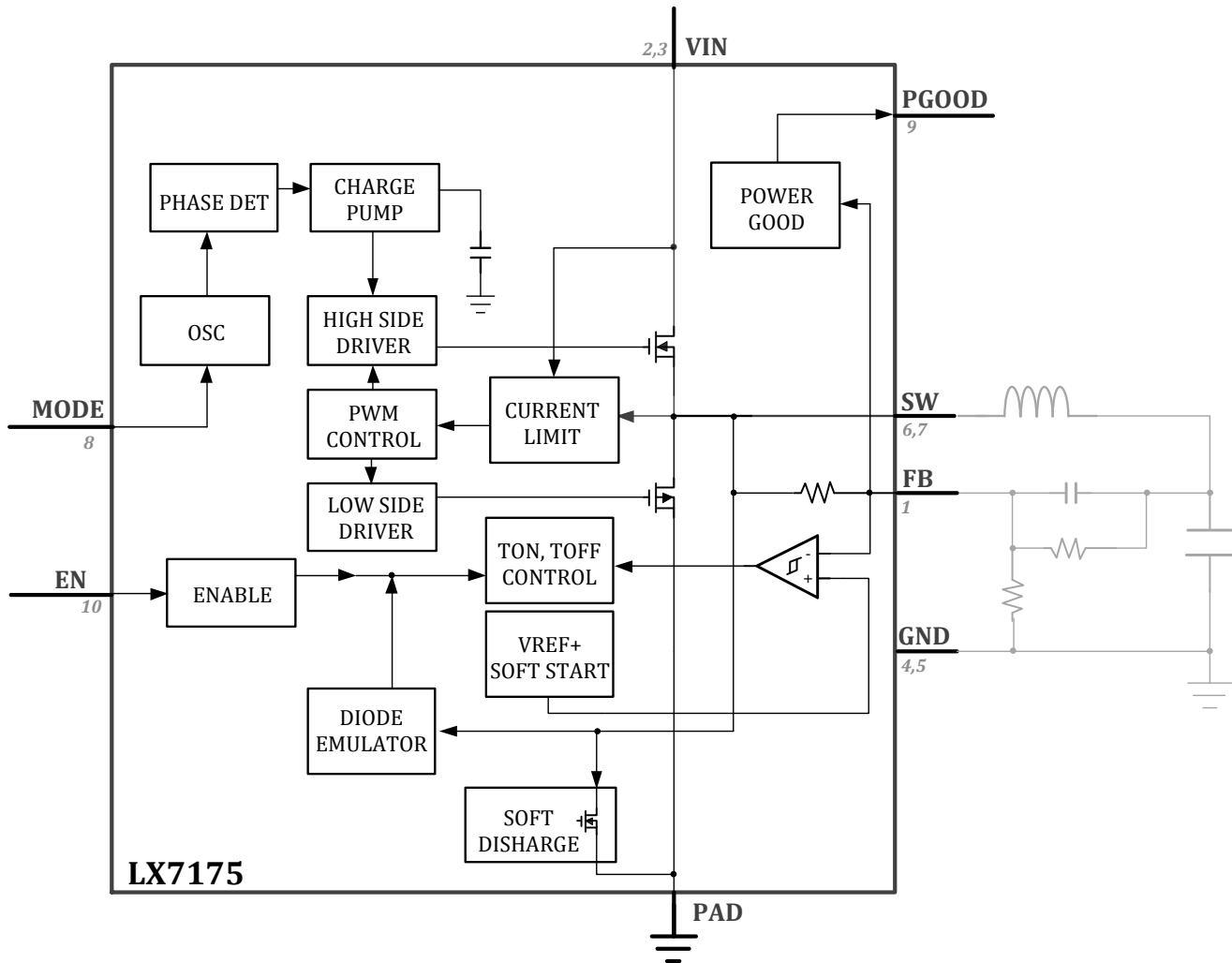


Figure 3 · Simplified Block Diagram of LX7175

Absolute Maximum Ratings

Parameter	Min	Max	Units
VIN, EN, FB, PGOOD, MODE to GND	-0.3	7	V
SW to GND	-0.3	7	V
SW to GND (Shorter than 15ns)	-4	7	V
Maximum Junction Temperature		150	°C
Storage Temperature	-65	150	°C
Peak Package Solder Reflow Temperature (40s, reflow)		260 (+0, -5)	°C

Note: Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability

Operating Ratings

	Min	Max	Units
VIN	3.0	5.5	V
V _{OUT}	0.8	3.3	V
Ambient Temperature	-10	85	°C
Output Current	0	3.5	A

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JA}	41.2	°C/W

Note: The θ_{JA} number assumes no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Note: The following specifications apply over the operating ambient temperature of $-10^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ except where otherwise noted with the following test conditions: $3.0 < V_{IN} < 5.5\text{V}$. Typical parameters refer to $T_J = 25^\circ\text{C}$, $V_{IN} = 5\text{V}$.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Operating Current						
I_Q	Input Current	$I_{LOAD} = 0$, $MODE = GND$		200	500	μA
I_{IN}	Input Current at Shut Down	$EN = GND$, $T_A = 25^\circ\text{C}$		0.1	1	μA

Symbol	Parameter	Test Condition	Min	Typ	Max	Units	
VIN INPUT UVLO							
VIN	Under Voltage Lockout	VIN rising		2.4	2.8	V	
V _{HYS}	UVLO Hysteresis			250		mV	
FEEDBACK							
V _{REF}	Feedback Voltage Internal Reference	T _A = 25°C	0.788	0.800	0.812	V	
		0 < T _J < 125°C	0.782		0.818	V	
I _{FB}	FB Pin Input Current				10	nA	
	Line Regulation	VIN from 3V to 5.5V, MODE = High, I _{LOAD} = 0.1A, V _{OUT} = 1V, L = 0.68μH, C _{OUT} = 44μF. GBD		0.065		%	
	Load Regulation	VIN = 5V, MODE = High I _{LOAD} = 0 to 3.5A, L = 0.68μH, C _{OUT} = 44μF. GBD	V _{OUT} = 1V	0.06		%A	
			V _{OUT} = 3.3V	0.08			
		VIN = 5V, MODE = Low I _{LOAD} = 0.2A to 3.5A, L = 0.68μH, C _{OUT} = 44μF. GBD	V _{OUT} = 1V	0.075		%A	
			V _{OUT} = 3.3V	0.11			
	Transient Response	Load from 0.1A to 1.5A, Tr = Tf = 1μs, V _{OUT} = 1V, L = 0.68μH, C _{OUT} = 44μF, MODE = High. GBD		±35		mV	
FB UVLO							
V _{FBULVO}	FB UVLO Threshold			40%	50%	V _{REF}	
OUTPUT DEVICE							
R _{DSON_H}	R _{DSON} of High Side			55	100	mΩ	
R _{DSON_L}	R _{DSON} of High Side			40	65	mΩ	
I _L	Current Limit	0 < T _J < 125°C. GBD	VIN = 5V.	4.5	5.9	7.3	A
			VIN = 3V.	3.89	5.3	6.74	
T _{SH}	Thermal Shut Down Threshold	GBD	140	163	185	°C	
T _H	Hysteresis	GBD		27		°C	
OSCILLATOR							
f	Switching Frequency	MODE = High	1.25	1.4	1.65	MHz	
F _{HYST}	Switching Frequency	In Boundary Conduction Mode, In Hysteretic Mode (The PLL is off)	0.3	0.445	0.6	MHz	
D _{MAX}	Maximum Duty Cycle		70			%	
SOFT START							
T _{SS}	Soft Start Time	From EN going high to V _{OUT} reaches regulation.	0.8	1.4	1.8	ms	

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
MODE						
M _{VIH}	Input High		1.1			V
M _{VIL}	Input Low				0.4	V
M _{VIH}	Input Bias			0.01	1	μA
EN INPUT						
EN _{VIH}	Input High		1.1			V
EN _{VIL}	Input Low				0.4	V
EN _H	Hysteresis			0.1		V
EN _{II}	Input Bias Current			0.01	1	μA
POWER-GOOD						
V _{PG}	Power-good Transition High Threshold	V _{FB} rising, in percentage of output voltage set-point.		83		%
V _{PGHY}	Hysteresis	Either V _{FB} rising or falling		40		mV
P _{GRDSON}	Power-good Internal FET R _{DSON}	V _{IN} = 5V, 0 < T _J < 125°C			100	Ω
	PGOOD FET Leakage Current			0.01	1	μA
	PGOOD Internal Glitch Filter			5		μs
OUTPUT DISCHARGE						
	Internal Discharge Resistor		80	300	600	Ω
GBD Guaranteed by design, not production tested.						

Typical Performance Curves (Efficiency & Line Regulation)

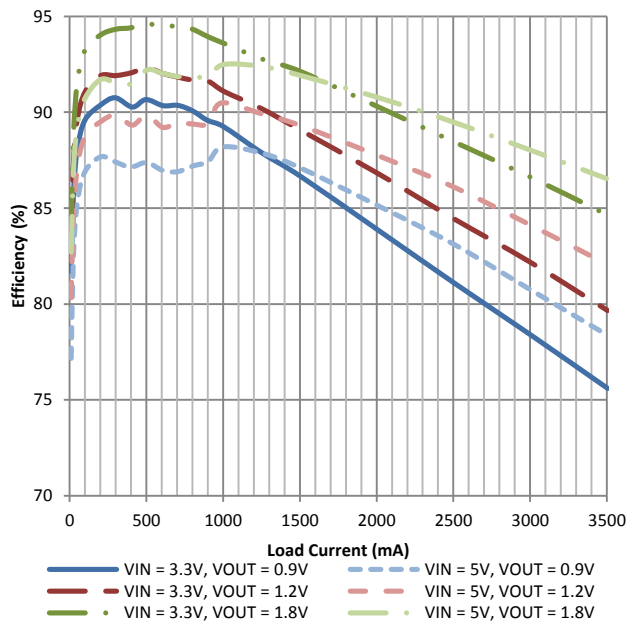


Figure 4 · PSM Mode Efficiency

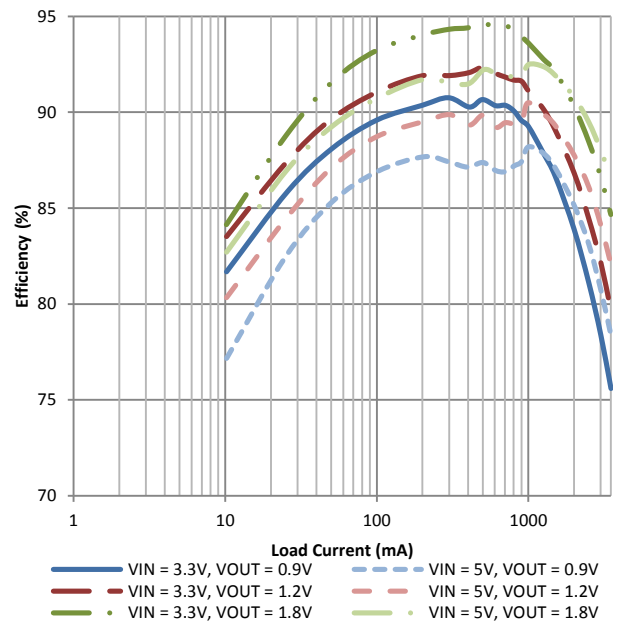


Figure 5 · PSM Mode Efficiency in Log Scale

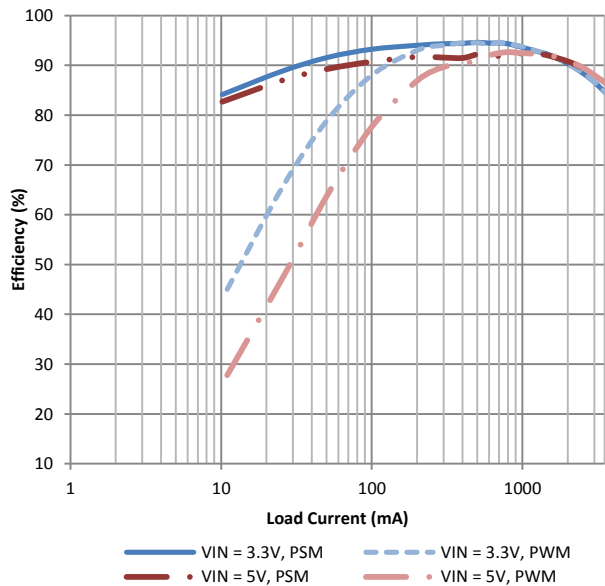


Figure 6 · PSM vs. PWM Efficiency with $V_{OUT}=1.8V$

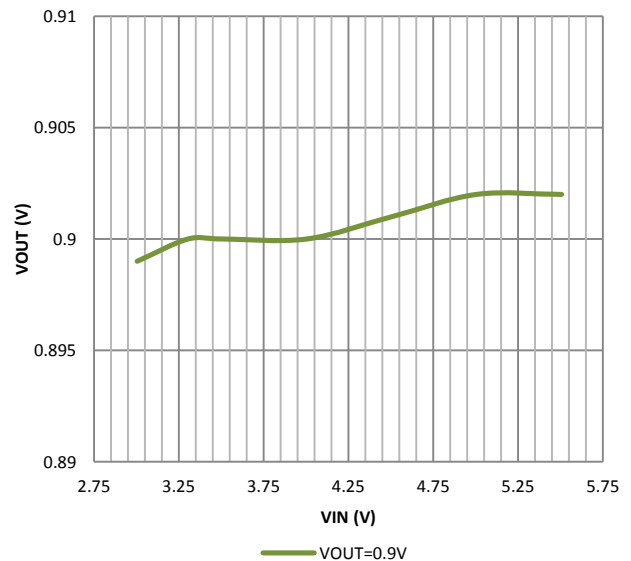


Figure 7 · Line Regulation $V_{OUT} = 0.9V$ (V_{OUT} vs. V_{IN})

Typical Performance Curves (Line Regulation & Load Regulation)

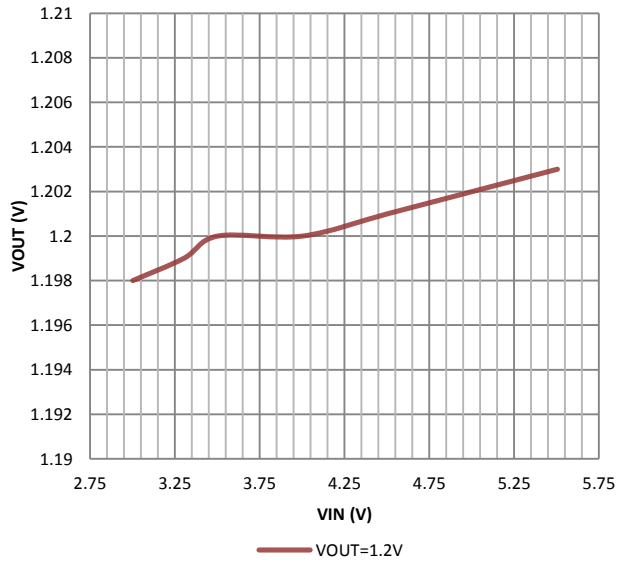


Figure 8 · Line Regulation V_{OUT} = 1.2V (V_{OUT} vs. V_{IN})

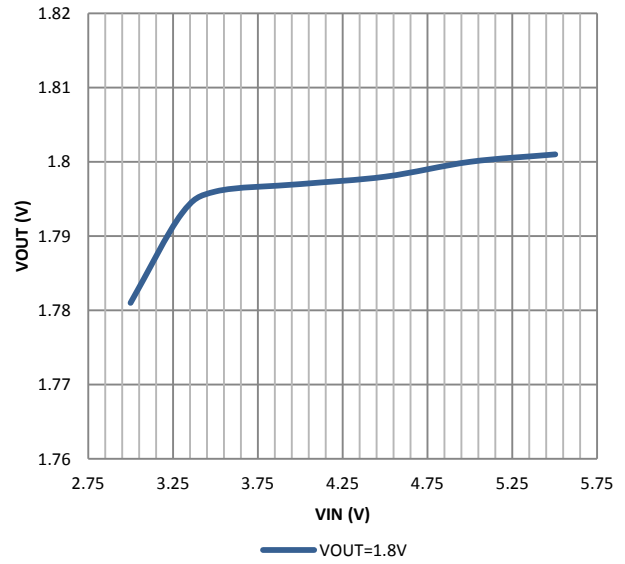


Figure 9 · Line Regulation V_{OUT} = 1.8V (V_{OUT} vs. V_{IN})

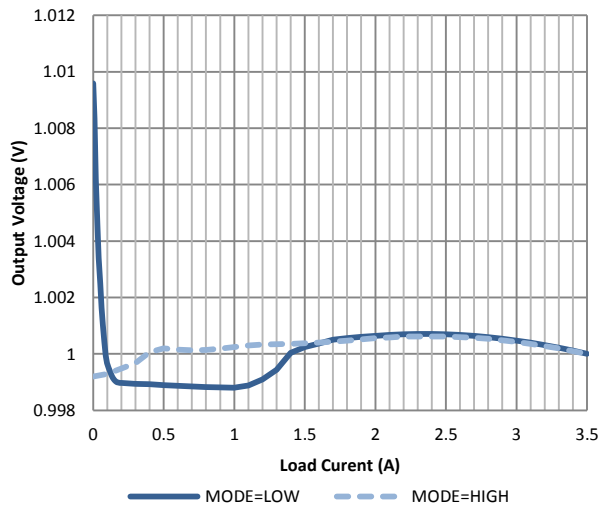


Figure 10 · Load Regulation VIN = 5V, V_{OUT} = 1.0V (V_{OUT} vs. Load Current)

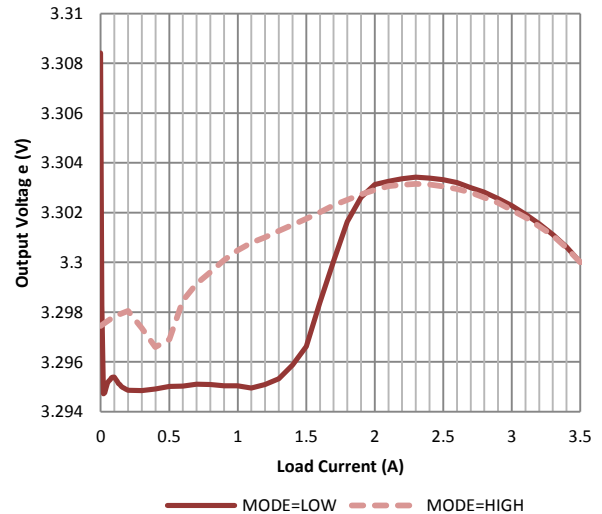


Figure 11 · Load Regulation VIN = 5V, V_{OUT} = 3.3V (V_{OUT} vs. Load Current)

Typical Performance Curves (Load Transient - $V_{IN} = 5V$, $V_{OUT} = 1V$)

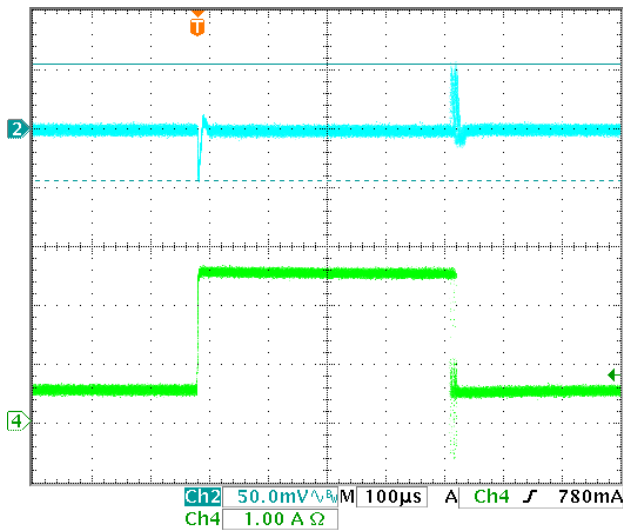


Figure 12 · $L = 0.68\mu H$, $C_{OUT}=44\mu F$

CH2: V_{OUT} , CH4: I_L

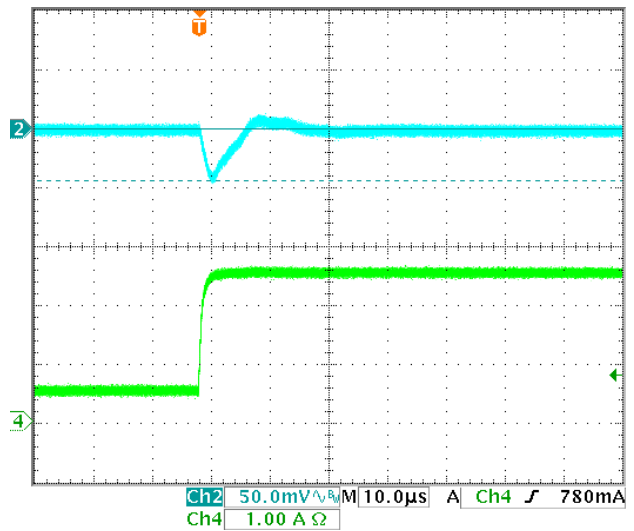


Figure 13 · $L = 0.68\mu H$, $C_{OUT}=44\mu F$, Rising Edge

CH2: V_{OUT} , CH4: I_L

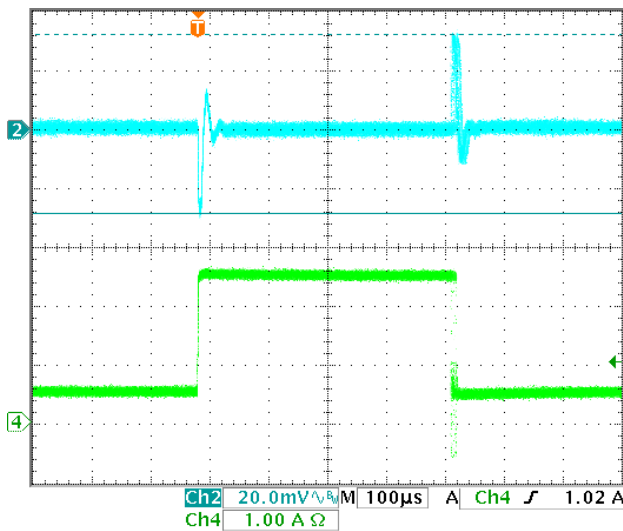


Figure 14 · $L = 0.68\mu H$, $C_{OUT}=154\mu F$

CH2: V_{OUT} , CH4: I_L

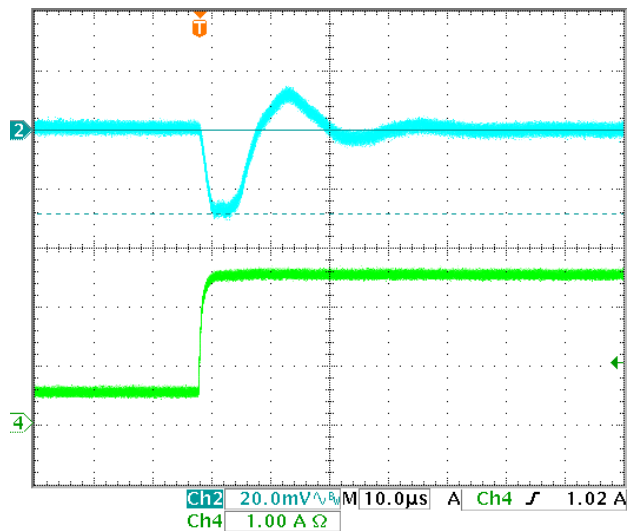


Figure 15 · $L = 0.68\mu H$, $C_{OUT}=154\mu F$ Rising Edge

CH2: V_{OUT} , CH4: I_L

Typical Performance Curves (Start Up - $V_{IN} = 5V$, $V_{OUT} = 1V$)

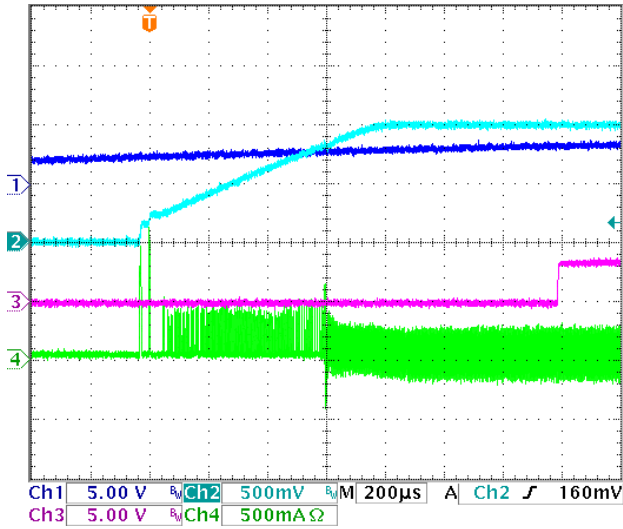


Figure 16 · Power up with no load, MODE = High

CH1: VIN, CH2: V_{OUT} , CH3: PGOOD,
CH4: Inductor Current

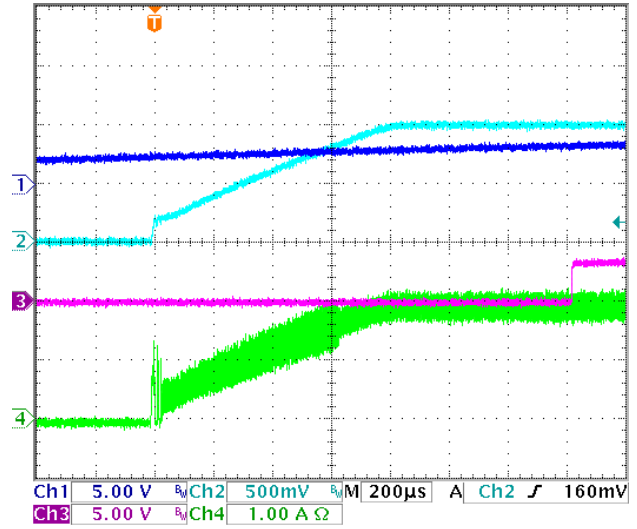


Figure 17 · Power up with resistive load, MODE = High

CH1: VIN, CH2: V_{OUT} , CH3: PGOOD,
CH4: Inductor Current

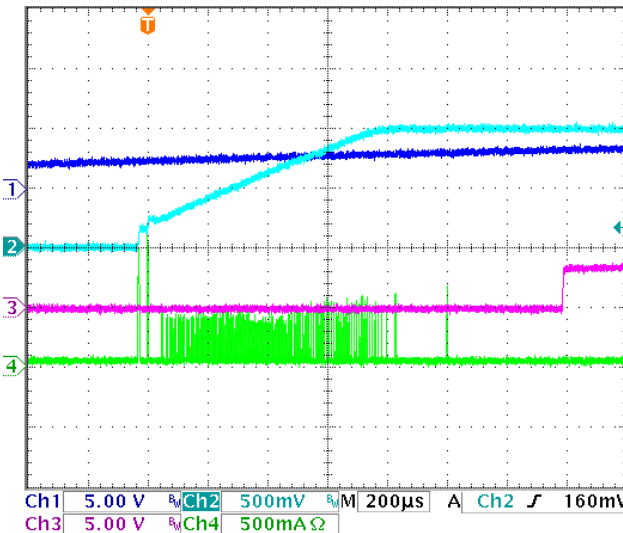


Figure 18 · Power up with no load, MODE = Low

CH1: VIN, CH2: V_{OUT} , CH3: PGOOD,
CH4: Inductor Current

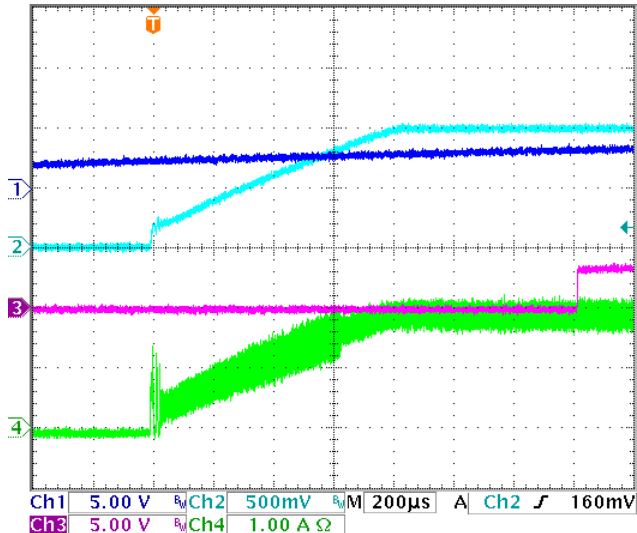


Figure 19 · Power up with resistive load

CH1: VIN, CH2: V_{OUT} , CH3: PGOOD,
CH4: Inductor Current

Typical Performance Curves (Short Condition)

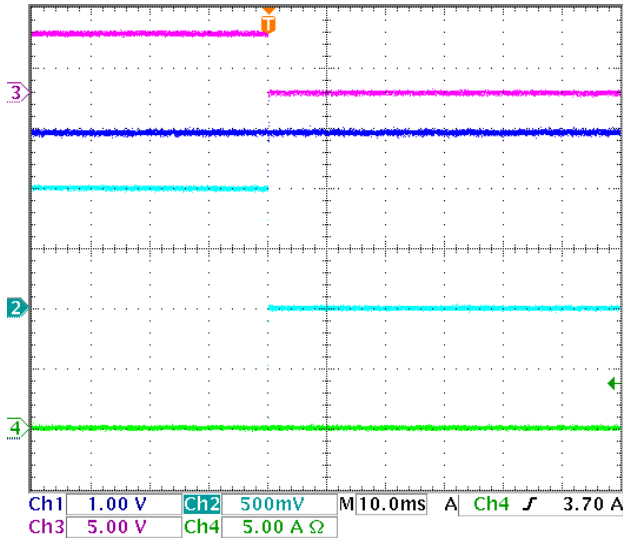


Figure 20 · Output Short 5V input 1V output

CH1: VIN, CH2: V_{OUT}, CH3: PGOOD,
CH4: Inductor Current

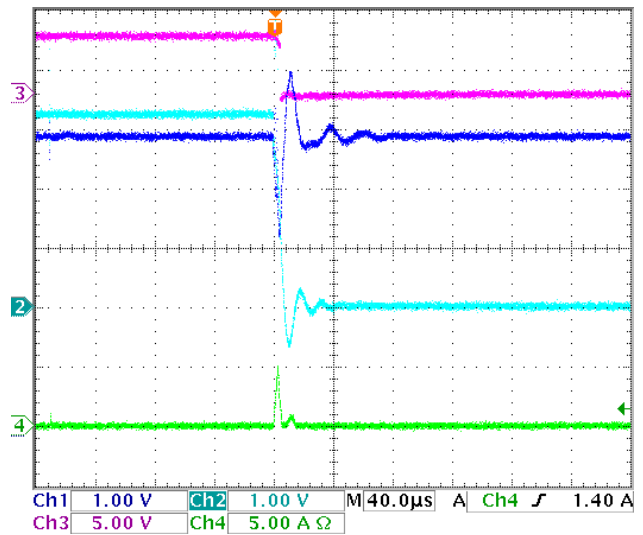


Figure 21 · Output Short 5V input 3.3V output

CH1: VIN, CH2: V_{OUT}, CH3: PGOOD,
CH4: Inductor Current

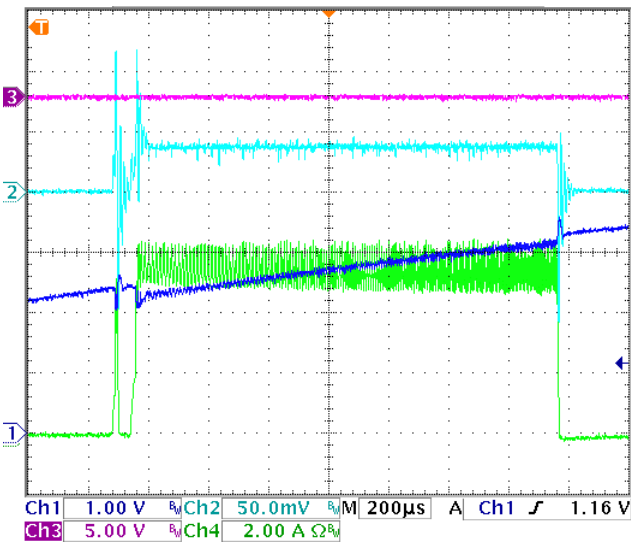


Figure 22 · Power into Short from VIN, VIN = 5V

CH1: VIN, CH2: V_{OUT}, CH3: PGOOD,
CH4: Inductor Current

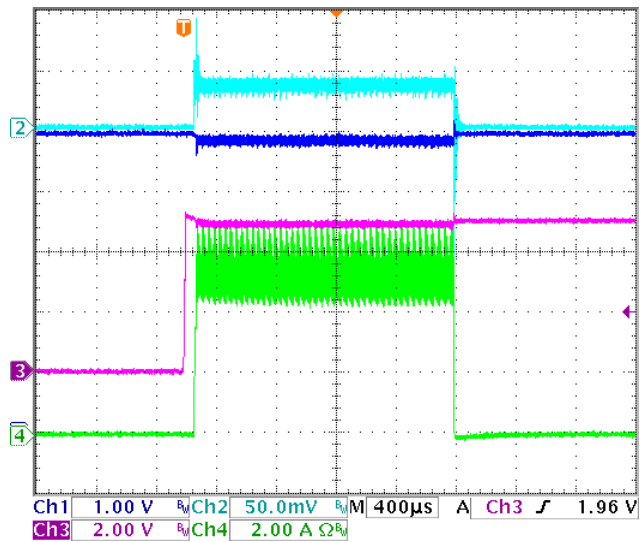


Figure 23 · Power into Short from EN, EN = VIN = 5V

CH1: VIN, CH2: V_{OUT}, CH3: PGOOD,
CH4: Inductor Current

Typical Performance Curves (Output Voltage Ripple)

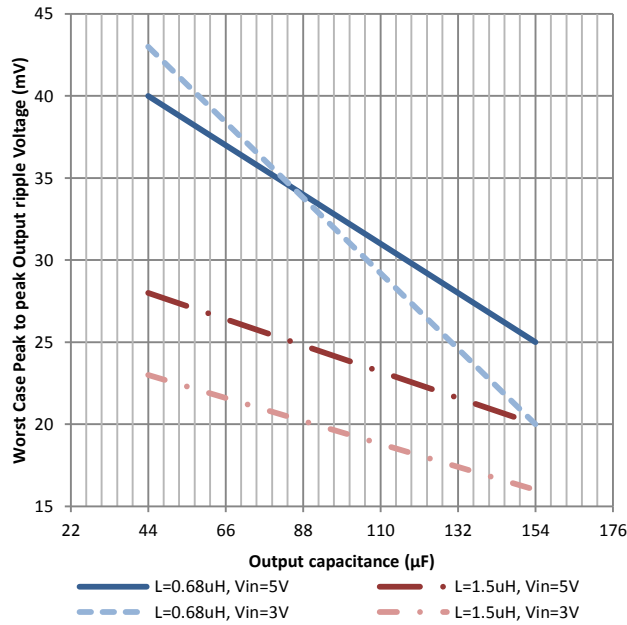


Figure 24 · No Load Peak to Peak Output Ripple

$V_{OUT} = 1V$

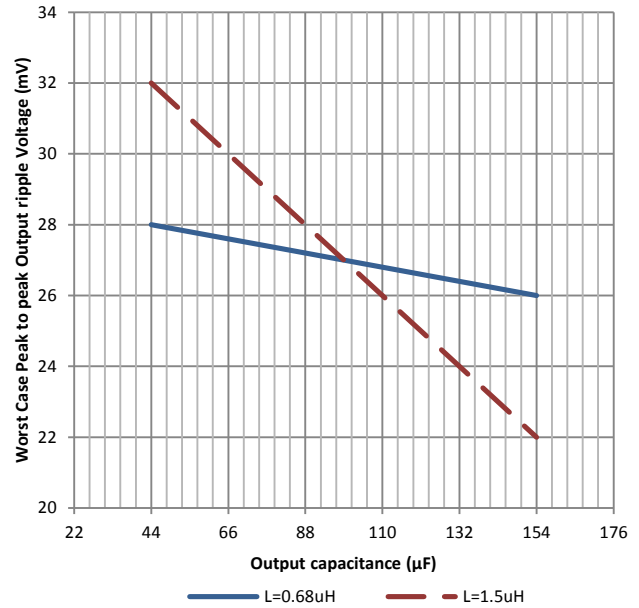


Figure 25 · No Load Peak to Peak Output Ripple

$V_{IN} = 5V, V_{OUT} = 3.3V$

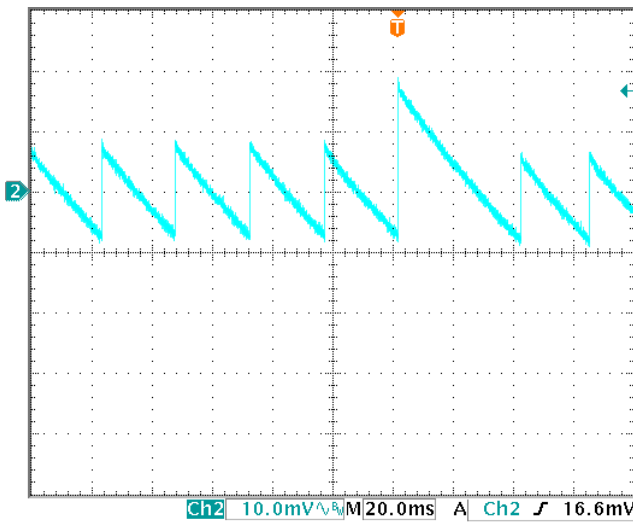


Figure 26 · No Load Peak to Peak Output Ripple

CH2: V_{OUT}
 $V_{IN} = 5V, V_{OUT} = 3.3V,$
 $L = 0.68\mu H, C_{OUT} = 154\mu F$

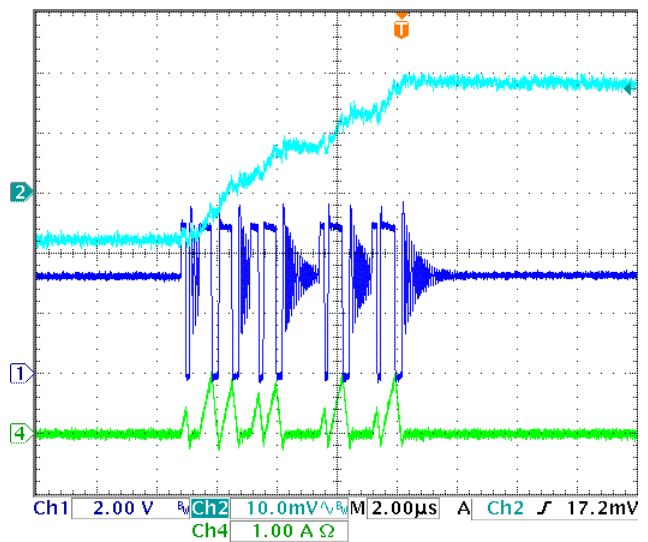


Figure 27 · Figure 26 Rising Edge Zoom In

CH1: SW, CH2: V_{OUT} , CH4: Inductor Current
 $V_{IN} = 5V, V_{OUT} = 3.3V,$
 $L = 0.68\mu H, C_{OUT} = 154\mu F$

Theory of Operation / Application Information

Basic Operation

The operation of the controller consists of comparing the V_{FB} voltage to an internal reference. When the V_{FB} voltage is lower than the V_{REF} , the upper switch turns on. When the V_{FB} voltage is higher than V_{REF} , the upper switch turns off and the lower switch turns on. An internal ramp and clock signal are used to stabilize the switching frequency and keep the V_{FB} immune to the output capacitor, C_o , value or parasitic components (i.e. ESR, ESL).

Setting of the Output Voltage

The values of R1 and R2 are chosen so according to the following equation:

$$V_{OUT} = \left(\frac{R1}{R2} + 1 \right) \times V_{REF}$$

Startup

The reference is ramped up from zero voltage to 0.8V in 1.4ms. During this time, the PGOOD is pulled low. When the reference reaches 0.8V, signaling the end of the soft start cycle, the PGOOD pin will go high within 5 μ S.

Over Current Protection

The IC has the ability to protect against all types of short circuit conditions. It has cycle by cycle short protection that turns off the upper MOSFET and ends the cycle when the current exceeds the OCP threshold. When this occurs, the off-time is at least 200ns before the upper FET is turned on again. This will clamp the current at the peak current threshold.

If the load requires more than the peak current threshold, the output voltage will drop since the current is clamped. If the output drops below the feedback UVLO threshold, the device will latch off. The enable pin can be cycled to restart the converter.

During the soft start sequence the current protection mechanism is different. If the peak current threshold is exceeded during soft start, the upper FET is turned off for approximately 1 μ s. After 1 μ s, the upper FET is turned back on. This will limit the peak output current at the peak current threshold. During soft start the feedback UVLO alarm is not active, so in the event of a short, the peak current will continue to trip until the end of the soft start period. After soft start, the feedback UVLO alarm will be active and the latch-off event will occur.

Output Component Selection Table

The table below shows the recommended resistor and feedforward capacitor values for a given output inductor and output capacitor value. See Figure 1 for the schematic location of R1, R2 and C1.

VIN	VOUT	L	Cout	R1	R2	C1
5V	1V	1.5 μ H	154 μ F (7x22 μ F)	24.9k	100k	180 pF
		0.68 μ H				100 pF
		1.5 μ H	44 μ F (2x22 μ F)			68 pF
		1 μ H				47pF
		0.68 μ H				33 pF
5V	3.3V	1.5 μ H	154 μ F (7x22 μ F)	100k	32.4k	330 pF
		0.68 μ H				220 pF
		1.5 μ H	44 μ F (2x22 μ F)			150 pF
		1 μ H				120pF
		0.68 μ H				100 pF
3V	1V	1.5 μ H	154 μ F (7x22 μ F)	24.9k	100k	180pF
		1 μ H	44 μ F (2x22 μ F)	24.9k	100k	47pF

DFN 3x3 10L PACKAGE OUTLINE DIMENSIONS

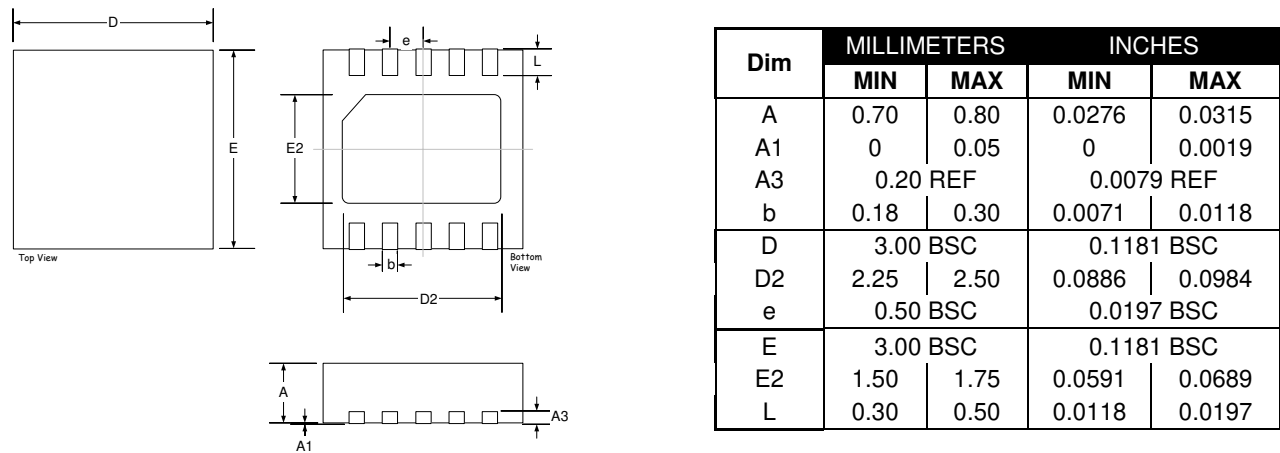


Figure 28 · Package Dimensions

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage

LAND PATTERN RECOMMENDATION

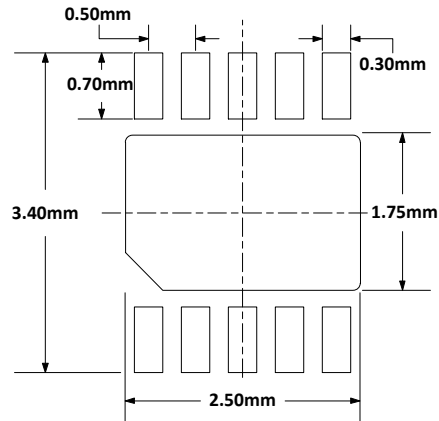


Figure 29 · Package Footprint

Disclaimer:

This PCB land pattern recommendation is based on information available to Microsemi by its suppliers. The actual land pattern to be used could be different depending on the materials and processes used in the PCB assembly, end user must account for this in their final layout. Microsemi makes no warranty or representation of performance based on this recommended land pattern.

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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