NAU8220
2Vrms Audio Line Driver

1 GENERAL DESCRIPTION

The NAU8220 is a high quality 2Vrms analog input and output line driver. This device includes an integrated charge pump enabling true ground referenced inputs and outputs and full 5.6Vpp output levels, while operating from only a single 3.3V positive supply voltage.

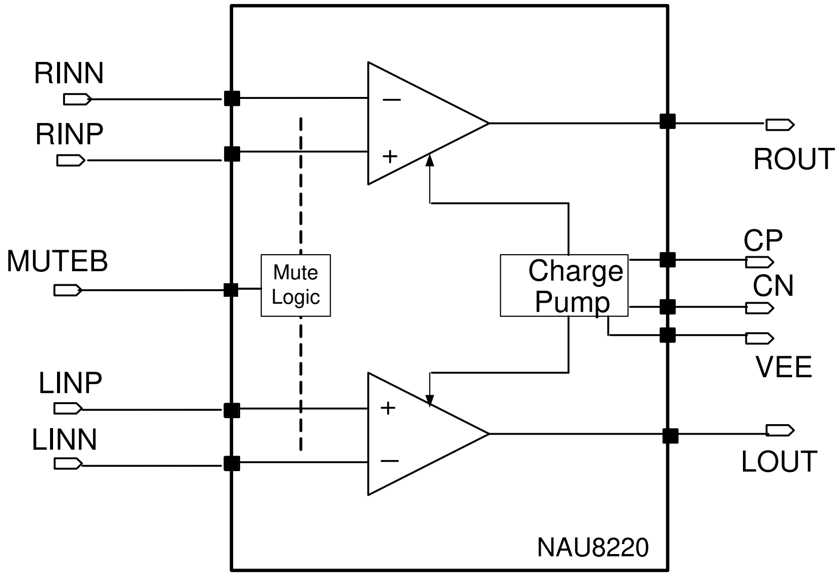
Additionally, the NAU8220 includes pop/click elimination features and high immunity to power supply and other system noise. This enables fast and efficient system integration while minimizing external component costs.

The NAU8220 is specified for operation from -40°C to +85°C, It is packaged in a cost-effective and space-saving 14-lead SOP and TSSOP packages.

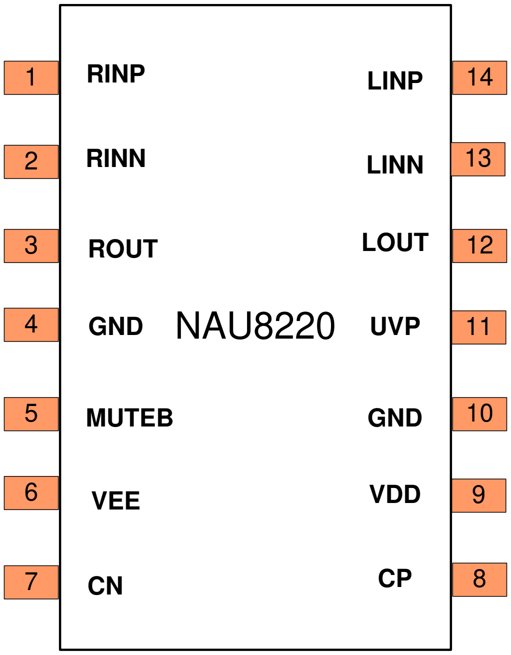
2 FEATURES

- Operating voltage: 3.0-3.6V
- Full 2Vrms output using only 3.3Vdc supply
- True Ground Referenced analog outputs
- Low cost, small footprint package
- Automatic pop/click elimination and output muting for power-on
- 108dB SNR A-weighted performance
- >90dB THD+N
- 114dB Mute Attenuation
- < 1mV Output Offset
- 110dB channel separation at 1kHz
- Low external parts count
- High system noise immunity
- Packages: Pb free 14-pin SOP and TSSOP
- Operating temperature range: -40 to +85°C
- ±8 kV HBM protection on line outputs

3 Block diagram



4 Pin Configuration



5 Pin Description

Pin No.	Pin Name	Type	Description
1	RINP	AI	Right Channel Positive Input
2	RINN	AI	Right Channel Negative Input
3	ROUT	O	Right Channel Line Output
4	GND	P	Ground
5	MUTEB	I	Mute Bar
6	VEE	IO	Charge Pump Decoupling Output (Negative Voltage)
7	CN	IO	Charge Pump Capacitor Negative Node
8	CP	IO	Charge Pump Capacitor Positive Node
9	VDD	P	Positive Voltage Supply
10	GND	P	Ground
11	UVP	I	Under Voltage Protection
12	LOUT	O	Left Channel Line Output
13	LINN	AI	Left Channel Negative Input
14	LINP	AI	Left Channel Positive Input

Table 1 Pin Description

6 Table of Contents

7 Absolute Maximum Ratings

DESCRIPTION	SYMBOL	CONDITION	MINIMUM	MAXIMUM	UNIT
VDD supply voltage	VDD	VDD–GND	-0.3	+4.0	V
Digital Input Voltage range	DV_{IN}	DV_{IN}– GND	GND – 0.3	VDD + 0.30	V
Analog Input Voltage	AV_{IN}	AV_{IN}– VEE	VEE – 0.3	VDD + 0.30	V
Operating Temperature	TA		-40	+85	°C
Storage Temperature	Tst		-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such Conditions may adversely influence product reliability and result in failures not covered by warranty. Follow IC handling procedures to avoid ESD damage.

8 Recommended Operating Conditions

DESCRIPTION	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Supply voltage	VDD	3.0	3.3	3.6	V
Ground	GND		0		V

9 Electrical Characteristics

Test Conditions VDD = 3.3V, TA = +25°C, 1 V rms 1 kHz signal, R1 (IN) = 15kΩ, R2 (FB) = 30kΩ, CP = 1µF, RL = 10kΩ unless otherwise stated.

Parameter	Sym	Test Conditions	Min	Typ	Max	Unit
Full Scale Output Voltage	Vout		2.0		-	Vrms
Signal to Noise Ratio	SNR	A-weighted	90	108	-	dB
Dynamic Range	DNR	A-weighted	90	108	-	dB
Total Harmonic Distortion + Noise	THD+N	20 kHz LPF	90	102	-	dB
Power Supply Rejection Ratio	PSRR	VDD = 3.0 V to 3.6 V		100		dB
Power Supply Rejection Ratio[1]	AC PSRR	100Hz	-	90	-	dB
		1kHz		75	-	dB
		20kHz	-	60	-	dB
Channel Separation		1kHZ	-	-110	-	dB
Noise Voltage	VN	A-weighted	-	8	-	µV
Mute Noise Voltage	VN	A-weighted MUTEB=GND	-	4	-	µV
Output Offset			-1	0.5	+1	mV
Output Impedance when muted	ZM	MUTEB = GND		0.6		Ω
Input to output attenuation when muted	MdB	MUTEB = GND		114		dB
UVP detect voltage	VUVP			1.2		Volts
UVP feedback current	IUVP			5		µA
Current Limit	ILIMIT	Output = GND		30		mA AC
Supply Current	IDD	VDD = 3.3 Volts		15		mA
Charge pump switching frequency	FCP	Pin CP		300		kHz
Low input level	VIL	MUTEB		40		% VDD
High input level	VIH	MUTEB		60		% VDD
Input current	IIN	MUTEB GND or VDD	-1		+1	µA
Load Resistance	RL	Maximum signal	600	10k		Ω
Load Capacitance	Cload	LOUT,R OUT	0	-	200	pF

Notes

1. The performance of AC PSRR depends upon the board layout.

10 Functional Description

The NAU8220 uses charge pump mechanism to get the full output signal swing. The charge pump uses the charge pump capacitor to put a negative voltage onto VEE, the charge pump decoupling node. An additional capacitor is needed from VDD to GND, pin 10. A low resistance one micro-farad capacitor is recommended for each of these capacitors. All of these connections need to be short. The negative voltage developed on pin 6 VEE enables the outputs to swing both positive and negative from GND.

Signal gain is set by the ratio of external resistors. The input signal can be either single ended or differential. The typical single ended application diagram is shown in figure 1 and differential in figure 2. For single ended inputs, the signal polarity of the output is inverted. A gain of two using R1 = 15 K Ohms and R2 = 30 K Ohms is recommended for good performance. R3 of 10 K Ohms helps to reject unwanted signals by balancing the inputs. For larger gains, R2 can be increased. R1 can also be decreased, but 10 K Ohms is the minimum recommended. For example, a gain of three could use R1 = 10 K Ohms, R2 = 30 K Ohms, and R3 = 7.5 K Ohms. For better performance R3 and R6 should be approximately equal to R1||R2 and R4||R5. Gains larger than ten are not recommended. Large gains will have more noise and distortion than the nominal gain of two. The following table shows the R1 and R2 resistance values for different gain settings.

Gain	Input Resistance, R1	Feedback Resistance, R2
-1	10k Ohms	10k Ohms
-2	15k Ohms	30k Ohms
-3	10k Ohms	30k Ohms
-10	10k Ohms	100k Ohms

Table 2 Recommended resistor values for different gain settings

Load of the line driver outputs is from 600 Ohms minimum to 10 K Ohms nominal. With VDD at 3.3 Volts, the maximum output signal is 2 Volts RMS. Capacitive loads up to 200 pF can be driven. If larger capacitive loads such as 2.2 nF (C_{PC}) need to be driven, then a resistance of at least 33 Ohms (R_{PC}) should be added in series to provide both stability and protection. R_{PC} and C_{PC} are resistance and capacitance of the protection circuit as shown in Figure 1 and Figure2. If this resistor and capacitor are added for protection, then the components need to be properly rated. For example, 100 volts rating for the capacitor may be needed to survive an output surge.

For best output offset voltages, the inputs can be AC coupled.

Upon the application of power to the VDD pin, the part will enter into a pop reduction mode which applies a resistive loading to the two outputs. After the VEE pin reaches more than about 1.5 Volts, a power up sequence begins that places the outputs into the Mute condition. This condition is held until both the MUTEB pin is held high and the UVP pin exceeds about 1.25 Volts. When the MUTEB pin rises, the outputs will follow the input signals. This pin should not be raised until a valid signal is available. The MUTEB pin is driven by a logic signal to GND or VDD.

The MUTE condition can be entered from normal operation by pulling MUTEB low. If power is interrupted, the UVP pin can be used to force the part into the MUTE condition.

The UVP pin can force the part into the Mute condition when the power supply voltage drops below the desired voltage. If this function is not needed, the UVP pin should be connected to VDD. Feed back is provided by a nominal 5 µA current developed across the external resistors applied. The turn on voltage sets the ratio of R11 and R12 compared to the internal 1.22 Volt reference. The formula for turn ON voltage is V_{ON} = 1.22V * (R11 + R12)/R11 and the formula for the turn off voltage is V_{OFF}= V_{ON} - (5uA * R12).

For example, for a turn on voltage of 3.0 Volts and a turn off voltage of 2.5 volts, the calculated resistors are R11 = 68.5kΩ and R12 = 100kΩ, or using standard values, R11 = 68kΩ and R12 = 100kΩ.

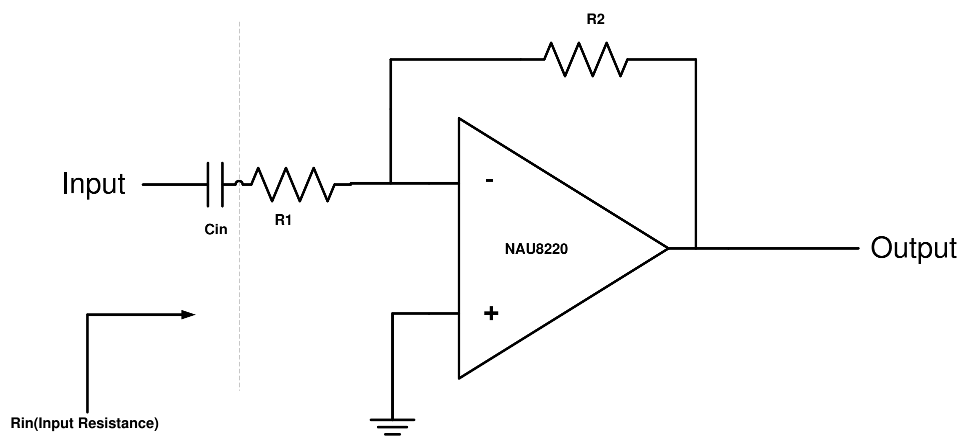
Important note: When using a LDO, the turn-on and turn-off voltages for the UVP should be set higher than the sum of 3.3V and the minimum required voltage drop across the LDO, to ensure proper operation.

11 Amplifier circuits

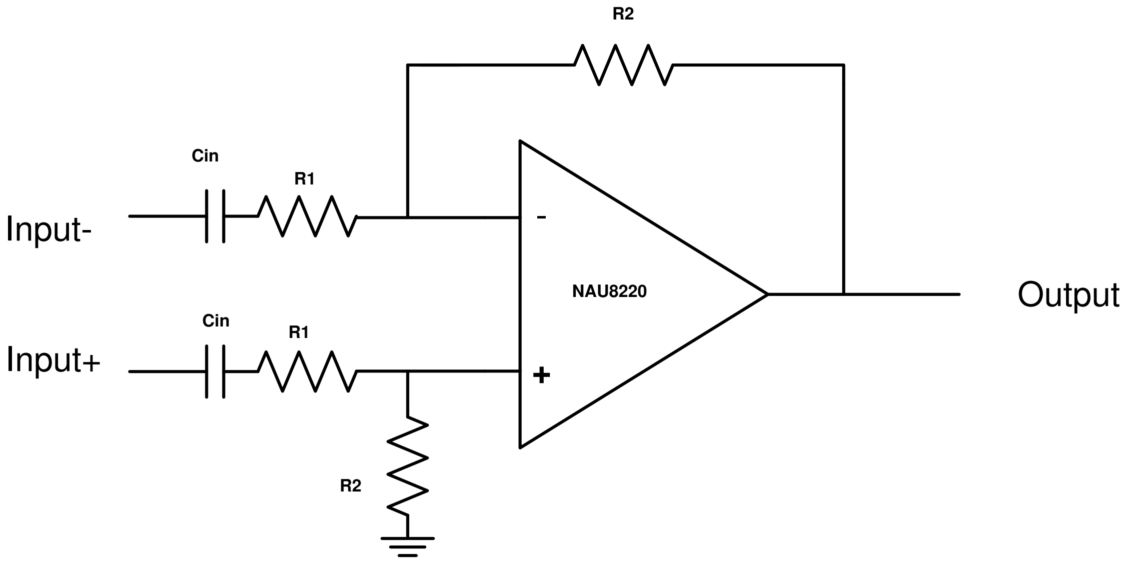
NAU8220 can be used to implement the amplifier configurations in single ended and differential mode. The following diagram shows the NAU8220 in single ended (inverting) and differential amplifier configuration modes. Notice the similarities between these two configurations. The differential input function is accomplished by duplicating the values used in single ended configuration. The required gain can be achieved by properly selecting the R1 and R2 values as per the Table 2.

An ac coupling capacitor (Cin) is used to block the dc content from the input source. The input resistance of the amplifier (Rin) together with the Cin will act as a high pass filter. So depending on the required cut off frequency the Cin can be calculated by using the following formula

$Cin = 1/2\pi Rinfc$ where fc is the desired cut off frequency of the High pass filter.



Inverting Amplifier Configuration



Differential Amplifier Configuration

12 Low Pass Filter Circuit

Many of the today's Digital to Analog Converters (DACs) requires low pass filter circuit to remove the out of band noise produced by the sigma-delta modulator. Most commonly used filter is multiple feedback (MFB) 2^{nd} order low pass filter. The advantage of the MFB filter is, it requires fewer components compared to the other filter configurations. The following diagrams show the 2^{nd} order Low pass filter in single ended and differential mode.

The transfer function for the MFB filter (single ended mode) is

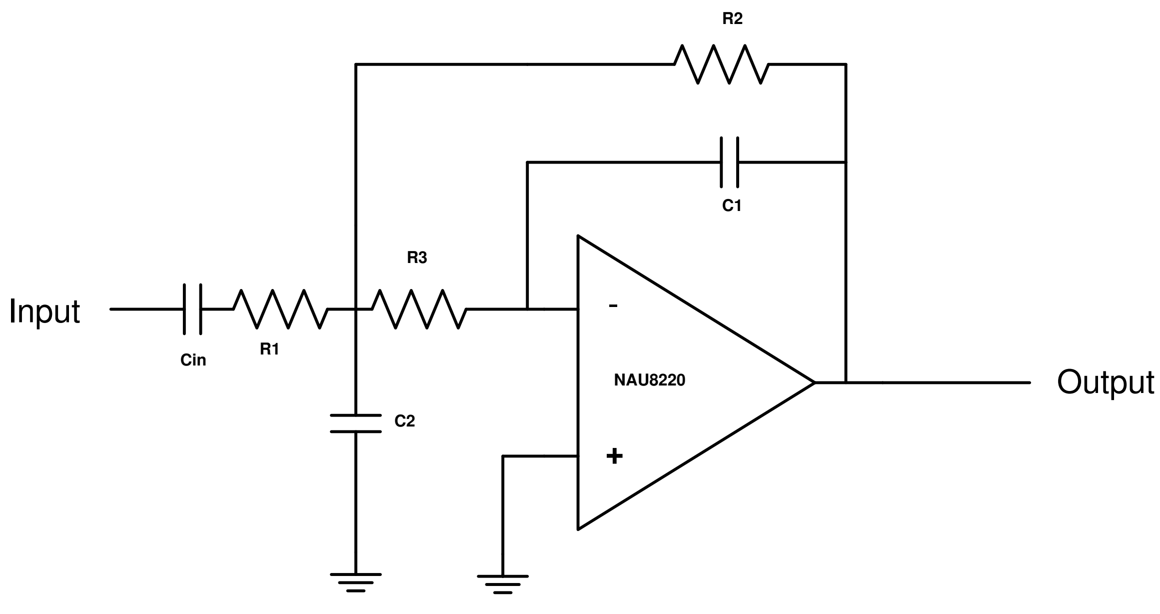
$$\frac{Vo}{Vi} = -\frac{\frac{1}{C1C2R1R3}}{S^2 + S\left(\frac{1}{C2}\right)\left(\frac{1}{R1}+\frac{1}{R2}+\frac{1}{R3}\right) + \left(\frac{1}{C1C2R3R2}\right)}$$

By comparing this equation with following the standard 2nd order Low pass filter equation, the component values can be calculated for a given cut off frequency (fc) and Q (Quality factor) value.

$$\frac{Vo}{Vi} = \frac{(2\pi fc)^2 K}{S^2 + 2\zeta(2\pi fc)S + (2\pi fc)^2}$$

Where $Q(Quality\ factor) = 1/2\zeta(Damping\ ratio)$

$$K(Gain) = -\frac{R2}{R1}$$



Single ended 2nd order Low pass filter

Example1: Design a second order single ended MFB Low pass filter with following specifications. Cut off Frequency = 50 kHz, Quality factor, Q= 0.707 and Gain, K = -2.

Step 1: Find R1 and R2 depending on the gain. By assuming R1 = 10kOhms and using the equation $K = -\frac{R2}{R1}$ the value of the R2 = 20kOhms.

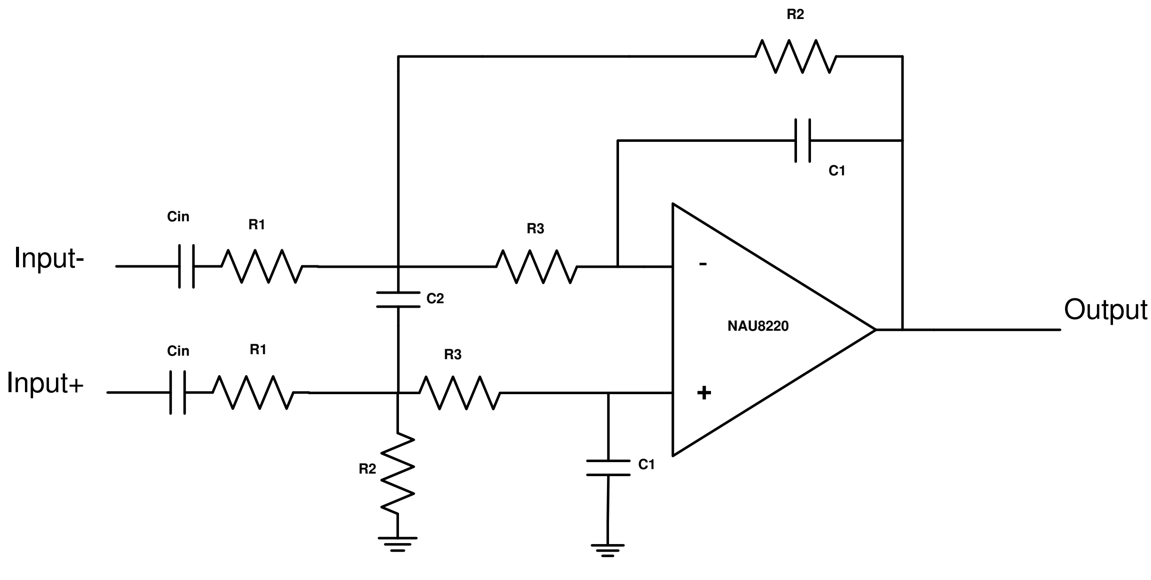
Step2: Using the equation $\frac{2\pi fc}{Q} = (\frac{1}{C2})(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3})$, Calculate R3 by assuming C2 = 1000pF

R3 = 3.3kOhms

Step3: Using the equation $(2\pi fc)^2 = \frac{1}{C1C2R3R2}$, the C1 = 150pF

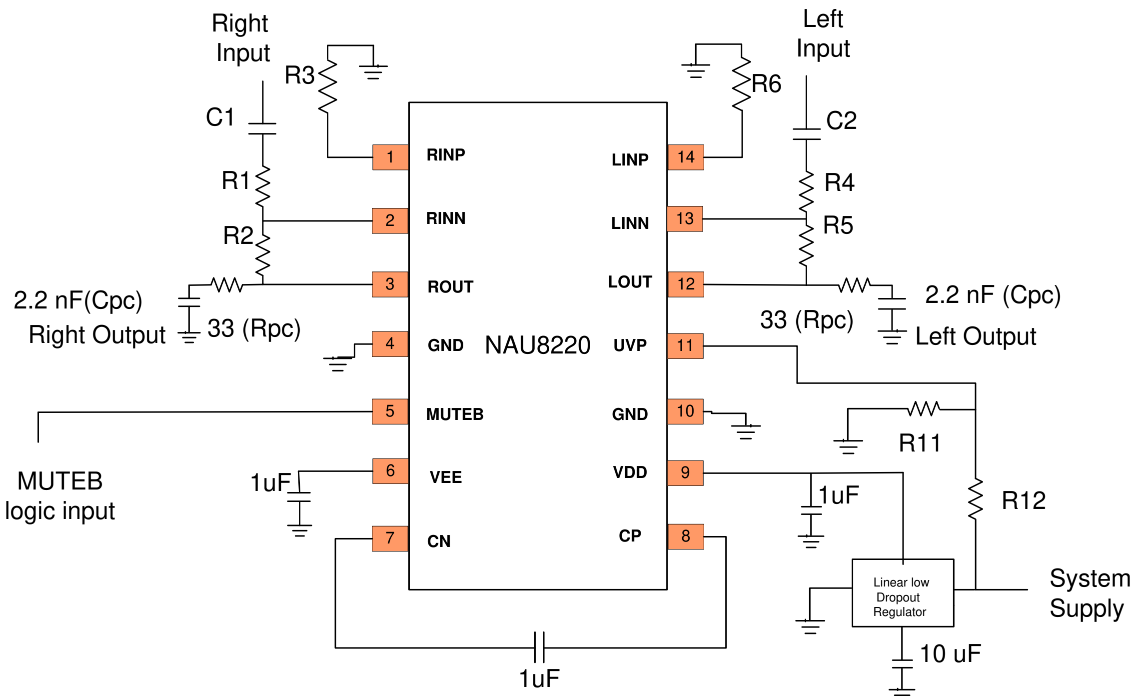
Example2: Design a second order differential mode MFB Low pass filter with following specifications. Cut off Frequency = 50 kHz, Quality factor, Q= 0.707 and Gain, K = -2.

The differential mode configuration can be achieved by duplicating the above example 1 values except the C2. The C2 value in this configuration is half of the value of the single ended configuration.



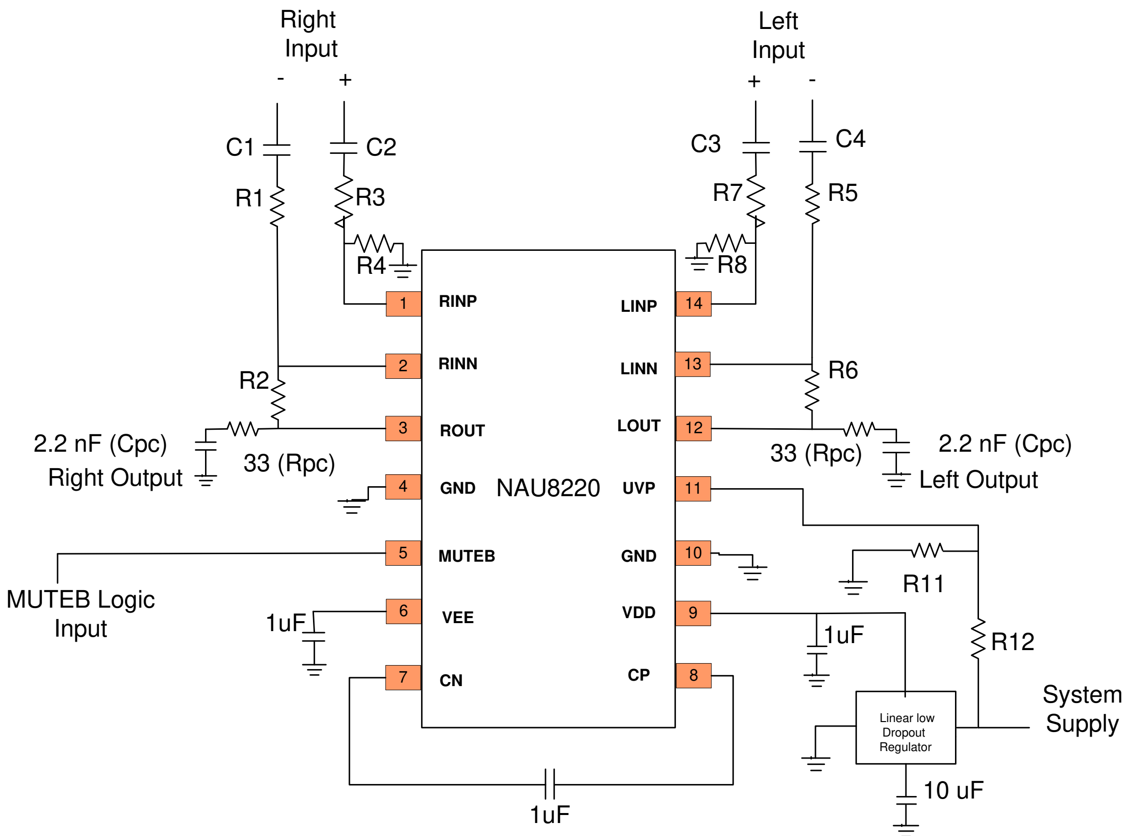
Differential 2nd order Low pass filter

13 Typical Application Diagram



R1 = R4 = 15 KOhms
R2 = R5 = 30 KOhms
R3 = R6 = 10 Kohms
C1 = C2 = 2.2 uF

Figure 1 Single Input Amplifier Configuration



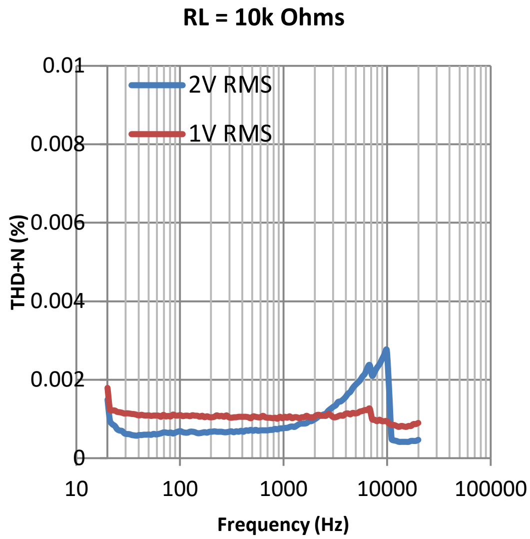
R1 = R3 = R5 = R7= 15 KOhms
R2 = R4 = R6 = R8 = 30 KOhms
C1 = C2 = C3 = C4 = 2.2 uF

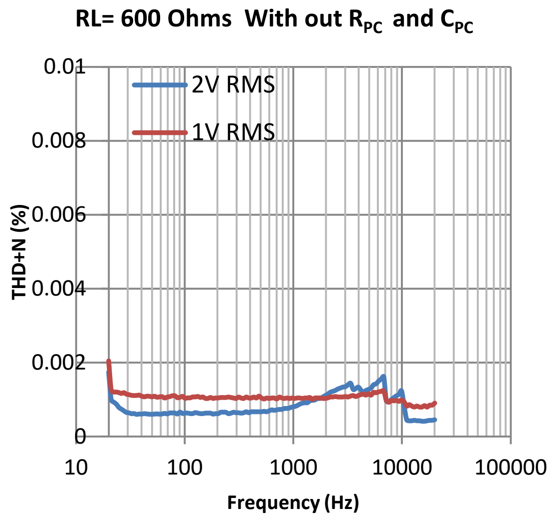
Figure 2 Differential Input Amplifier Configuration

14 Typical Characteristics

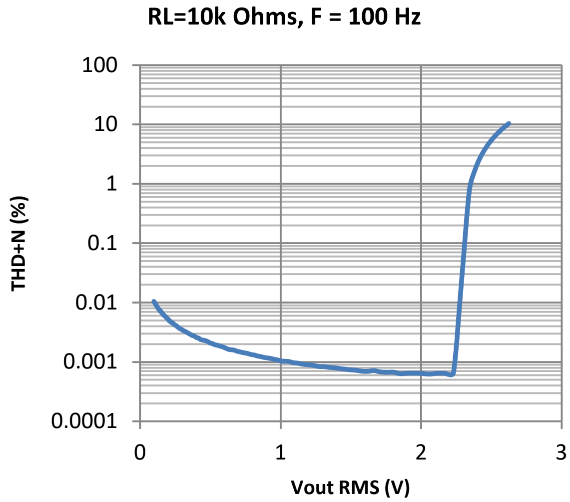
Test Conditions VDD = 3.3V, TA = +25°C, 1kHz signal, R1 (IN) = 15kΩ, R2 (FB) = 30kΩ, CP = 1µF, RL = 10kΩ, C_{PC} = 2200pF, R_{PC}= 33 Ohms unless otherwise stated.

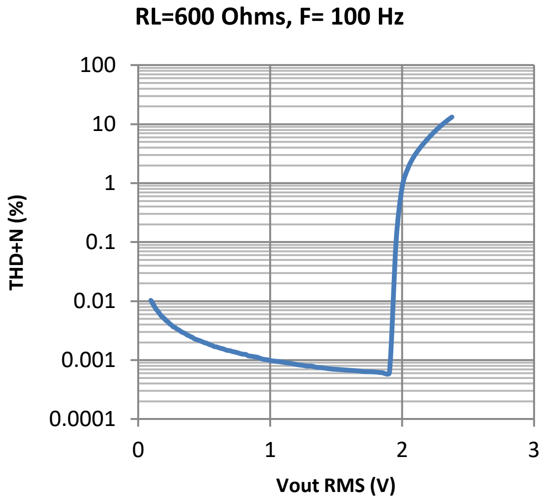
Total Harmonic Distortion + Noise Vs Frequency

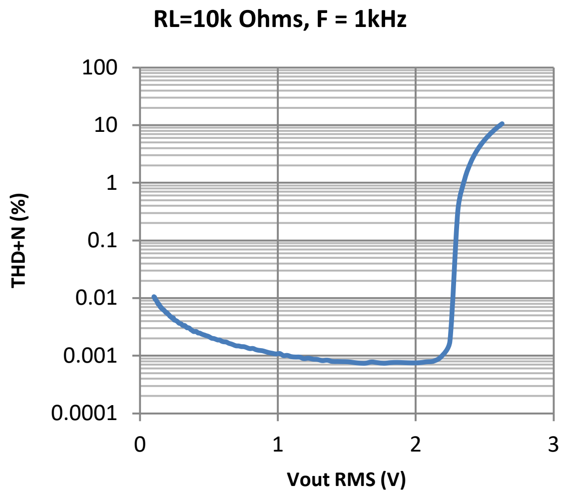


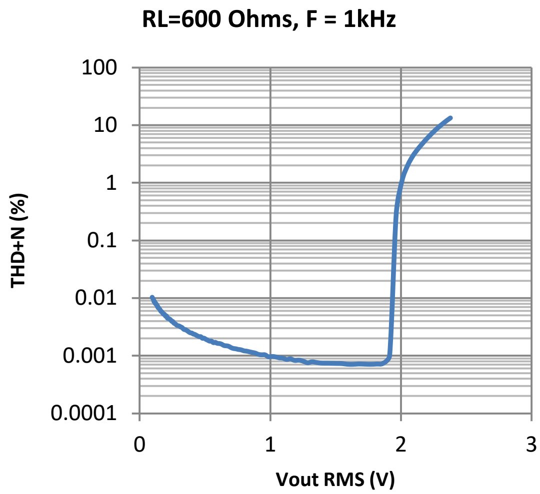


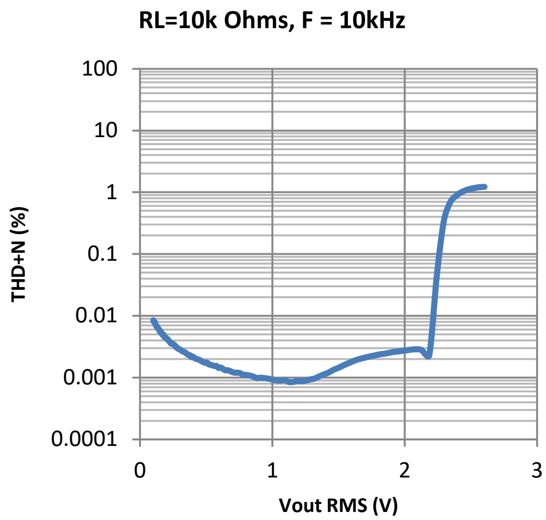
Total Harmonic Distortion + Noise Vs Output Voltage

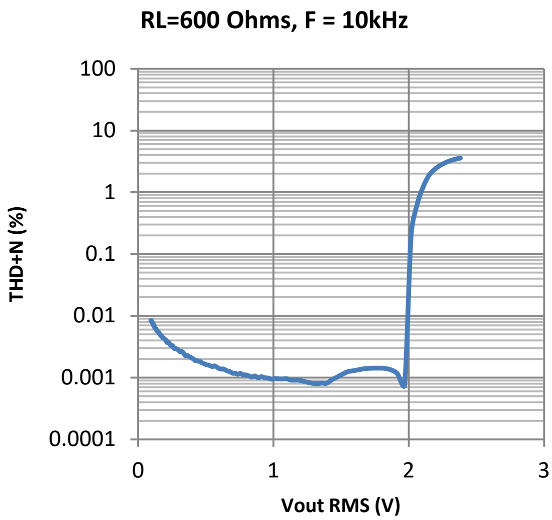




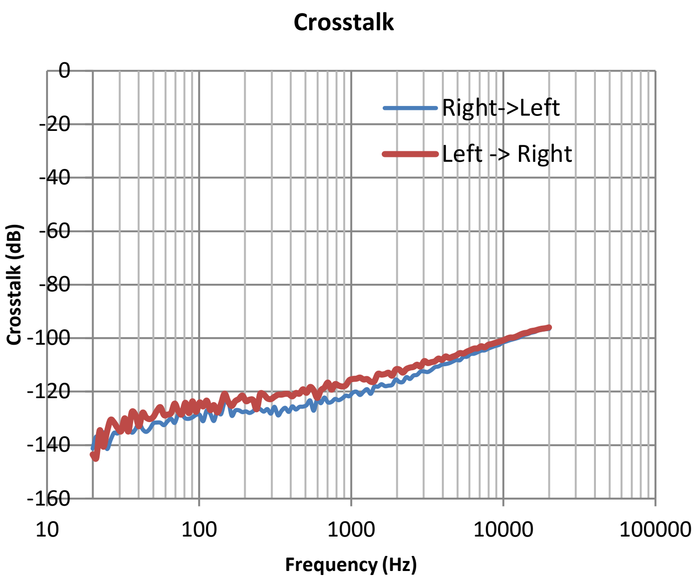

RL=10k Ohms, F = 1kHz
100
10
1
0.1
0.01
0.001
0.0001
THD+N (%)
0
1
2
3
Vout RMS (V)


RL=600 Ohms, F = 1kHz
100
10
1
0.1
0.01
0.001
0.0001
THD+N (%)
0
1
2
3
Vout RMS (V)


RL=10k Ohms, F = 10kHz
100
10
1
0.1
0.01
0.001
0.0001
THD+N (%)
0
1
2
3
Vout RMS (V)

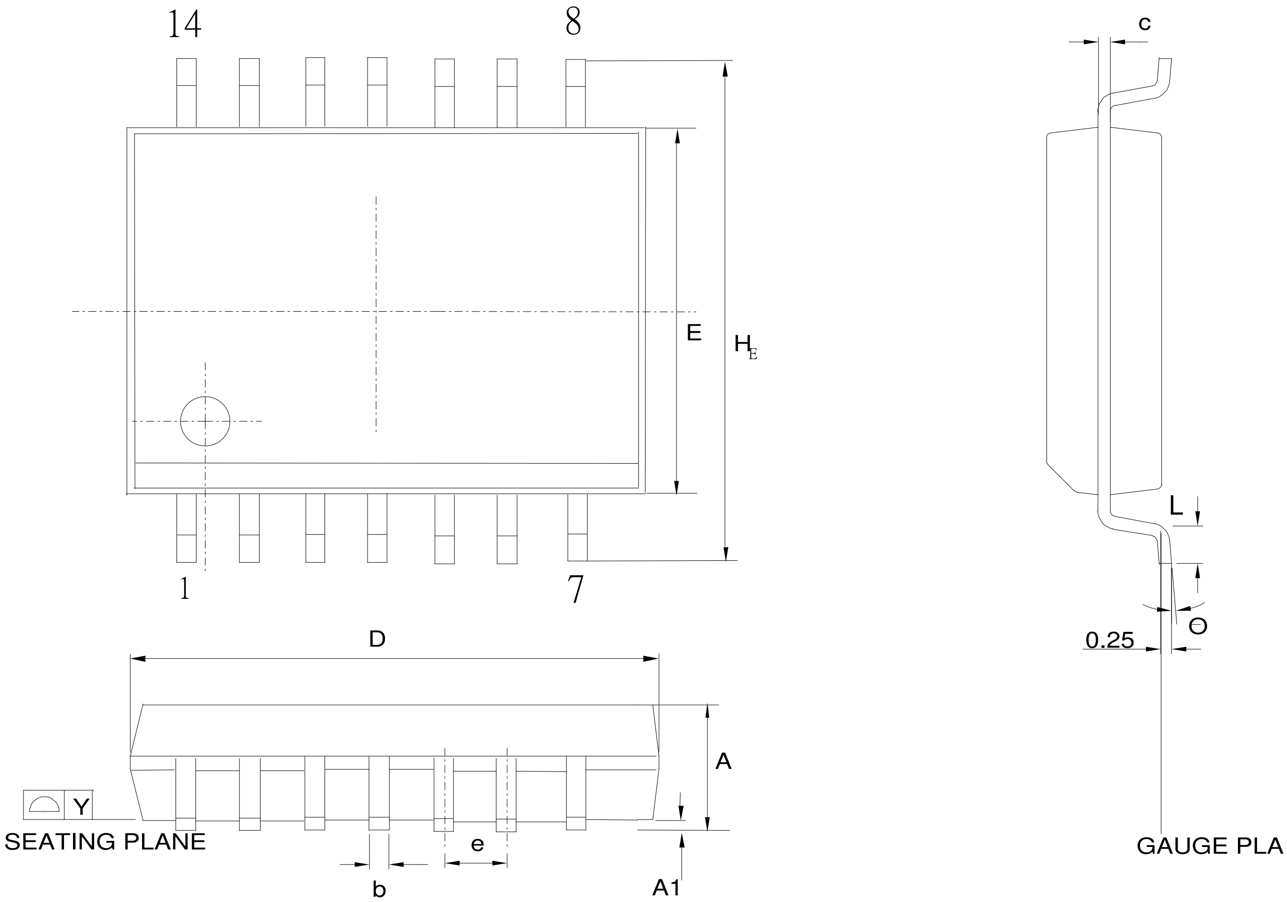

RL=600 Ohms, F = 10kHz
100
10
1
0.1
0.01
0.001
0.0001
THD+N (%)
0
1
2
3
Vout RMS (V)

Cross talk Vs Frequency



15 Package Specification

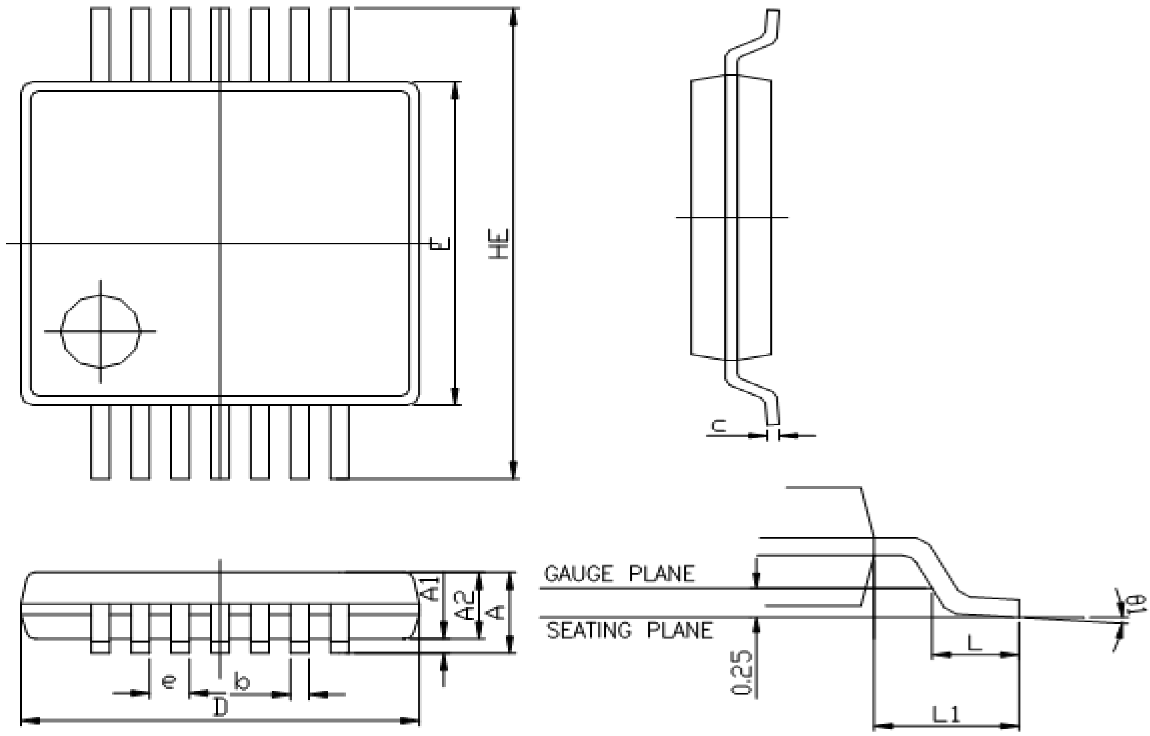
15.1 SOP-14 PACKAGE



Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E	3.80	4.00	0.150	0.157
D	8.55	8.75	0.337	0.344
e	1.27 BSC		0.050 BSC	
H_E	5.80	6.20	0.228	0.244
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

15.2 TSSOP-14 Package (14L 4.4X5.0 MM^2)



CONTROLLING DIMENSION: MILLMETERS						
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	---	---	1.20	---	---	0.043
A1	0.05	---	0.15	0.02	---	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
L	0.50	0.60	0.75	0.020	0.024	0.030
HE	6.40 BSC.			0.252 BSC.		
E	4.30	4.40	4.50	0.169	0.173	0.177
D	4.90	5.00	5.10	0.193	0.197	0.201
b	0.19	---	0.30	0.007	---	0.012
c	0.09	---	0.20	0.004	---	0.008
L1	1.0 REF.			0.039 REF.		
e	0.65 BSC.			0.026 BSC.		
θ1	0	---	8	0	---	8

16 Ordering Information

Part Number	Dimension	Package	Package Material
NAU8220SG	8.75x4 mm	SOP-14	Green
NAU8220WG	5x4.4 mm	TSSOP-14	Green

NAU8220 _ _

Package Material:

G = Pb-free Package

Package Type:

S = 14-Pin SOP Package

W = 14-Pin TSSOP Package

Revision History

VERSION	DATE	PAGE	DESCRIPTION
1.8	Feb 2012	9	Added application circuit diagram with differential configuration.
1.9	March 2012	14	Added TSSOP package dimensions information
2.0	June, 2012	6,8-11,12,13	1. Corrected Application circuit diagram. Changed value of input DC blocking capacitors to 2.2 uF. 2.Added Load resistance and Load capacitance column in the Electrical characteristics table 3.Added amplifier circuit and 2^{nd} order LPF circuit

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.