

Low voltage low on-resistance SPDT switch with break-before-make feature



SOT323-6L

Features

- High speed:
 - $t_{PD} = 0.3 \text{ ns}$ (max) at $V_{CC} = 4.5 \text{ V}$
 - $t_{PD} = 0.8 \text{ ns}$ (max) at $V_{CC} = 3.0 \text{ V}$
 - $t_{PD} = 1.2 \text{ ns}$ (max) at $V_{CC} = 2.3 \text{ V}$
- Ultra low power dissipation:
 - $I_{CC} = 1 \mu\text{A}$ (max) at $T_A = 85 \text{ }^\circ\text{C}$
- Low on-resistance; at $V_{IN} = 0 \text{ V}$:
 - $R_{ON} = 7 \Omega$ (max $T_A = 85 \text{ }^\circ\text{C}$) at $V_{CC} = 4.5 \text{ V}$
 - $R_{ON} = 9 \Omega$ (max $T_A = 85 \text{ }^\circ\text{C}$) at $V_{CC} = 3.0 \text{ V}$
- Wide operating voltage range:
 - V_{CC} (OPR) = 1.65 V to 5.5 V single supply
- TTL threshold ON control input at $V_{CC} = 2.7$ to 3.6 V
- Pin and function compatible with 74 series 3157
- Latch-up performance exceeds 150 mA (JESD 17)

Description

The **STG3157** is a high-speed CMOS analog SPDT (single-pole double-throw) switch or 2:1 multiplexer/demultiplexer bus switch manufactured using silicon gate CMOS technology. It is designed to operate from a 1.65 V to 5.5 V supply, making the device ideal for portable applications.

The **STG3157** features very low on-resistance ($< 9 \Omega$) at $V_{CC} = 3.0 \text{ V}$. The IN input is provided to control the SPDT switch, and is compatible with standard CMOS output. Switch S1 is ON (connected to common port D) when the IN input is held high, and OFF (a high impedance state exists between the two ports) when IN is held low.

Switch S2 is ON (connected to common port D) when the IN input is held low and OFF (a high impedance state exists between the two ports) when IN is held high.

Additional key features are fast switching speed, break-before-make delay time, and very low power consumption. All inputs and outputs are equipped with protection circuits to protect against static discharge, giving them immunity from ESD and transient excess voltage.

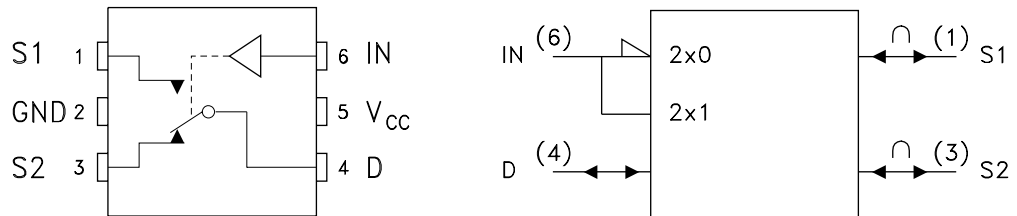
Maturity status link

[STG3157](#)

Device summary

Order code	STG3157CTR
Package	SOT323-6L
Packing	Tape and reel

1 Pin configuration

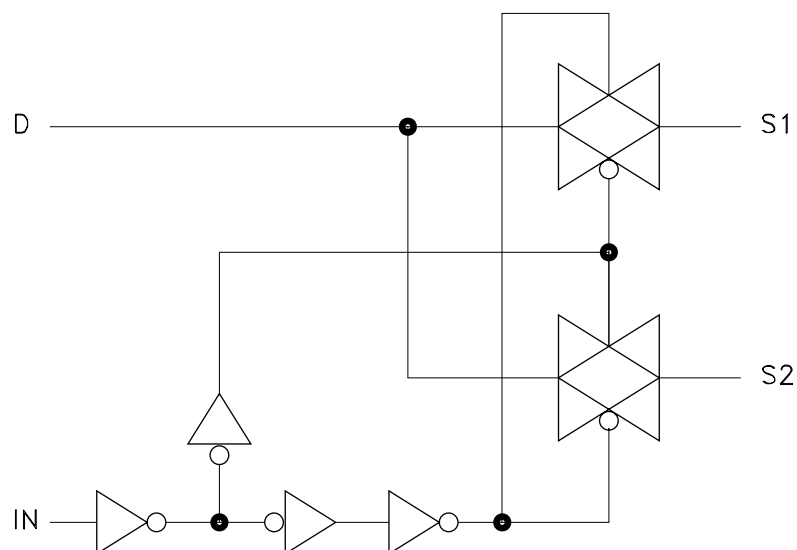
Figure 1. Pin connections and IEC logic symbols

Table 1. Truth table

IN	Switch S1	Switch S2
H	ON	OFF ⁽¹⁾
L	OFF ⁽¹⁾	ON

1. High impedance

Table 2. Pin descriptions

Pin N°	Symbol	Name and function
1, 3	S1, S2	Independent channels
4	D	Common channels
6	IN	Control
5	VCC	Positive supply voltage
2	GND	Ground (0 V)

Figure 2. Input equivalent circuit


2 Maximum ratings

Stressing the device above the ratings listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_{IC}	DC control input voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IKC}	DC input diode current on control pin ($V_{IN} < 0$ V)	±50	mA
I_{IK}	DC input diode current ($V_{IN} < 0$ V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	+128	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 s)	300	°C

Table 4. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	1.65 to 5.5	V
V_I	Input voltage	0 to V_{CC}	V
V_{IC}	Control input voltage	0 to 5.5	V
V_O	Output voltage	0 to V_{CC}	V
T_{op}	Operating temperature	-55 to 125	°C
dt/dv	Input rise and fall time control input	$V_{CC} = 1.65$ V to 2.7 V	0 to 20
		$V_{CC} = 3.0$ to 4.5 V	0 to 10

1. Truth table guaranteed: 1.2 V to 6.0 V

3 Electrical characteristics

3.1 DC Electrical characteristics

Table 5. DC specifications

Symbol	Parameter	Test conditions		Value						Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High level input voltage	1.65-1.95		0.75V _C			0.75V _{CC}		0.75V _{CC}		V
		2.3-2.5		0.7V _{CC}			0.7V _{CC}		0.7V _{CC}		
		2.7-3.6		2			2		2		
V _{IL}	Low level input voltage	1.65-1.95				0.25V _{CC}		0.25V _{CC}		0.25V _{CC}	V
		2.3-2.5				0.3V _{CC}		0.3V _{CC}		0.3V _{CC}	
		2.7-3.6				0.8		0.8		0.8	
R _{ON}	Switch on-resistance	4.5	V _S = 0 V I _S = 30 mA	4.4	7		7		9	Ω	
			V _S = 2.4 V I _S = 30 mA	4.9	12		12		14.5		
			V _S = 4.5 V I _S = 30 mA	6.1	15		15		18		
		3.0	V _S = 0 V I _S = 100 mA	5.2	9		9		11		
			V _S = 3 V I _S = 24 mA	7.8	20		20		24		
		2.3	V _S = 0 V I _S = 8 mA	6.5	12		12		14.5		
			V _S = 2.3 V I _S = 8 mA	9.6	30		30		36		
		1.65	V _S = 0 V I _S = 4 mA	9.0	20		20		24		
V _S = 1.65 V I _S = 4 mA	14		50		50		60				
ΔR _{ON}	On-resistance match between channels	4.5	V _S = 3.15 V I _S = 30 mA	0.10						Ω	
		3.0	V _S = 2.1 V I _S = 24 mA	0.10							
		2.3	V _S = 1.6 V I _S = 8 mA	0.20							
		1.65	V _S = 1.15 V I _S = 4 mA	0.35							

Symbol	Parameter	Test conditions		Value						Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
R _{FLAT}	On-resistance flatness	5.0	V _S = 0 V to V _{CC} I _S = 30 mA		3						Ω
		3.3	V _S = 0 V to V _{CC} I _S = 24 mA		6						
		2.5	V _S = 0 V to V _{CC} I _S = 8 mA		14						
		1.8	V _S = 0 V to V _{CC} I _S = 4 mA		80						
I _{OFF}	OFF state leakage current	1.65 - 195	V _S = 0 to V _{CC}		±0.05	±0.1		± 1		± 10	μA
I _{IN}	Input leakage current	0 - 5.5	V _{IN} = 0 to 5.5 V		±0.05	±0.1		± 1		± 10	μA
I _{CC}	Quiescent supply current	1.65 - 4.3	V _{IN} = V _{CC} or GND			1		1		10	μA

3.2 AC Electrical characteristics

 $C_L = 50 \text{ pF}$, $R_L = 500 \text{ } \Omega$
Table 6. AC specification

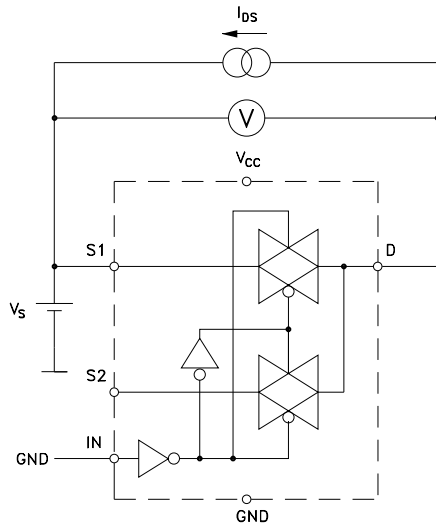
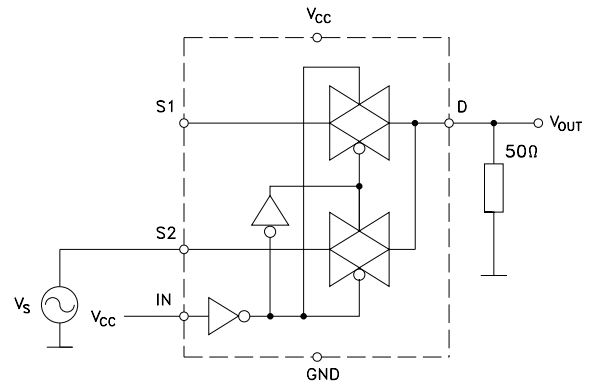
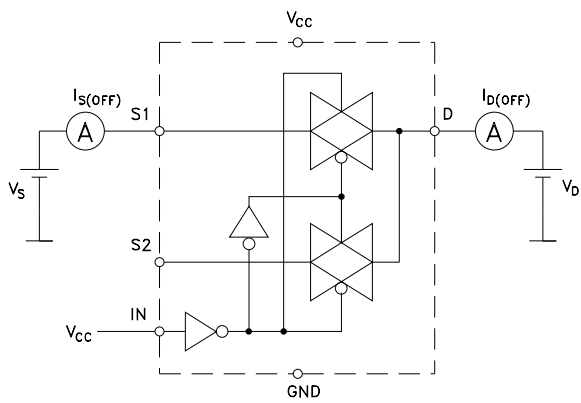
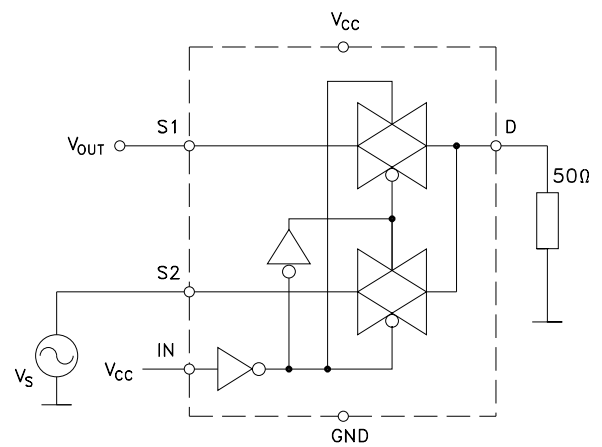
Symbol	Parameter	Test conditions		Value						Unit	
		$V_{CC}(V)$		$T_A = 25 \text{ } ^\circ\text{C}$			$-40 \text{ to } 85 \text{ } ^\circ\text{C}$		$-55 \text{ to } 125 \text{ } ^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{LH} , t_{HL}	Propagation delay	1.65-1.95	$V_I = \text{Open}$								ns
		2.3-2.7				1.2		1.2		1.8	
		3.0-3.3				0.8		0.8		1.2	
		4.5-5.5				0.3		0.3		0.5	
t_{PZH} , t_{PZL}	Output enable time (D to Sn)	1.65-1.95		7		15	7	20	7	27	ns
		2.3-2.7		3.5		11	3.5	14	3.5	17	
		3.0-3.3		2.5		7	2.5	7.6	2.5	9	
		4.5-5.5		1.7		5.2	1.7	5.7	1.7	7	
t_{PLZ} , t_{PHZ}	Output disable time (D to Sn)	1.65-1.95		3		10	3	13	3	16	ns
		2.3-2.7		2		7	2	7.5	2	9	
		3.0-3.3		1.5		5	1.5	5.3	1.5	6.5	
		4.5-5.5		1.7		3.5	1.7	3.8	1.7	5	
t_D	Break-before-make time delay	1.65-5.5		0.5			0.5		0.5		ns
Q	Charge injection	5			23						pC
		3.3			19						

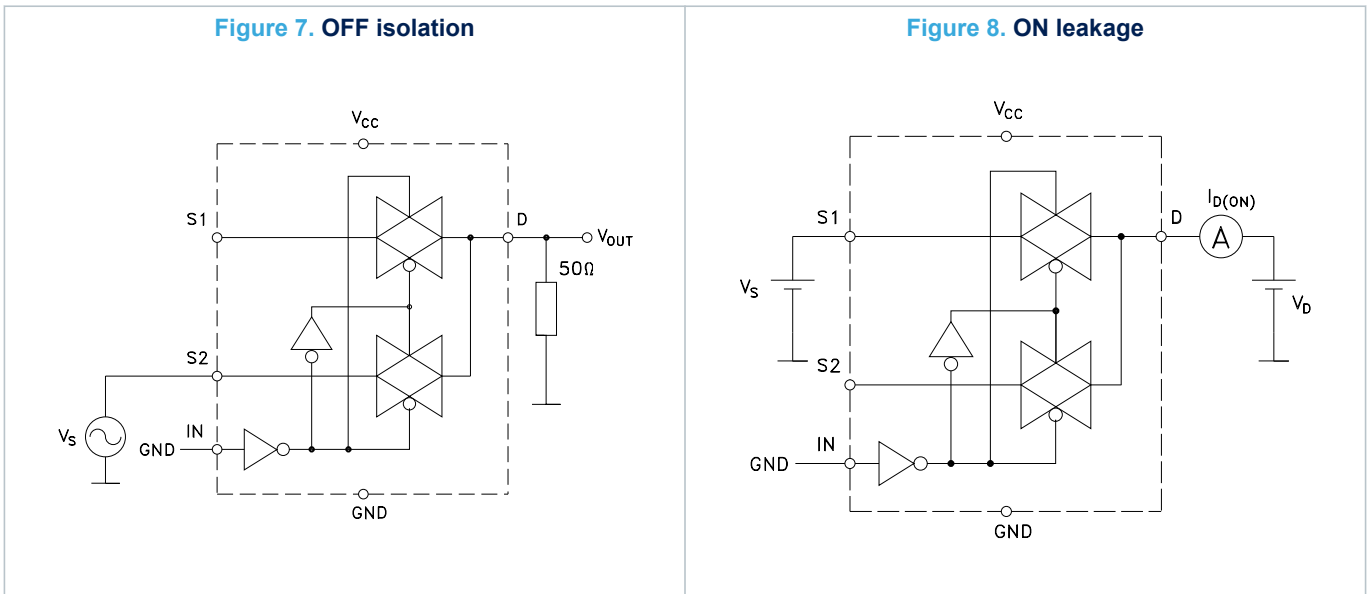
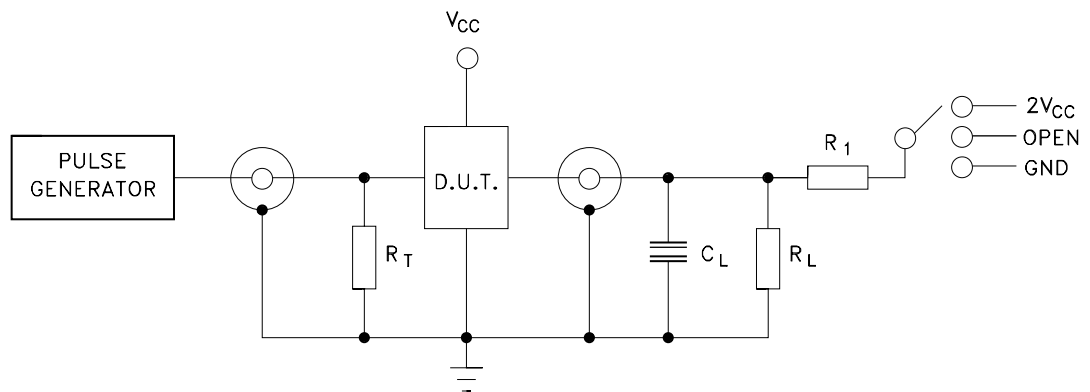
3.3 Analog switch characteristics

 $C_L = 5 \text{ pF}$, $R_L = 50 \text{ } \Omega$, $T_A = 25 \text{ } ^\circ\text{C}$
Table 7. Analog switch characteristics

Symbol	Parameter	Test conditions		Value						Unit	
		$V_{CC}(V)$		$T_A = 25 \text{ } ^\circ\text{C}$			$-40 \text{ to } 85 \text{ } ^\circ\text{C}$		$-55 \text{ to } 125 \text{ } ^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
OIRR	Off isolation	1.65-5.5	$R_L = 50 \text{ } \Omega$ $f = 10 \text{ MHz}$		-57						dB
Xtalk	Crosstalk	1.65-5.5	$R_L = 50 \text{ } \Omega$ $f = 10 \text{ MHz}$		-54						dB
BW	- 3 dB bandwidth	1.65-5.5	$R_L = 50 \text{ } \Omega$		250						MHz
C_{IN}	Control pin input capacitance				5						pF
CS_n	Sn port capacitance	5.0	$f = 1 \text{ MHz}$		13						
C_D	D port capacitance when switch is enabled	5.0	$f = 1 \text{ MHz}$		21						

4 Test circuits

Figure 3. On-resistance

Figure 4. Bandwidth

Figure 5. OFF leakage

Figure 6. Channel-to-channel crosstalk



Figure 9. Test circuit

Table 8. Test circuit

Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	V_{CC}
t_{PZH} , t_{PHZ}	GND

Note: $C_L = 5/35 \text{ pF}$ or equivalent: (includes jig capacitance)
 $R_L = 50 \Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 10. Break-before-make time delay

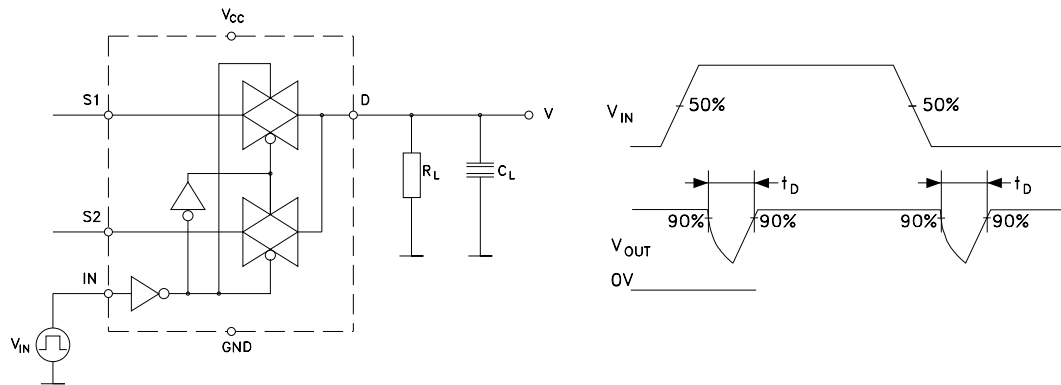


Figure 11. Switching time and charge injection

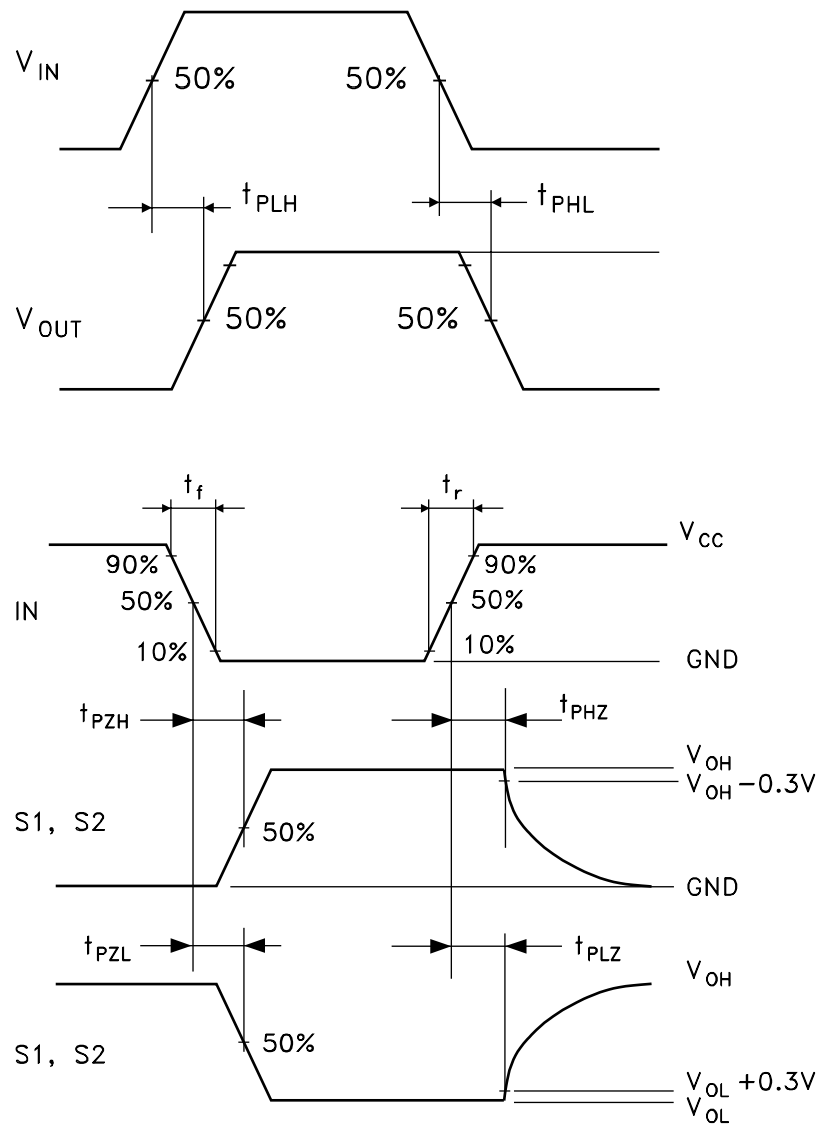
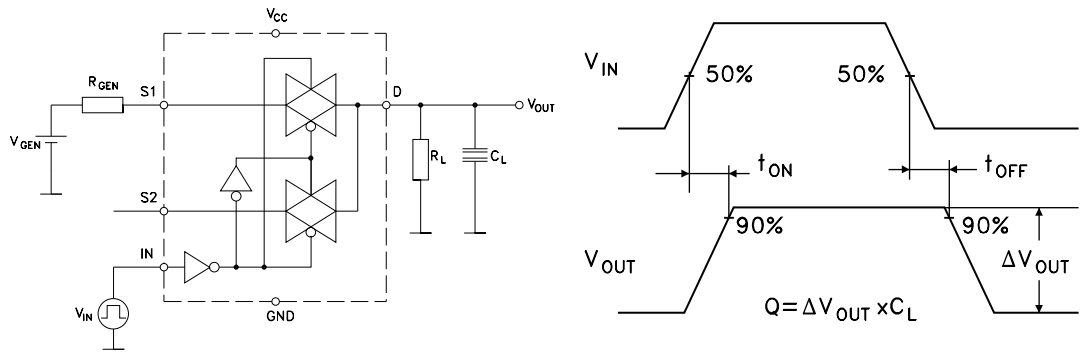


Figure 12. Charge injection ($V_{GEN} = 0\text{ V}$, $R_{GEN} = 0\ \Omega$, $R_L = 1\text{ M}\Omega$, $C_L = 100\text{ pF}$)



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 SOT323-6L package information

Figure 13. SOT323-6L package drawing outline

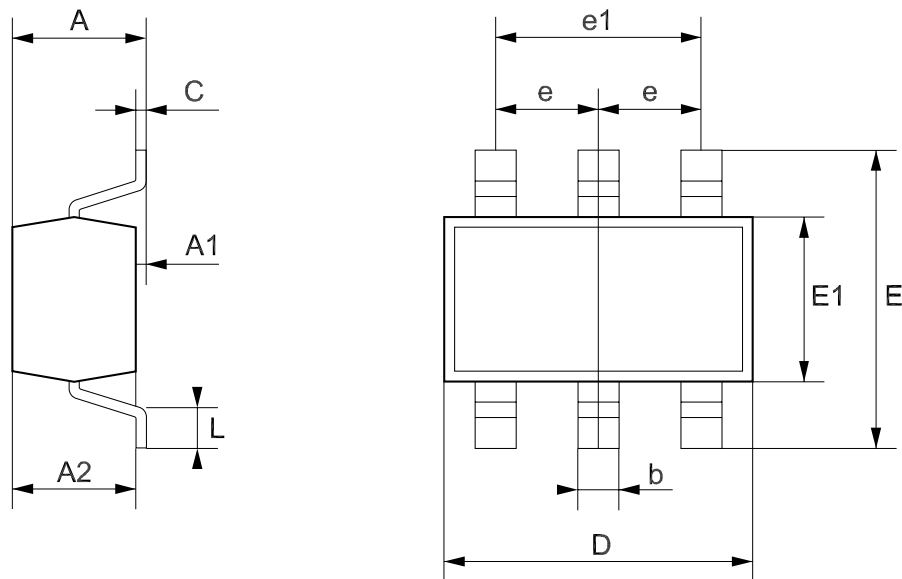


Table 9. SOT323-6L mechanical data

Dim.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	31.5		43.3
A1	0.00		0.10	0.0		3.9
A2	0.80		1.00	31.5		39.4
b	0.15		0.30	5.9		11.8
C	0.10		0.18	3.9		7.1
D	1.80		2.20	70.9		86.6
E	1.80		2.40	70.9		94.5
E1	1.15		1.35	45.3		53.1
e		0.65			25.6	
e1		1.3			51.2	
L	0.10		0.30	3.9		11.8

Figure 14. SOT323-6L footprint recommendation

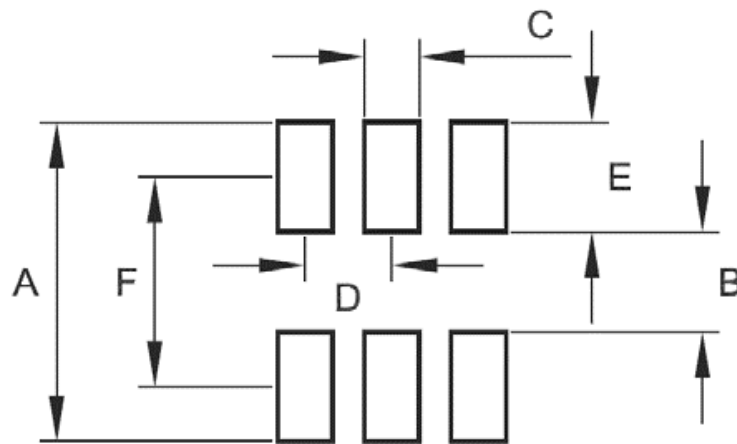


Table 10. SOT323-6L footprint recommendation

Dim.	mm.	inch
A	2.88	0.113
B	0.78	0.031
C	0.36	0.014
D	0.65	0.026
E	1.05	0.041
F	1.65	0.065

5.2 SOT323-6L packing information

Figure 15. SOT323-6L tape information

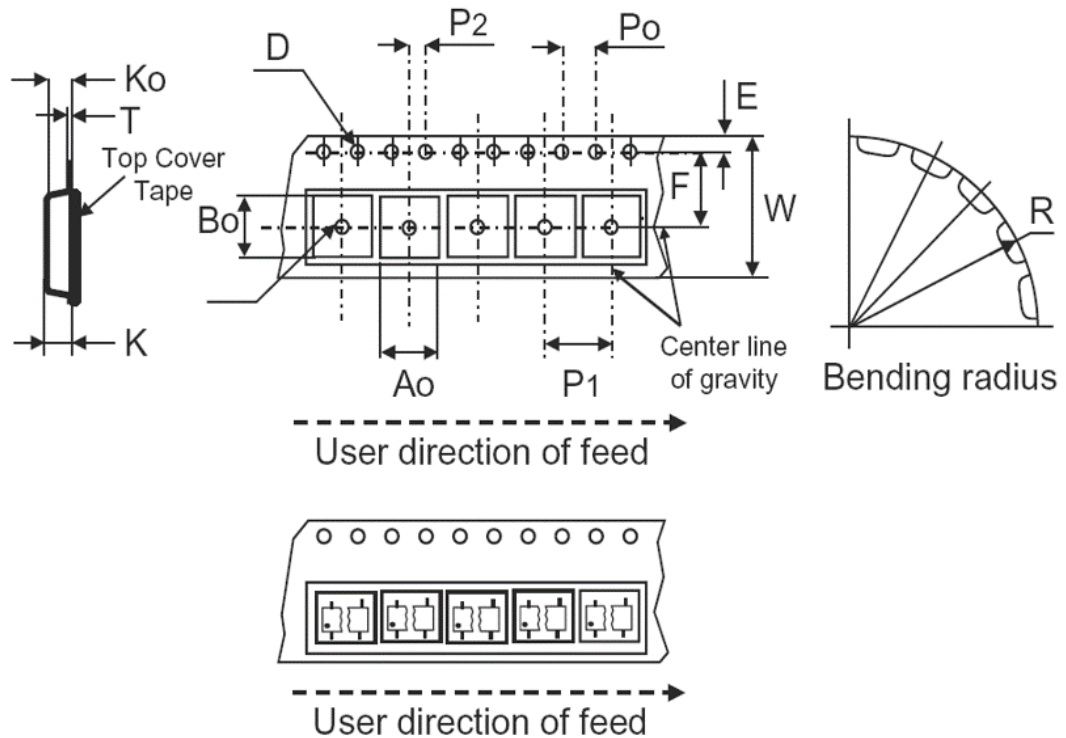


Table 11. SOT323-6L tape information

Dim	mm.	inch
D	1.50 +0.1/0	0.059 +0.004/0
E	1.75 ±0.1	0.069 ±0.004
Po	4.00 ±0.1	0.157 ±0.004
T max.	0.40	0.016
D1 min.	1	0.039
F	3.5 ±0.05	0.138 ±0.002
K max.	2.40	0.094
P2	2.00 ±0.05	0.079 ±0.002
R	25	0.984
W	8.00 ±0.30	0.315 ±0.012
P1	4.00	0.157
Ao, Bo, Ko	0.05 min to 0.50 max	0.002 min to 0.020 max

Figure 16. SOT323-6L reel information

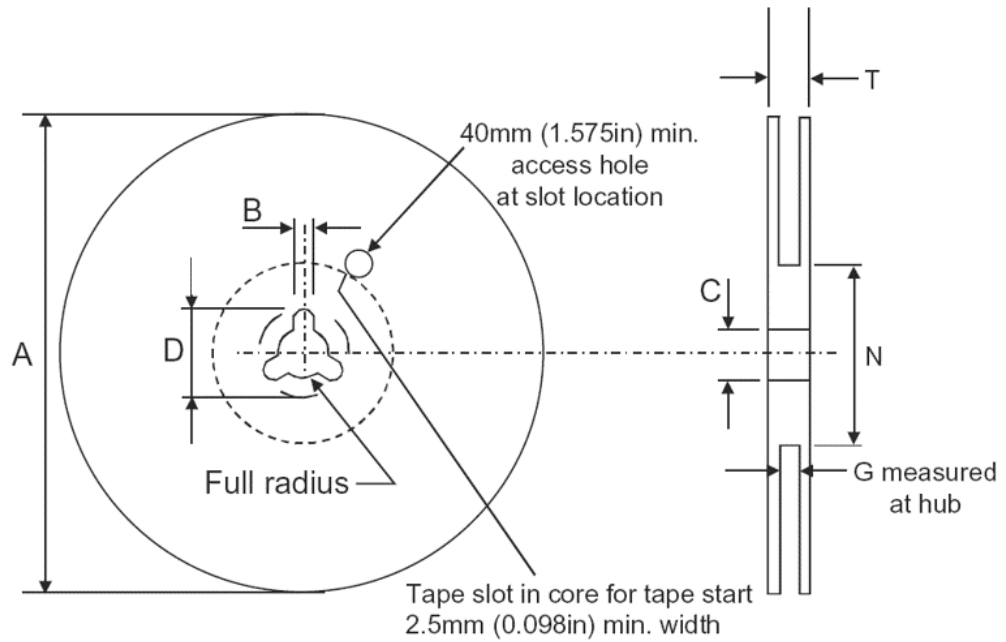


Table 12. SOT323-6L reel information

Dim	mm.	inch
Tape size	8.0 ±0.30	0.315 ±0.012
A max.	180.0	7.086
B min.	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D min.	20.2	0.795
N min.	60	2.362
G	8.4 +2/-0	0.319 +0.079/-0
T max.	14.4	0.567

6 Ordering information

Table 13. Order code

Order code	Package	Packing	Marking
STG3157CTR	SOT323-6L	Tape and reel	VU

Revision history

Table 14. Document revision history

Date	Revision	Changes
02-Sep-2002	1	Initial release.
19-Apr-2010	2	Document reformatted. In the Features list on the coverpage, updated the "Latch-up performance exceeds" value from 300 mA to 150 mA. Minor text changes throughout the document. Replaced Order codes table on the coverpage with Table 1: Device summary. Added ECOPACK® statement in Section 5: Package information.
29-Nov-2018	3	Updated V_{CC} value on Table 4. Recommended operating conditions.
20-Jul-2021	4	Added new Section 6 Ordering information .

Contents

1	Pin configuration	2
2	Maximum ratings	3
3	Electrical characteristics	4
3.1	DC Electrical characteristics	4
3.2	AC Electrical characteristics	6
3.3	Analog switch characteristics	6
4	Test circuits	7
5	Package information	11
5.1	SOT323-6L package information	11
5.2	SOT323-6L packing information	13
6	Ordering information	15
	Revision history	16
	List of tables	18
	List of figures	19

List of tables

Table 1.	Truth table	2
Table 2.	Pin descriptions	2
Table 3.	Absolute maximum ratings	3
Table 4.	Recommended operating conditions	3
Table 5.	DC specifications	4
Table 6.	AC specification	6
Table 7.	Analog switch characteristics	6
Table 8.	Test circuit	8
Table 9.	SOT323-6L mechanical data	11
Table 10.	SOT323-6L footprint recommendation	12
Table 11.	SOT323-6L tape information	13
Table 12.	SOT323-6L reel information	14
Table 13.	Order code	15
Table 14.	Document revision history	16

List of figures

Figure 1.	Pin connections and IEC logic symbols	2
Figure 2.	Input equivalent circuit	2
Figure 3.	On-resistance	7
Figure 4.	Bandwidth	7
Figure 5.	OFF leakage	7
Figure 6.	Channel-to-channel crosstalk	7
Figure 7.	OFF isolation	8
Figure 8.	ON leakage	8
Figure 9.	Test circuit	8
Figure 10.	Break-before-make time delay	9
Figure 11.	Switching time and charge injection	9
Figure 12.	Charge injection ($V_{GEN} = 0\text{ V}$, $R_{GEN} = 0\ \Omega$, $R_L = 1\text{ M}\Omega$, $C_L = 100\text{ pF}$)	10
Figure 13.	SOT323-6L package drawing outline	11
Figure 14.	SOT323-6L footprint recommendation	12
Figure 15.	SOT323-6L tape information	13
Figure 16.	SOT323-6L reel information	14

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