

DESCRIPTION

The MP5418A is a monolithic negative charge pump with a built-in adjustable negative regulator. It has a 2.3V to 5V input range, and provides an unregulated output that equals negative input voltage. The MP5418A also provides a regulated output between 0V and negative input voltage.

No external inductor is required for simplicity and compactness. An internal soft-start circuit effectively reduces the inrush current during start-up.

The MP5418A is available in an ultra-low profile QFN-10 (1.4mmx1.8mm) package. The MP5418A requires four ceramic capacitors to get the minimum solution size. It is ideal for a wide range of applications, including optical modules, RF amplifiers, and sensor supplies.

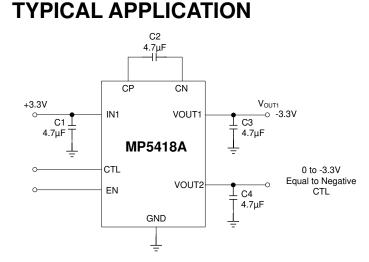
FEATURES

- 2.3V to 5V V_{IN} Range
- Up to 200mA Output Current
- Only 4 x 4.7µF Capacitor Required for 60mA
- Low V_O Ripple with Fixed Frequency Control
- EN Control
- No Inrush Current during Start-Up
- Short Current Protection
- Dual-Output:
 - o -1x Charge Pump
 - \circ Regulated Output between 0V and -V_{IN}
- Available in a QFN-10 (1.4mmx1.8mm) Package

APPLICATIONS

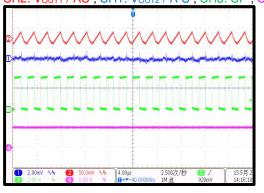
- Optical Modules
- Bias for RF Amplifiers
- Sensor Supply in Portable Instruments

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Steady State

Iout1 = 0A, Iout2 = 60mA CH2: Vout1 / AC ; CH1: Vout2 / A C ; CH3: CP ; CH4: CTL





ORDERING INFORMATION

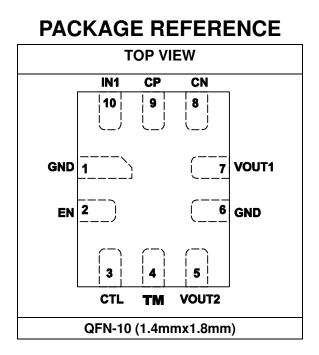
Part Number*	Package	Top Marking	MSL Rating	
MP5418AGQG	QFN10 (1.4mmx1.8mm)	See Below	1	

* For Tape & Reel, add suffix –Z (e.g. MP5418AGQG–Z).

TOP MARKING

KG LL

KG: Product code of MP5418AGQG LLL: Lot number



MP5418A Rev. 1.0 4/15/2020 MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited. © 2020 MPS. All Rights Reserved.



PIN FUNCTIONS

Pin #	Name	Description
1	GND	Power ground.
2	EN	On/off control.
3	CTL	Analog input voltage. The VOUT2 voltage is -1x the CTL pin voltage.
4	ТМ	Test mode pin. For factory use only. Float TM or connect it to GND. Do not connect TM to other pins.
5	VOUT2	Negative linear regulator output. A decoupling capacitor is required.
6	GND	Power ground.
7	VOUT1	Negative charge pump output. A decouple capacitor is needed.
8	CN	Fly capacitor negative terminal.
9	CP	Fly capacitor positive terminal.
10	IN1	Supply voltage. The MP5418A operates from a 2.3V to 5V unregulated input. Decouple capacitor is required to prevent large voltage spikes from appearing at the input.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V _{IN})	6V
V _{CP}	
V _{CN}	V _{OUT} - 0.3V to +0.3V
V _{OUT1}	6V to +0.3V
V _{OUT2}	V _{OUT1} to 0.3V
All other pins(except Pin4)	0.3V to +6V
Junction temperature	150°C
Lead temperature	260°C
Continuous power dissipatio	on (T _A = 25°C) ^{(2) (4)}
	1.47W
Storage temperature	65°C to +150°C

ESD Rating

Human body model (HBM)	±2kV
Charged device model (CDM)	±2kV

Recommended Operating Conditions ⁽³⁾

Thermal ResistanceθJAθJcQFN-10 (1.4mmx1.8mm)

EV5418A-G-00A ⁽⁴⁾	85	45 °C/W
JESD51-7 ⁽⁵⁾	140	30 °C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-toambient thermal resistance, θ_{JA} , and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on EV5418A-G-00A, 2-layer, 1OZ, 63mmx63mm PCB.
- 5) The value of 0_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.



ELECTRICAL CHARACTERISTICS

 V_{IN} = 3.3V, T_J = -40°C to +125°C ⁽⁶⁾, typical value is tested at T_J = 25°C. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units
V _{IN} Range			2.3		5	V
Under-voltage lockout rising threshold				2.2	2.3	V
Under-voltage lockout hysteresis threshold			100	180	260	mV
Shutdown supply current		$V_{EN} = 0V$		1.5	3	μA
		$V_{EN} = 2V$, no load, $T_J = 25^{\circ}C$	650	960	1270	μA
Quiescent supply current		V _{EN} = 2V, no load, T _J = -40°C to +125°C	600	960	1320	μA
		Detect V_{IN} and V_{OUT1} , $T_J = 25^{\circ}C$	320	455	590	kHz
Charge pump frequency		Detect V _{IN} and V _{OUT1} , $T_J = -40^{\circ}C$ to $+125^{\circ}C$	250		590	kHz
Charge pump MOSFET on resistance	Ron			0.24		Ω
Charge pump current limit			0.6	1		А
Negative Linear Regulator						
Load current limit (7)		$V_{IN} = 3.3V, V_{OUT2} = -2.5V$		200	250	mA
Output accuracy		Compared with CTL voltage, T _J = 25°C, $I_{OUT2} = 10mA$	-1		1	%
		Over temp, I _{OUT2} = 10mA	-2		2	%
Output offset		$I_{OUT2} = 10mA, T_J = 25^{\circ}C$	-20		20	mV
Dropout voltage	VDROP	$V_{IN} = 2.5V, I_{OUT2} = 60mA$	30		90	mV
Diopoul vollage	V DROP	$V_{IN} = 3.3V, I_{OUT2} = 60mA$	20		80	mV
Load regulation (7)		$V_{OUT1} = -3.3V, CTL = 1V$		0.005	0.01	%/mA
		100Hz, C _{OUT1} = 100pF, C _{OUT2} = 1μF, I _{OUT2} = 10mA		60		
PSRR ⁽⁷⁾		50kHz, $C_{OUT1} = 100pF$, $C_{OUT2} = 1\mu$ F, $I_{OUT2} = 10$ mA		50		dB
		$300kHz$, $C_{OUT1} = 100pF$, $C_{OUT2} = 1\mu F$, $I_{OUT2} = 10mA$		40		
Soft-start slew rate				5		V/ms
EN turn-on delay			135		285	μs
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
Output discharge resistor	R _{DIS1}	$V_{EN} = 0V, VOUT1 rail$	170		310	Ω
Culput discharge resision	R _{DIS2}	$V_{EN} = 0V$, VOUT2 rail	80		146	Ω
EN input current		$V_{EN} = 2V$	1.4	1.8	2.2	μA
		$V_{EN} = 0V$		0		μΑ
Thermal shutdown (7)				160		°C



ELECTRICAL CHARACTERISTICS (continued)

 V_{IN} = 3.3V, T_J = -40°C to +125°C ⁽⁶⁾, typical value is tested at T_J = 25°C. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units
Thermal hysteresis (7)				30		°C
System Level (7)						
Recommended input capacitance	CIN	V _{IN} = 3.3V		4.7		μF
Recommended fly capacitor	C _{FLY}			4.7		μF
Recommended VOUT1 capacitor				4.7		μF
Recommended VOUT2 capacitor				4.7		μF
VOUT1 voltage				-1x		VIN
Output ripple	VRIPPLE_OUT1	$\label{eq:VIN} \begin{array}{l} V_{\text{IN}} = 3.3V, \ V_{\text{OUT1}} = -3.3V, \\ C_{\text{FLY}} = C_{\text{OUT1}} = 4.7 \mu F, \\ I_{\text{OUT1}} = 60 m A \end{array}$		50		mV
	VRIPPLE_OUT2	$\label{eq:VIN} \begin{split} V_{\text{IN}} &= 3.3V, V_{\text{OUT2}} = 2.5V, \\ C_{\text{OUT2}} &= 1\mu F, I_{\text{OUT2}} = 60 m A \end{split}$		1		mV

Notes:

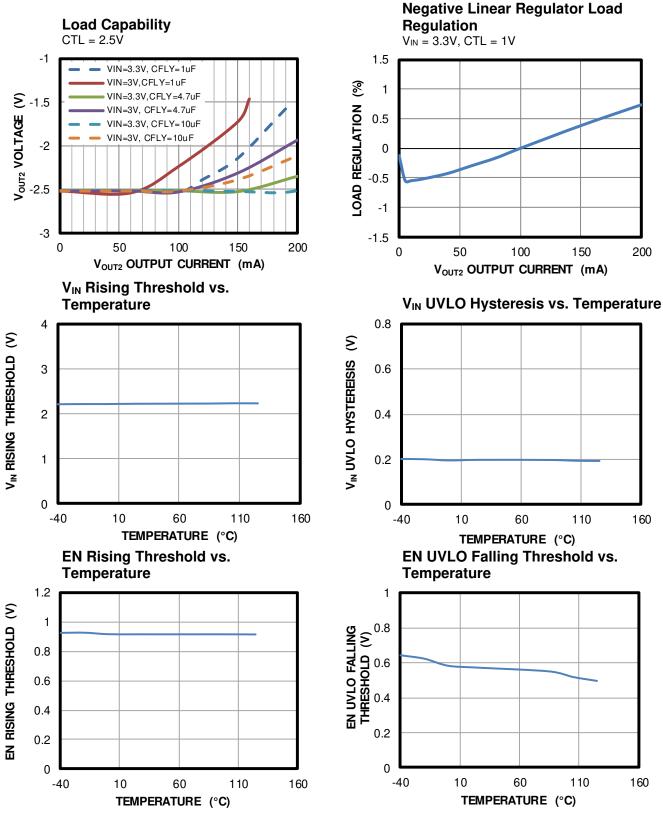
6) Guaranteed by over-temperature correlation. Not tested in production.

7) Guaranteed by engineering sample characterization.



TYPICAL PERFORMANCE CHARACTERISTICS

 V_{IN} = 3.3V, V_{OUT1} = -3.3V, V_{OUT2} = -1V, C_{IN} = C_{FLY} = C_{OUT1} = C_{OUT2} = 4.7µF, T_A = 25°C, unless otherwise noted.



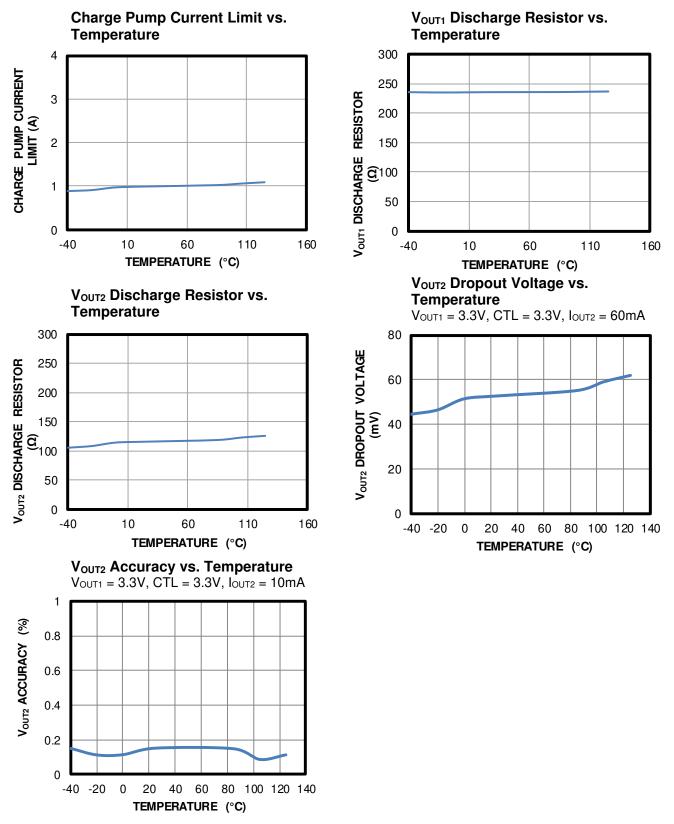
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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

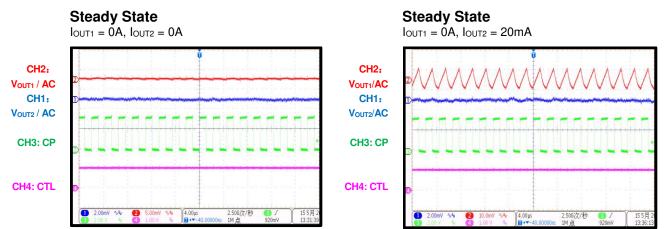
 V_{IN} = 3.3V, V_{OUT1} = -3.3V, V_{OUT2} = -1V, C_{IN} = C_{FLY} = C_{OUT1} = C_{OUT2} = 4.7µF, T_A = 25°C, unless otherwise noted.

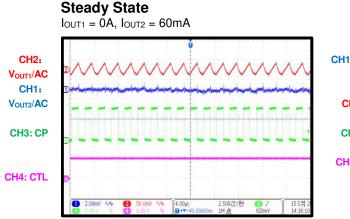




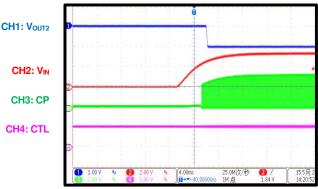
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

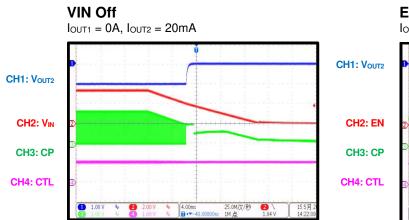
 V_{IN} = 3.3V, V_{OUT1} = -3.3V, V_{OUT2} = -1V, C_{IN} = C_{FLY} = C_{OUT1} = C_{OUT2} = 4.7 $\mu\text{F},~T_{\text{A}}$ = 25°C, unless otherwise noted.

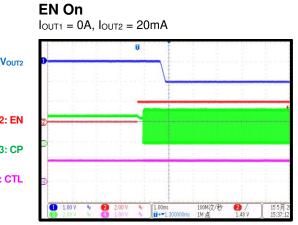








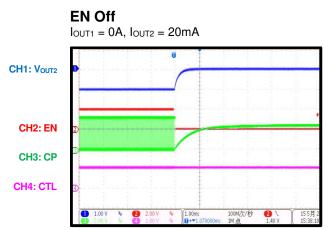






TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 V_{IN} = 3.3V, V_{OUT1} = -3.3V, V_{OUT2} = -1V, C_{IN} = C_{FLY} = C_{OUT1} = C_{OUT2} = 4.7 $\mu\text{F},~T_{\text{A}}$ = 25°C, unless otherwise noted.





FUNCTIONAL BLOCK DIAGRAM

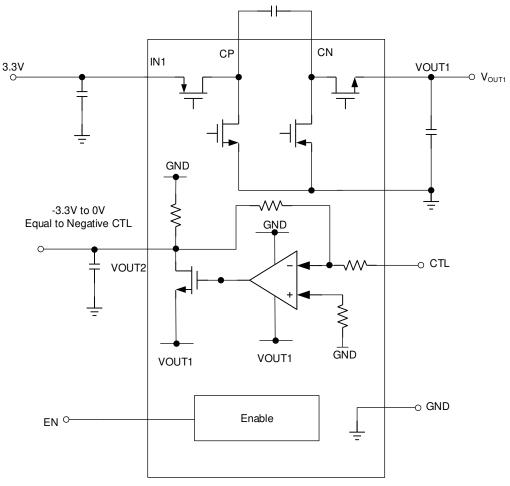


Figure 1: Functional Block Diagram



OPERATION

The MP5418A is a monolithic negative charge pump with a built-in adjustable negative regulator. It has a 2.3V to 5V, input range and can provide an unregulated output that is equal to the negative input voltage. The MP5418A also offers a regulated output between the negative input voltage and 0V.

For simplicity, the MP5418A does not require an external inductor. The internal soft-start circuit effectively reduces the inrush current during start-up.

Negative Charge Pump

The MP5418A uses a switched capacitor charge pump to achieve an unregulated negative voltage. The absolute value of this voltage is the input voltage (V_{IN}). The switching signal drives the charge pump, and is created by an integrated oscillator within the control circuit block. The oscillator charge pump switching frequency is 455kHz.

When the absolute value of VOUT1 is below 1V, the charge pump triggers an over-current condition. The MP5418A forces the oscillator frequency to 45kHz for foldback.

There is a diode between the VOUT1 and GND pins. When the VOUT1 voltage (V_{OUT1}) exceeds 0.3V, the diode discharges VOUT1.

Negative Linear Regulator

The negative linear regulator receives power from the negative charge pump output. The regulator provides a low dropout voltage, quiescent supply, and low output noise. Its output ranges from 0V to V_{OUT1} .

The regulator uses an internal feedback loop to control the output voltage, which equals to -1x the CTL pin voltage. This is an easy interface for DAC. Through a high precise DAC, its output voltage can be set by the external signal.

The PSRR of the negative linear regulator is specifically designed for its charge pump. The regulator has a low output ripple.

Load Capability

The MP5418A's load capability is 200mA. This means the sum of I_{OUT1} and I_{OUT2} remains below 200mA. The load capability is related to the fly

capacitor and output capacitor. A smaller capacitance results in a smaller load capability.

Over-Current Protection (OCP)

The charge pump current is limited internally. The peak charge pump input current is limited to 1A, and the device also provides protections against overload and over-temperature (OT) conditions.

Over-Temperature Protection (OTP)

When the junction temperature exceeds 160°C, the thermal sensor sends a signal to the control logic, and the IC shuts down. The IC restarts once the temperature drops by about 30°C.

Enable (EN)

When the input voltage exceeds the undervoltage lockout (UVLO) threshold (typically 2.2V), the device can be enabled by pulling the EN pin above 1.2V. To disable the device, float EN or pull it to ground. There is an internal $1M\Omega$ resistor between the EN and GND pins.

When the device is disabled, the part automatically goes into output discharge mode. The internal discharge MOSFET provides a resistive discharge path for the output capacitor.

Equivalent Output Resistance

The equivalent output resistance (R_O) is related to the fly capacitance (C_{FLY}) and charge pump frequency (f). R_O can be calculated with Equation (1):

$$R_{O} = \frac{1}{f \times C_{FLY}} + 8 \times R_{ON}$$
(1)

Where R_{ON} is the on resistance of each switching MOSFET in the charge pump.

The output OUT1 voltage (V_{OUT1}) is related to I_O and R_O . V_{OUT1} can be estimated with Equation (2):

$$V_{OUT1} = -(V_{IN} - I_O \times R_O)$$
 (2)

Soft Start (SS)

The MP5418A has an internal soft start (SS) pin that ramps up the output voltage at a controlled slew rate to avoid overshoot at start-up. The soft-start slew rate is internally set to 5V/ms.

APPLICATION INFORMATION COMPONENT SELECTION

Selecting the Output Capacitor

The output capacitors (C_{OUT1} and C_{OUT2}) stabilize the DC output voltage. It is recommended to use ceramic X5R or X7R capacitors for the best performance. C_{OUT1} should be 1µF, while C_{OUT2} can be between 1µF and 10µF. A larger C_{OUT2} value improves load transient response and reduces noise.

Other dielectric output capacitors can be used, but they are not recommended, as their capacitance can deviate greatly from their rated value under an over-temperature condition. The characteristics of the output capacitor affect the stability of the regulation system.

Selecting the Input Capacitor

For proper operation, place a 1μ F to 10μ F ceramic capacitor (C_{IN}) with X5R or X7R dielectrics between the IN and GND pins. A larger-value C_{IN} improves the line transient response.

Selecting the Fly Capacitor

The fly capacitor can affect the output resistance and OUT1 voltage. Therefore, if the output current is higher, the larger fly capacitor is recommended. The fly capacitor is also recommended to close C_{IN} and C_{OUT1} . To use the same capacitor for C_{IN} , C_{OUT1} , and C_{FLY} is better.

Setting the Output Voltage

The linear regulator follows the CTL voltage. The output value is regulated to -1x the CTL voltage. The CTL pin is an analog input, and can be directly connected to the DAC output. Figure 2 shows the application circuit.

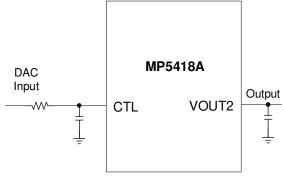


Figure 2: Output Voltage Setting

Design Example

Table 1 provides a design example based on the application guidelines.

Table	1:	Design	Example
Table		Design	

V _{IN}	+3.3V
V _{OUT1}	-3.3V
V _{CTL}	+1V
V _{OUT2}	-1V

For a detailed application schematic, see the Typical Application Circuit section on page 15. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 6. For more device applications, refer to the related evaluation board datasheet.



PCB Layout Guidelines

PCB layout is critical for good regulation, ripple rejection, transient response, and thermal performance. It is highly recommended to duplicate the EVB layout for optimal performance. For the best results, refer to Figure 3 and follow the guidelines below:

- 1. Place the high-current paths (GND, IN, CP, and CN) very close to the device with short, direct, and wide traces.
- 2. Place the input capacitor as close as possible to the IN and GND pins.
- 3. Place the output capacitor at the GND pin, close the chip GND pins.

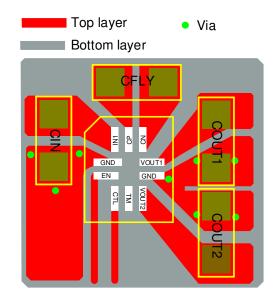


Figure 3: Recommended PCB Layout



TYPICAL APPLICATION CIRCUIT

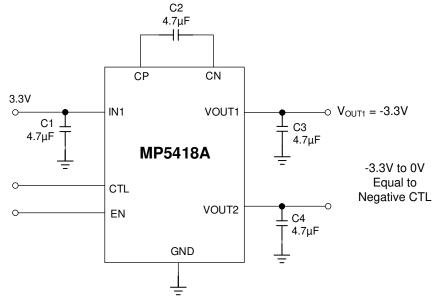


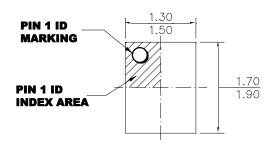
Figure 4: Typical Application Circuit



0.35

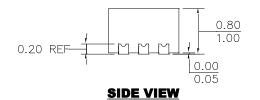
PACKAGE INFORMATION

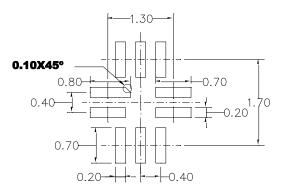
QFN-10 (1.4mmx1.8mm)



0.45 0.45 8 10 PIN 1 ID 0.10X45° TYP 0.15 0.40 0.25 BSC 6 0.35 0.45 0.15 5 |30.40 0.25 BSC

TOP VIEW





RECOMMENDED LAND PATTERN

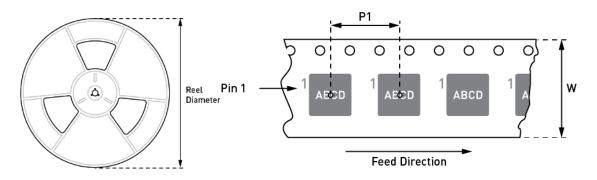
BOTTOM VIEW

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS. 2) LEAD COPLANARITY SHALL BE 0.08 **MILLIMETERS MAX.** 3) JEDEC REFERENCE IS MO-220. 4) DRAWING IS NOT TO SCALE.



CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5418AGQG-Z	QFN-10 (1.4mmx1.8mm)	5000	N/A	13in	12mm	4mm

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