Features

- ESD Protection for 1 line with Bi-directional
- Provide ESD protection for the protected line to
  IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 42A (8/20μs)
- For low operating voltage applications: 3.3V
- **0402 small DFN package** saves board space
- Protect one I/O line or power line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green Part***

Applications

- Power Line Protection
- Audio Protection
- Mobile Phones
- Control Signal Line Protection
- Hand Held Portable Applications

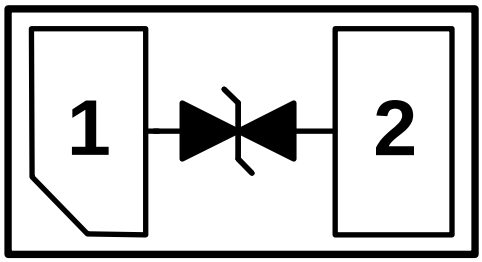
Description

AZ5883-01F is a design which includes one bi-directional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ5883-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ5883-01F is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5883-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



DFN1006P2E (Bottom View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A= 25°C, unless otherwise specified)			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp=8/20μs)	I_{PP-1} (Note 1) I_{PP-2} (Note 2)	42 33	A
Operating Supply Voltage	V_{DC}	±3.6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	T=25 °C.	-3.3		3.3	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = ±3.3V, T=25 °C.			0.5	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C.	4.5		6.8	V
Surge Clamping Voltage (Note 1)	$V_{CL-surge}$	I_{PP}= 5A, tp=8/20μs, T=25 °C.		4.5		V
		I_{PP}= 42A, tp=8/20μs, T=25 °C.		9		
ESD Clamping Voltage (Note 3)	V_{clamp}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), contact mode, T=25 °C.		5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, contact mode, T=25 °C.		0.04		Ω
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 °C.		70	85	pF

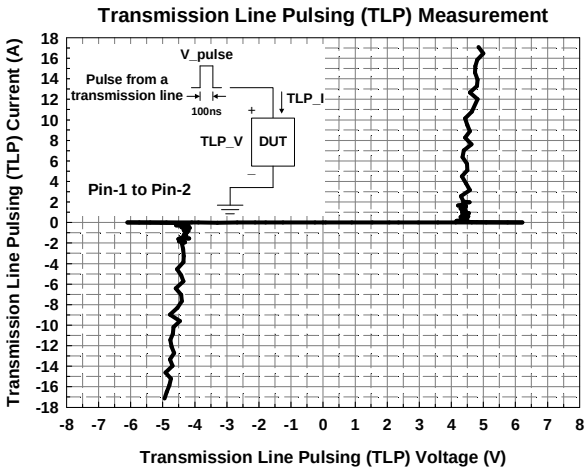
Note 1: The Peak Pulse Current measured conditions: tp = 8/20μs, 2ohm source impedance.

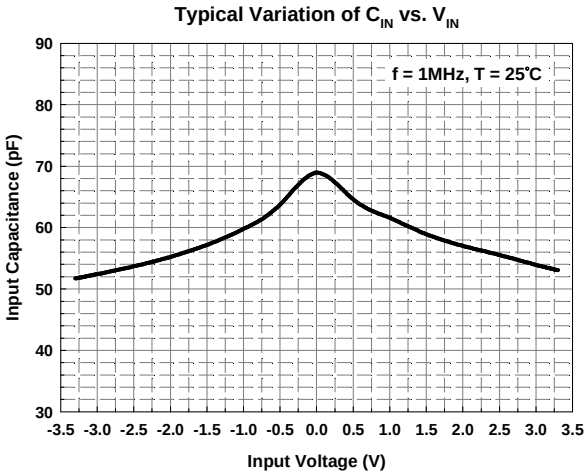
Note 2: The Peak Pulse Current measured conditions: tp = 8/20μs, 42ohm source impedance.

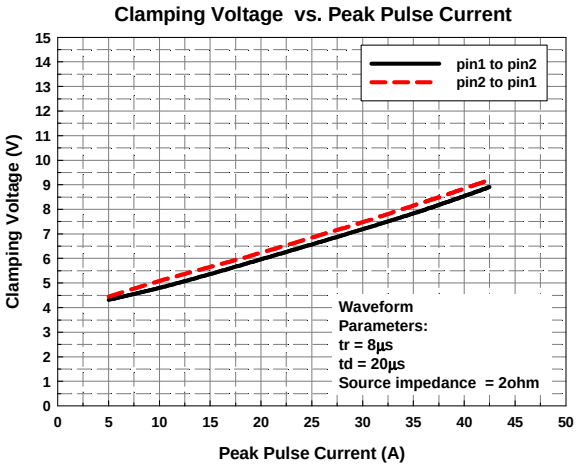
Note 3: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics







Applications Information

The AZ5883-01F is designed to protect one line against System ESD/EFT/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5883-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5883-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5883-01F.
- Place the AZ5883-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

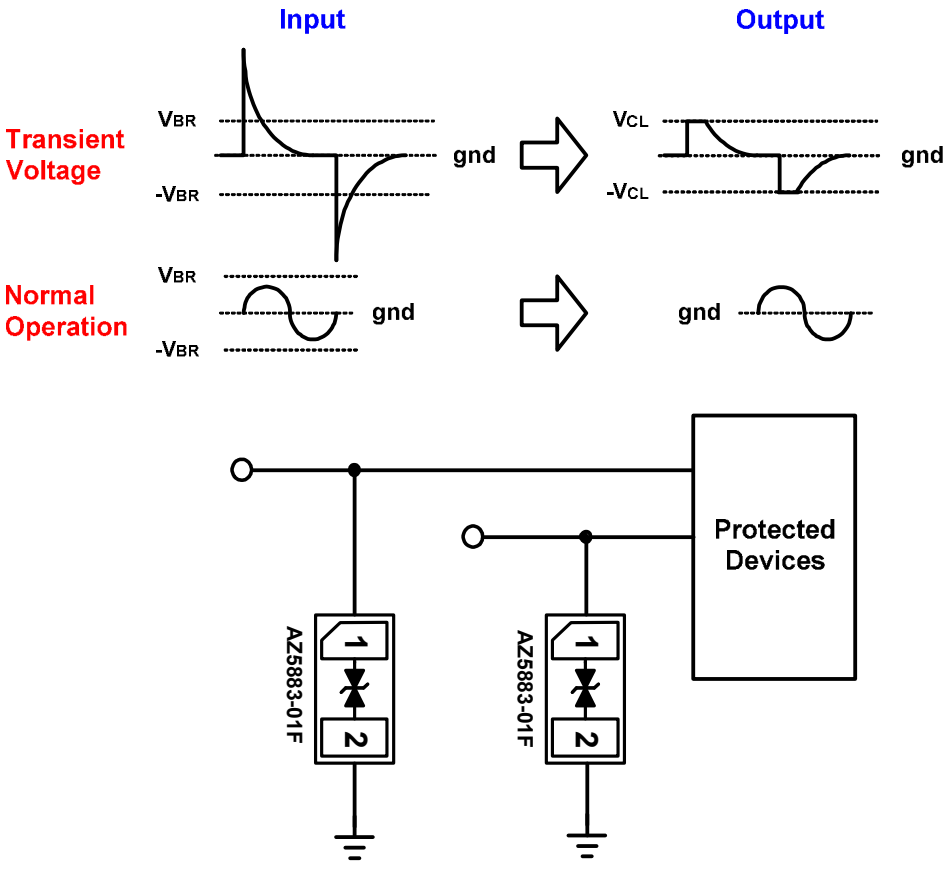
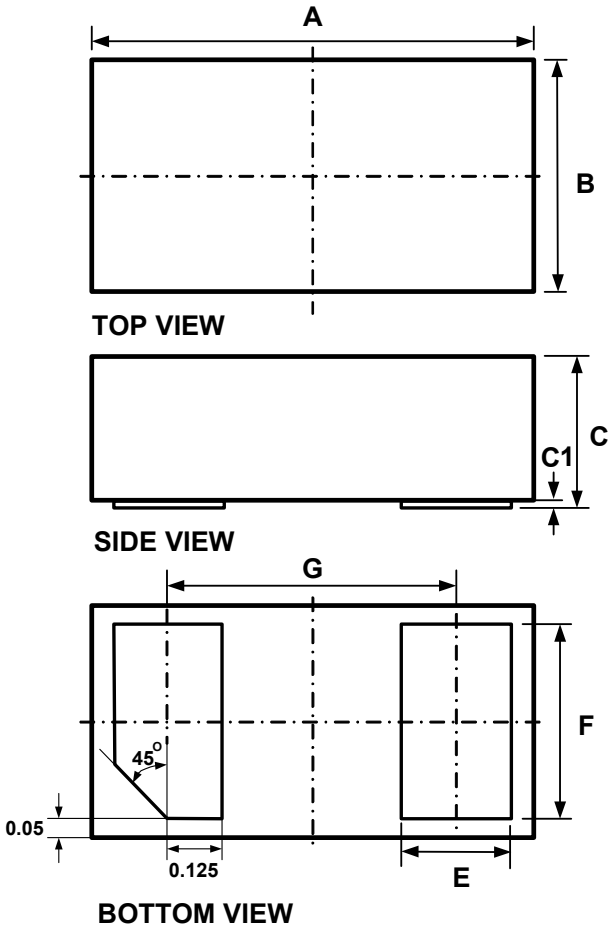


Fig. 1

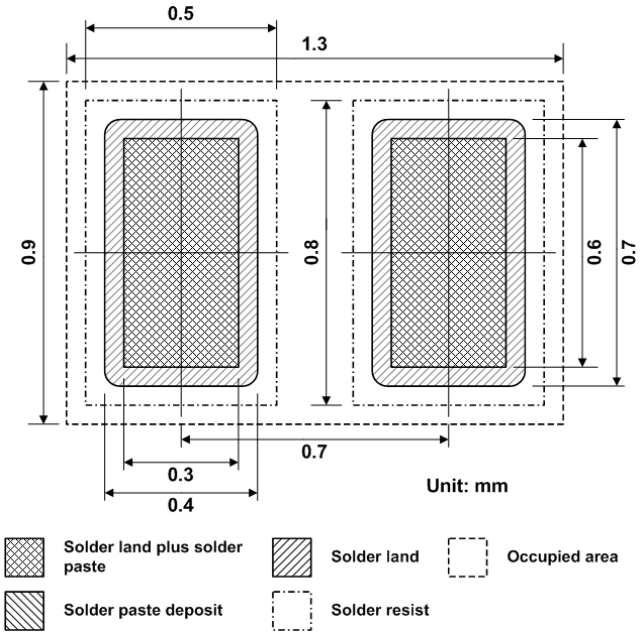
Mechanical Details

DFN1006P2E
PACKAGE DIAGRAMS



Symbol	Millimeters			Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95	1.00	1.05	0.037	0.039	0.041
B	0.55	0.60	0.65	0.022	0.024	0.026
C	0.45	0.50	0.55	0.018	0.020	0.022
C1	0.00	0.02	0.05	0.000	0.001	0.002
E	0.20	0.25	0.30	0.008	0.010	0.012
F	0.45	0.50	0.55	0.018	0.020	0.022
G	0.65 BSC			0.026 BSC		

LAND LAYOUT

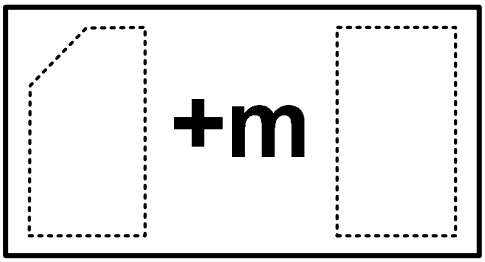


(Unit: mm)

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Top View

Part Number	Marking Code
AZ5883-01F.R7GR (Green Part)	m

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5883-01F.R7GR	Green	T/R	7 inch	12,000/reel	4 reels =48,000/box	6 boxes =288,000/carton

Revision History

Revision	Modification Description
Revision 2017/04/25	Formal Release.