

RFG45N06 RFP45N06

45A, 60V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs (MegaFETs)

January 1994

Features

- 45A, 60V
- $r_{DS(ON)} = 0.028\Omega$
- Temperature Compensating PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

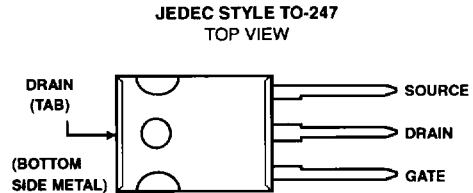
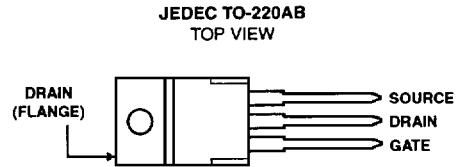
Description

The RFG45N06, RFP45N06 N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

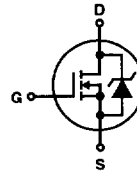
The RFG45N06 is supplied in a JEDEC style TO-247 plastic package and the RFP45N06 is supplied in the JEDEC TO-220AB plastic package.

Formerly developmental type TA49028.

Packaging



Symbol



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$)

		RFG45N06, RFP45N06	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	± 20	V
Drain Current			
RMS Continuous	I_D	45	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Maximum Avalanche Current	I_{AM}	125	A
Power Dissipation			
$T_C = +25^\circ\text{C}$	P_D	131	W
Derate above +25°C	P_T	0.877	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

Specifications RFG45N06, RFP45N06

Electrical Specifications $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Drain-Source Breakdown Voltage	V_{DS}	$I_D = 0.25\text{mA}$, $V_{GS} = 0\text{V}$	60	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 0.25\text{mA}$	2	-	4	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{V}$, $V_{GS} = 0\text{V}$	$T_C = +25^\circ\text{C}$	-	-	1	μA
			$T_C = +150^\circ\text{C}$	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	100	nA	
On Resistance	$r_{DS(ON)}$	$I_D = 45\text{A}$, $V_{GS} = 10\text{V}$	-	-	0.028	Ω	
Turn-On Time	t_{ON}	$V_{DD} = 30\text{V}$, $I_D = 45\text{A}$ $R_L = 0.667\Omega$, $V_{GS} = +10\text{V}$ $R_{GS} = 3.6\Omega$	-	-	120	ns	
Turn-On Delay Time	$t_{D(ON)}$		-	12	-	ns	
Rise Time	t_R		-	74	-	ns	
Turn-Off Delay Time	$t_{D(OFF)}$		-	37	-	ns	
Fall Time	t_F		-	16	-	ns	
Turn-Off Time	t_{OFF}		-	-	80	ns	
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 0$ to 20V	$V_{DD} = 48\text{V}$, $I_D = 45\text{A}$, $R_L = 1.07\Omega$	-	125	150
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0$ to 10V	-		67	80	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to 2V	-		3.7	4.5	nC
Plateau Voltage	$V_{(PLATEAU)}$	$I_D = 45\text{A}$, $V_{DS} = 15\text{V}$	-	-	7.5	V	
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	2050	-	pF	
Output Capacitance	C_{OSS}		-	600	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	200	-	pF	
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1.14	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	80	$^\circ\text{C/W}$	

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Forward Voltage	V_{SD}	$I_{SD} = 45\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 45\text{A}$, $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

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N-CHANNEL
POWER MOSFETS

Typical Performance Curves

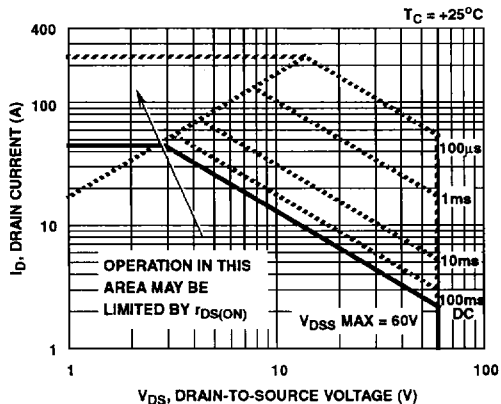


FIGURE 1. SAFE- OPERATING AREA CURVE

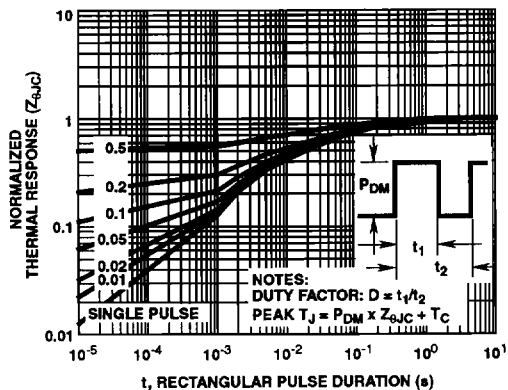


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

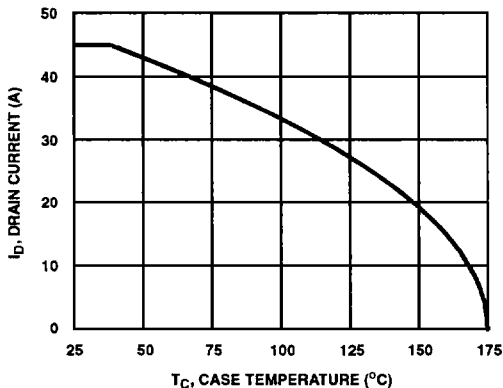


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

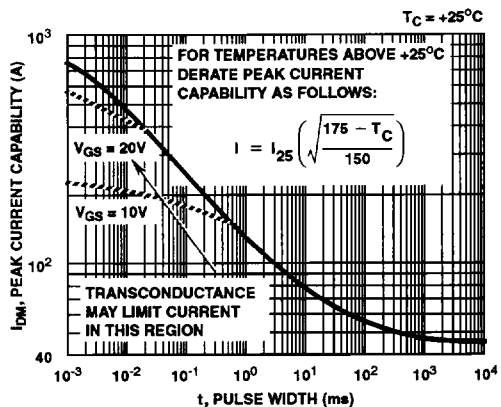


FIGURE 4. PEAK CURRENT CAPABILITY

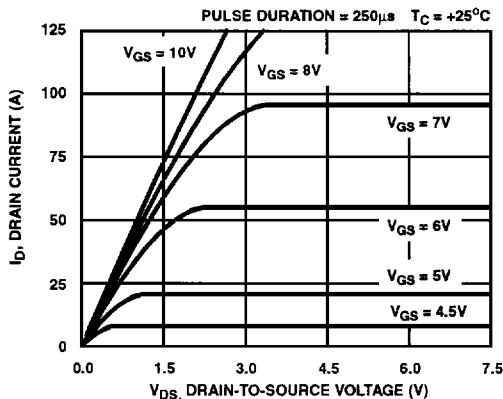


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

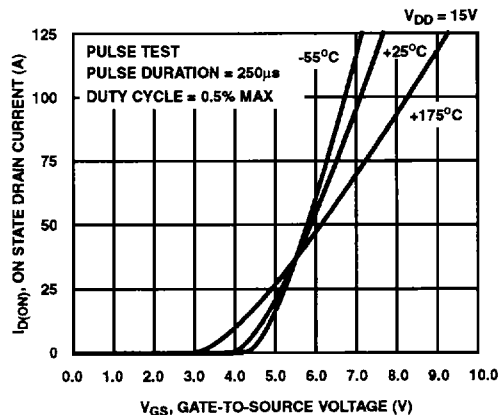


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

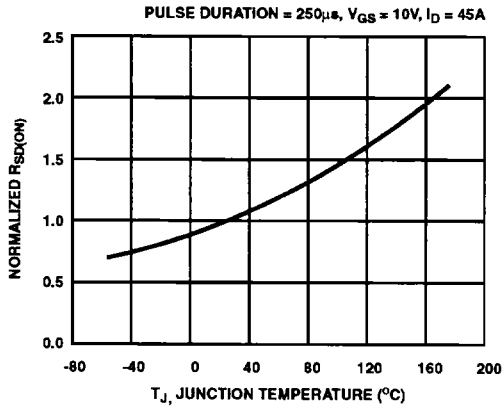


FIGURE 7. NORMALIZED $R_{DS(ON)}$ vs JUNCTION TEMPERATURE

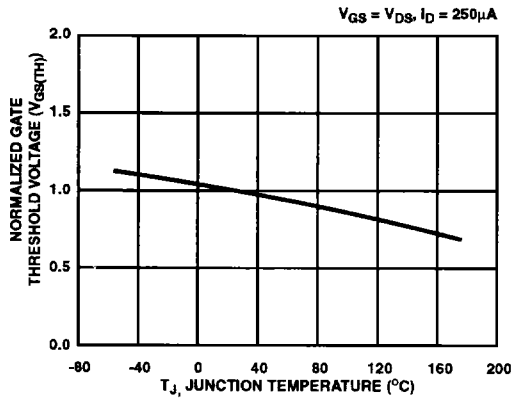


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

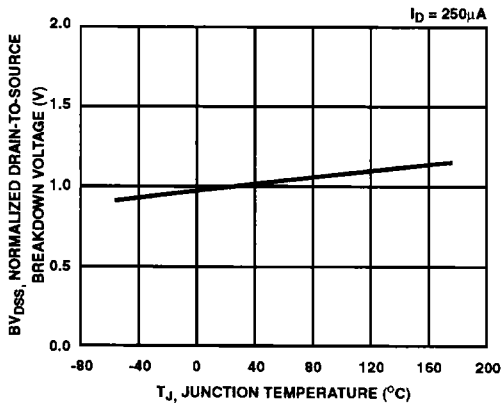


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

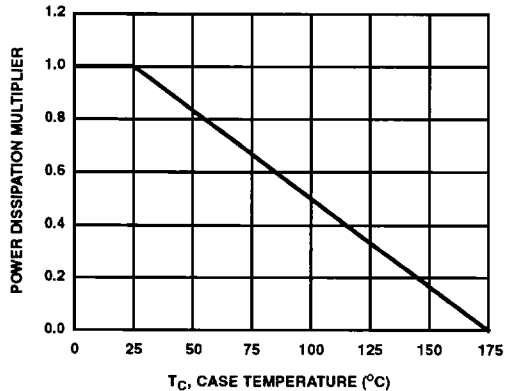


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

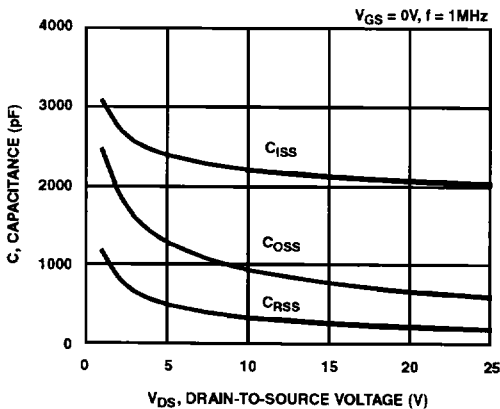


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

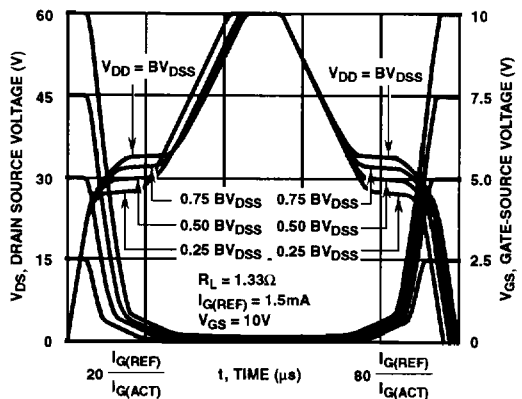


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

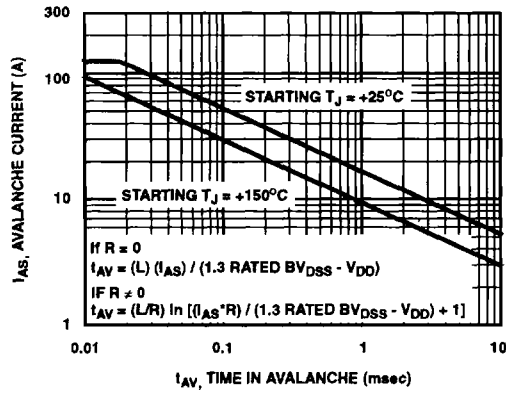


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits

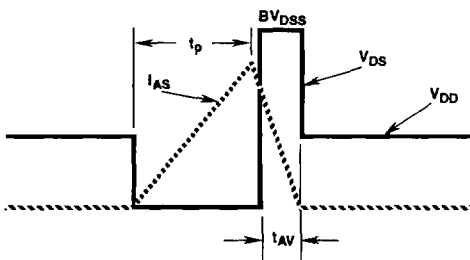


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

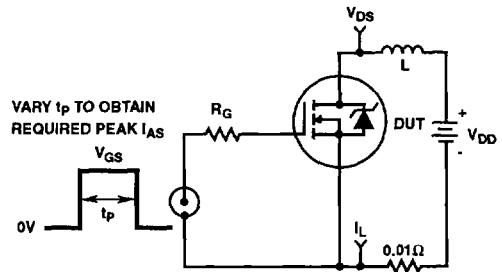


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

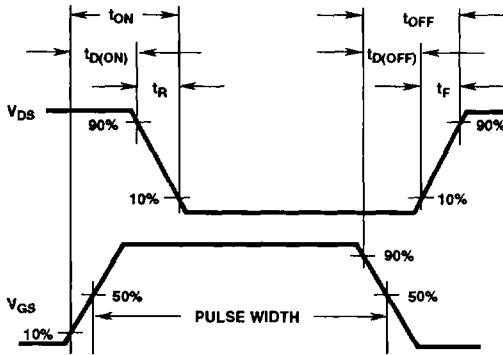


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

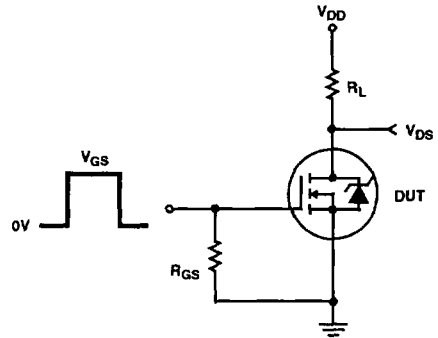


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

P Spice Model Listing

Temperature Compensated PSPICE Model for the RFG45N06, RFP45N06

.SUBCKT RFP45N06 2 1 3

REV 1/18/93

*NOM TEMP = +25°C

CA 12 8 3.49E-9
 CB 15 14 3.8E-9
 CIN 6 8 2E-9

DBODY 7 5 DBDMOD
 DBREAK 5 11 DBKMOD
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 66.5
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 6 8 1
 EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1E-9
 LGATE 1 9 5.65E-9
 LSOURCE 3 7 4.13E-9

MOS1 16 6 8 8 MOSMOD M=0.99
 MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
 RDRAIN 5 16 RDSMOD 3.58E-3
 RGATE 9 20 0.681
 RIN 6 8 1E9
 RSOURCE 8 7 RDSMOD 13.6E-3
 RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
 VTO 21 6 0.92

.MODEL DBDMOD D (IS=8.2E-13 RS=7.86E-3 TRS1=2.26E-3 TRS2=2.90E-6 CJO=2.07E-9 TT=5.72E-8)
 .MODEL DBKMOD D (RS=1.93E-1 TRS1=5.13E-4 TRS2=-2.15E-5)
 .MODEL DPLCAPMOD D (CJO=1.25E-9 IS=1E-30 N=10)
 .MODEL MOSMOD NMOS (VTO=3.862 KP=55.57 IS=1E-30 N=10 TOX=1 L=1U W=1U)
 .MODEL RBKMOD RES (TC1=1.12E-3 TC2=-5.18E-7)
 .MODEL RDSMOD RES (TC1=4.64E-3 TC2=1.58E-5)
 .MODEL RVTOMOD RES (TC1=-4.27E-3 TC2=-6.55E-6)
 .MODEL S1AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-6.5 VOFF=-1.7)
 .MODEL S1BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-1.7 VOFF=-6.5)
 .MODEL S2AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-3.0 VOFF=2)
 .MODEL S2BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=2.0 VOFF=-3.0)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

