TS9002

Low-Power Single/Dual-Supply Dual Comparator with Reference

FEATURES

- ♦ Ultra-Low Quiescent Current:
  4µA (max), Both Comparators plus Reference
- ♦ Single or Dual Power Supplies:
  Single: +2.5V to +11V
  Dual: ±1.25V to ±5.5V
- ♦ Input Voltage Range Includes Negative Supply
- ♦ 7µs Propagation Delay
- ♦ Push-pull TTL/CMOS-Compatible Outputs
- ♦ Crowbar-Current-Free Switching
- ♦ Continuous Source Current Capability: 40mA
- ♦ Internal 1.182V ±0.75% Reference
- ♦ Adjustable Hysteresis
- ♦ 8-pin MSOP Package

APPLICATIONS

Threshold Detectors
Window Comparator
Level Translators
Oscillator Circuits
Battery-Powered Systems

DESCRIPTION

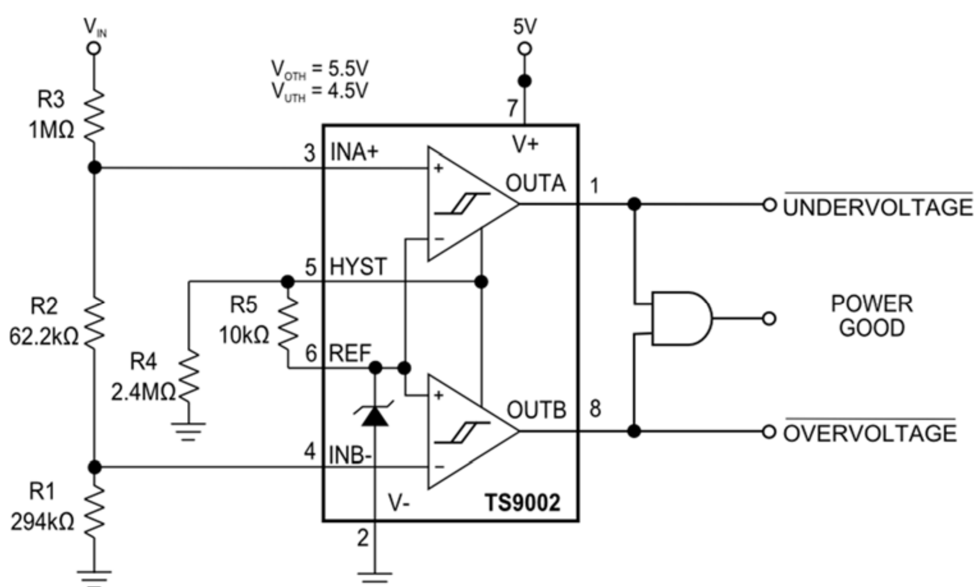
The TS9002 low-voltage, micropower dual analog comparator is form-factor identical to the MAX923 analog comparator with improved electrical specifications. Ideal for 3V or 5V single-supply applications, the TS9002 draws 11% lower supply current with a 25%-better initial accuracy reference voltage. The TS9002 joins the TS9001-1/2 analog comparators in the "NanoWatt Analog™" high performance analog integrated circuits portfolio. The TS9002 can operate from single +2.5V to +11V supplies or from ±1.25V to ±5.5V dual supplies.

The TS9002 exhibits an input voltage range from the negative supply rail to within 1.3V of the positive supply rail. In addition, its push-pull output stage is TTL/CMOS compatible and capable of sinking and sourcing current. It also incorporates an internal 1.182V ±0.75% voltage reference. Without complicated feedback configurations and only requiring two additional resistors, adding external hysteresis via a separate pin is available on the TS9002's HYST pin.

The TS9002 is fully specified over the -40ºC to +85ºC temperature range and is available in an 8-pin MSOP package.

TYPICAL APPLICATION CIRCUIT

A 5V, Low-Parts-Count, High-Accuracy Window Detector



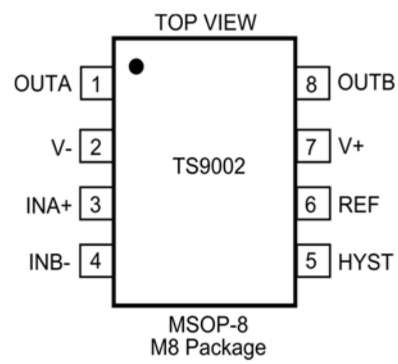
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-, V+ to GND, GND to V-)......-0.3V, +12V
Voltage Inputs
(IN+, IN-)..(V+ + 0.3V) to (V- - 0.3V)
HYST…………………………………….(REF + 5V) to (V- - 0.3V)
Output Voltage
REF...(V+ + 0.3V) to (V- - 0.3V)
OUT ....(V+ + 0.3V) to (V- - 0.3V)
Input Current (IN+, IN-, HYST)...20mA
Output Current
REF………………………………………………………….20mA
OUT………………………………………………………….40mA
Output Short-Circuit Duration (V+ ≤ 5.5V) ....Continuous

Continuous Power Dissipation (T_A = +70°C)
8-Pin MSOP (derate 4.1mW/°C above +70°C) 330mW
Operating Temperature Ranges..............................-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Electrical and thermal stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

PACKAGE/ORDERING INFORMATION



ORDER NUMBER	PART MARKING	CARRIER	QUANTITY
TS9002IM8	TADG	Tube	50
TS9002IM8T		Tape & Reel	2500

Lead-free Program: Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS – 5V OPERATION

V+ = 5V, V- = GND = 0V; T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at T_A = +25ºC. See Note 1.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage Range				2.5		11	V
Supply Current	IN+ = IN- + 100mV	HYST = REF	T_A = +25°C		2.6	4	µA
			-40°C to +85°C			5.2	µA
COMPARATOR							
Input Offset Voltage	V_{CM} = 2.5V		T_A = +25°C			±3.5	mV
			-40°C to +85°C			±10	mV
Input Leakage Current (IN-, IN+)	IN+ = IN- = 2.5V		T_A = +25°C		±0.01	±2	nA
			-40°C to +85°C		±0.01	±5	nA
Input Leakage Current (HYST)			T_A = +25°C		±0.02		nA
			-40°C to +85°C		±0.02		nA
Input Common-Mode Voltage Range				V-		V+ – 1.3V	V
Common-Mode Rejection Ratio	V- to (V+ – 1.3V)				0.1	1	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V				0.1	1	mV/V
Output Voltage Noise	100Hz to 100kHz				20		μV_{RMS}
Hysteresis Input Voltage Range				REF- 0.05V		REF	V
Response Time (High-to-Low Transition)	T_A = +25°C, 100pF load		Overdrive = 10 mV		17		µs
			Overdrive = 100 mV		7		µs
Response Time (Low-to-High Transition)	T_A = +25°C, 100pF Load		Overdrive = 10 mV		17		µs
			Overdrive = 100 mV		7		µs
Output High Voltage		-40°C to +85°C; I_{OUT} = 17mA		V+ – 0.4			V
Output Low Voltage		-40°C to +85°C; I_{OUT} = 1.8mA				GND + 0.4	V
	Dual Supply	-40°C to +85°C; I_{OUT} = 1.8mA				V- + 0.4	V
REFERENCE							
Reference Voltage			T_A = +25°C	1.173	1.182	1.191	V
			-40°C to +85°C	1.164		1.199	V
Reference Line Regulation	2.5V ≤ (V+ - V-) ≤ 11V		T_A = +25°C		0.25		mV/V
Source Current	ΔVREF = 1%		T_A = +25°C	20	25		µA
			-40°C to +85°C	6			µA
Sink Current	ΔVREF = 1%		T_A = +25°C	10	15		µA
			-40°C to +85°C	4			µA
Output Voltage Noise	100Hz to 100kHz				100		μV_{RMS}

ELECTRICAL CHARACTERISTICS – 3V OPERATION

V+ = 3V, V- = GND = 0V; T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at T_A = +25ºC. See Note 1.

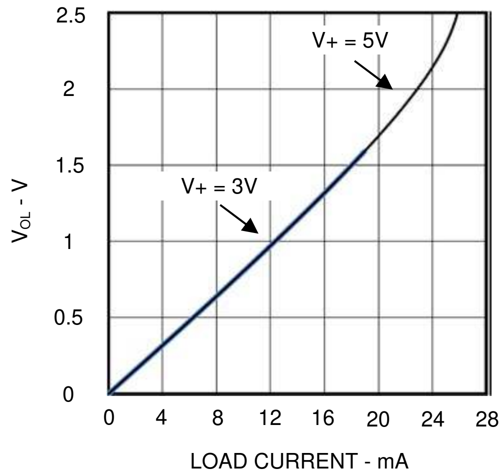
PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Current	IN+ = IN- + 100mV	HYST = REF	T_A = +25°C		2	3.8	μA
			-40°C to +85°C			5.3	
COMPARATOR							
Input Offset Voltage	V_{CM} = 1.5V		T_A = +25°C			±3.5	mV
			-40°C to +85°C			±10	
Input Leakage Current (IN-, IN+)	IN+ = IN- = 1.5V		T_A = +25°C		±0.01	±2	nA
			-40°C to +85°C		±0.01	±5	nA
Input Leakage Current (at HYST Pin)			T_A = +25°C		±0.02		nA
			-40°C to +85°C		±0.02		nA
Input Common-Mode Voltage Range				V-		V+ – 1.3V	V
Common-Mode Rejection Ratio	V- to (V+ – 1.3V)				0.1	1	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V				0.1	1	mV/V
Output Voltage Noise	100Hz to 100kHz				20		μV_{RMS}
Hysteresis Input Voltage Range				REF- 0.05V		REF	V
Response Time (High-to-Low Transition)	T_A = +25°C, 100pF load		Overdrive = 10 mV		17		μs
			Overdrive = 100 mV		7		
Response Time (Low-to-High Transition)	T_A = +25°C, 100pF Load		Overdrive = 10 mV		17		μs
			Overdrive = 100 mV		7		
Output High Voltage		-40°C to +85°C; I_{OUT} = 10mA		V+ – 0.4			V
Output Low Voltage		-40°C to +85°C; I_{OUT} = 1.8mA				GND + 0.4	V
	Dual Supply	-40°C to +85°C; I_{OUT} = 1.8mA				V- + 0.4	V
REFERENCE							
Reference Voltage			T_A = +25°C	1.173	1.182	1.191	V
			-40°C to +85°C	1.164		1.199	
Reference Line Regulation	2.5V ≤ (V+ - V-) ≤ 5V		T_A = +25°C		0.25		mV/V
Source Current	ΔVREF = 1%		T_A = +25°C	20	25		μA
			-40°C to +85°C	6			
Sink Current	ΔVREF = 1%		T_A = +25°C	10	15		μA
			-40°C to +85°C	4			
Output Voltage Noise	100Hz to 100kHz				100		μV_{RMS}

Note 1: All specifications are 100% tested at T_A = +25°C. Specification limits over temperature (T_A = T_{MIN} to T_{MAX}) are guaranteed by device characterization, not production tested.

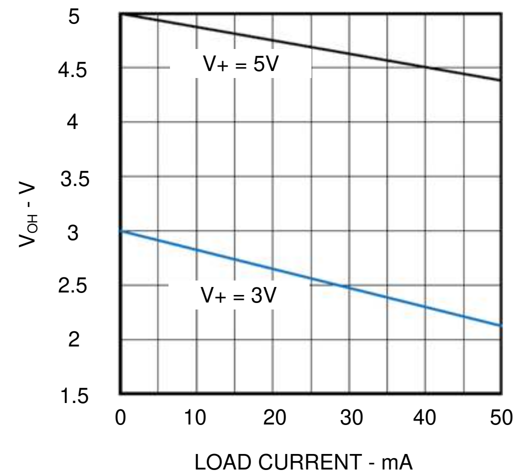
TYPICAL PERFORMANCE CHARACTERISTICS

V_+ = 5V; V_- = GND; T_A = +25°C, unless otherwise noted.

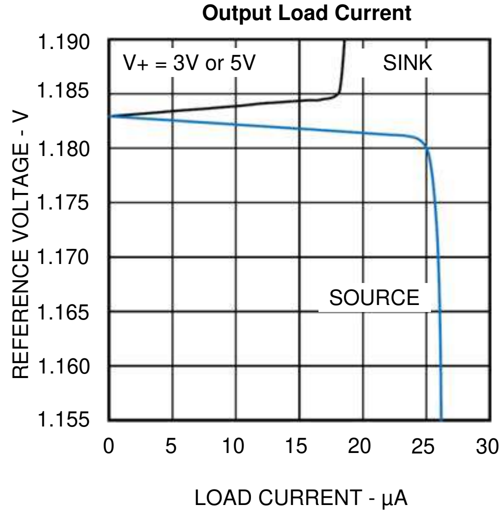
Output Voltage Low vs Load Current



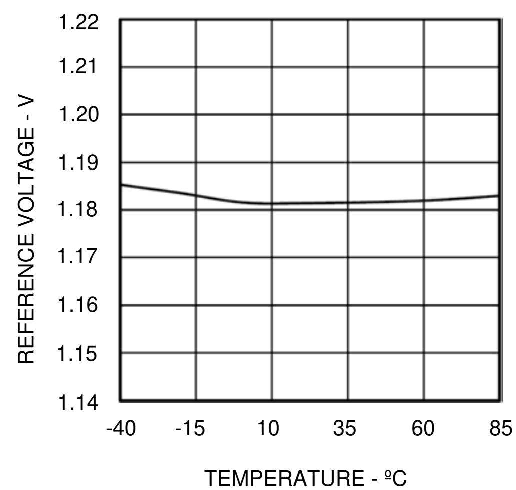
Output Voltage High vs Load Current



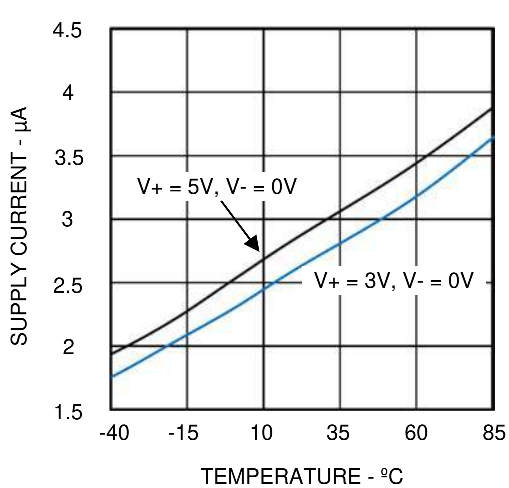
Reference Output Voltage vs Output Load Current



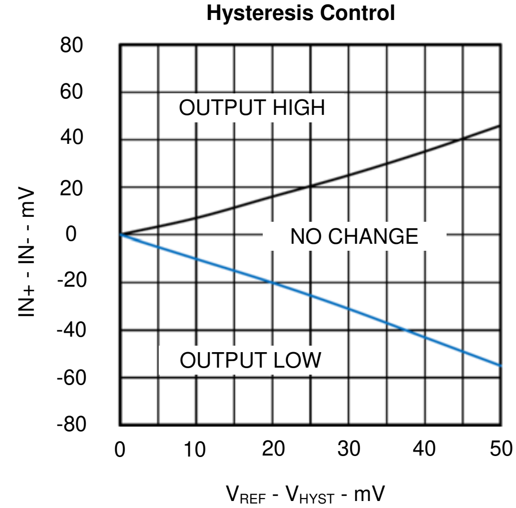
Reference Voltage vs Temperature



Supply Current vs Temperature



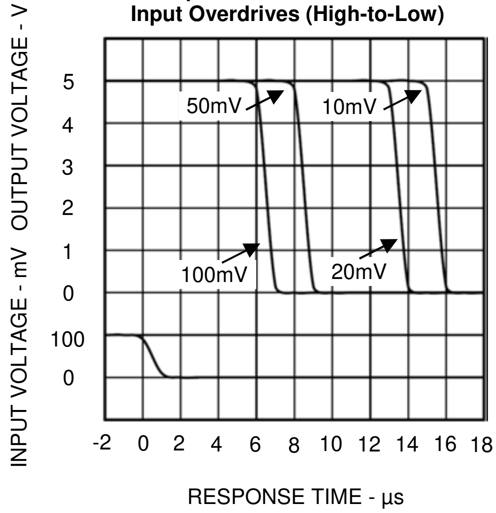
Hysteresis Control



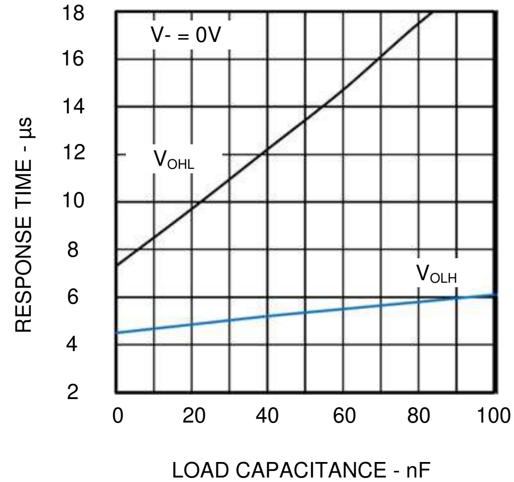
TYPICAL PERFORMANCE CHARACTERISTICS

$V_+ = 5V$; $V_- = GND$; $T_A = +25°C$, unless otherwise noted.

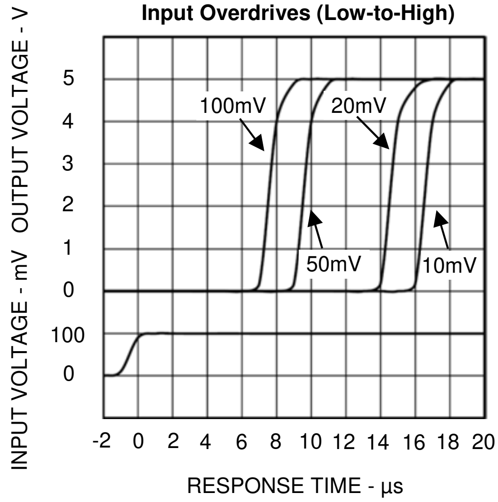
Response Time For Various Input Overdrives (High-to-Low)



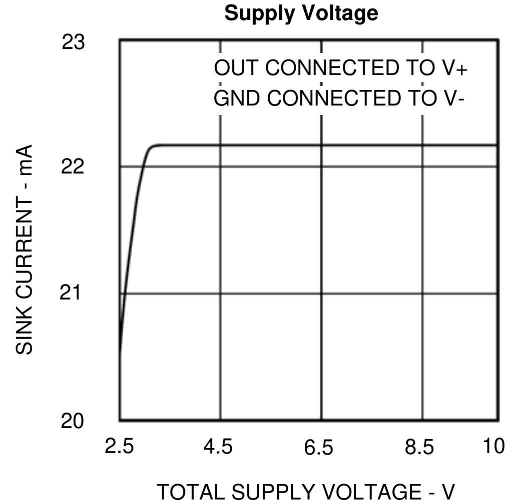
Response Time vs Load Capacitance



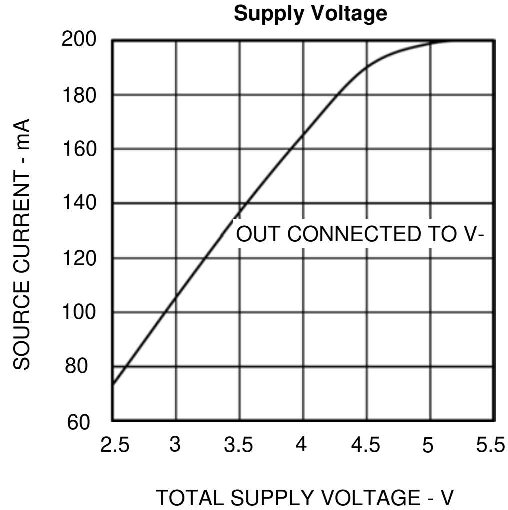
Response Time For Various Input Overdrives (Low-to-High)



Short-Circuit Sink Current vs Supply Voltage



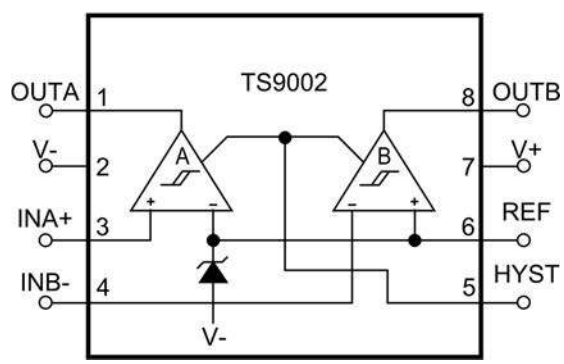
Short-Circuit Source Current vs Supply Voltage



PIN FUNCTIONS

TS9002 MSOP-8	NAME	FUNCTION
1	OUTA	Comparator A Output. Sinks and sources current. Swings from V+ to V-.
2	V-	Negative Supply Voltage. Connect to ground for single-supply operation.
3	INA+	Comparator A Noninverting Input
4	INB-	Comparator B Inverting Input
5	HYST	Hysteresis Input. Connect to REF if not used. Input voltage range is from VREF to (VREF - 50mV).
6	REF	1.182V Reference Output with respect to V-.
7	V+	Positive Supply Voltage
8	OUTB	Comparator B Output. Sinks and sources current. Swings from V+ to V-.

BLOCK DIAGRAM



THEORY OF OPERATION

The TS9002 dual, low-voltage, micropower analog comparator provides excellent flexibility and performance while sourcing continuously up to 40mA of current. The TS9002 draws less than 5.5µA (total) over temperature for both comparators, including the reference. It also exhibits an input offset voltage of ±3.5mV, and has an on-board +1.182V ±0.75% voltage reference. To minimize glitches that can occur with parasitic feedback or a less than optimal board layout, the design of the TS9002 output stage is optimized to eliminate crowbar glitches as the output switches. To minimize current consumption while providing flexibility, TS9002 has an on-board HYST pin in order to add additional hysteresis.

Power-Supply and Input Signal Ranges

The TS9002 can operate from a single supply voltage range of +2.5V to +11V, provides a wide common mode input voltage range of V- to V+-1.3V, and accepts input signals ranging from V- to V+ - 1V. The inputs can accept an input as much as 300mV above and below the power supply rails without damage to the part. The TS9002 is TTL compatible with a single +5V supply.

Comparator Output

The output design of the TS9002 can source and sink more than 40mA and 5mA, respectively, while simultaneously maintaining a quiescent current less than 3µA. If the power dissipation of the package is maintained within the max limit, the output can source pulses of 100mA of current with V+ set to +5V. In an effort to minimize external components needed to address power supply feedback, the TS9002 output does not produce crowbar switching current as the output switches. At a power supply voltage of 3V, the propagation delay of the TS9002 is 6µs when the output switches from high-to-low and low-to-high.

Voltage Reference

The TS9002 has an on-board +1.182V voltage reference with an accuracy of ±0.75%. The REF pin is able to source and sink 20µA and 10µA of current, respectively. The REF pin is referenced to V- and it should not be bypassed.

Noise Considerations

Noise can play a role in the overall performance of the TS9002. Despite having a large gain, if the input voltage is near or equal to the input offset voltage, the output will randomly switch HIGH and LOW. As a result, the TS9002 produces a peak-to-peak noise of about $0.3mV_{PP}$ while the reference voltage produces a peak-to-peak noise of about $1mv_{PP}$. Furthermore, it is important to design a layout that minimizes capacitive coupling from a given output to the reference pin as crosstalk can add noise and as a result, degrade performance.

APPLICATIONS INFORMATION

Hysteresis

As a result of circuit noise or unintended parasitic feedback, many analog comparators often break into oscillation within their linear region of operation especially when the applied differential input voltage approaches 0V (zero volt). Externally-introduced hysteresis is a well-established technique to stabilizing analog comparator behavior and requires external components. As shown in Figure 1, adding comparator hysteresis creates two trip points: V_{THR} (for the rising input voltage) and V_{THF} (for the falling input voltage). The hysteresis band (V_{HB}) is defined as the voltage difference between the two trip points. When a comparator's input voltages are equal, hysteresis effectively forces one comparator input to move quickly past the other input, moving the input out of the region where oscillation occurs. Figure 1 illustrates the case in which an IN- input is a fixed voltage and an IN+ is varied. If the input signals were reversed, the figure would be the same with an inverted output. Hysteresis can be generated with two external resistors using positive feedback as shown in Figure 2. Resistor R1 is connected between REF and HYST and R2 is connected between HYST and V-. This will increase the trip point for the rising input voltage, V_{THR}, and decrease the trip point for the falling input voltage, V_{THF}, by the same amount. If no hysteresis is required, connect HYST to REF. The hysteresis band, V_{HB}, is voltage across the REF and HYST pin multiplied by a factor of 2. The HYST pin can accept a voltage between REF and REF-50mV, where a voltage of REF-50mV generates the maximum voltage across R1 and thus, the maximum hysteresis and hysteresis band of 50mV and 100mV, respectively. To design the circuit for a desired hysteresis band, consider the equations below to acquire the values for resistors R1 and R2:

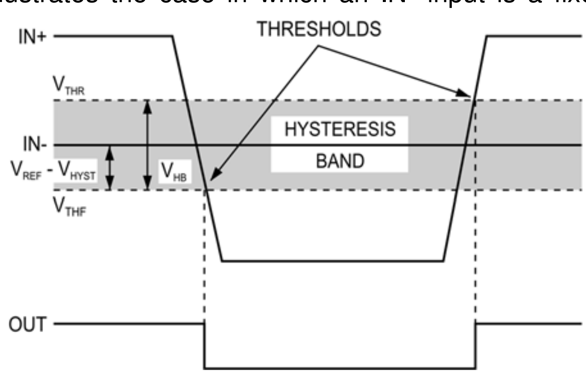


Figure 1. Threshold Hysteresis Band

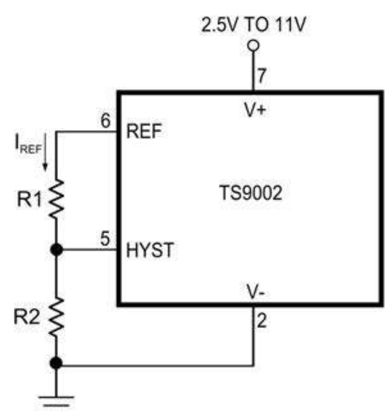


Figure 2. Programming the HYST Pin

$$R1 = \frac{V_{HB}}{(2 \times I_{REF})}$$

$$R2 = \frac{1.182 - \frac{V_{HB}}{2}}{I_{REF}}$$

where I_{REF} is the primary source of current out of the reference pin and should be maintained within the maximum current the reference can source. It is safe to maintain the current within 20µA. It is also important to ensure that the current from reference is much larger than the HYST pin input current. Given R2 = 2.4MΩ, the current sourced by the reference is 0.5µA. This allows the hysteresis band and R1 to be approximated as follows:

$$R1(k\Omega) = V_{HB}(mv)$$

Note the hysteresis is the same for both comparators.

Board Layout and Bypassing

While power-supply bypass capacitors are not typically required, it is good engineering practice to use 0.1µF bypass capacitors close to the device's power supply pins when the power supply impedance is high, the power supply leads are long, or there is excessive noise on the power supply traces. To reduce stray capacitance, it is also good engineering practice to make signal trace lengths as short as possible. Also recommended are a ground plane and surface mount resistors and capacitors.

Window Detector

The schematic shown in Figure 3 is for a 4.5V undervoltage threshold detector and a 5.5V overvoltage threshold detector using the TS9002. Resistor components R1, R2, and R3 can be selected based on the threshold voltage desired while resistors R4 and R5 can be selected based on the hysteresis desired. Adding hysteresis to the circuit will minimize chattering on the output when the input voltage is close to the trip point. OUTA and OUTB generate the active low undervoltage indication and active-low overvoltage indication, respectively. If both OUTA and OUTB signals are ANDed together, the resulting output of the AND gate is an active-high, power-good signal. To design the circuit, the following procedure needs to be followed:

1. As described below, determine the desired hysteresis and select resistors R4 and R5 accordingly. This circuit has ±5mV of hysteresis at the input where the input voltage V_{IN} will appear larger due to the input resistor divider.

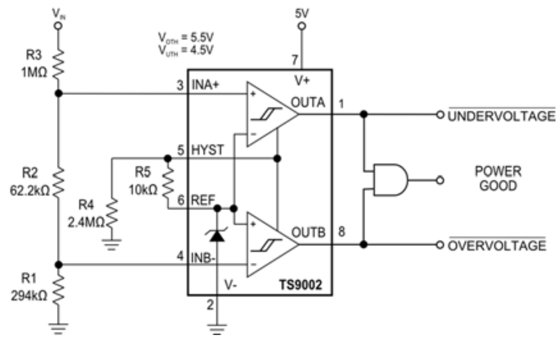


Figure 3. Window Detector

2. Choosing R1. As the leakage current at the INB- pin is less than 1nA, the current through R1 should be at least 100nA to minimize offset voltage errors caused by the input leakage current. Values within 100kΩ and 1MΩ are recommended. In this example, a 294kΩ, 1% standard value resistor is selected for R1.

3. Calculating R2 + R3. As the input voltage V_{IN} rises, the overvoltage threshold should be 5.5V. Choose R2 + R3 as follows:

$$R1 + R3 = R1 \times \left(\frac{V_{OTH}}{V_{REF}+V_{HYS}} - 1\right)$$

$$= 294k\Omega \times \left(\frac{5.5V}{1.182V + 5mV} - 1\right)$$

$$= 1.068M\Omega$$

4. Calculating R2. As the input voltage V_{IN} falls, the undervoltage threshold should be 4.5V. Choose R2 as follows:

$$R2 = (R1 + R2 + R3) \times \frac{(V_{REF}-V_{HYS})}{V_{UTH}} - 294k$$

$$= (294k\Omega + 1.068M\Omega) \times \frac{(1.182V-5mV)}{4.5} - 294k$$

$$= 62.2k\Omega$$

In this example, a 61.9kΩ, 1% standard value resistor is selected for R2.

5. Calculating R3.

$R3 = (R2 + R3) - R2$
$= 1.068M\Omega - 61.9k\Omega$

$= 1.006M\Omega$

In this example, a 1MΩ, 1% standard value resistor is selected for R3.

6. Using the equations below, verify all resistor values selected:

$$V_{OTH} = (V_{REF} + V_{HYS}) \times \frac{(R1 + R2 + R3)}{R1}$$

$= 5.474V$

$$V_{OTH} = (V_{REF} - V_{HYS}) \times \frac{(R1 + R2 + R3)}{(R1+R2)}$$

$= 4.484V$

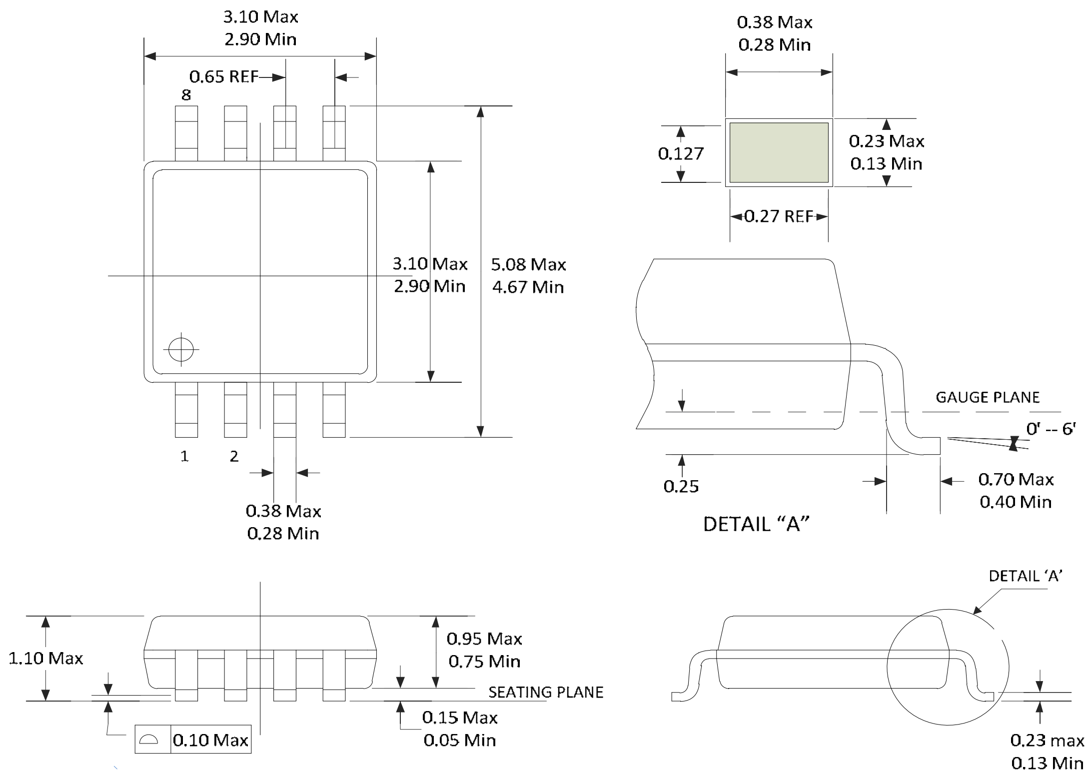
Where the hysteresis voltage is given by:

$$V_{HYS} = V_{REF} \times \frac{R5}{R4}$$

PACKAGE OUTLINE DRAWING

8-Pin MSOP Package Outline Drawing

(N.B., Drawings are not to scale)



NOTE:

1. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
2. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTUSIONS.
3. CONTROLLING DIMENSION IN MILIMETERS.
4. THIS PART IS COMPLIANT WITH JEDEC MO-187 VARIATIONS AA
5. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.

Patent Notice

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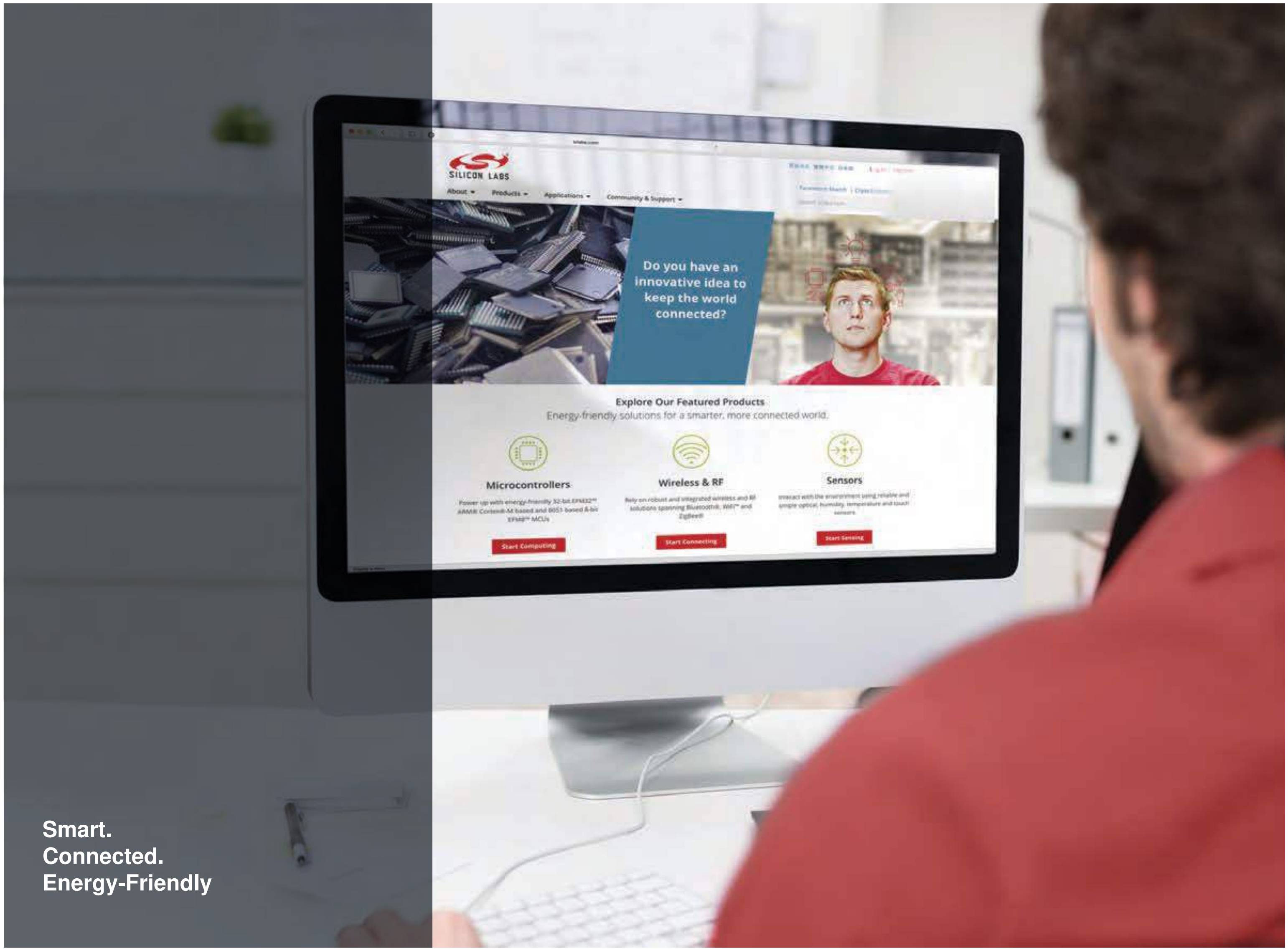

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