150mA LDO Regulator with PGOOD

General Description

The RT9181 is a low dropout voltage regulator with an output 2% accuracy and supply a continuous 150mA current within operating range from a +3V to +5.5V input. The power good function monitors the output voltage and indicates by pulling low the power good output (open drain).

The RT9181 requires a small output capacitor with low ESR for stabilizing output voltage. The device also minimizes output overshoot during power up.

The RT9181 uses an internal P-MOSFET as the pass device, which consumes 160µA supply current independent of load and dropout conditions. The EN pin controls the output and consumes no input bias current. Other features include current limiting, over temperature protection, and under voltage lockout.

Ordering Information

RT9181-□□ □□

- Package Type
  B : SOT-23-5
- Lead Plating System
  P : Pb Free
  G : Green (Halogen Free and Pb Free)
- Output Voltage
  Default : 1.2V
  18 : 1.8V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

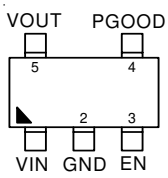
- **Low Dropout Voltage Regulator**
- **Up to 150mA Output Current**
- **Power Good (PGOOD) Function**
- **Chip Enable/Shutdown Function**
- **Load Independent, Low Quiescent Current, 160µA**
- **Current Limiting and Thermal Protection**
- **Under Voltage Lockout (UVLO)**
- **Low Variation Due to Load and Line Regulation**
- **Output Stable with Low ESR Capacitors**
- **SOT-23-5 Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Processor Power-Up Sequencing
- Laptop, Notebook, and Palmtop Computers

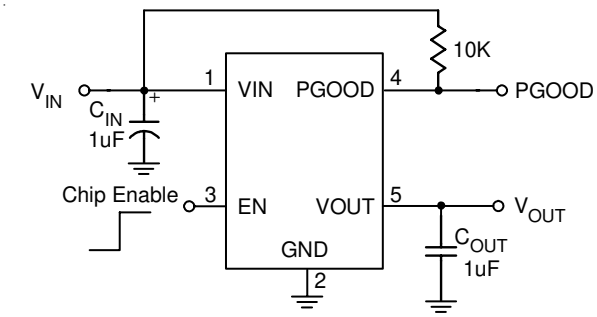
Pin Configurations

(TOP VIEW)

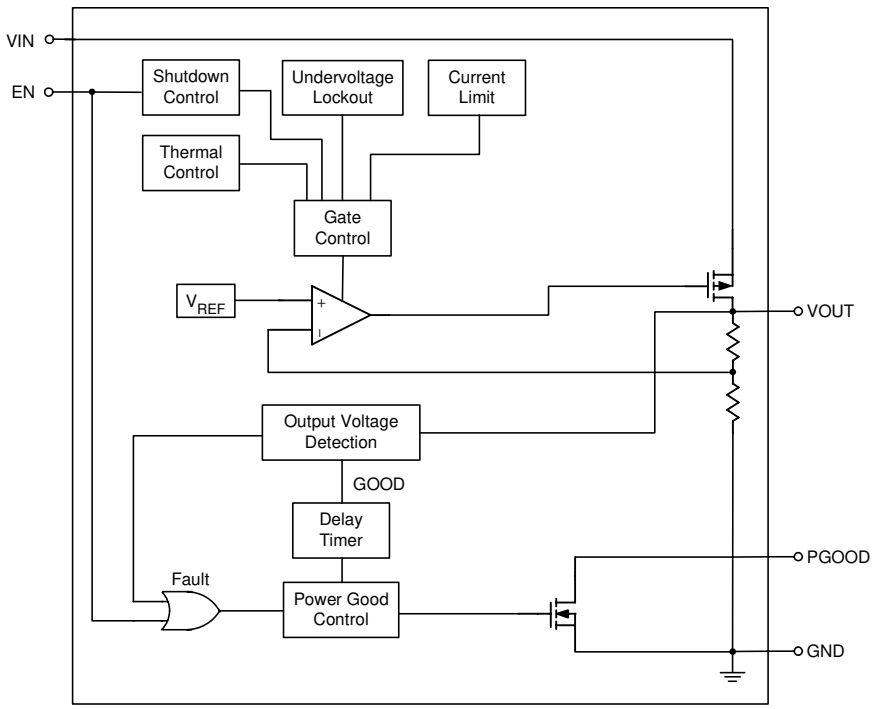


SOT-23-5

Typical Application Circuit



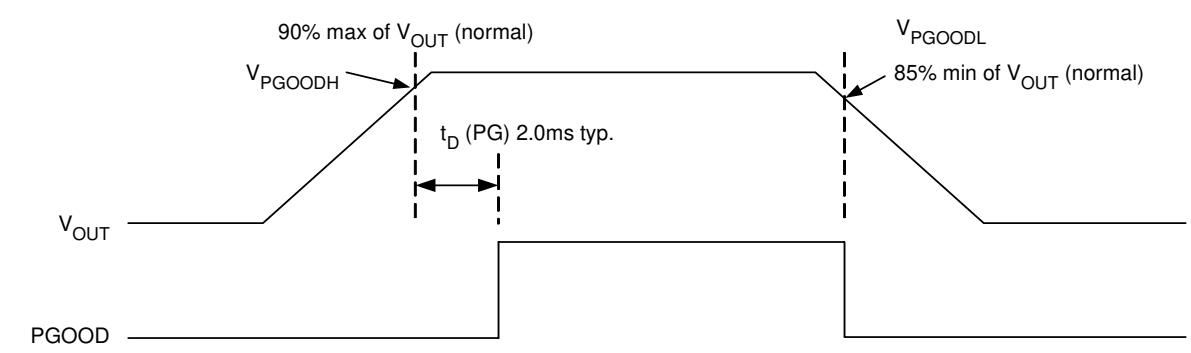
Function Block Diagram



Functional Pin Description

Pin Name	Pin Function
VIN	Power Input Voltage
GND	Ground
EN	Chip Enable (Active High)
PGOOD	Power Good Indicator
VOUT	Output Voltage

Timing Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- 7V
- Enable Input Voltage ---------- 7V
- Power Good Output Voltage ---------- 7V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-5 ---------- 0.4W
- Package Thermal Resistance (Note 2)
  SOT-23-5, θ_{JA} ---------- 250°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 3V to 5.5V
- Enable Input Voltage ---------- 0V to 5.5V
- Junction Temperature Range ---------- –40°C to 110°C

Electrical Characteristics

(V_{IN} = 5V, C_{IN} = C_{OUT} = 1μF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT} = 25mA	–1.5	--	1.5	%
			I_{OUT} = 0.1mA, T_A = 0°C to 70°C (Note 4)	–2	--	+2	
Current Limit		I_{LIM}	R_{LOAD} = 1Ω	160	300	--	mA
Quiescent Current (Note 5)		I_Q	I_{OUT} = 0mA	90	160	250	μA
Line Regulation		ΔV_{LINE}	V_{IN} = 3V to 5.5V, I_{OUT} = 0.1mA	–0.3	--	+0.3	%
Load Regulation (Note 6)		ΔV_{LOAD}	I_{OUT} = 0.1mA to 150mA	--	1.5	+3	%
EN Threshold	Logic-Low	V_{IL}	V_{IN} = 3V to 5.5V, Shutdown	--	--	0.8	V
	Logic-High	V_{IH}	V_{IN} = 3V to 5.5V, Enable	2.0	--	--	
EN Input Bias Current			EN = GND or V_{IN}	0	--	100	nA
Shutdown Current			EN = GND	0	0.01	1	μA
Power Good Low Threshold		V_{PGOODL}	Output falls % of V_{OUT} (power NOT good)	85	--	--	%
Power Good High Threshold		V_{PGOODH}	Output reaches % of V_{OUT}, start delay timer (power good)	--	--	90	%
Power Good Output Logic Low		V_{OL}	V_{IN} = 3.3V, I_{OL} = 2mA, $R_{DSON(max)}$ = 75Ω	0	--	0.15	V
Delay Time to Power Good		$t_{D(PGOOD)}$	See timing diagram	1	2	5	ms
Power Up Overshoot		V_{PGOODL}	Maximum voltage overshoot allowed on output during power-up	--	1	--	%

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Shutdown Temperature	T_{SD}		110	140	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C
Power Supply Rejection Rate	PSRR	f = 100Hz, C_{OUT} = 1μF	--	−62	--	dB

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

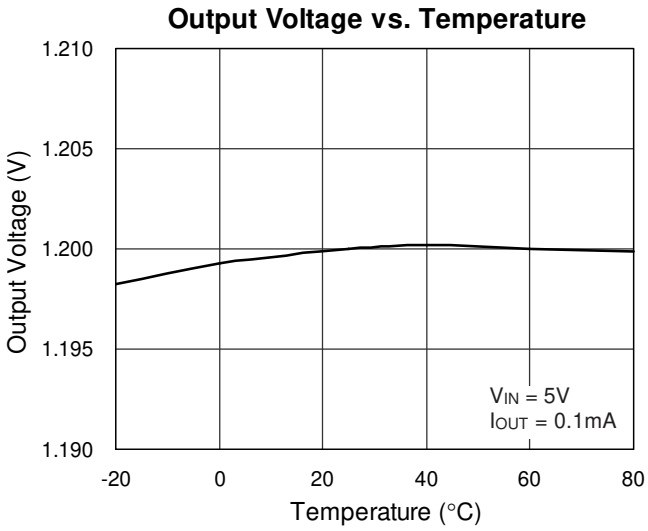
Note 3. Devices are ESD sensitive. Handling precaution recommended.

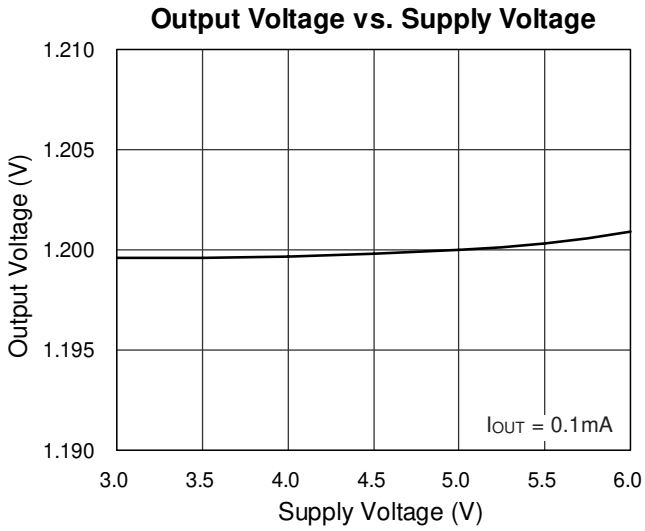
Note 4. The device is not guaranteed to function outside its operating conditions.

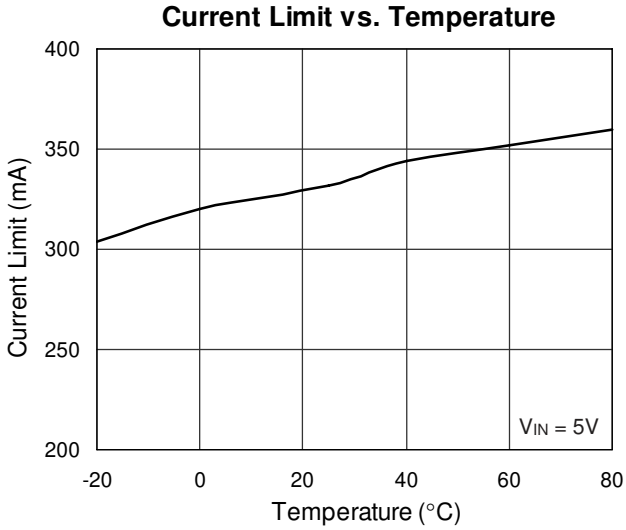
Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

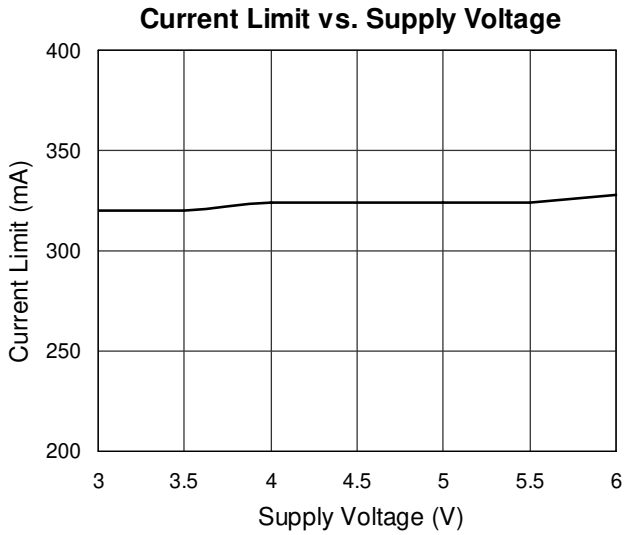
Note 6. Regulation is measured at constant junction temperature by using a 20ms current pulse. Devices are tested for load regulation in the load range from 0.1mA to 150mA.

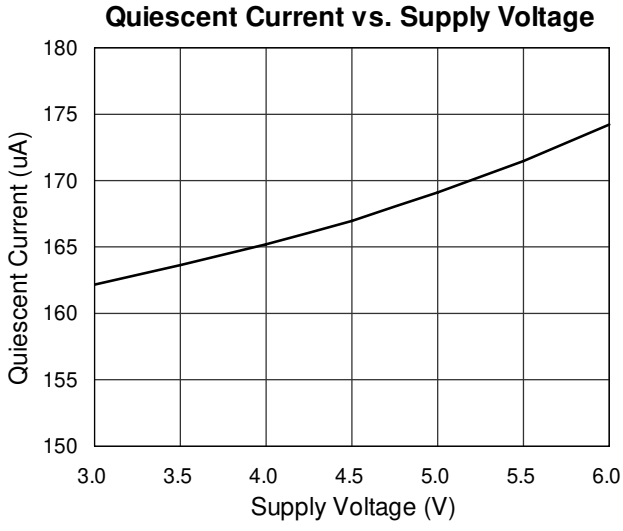
Typical Operating Characteristics

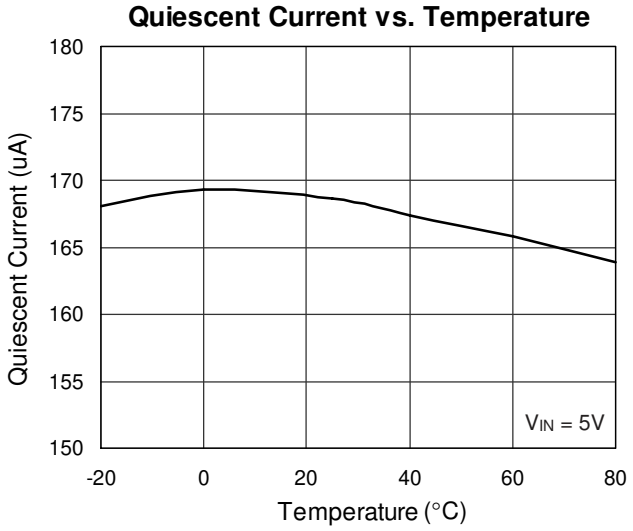




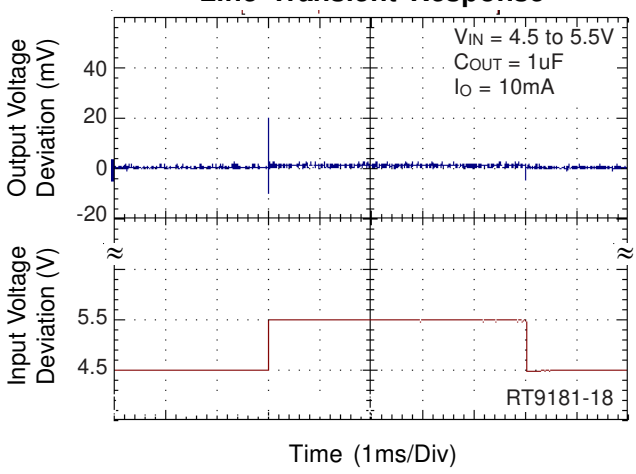




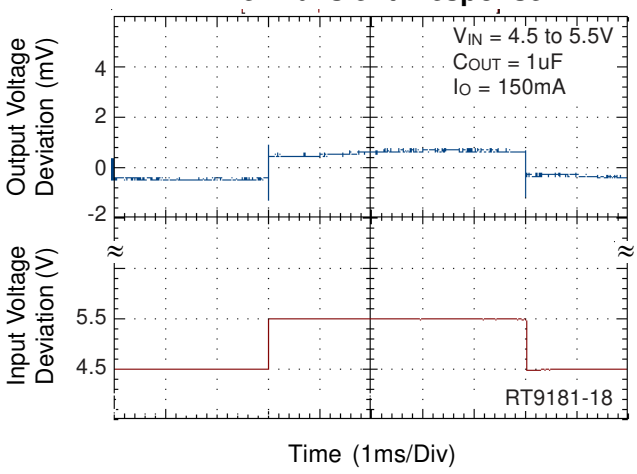




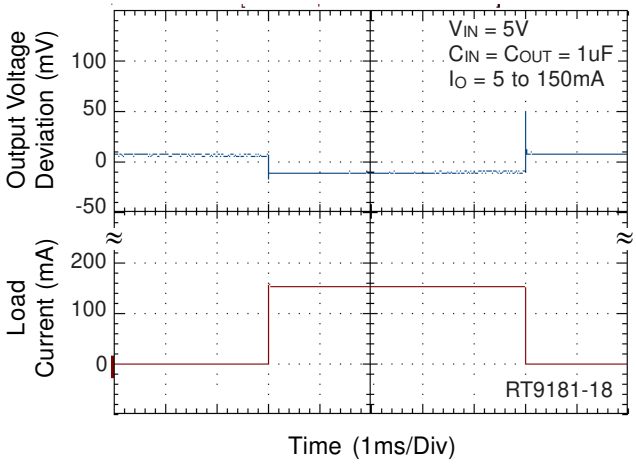
Line Transient Response



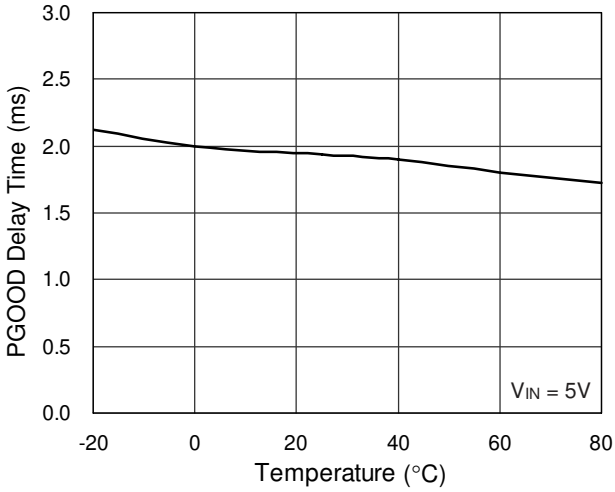
Line Transient Response



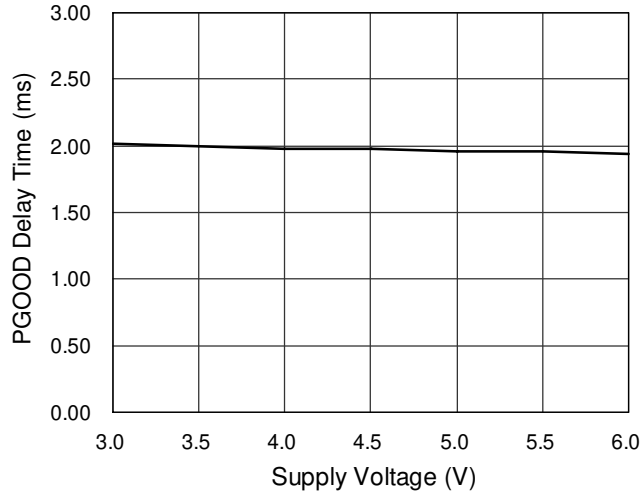
Load Transient Response



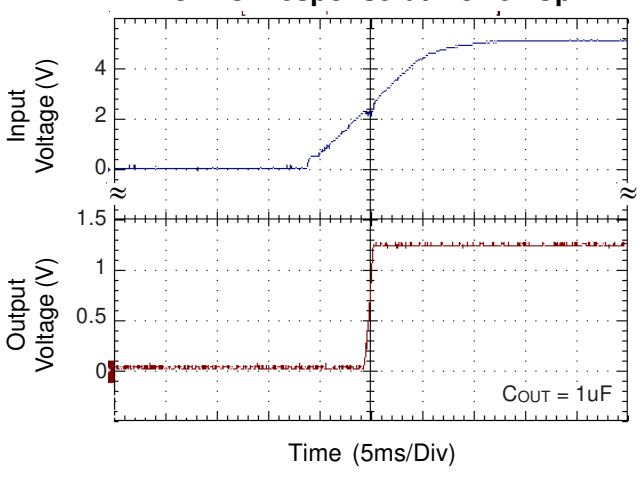
PGOOD Delay Time vs. Temperature

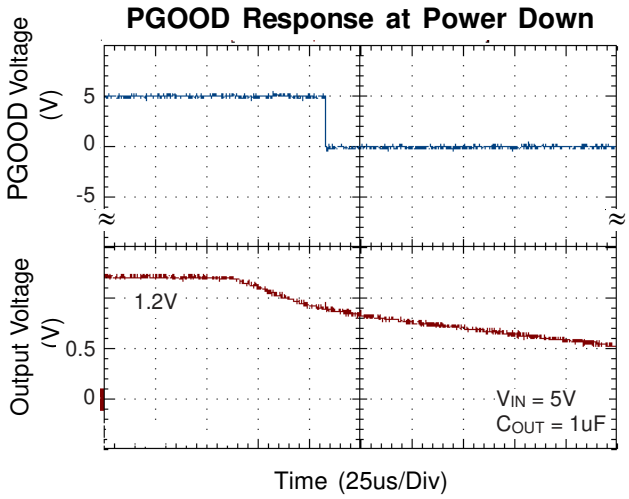


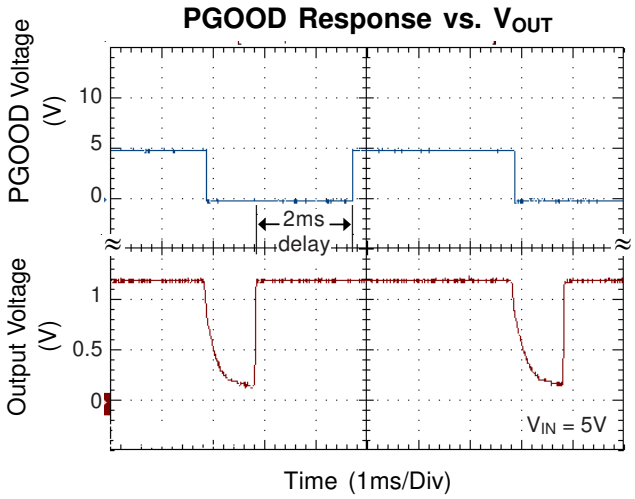
PGOOD Delay Time vs. Supply Voltage



UVLO Response at Power Up




PGOOD Response at Power Down
PGOOD Voltage (V)
5
0
-5
Output Voltage (V)
1.2V
0.5
0
VIN = 5V
COUT = 1uF
Time (25us/Div)


PGOOD Response vs. VOUT
PGOOD Voltage (V)
10
5
0
2ms
delay
Output Voltage (V)
1
0.5
0
VIN = 5V
Time (1ms/Div)

Application Information

EN

The RT9181 is enabled by driving the EN input high, and shutdown by pulling the input low. If this feature is not to be used, the EN input should be tied to VIN to keep the regulator enabled at all times (the EN input must **not** be left floating).

Internal P-Channel Pass Transistor

The RT9181 features a P-Channel MOSFET pass transistors. It provides several advantages over similar designs using PNP pass transistors, including longer battery life. The P-Channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP-based regulators waste considerable current in dropout when the pass transistor saturates, They also use high base-drive currents under large loads. The RT9181 does not suffer from these problems and consume only 160μA of quiescent current whether in dropout, light-load, or heavy-load applications.

Power Good

The power good output is an open-drain output. It is designed essentially to work as a power-on reset generator once the regulated voltage was up or a fault condition. The output of the power good drives low when a fault condition occurs. The power good output come back up once the output has reached 90% of its nominal value and a 2ms (typ.) delay has passed. See Timing Diagram. The output voltage level will be drooped at the fault conditions including current limit, thermal shutdown, or shutdown and triggers the PGOOD detector to alarm a fault condition. This output is fed into an on-board delay circuitry that drives the open drain transistor to indicate a fault.

Because at shutdown mode, a fault condition occurs by pulling the PGOOD output low, it will sink a current from the open drain and the external power. Selecting a suitable pulling resistance will be well to control this dissipated power.

Current Limit and Thermal Protection

The RT9181 includes a current limit structure which monitor and control the pass transistor's gate voltage limiting the guaranteed maximum output current to 160mA minimum.

Thermal-overload protection limits total power dissipation in the RT9181. When the junction temperature exceeds T_J = +140°C, the thermal sensor signals the shutdown logic turning off the pass transistor and allowing the IC to cool. The thermal sensor will turn the pass transistor on again after the IC's junction temperature cools by 20°C, resulting in a pulsed output during continuous thermal-overload conditions. Thermal-overloaded protection is designed to protect the RT9181 in the event of fault conditions. Do not exceed the recommended maximum junction-temperature rating of T_J = +110°C for continuous operation. The output can be shorted to ground for and indefinite amount of time without damaging the part by cooperation of current limit and thermal protection.

Operating Region and Power Dissipation

The maximum power dissipation of RT9181 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation across the device is

$$P = I_{OUT} (V_{IN} - V_{OUT})$$

The GND pin of the RT9181 performs the dual function of providing an electrical connection to ground and channeling heat away, Connect the GND pin to ground using a large pad or ground plane.

Capacitor Selection and Regulator Stability

Like any low-dropout regulator, the external capacitors used with the RT9181 must be carefully selected for regulator stability and performance. Using a capacitor whose value is ≥ 1μF on the RT9181 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5" from the input pin of the IC and returned to a clean analog ground.

Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDO applications. The RT9181 is designed specifically to work with low-ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 5mΩ on the RT9181 output ensures stability. The RT9181 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load-transient response, stability, and PSRR. The output capacitor should be located not more than 0.5" from the V_{OUT} pin of the RT9181 and returned to a clean analog ground.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. It may be necessary to use 2.2μF or more to ensure stability at temperatures below -10°C in this case. Also, tantalum capacitors, 2.2μF or more may be needed to maintain capacitance and ESR in the stable region for strict application environment.

Tantalum capacitors maybe suffer failure due to surge current when it is connected to a low-impedance source of power (like a battery or very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed to have a surge current rating sufficient for the application by the manufacturer.

Load-Transient Considerations

The RT9181 load-transient response graphs show two components of the output response: a DC shift from the output impedance due to the load current change, and the transient response. The DC shift is quite small due to the excellent load regulation of the IC. Typical output voltage transient spike for a step change in the load current from 0mA to 50mA is tens mV, depending on the ESR and ESL of the output capacitor. Increasing the output capacitor's value and decreasing the ESR and ESL attenuates the overshoot.

Reverse Current Path

The power transistor used in the RT9181 has an inherent diode connected between each regulator input and output (see Figure 1). If the output is forced above the input by more than a diode-drop, this diode will become forward biased and current will flow from the V_{OUT} terminal to V_{IN}. This diode will also be turned on by abruptly stepping the input voltage to a value below the output voltage. To prevent regulator mis-operation, a Schottky diode could be used in the applications where input/output voltage conditions can cause the internal diode to be turned on (see Figure 2). As shown, the Schottky diode is connected in parallel with the internal parasitic diode and prevents it from being turned on by limiting the voltage drop across it to about 0.3V @ 100mA to prevent damage to the part.

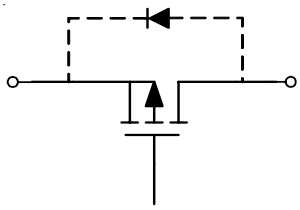


Figure 1

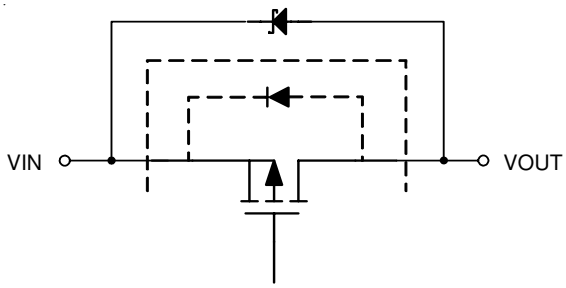
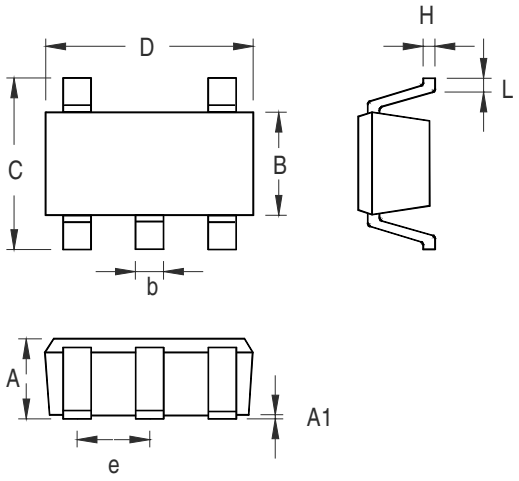


Figure 2

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package

Richtek Technology Corporation
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation
Taipei Office (Marketing)
5F, No. 95, Minchiuan Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)86672399 Fax: (8862)86672377
Email: marketing@richtek.com