Title	***Reference Design Report for a 12 W Dual Output Power Supply Using InnoSwitch3™-TN INN3074M***
Specification	85 VAC – 265 VAC Input 5 V, 1.4 A and 12 V, 0.42 A Outputs
Application	Dual Output Open Frame Appliance Power Supply
Author	Applications Engineering Department
Document Number	RDR-710
Date	November 10, 2021
Revision	1.1

Summary and Features

- 12 W output from 85 VAC to 265 VAC
- Built in synchronous rectification for >85% efficiency at nominal AC input
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
- <10 mW no-load input power typically
- <260 mW standby input power at 5 V / 30 mA load
- Primary sensed output overvoltage protection (OVP) eliminates optocoupler for fault protection
- Accurate thermal protection with hysteretic shutdown

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Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 1.4 A, 5 V and 0.42 A, 12 V dual output embedded power supply utilizing INN3074M from the InnoSwitch3-TN family of ICs.

This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

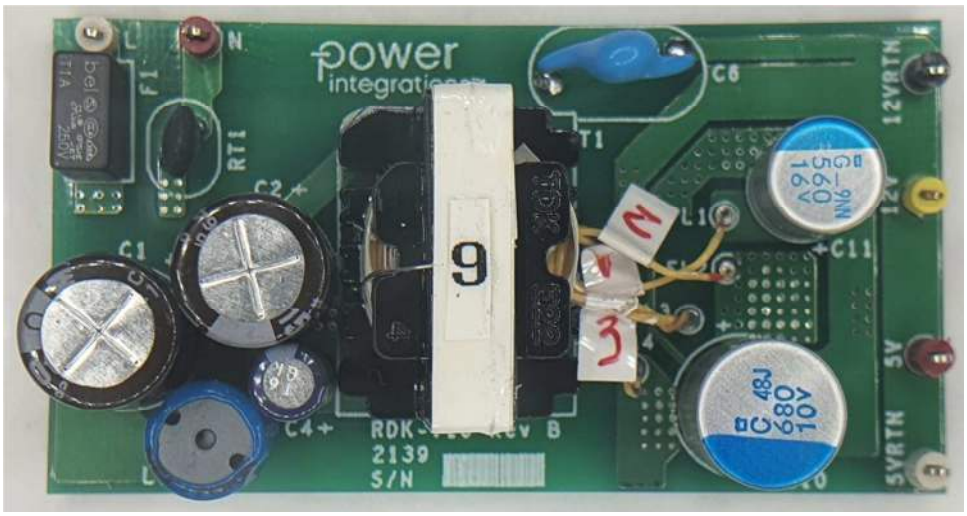


Figure 1 – Populated Circuit Board Photograph, Top.

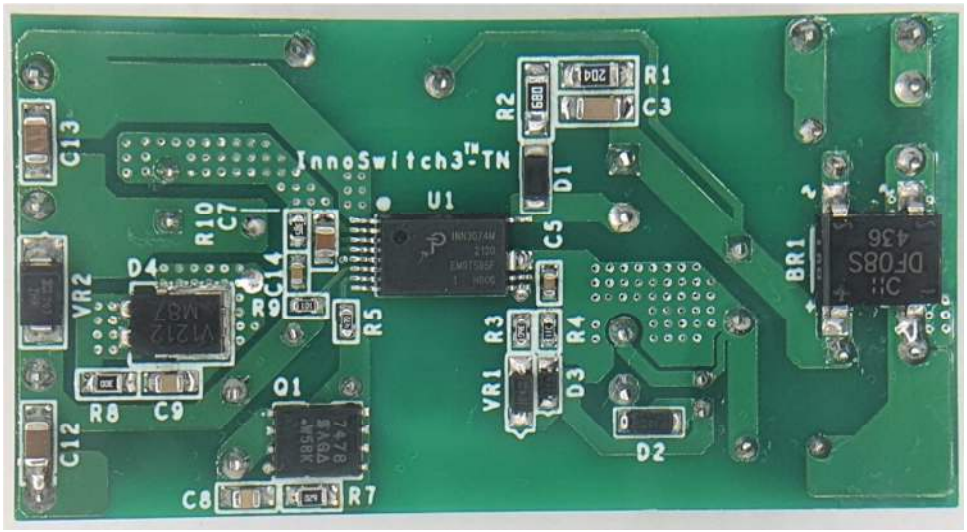


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	115/230	265	VAC	2 Wire Input.
Frequency	f_{LINE}		50/60		Hz	
No-Load Input Power				30	mW	
Standby Power (5 V / 30 mA)				300	mW	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	±5 %
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0	1.4		A	
Output Voltage 2	V_{OUT2}	10.2	12	13.8	V	±15 %, (±10 % with 10% Min Load on 12 V.)
Output Ripple Voltage 2	$V_{RIPPLE2}$			120	mV	20 MHz Bandwidth.
Output Current 2	I_{OUT2}	0	0.42		A	
Total Output Power						
Continuous Output Power	P_{OUT}			12	W	
Efficiency						
Average 25%, 50%, 75%, and 100%	$\eta_{AVE[BRD]}$	85			%	Measured at 115 / 230 VAC, P_{OUT} 25 ºC. V_{IN} at 230 VAC.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B Load Floating				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge						
Differential		1			kV	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω.
Common mode Ring Wave		6			kV	100 kHz Ring Wave, 12 Ω Common Mode.
EFT		2			kV	100 kHz, 15 ms burst time, 120s repetition time, 12 Ω EFT
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

3 Schematic

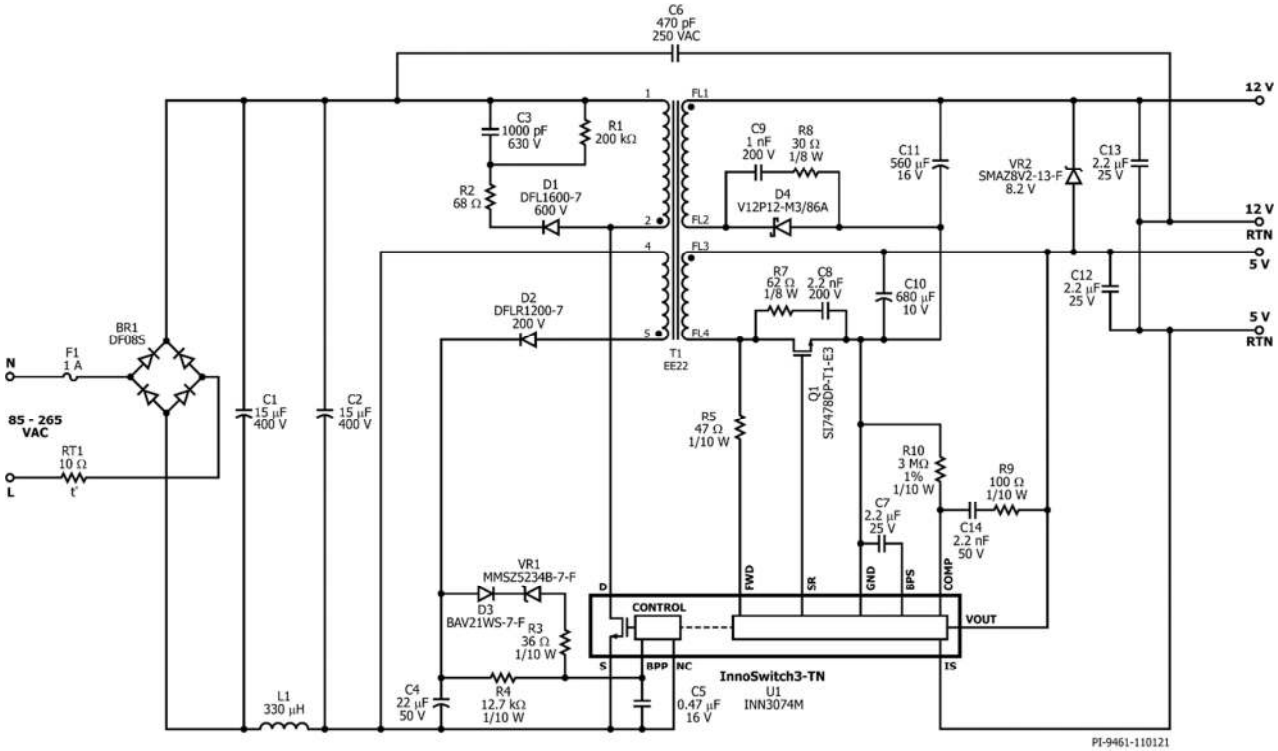


Figure 3 – Schematic.

4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 isolates the circuit and provides protection from component failure and thermistor RT1 limits inrush current and for surge protection.

Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of C1 and C2. The differential inductance of L1 with capacitors C1 and C2 provide differential noise filtering.

4.2 *InnoSwitch3-TN Primary*

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 725 V power MOSFET inside the InnoSwitch3-TN IC (U1).

A low cost RCD clamp formed by D1, R2, R1, and C3 limits the peak drain voltage due to the effects of transformer leakage inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C5, when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C4, and fed in the BPP pin via a current limiting resistor R4. The primary-side overvoltage protection is obtained using VR1, D3, R3 circuit. In the event of overvoltage at output, the increased voltage at the output of the bias winding cause the Zener diode VR1 to conduct and triggers the OVP latch in the primary side controller of the InnoSwitch3-TN IC.

4.3 *InnoSwitch3-TN IC Secondary*

The secondary-side of the InnoSwitch3-TN provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Output rectification for the 5 V output is provided by SR FET Q1. Very low ESR capacitor C10 and ceramic capacitor C12, provides filtering and significantly attenuates the high frequency ripple and noise at the 5 V output.

Output rectification for the 12 V output is provided by Schottky diode D4. Very low ESR capacitor C11 and ceramic capacitor C13, provides filtering and significantly attenuates the high frequency ripple and noise at the 12 V output.

RC snubber networks comprising R7 and C8 for Q1, R8 and C9 for D4 damp high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances.

The gate of Q1 are turned on based on the winding voltage sensed via R5 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary-side control of the primary-side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, fed into the VO pin and charges the decoupling capacitor C7 and an internal regulator. The unit enters auto-restart when the sensed output voltage is lower than 3 V.

This IC has internal feedback, no need for voltage divider network. Resistor R10 boosts the output voltage above 5 V. Zener diode VR2 improves the cross regulation when only the 5 V output is loaded, which results in the 12 V output operating at the higher end of the specification. The InnoSwitch3-TN IC has an internal reference of 1.265 V. Feedback compensation network comprising capacitor C14 and resistor R2 reduce the output ripple voltage.

5 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 71 µm) unless otherwise stated.

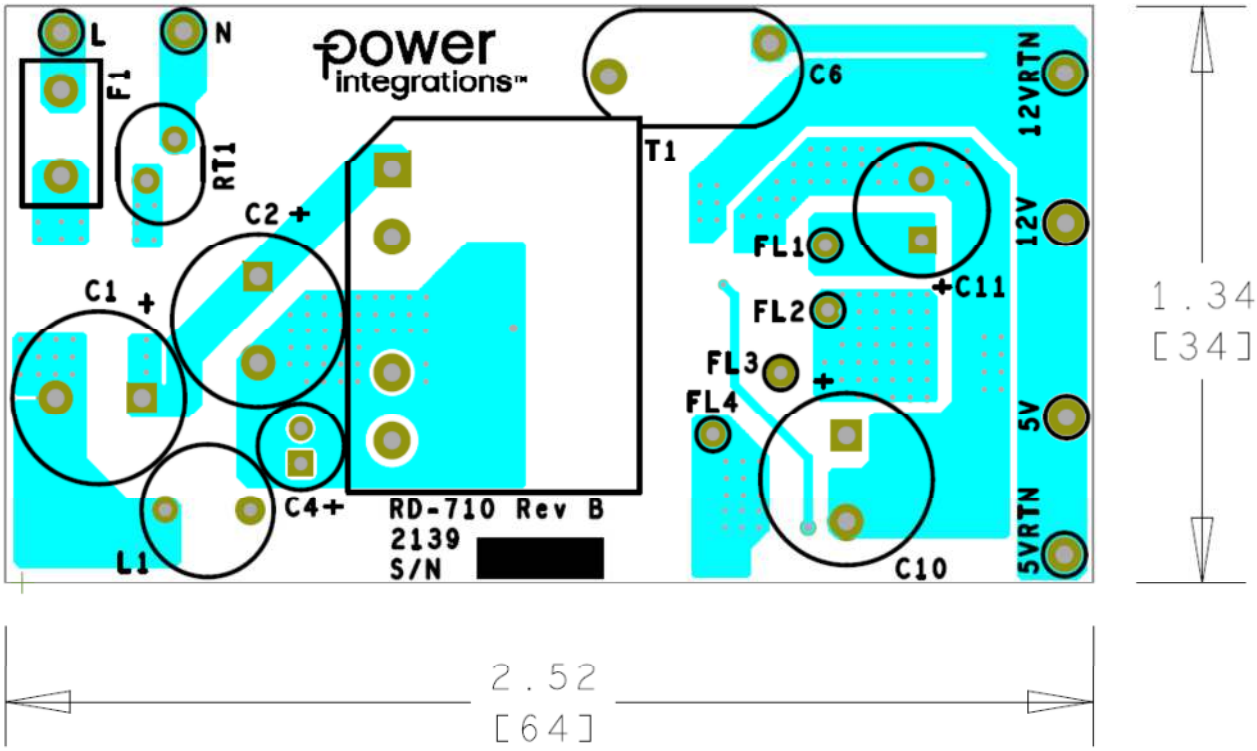


Figure 4 – Printed Circuit Layout, Top.

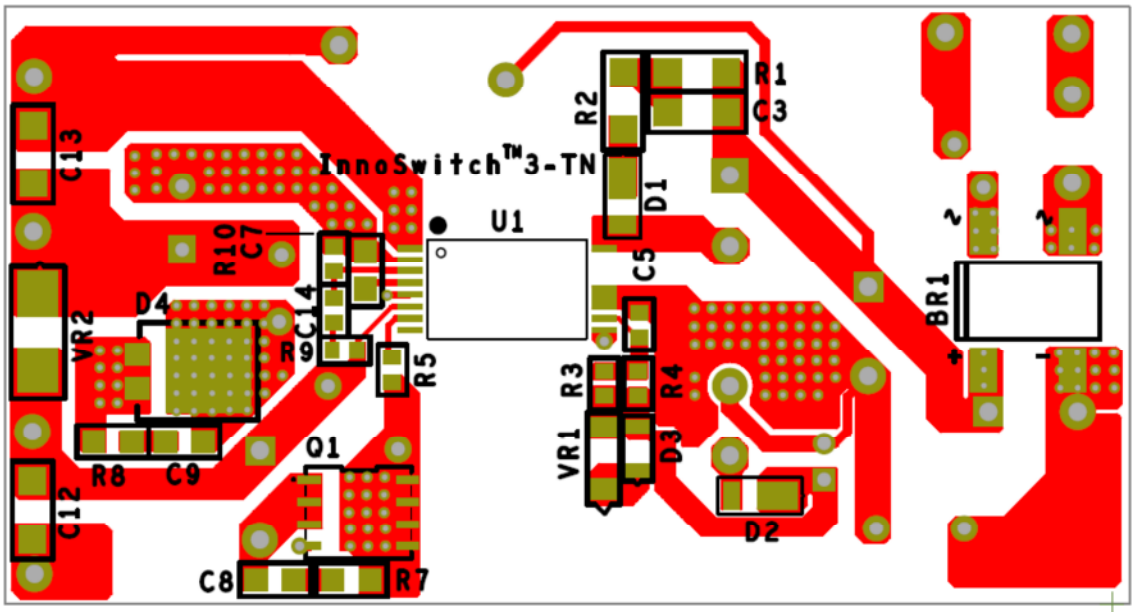


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	800 V, 1 A, Bridge Rectifier, SMD, DFS 1000 V, 1 A, Bridge Rectifier, SMD, DFS	DF08S DF10S-T	Diodes, Inc.
2	2	C1 C2	15 µF, 400 V, Electrolytic, (10 x 16)	UVC2G150MPD	Nichicon
3	1	C3	1000 pF, 630 V, Ceramic, X7R, 1206	C1206C102KBRACTU	Kemet
4	1	C4	22 µF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
5	1	C5	0.47 µF, 10%, 16 V, X7R, 0603	GRM188R71C474KA88D	Murata
6	1	C6	470 pF, ±10%, 250 VAC, X1, Y1, Ceramic, Radial, Disc	DE1B3RA471KN4AN01F	Murata
7	1	C7	2.2 µF, ±20%, 25 V, Ceramic, X7R, 0805	CGA4J3X7R1E225M125AB	TDK
8	1	C8	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX
9	1	C9	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
10	1	C10	680 µF, 10 V, Al Polymer, Low ESR 7 mΩ, 20%, (10 x 11.5)	APSC100ELL681MJB5S	United Chemi-Con
11	1	C11	560 µF, 16 V, Al Polymer, Low ESR 8 mΩ, 20%, (8 x 13)	APSG160ELL561MHB5J	United Chemi-con
12	2	C12 C13	2.2 µF, ±10%, 25 V, Ceramic, X7R, 1206	12063C225K4Z2A	AVX
13	1	C14	2.2 nF 50 V, Ceramic, X7R, 0603	C0603C222K5RACTU	Yageo
14	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
15	1	D2	200 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
16	1	D3	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
17	1	D4	Diode, Schottky, 120 V, 12 A, SMT, TO-277A (SMPC)	V12P12-M3/86A	Vishay
18	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
19	1	L1	330 µH, 0.55 A, 9 x 11.5 mm	SBC3-331-551	Tokin
20	1	Q1	60 V, 15 A, N-Channel, PowerPAK SO-8	SI7478DP-T1-E3	Vishay
21	1	R1	RES, 200 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
22	1	R2	RES, 68 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ680V	Panasonic
23	1	R3	RES, 36 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ360V	Panasonic
24	1	R4	RES, 12.7 kΩ, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1272V	Panasonic
25	1	R5	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
26	1	R7	RES, 62 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ620V	Panasonic
27	1	R8	RES, 30 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ300V	Panasonic
28	1	R9	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
29	1	R10	RES, 3 MΩ, ±1%, 1/10 W, Chip Resistor, 0603, Moisture Resistant Thick Film	RC0603FR-073ML	Yageo
30	1	RT1	NTC Thermistor, 10 Ω, 0.7 A	MF72-010D5	Cantherm
31	1	T1	Bobbin, EE22. Vertical,10 pins Trransformer	BE-22-1110CPFR POL-INN050	TDK Premeir Magnetics
32	1	U1	InnoSwitch3-TN, MinSOP-16	INN3074M	Power Integrations
33	1	VR1	Diode, Zener 6.2 V 500 mW SOD123	MMSZ5234B-7-F	Diodes, Inc.
34	1	VR2	Diode, Zener, 8.2 V, ±5%, 1 W, DO-214AC, SMA	SMAZ8V2-13-F	Diodes, Inc.
35	1	12V	TEST POINT, PC MINI, .040"(1.02mm)D, YELLOW, THRU-HOLE MOUNT	5004	Keystone
36	2	12VRTN NEUTRAL	Test Point, BLK,Miniature THRU-HOLE MOUNT	5001	Keystone
37	1	5V	Test Point, RED,Miniature THRU-HOLE MOUNT	5000	Keystone
38	2	5VRTN LINE	Test Point, WHT,Miniature THRU-HOLE MOUNT	5002	Keystone

7 Transformer (T1) Specification

7.1 *Electrical Diagram*

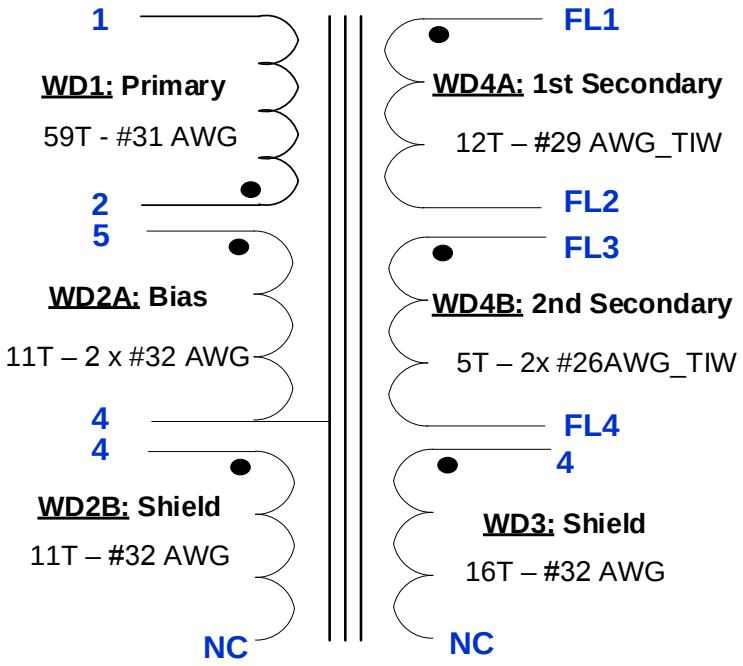


Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and 2, with all other windings open.	948 µH ±3%
Primary Leakage Inductance	Between pin 1 and 2, with FL1, FL2, FL3, FL4 shorted.	40 µH (Max).

7.3 *Material List*

Item	Description
[1]	Core: EE22; ACME, P4 or Equivalent; Gapped for AL±25% of 1900nH/T².
[2]	Bobbin: EE22 - Vertical – 10 pins, TDK.
[3]	Magnet Wire: #31 AWG, Double Coated.
[4]	Magnet Wire: #32 AWG, Double Coated.
[5]	Magnet Wire: #29 AWG, Triple Insulated Wire.
[6]	Magnet Wire: #26 AWG, Triple Insulated Wire.
[7]	Barrier Tape: 3M 1298 Polyester Film, 1 mil Thickness, 9 mm Wide.
[8]	Copper Foil: 2 mil Thick, 5.7 mm x 22.0 mm.
[9]	Tape: 3M Polyester Film, 1 mil Thick, 5.7 mm Wide.
[10]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

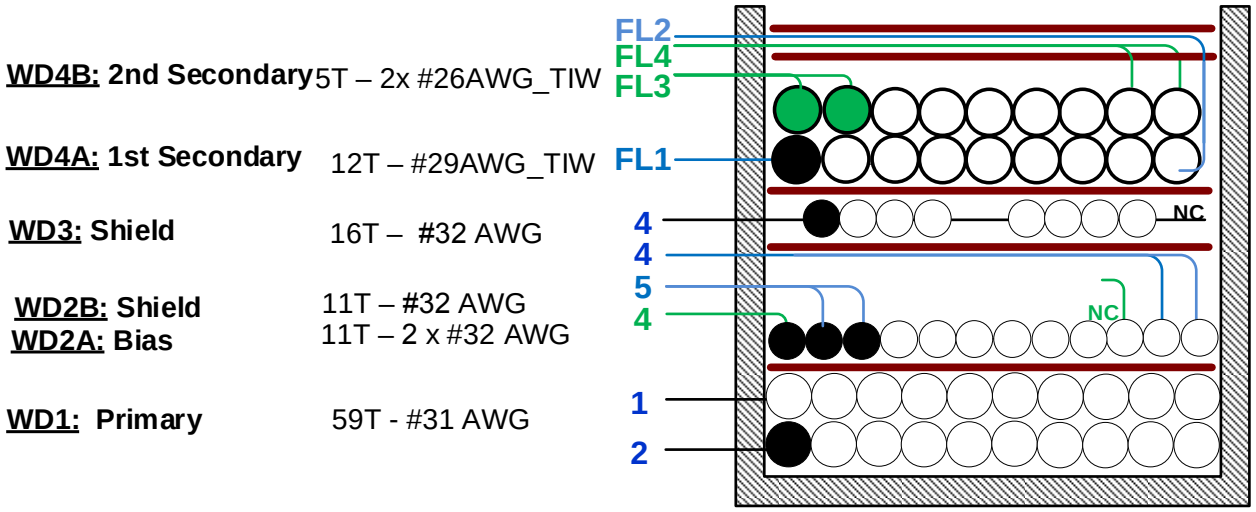
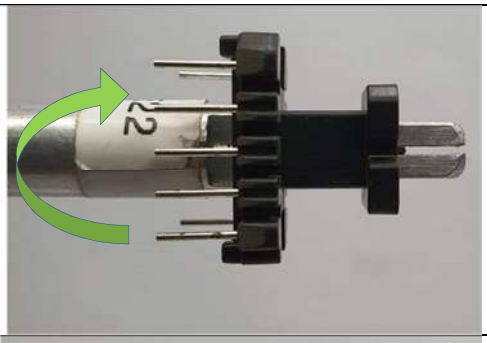
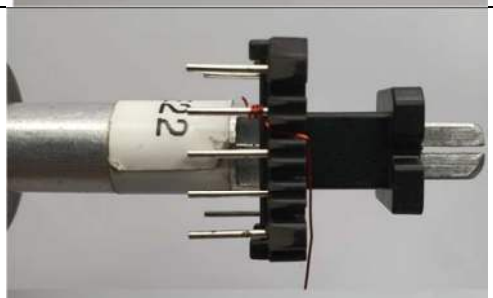
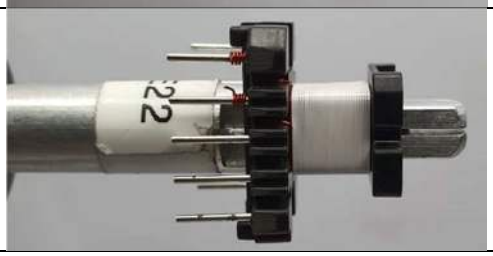


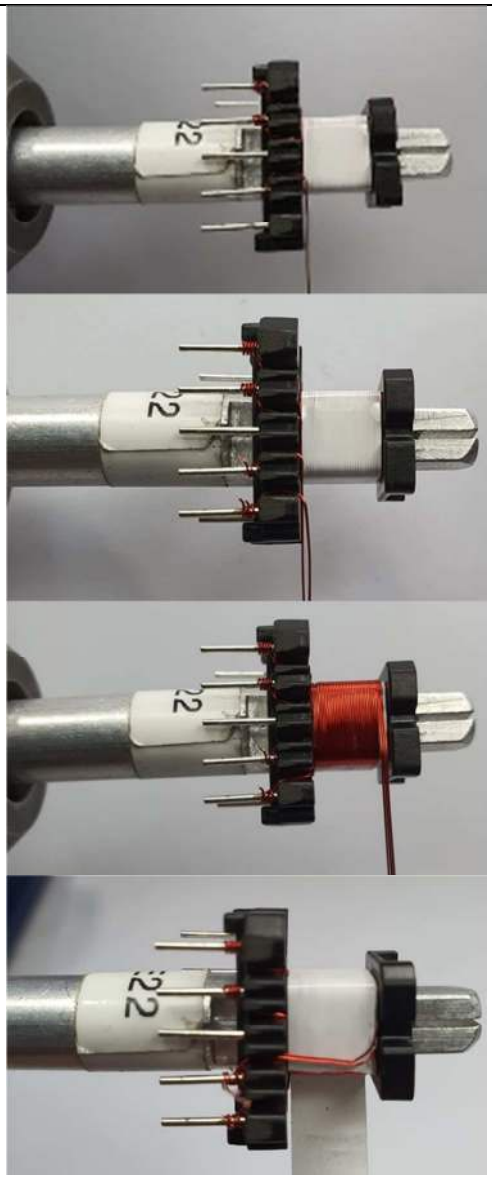
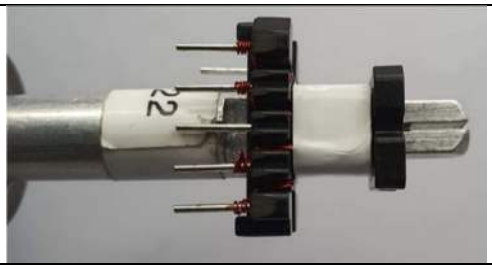
Figure 7 – Transformer Electrical Diagram.

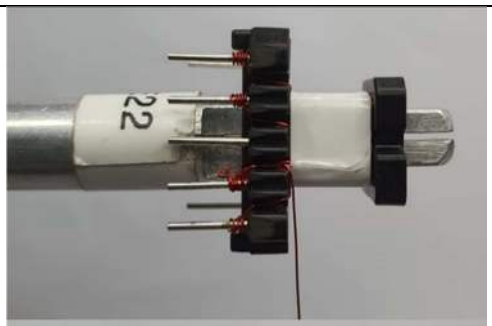
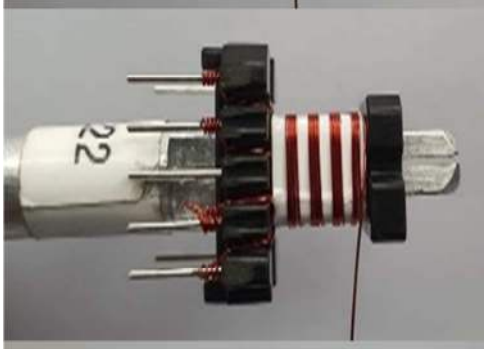
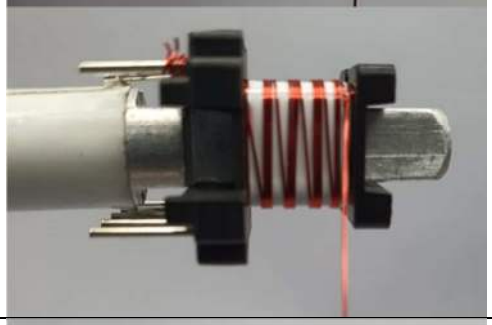
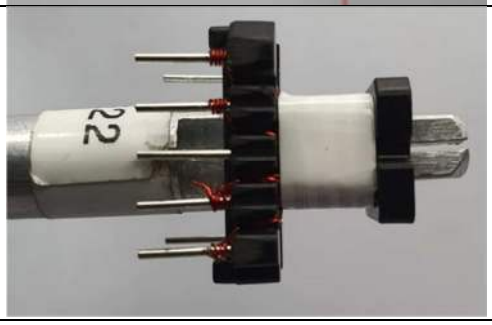
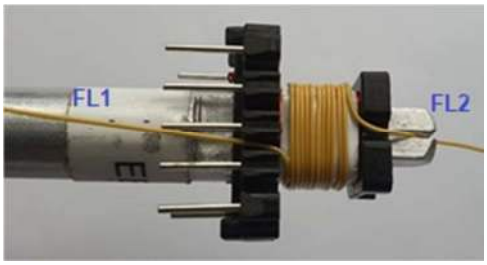
7.5 *Winding Instructions*

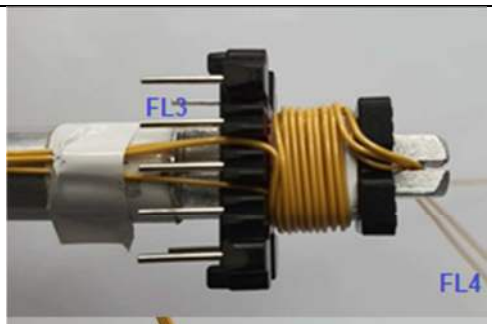
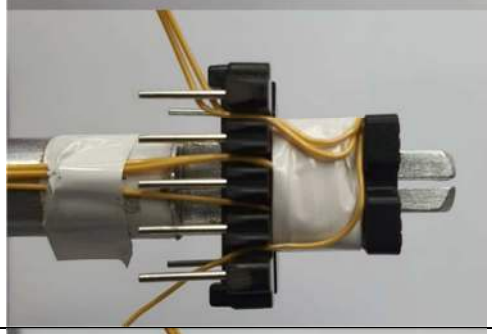
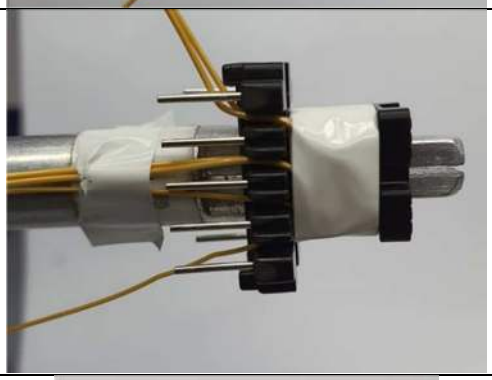
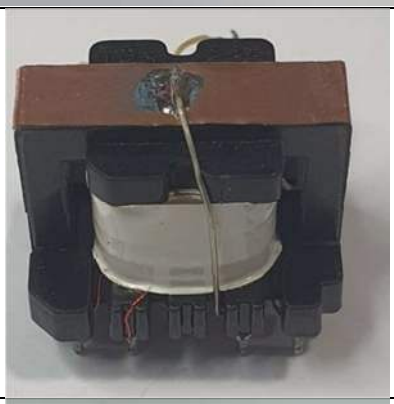
WD1 Primary	Start at pin 2, wind 30 turns of wire Item [3] from left to right. Continue to wind 29 turns on the second layer using the same wire from right to left and terminate the wire on pin 1.
Insulation	1 layer of tape Item [7] for insulation.
WD2A Bias & WD2B Shield	Take 3 wires Item [4], start at pin 5 for 2 wires (Bias), start at pin 4 for 1 wire (Shield), wind 11 turns for all 3 wires from left to right, cut 1 wire (Shield) and leave no-connection for WD2B-Shield. Bring other 2 wires (Bias) to the left and terminate to pin 4.
Insulation	1 layer of tape Item [7] for insulation.
WD3 Shield	Take 1 wire Item [4], start at pin 4 wind 16 turns from left to right, leave no-connection for WD3-Shield. Shield should be wind equally spaced and by 4 turns (Please see illustration).
Insulation	1 layer of tape Item [7] for insulation.
WD4A 1st Secondary & WD4B 2nd Secondary	Take 1 wire Item [5], designate start leads FL1 for WD4A. Wind 12 turns for WD4A and designate the finish lead to FL2. Take 2 wire Item [6] and designate start leads FL3 for WD4B, wind 5 turns and designate the finish lead to FL4. Please see illustration. Turn 1 layer of tape and bring three wire to the left and turn another 1 layer of tape for insulation.
Finish	Cut short FL1 & FL2 to ~22.0 mm and FL3 & FL4 to ~19.0 mm. Gap the core halves to get 948 µH. Prepare copper foil Item [8], solder wire Item [3] at the middle to connect to pin 4, and then place on top core halves. Then secure 2 core halves with 2 layers of tape Item [9]. Remove pins: 3, 6,7,8,9 and 10. Varnish with Item [10].

7.6 *Winding Illustrations*

Winding Preparation		For the purpose of these instructions, bobbin Item [1] is oriented on winder such that pin side is on the left side.
WD1 Primary (1st Layer)	 	Start at pin 2, wind 30 turns of wire Item [3] from left to right. Continue to wind 29 turns on the second layer using the same wire from right to left and terminate the wire on pin 1.
Insulation		1 layer of tape Item [7] for insulation.

WD2A Bias & WD2B Shield		Take 3 wires Item [4], start at pin 5 for 2 wires (Bias), start at pin 4 for 1 wire (Shield), wind 11 turns for all 3 wires from left to right, Cut 1 wire (Shield) and leave no-connection for WD2B-Shield. Bring other 2 wires (Bias) to the left and terminate to pin 4.
Insulation		1 layer of tape Item [7] for insulation.

WD3 Shield	  	Take 1 wire Item [4], start at pin 3 wind 16 turns from left to right. Shield should be wind equally spaced and by 4 turns. Back view (secondary side).
Insulation		1 layer of tape Item [7] for insulation.
WD4A 1st Secondary and WD4B 2nd Secondary		Take 1 wire Item [5], designate start leads FL1 for WD4A. Wind 12 turns for WD4A and designate the finish lead to FL2. Take 2 wire Item [6] and designate start leads FL3

	 	for WD4B, wind 5 turns and designate the finish lead to FL4. Please see illustration. Turn 1 layer of tape and bring three wire to the left.
Insulation		1 layer of tape Item [7] for insulation.
Finish		Cut short FL1 & FL2 to ~22.0 mm and FL3 & FL4 to ~19.0 mm. Gap the core halves to get 948 μH. Prepare copper foil Item [8], solder wire Item [3] at the middle to connect to pin 4, and then place on top core halves.
Insulation		Then secure 2 core halves with 2 layers of tape Item [9]. Remove pins: 3, 6,7,8,9 and 10. Varnish with Item [10].

7.7 *Transformer Design Spreadsheet*

ACDC_InnoSwitch3-TN_Flyback_092121; Rev.0.2; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 TN Flyback Design Spreadsheet
APPLICATION VARIABLES					
VIN_MIN			85	V	Minimum AC input voltage
VIN_MAX			265	V	Maximum AC input voltage
VIN_RANGE			UNIVERSAL		Range of AC input voltage
LINEFREQ			60	Hz	AC Input voltage frequency
CAP_INPUT	30.0		30.0	uF	Input capacitor
VOUT			5.00	V	Output voltage at the board
CDC	0		0	mV	Cable drop compensation desired at full load
IOUT	2.400		2.400	A	Output current
POUT			12.00	W	Output power
EFFICIENCY			0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
FACTOR_Z			0.50		Z-factor estimate
ENCLOSURE			OPEN FRAME		Power supply enclosure
PRIMARY CONTROLLER SELECTION					
ILIMIT_MODE			INCREASED		Device current limit mode
DEVICE_GENERIC	INN3074		INN3074		Generic device code
DEVICE_CODE			INN3074M		Actual device code
POUT_MAX			16.0	W	Power capability of the device based on thermal performance
ICC_MIN			2.40	A	Minimum constant current regulation threshold of the device
ICC_TYP			2.60	A	Typical constant current regulation threshold of the device
ICC_MAX			2.80	A	Maximum constant current regulation threshold of the device
RDSON_100DEG			5.74	Ω	Primary switch on time drain resistance at 100 degC
ILIMIT_MIN			0.690	A	Minimum current limit of the primary switch
ILIMIT_TYP			0.750	A	Typical current limit of the primary switch
ILIMIT_MAX			0.810	A	Maximum current limit of the primary switch
VDRAIN_BREAKDOWN			725	V	Device breakdown voltage
VDRAIN_ON_PRSW			0.79	V	Primary switch on time drain voltage
VDRAIN_OFF_PRSW			503.4	V	Peak drain voltage on the primary switch during turn-off
WORST CASE ELECTRICAL PARAMETERS					
FSWITCHING_MAX	65000		65000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
VOR	60.0		60.0	V	Secondary voltage reflected to the primary when the primary switch turns off
VMIN			92.84	V	Valley of the minimum input AC voltage at full load
KP			0.92		Measure of continuous/discontinuous mode of operation
MODE_OPERATION			CCM		Mode of operation
DUTYCYCLE			0.395		Primary switch duty cycle
TIME_ON			7.74	us	Primary switch on-time
TIME_OFF			9.31	us	Primary switch off-time
LPRIMARY_MIN			919.4	uH	Minimum primary inductance
LPRIMARY_TYP			947.9	uH	Typical primary inductance
LPRIMARY_TOL	3.0		3.0	%	Primary inductance tolerance

LPRIMARY_MAX			976.3	uH	Maximum primary inductance
PRIMARY CURRENT					
IPEAK_PRIMARY			0.736	A	Primary switch peak current
IPEDESTAL_PRIMARY			0.052	A	Primary switch current pedestal
IAVG_PRIMARY			0.138	A	Primary switch average current
IRIPPLE_PRIMARY			0.736	A	Primary switch ripple current
IRMS_PRIMARY			0.261	A	Primary switch RMS current
SECONDARY CURRENT					
IPEAK_SECONDARY			**8.687**	**A**	**Secondary winding peak current**
IPEDESTAL_SECONDARY			0.608	A	Secondary winding current pedestal
IRMS_SECONDARY			3.810	A	Secondary winding RMS current
TRANSFORMER CONSTRUCTION PARAMETERS					
CORE SELECTION					
CORE	EE22		EE22		Core selection. Refer to the 'Transformer Construction' tab to see the detailed report
CORE CODE	EE22 P4 ACME	Info	PC40EE22-Z		Either custom core code is not entered or a standard core code has been overwritten
AE	36.26		36.26	mm^2	Core cross sectional area
LE	41.96		41.96	mm	Core magnetic path length
AL	1900		1900	nH/turns^2	Ungapped core effective inductance
VE	1610.0		1610.0	mm^3	Core volume
BOBBIN			BE22-118CPFR		Bobbin
AW			20.00	mm^2	Window area of the bobbin
BW			8.45	mm	Bobbin width
MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
PRIMARY WINDING					
NPRIMARY			59		Primary turns
BPEAK			3783	Gauss	Peak flux density
BMAX			3330	Gauss	Maximum flux density
BAC			1665	Gauss	AC flux density (0.5 x Peak to Peak)
ALG			272	nH/turns^2	Typical gapped core effective inductance
LG			0.143	mm	Core gap length
SECONDARY WINDING					
NSECONDARY	5		5		Secondary turns
BIAS WINDING					
NBIAS			11		Bias turns
PRIMARY COMPONENTS SELECTION					
BIAS DIODE					
VBIAS	10.0		10.0	V	Rectified bias voltage
VF_BIAS			0.70	V	Bias winding diode forward drop
VREVERSE_BIASDIODE			79.61	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
CBIAS			22	uF	Bias winding rectification capacitor
CBPP			4.70	uF	BPP pin capacitor
MULTIPLE OUTPUT PARAMETERS					
OUTPUT 1					
VOUT1			5.00	V	Output 1 voltage
IOUT1	1.40		1.40	A	Output 1 current
POUT1			7.00	W	Output 1 power
IRMS_SECONDARY1			2.222	A	Root mean squared value of the secondary current for output 1
IRIPPLE_CAP_OUTPUT1			1.726	A	Current ripple on the secondary waveform for output 1
NSECONDARY1			5		Number of turns for output 1
VREVERSE_RECTIFIER1			36.64	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
SRFET1	Auto		Si4436DY		Secondary rectifier (Logic MOSFET) for output 1

VF_SRFET1			0.060	V	SRFET on-time drain voltage for output 1
VBREAKDOWN_SRFET1			60	V	SRFET breakdown voltage for output 1
RDSON_SRFET1			43.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
OUTPUT 2					
VOUT2	12.00		12.00	V	Output 2 voltage
IOUT2	0.420		0.420	A	Output 2 current
POUT2			5.04	W	Output 2 power
IRMS_SECONDARY2			0.667	A	Root mean squared value of the secondary current for output 2
IRIPPLE_CAP_OUTPUT2			0.518	A	Current ripple on the secondary waveform for output 2
NSECONDARY2			12		Number of turns for output 2
VREVERSE_RECTIFIER2			87.94	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 2
SRFET2	Auto		AON7254		Secondary rectifier (Logic MOSFET) for output 2
VF_SRFET2			0.028	V	SRFET on-time drain voltage for output 2
VBREAKDOWN_SRFET2			150	V	SRFET breakdown voltage for output 2
RDSON_SRFET2			66.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 2
PO_TOTAL		Info	12	W	The total power of all outputs does not add up to the total power of the design
NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

8 Performance Data

8.1 *Average Efficiency*

Requirement	
Average	**74% (DOE6) 80% (CoC II)**
10%	**71%**

8.1.1 115 VAC Input

% Load	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (A_{DC})	$12V_{OUT}$ (V_{DC})	$12I_{OUT}$ (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100%	114.93	231.04	14.18	5.15	1.4	12.30	0.42	12.36	87.16	
75%	114.94	181.07	10.66	5.16	1.05	12.32	0.31	9.28	87.12	
50%	114.95	126.47	7.13	5.20	0.70	12.38	0.21	6.22	87.2	
25%	114.96	69.47	3.57	5.20	0.35	12.39	0.10	3.10	86.78	**87.06**
10%	114.96	32.33	1.47	5.20	0.14	12.36	0.41	1.22	**83.14**	

8.1.2 230 VAC Input

% Load	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	$5V_{OUT}$ (V_{DC})	$5I_{OUT}$ (A_{DC})	$12V_{OUT}$ (V_{DC})	$12I_{OUT}$ (A_{DC})	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100%	229.89	143.98	14.41	5.15	1.4	12.32	0.42	12.36	85.82	
75%	229.89	111.7	10.85	5.19	1.05	12.42	0.31	9.35	86.15	
50%	229.9	78.91	7.27	5.20	0.70	12.42	0.21	6.23	85.75	
25%	229.9	44.03	3.71	5.21	0.35	12.42	0.10	3.11	83.73	**85.36**
10%	229.9	21.08	1.59	5.20	0.14	12.37	0.41	1.22	**77.17**	

8.2 *Full Load Efficiency vs. Line*

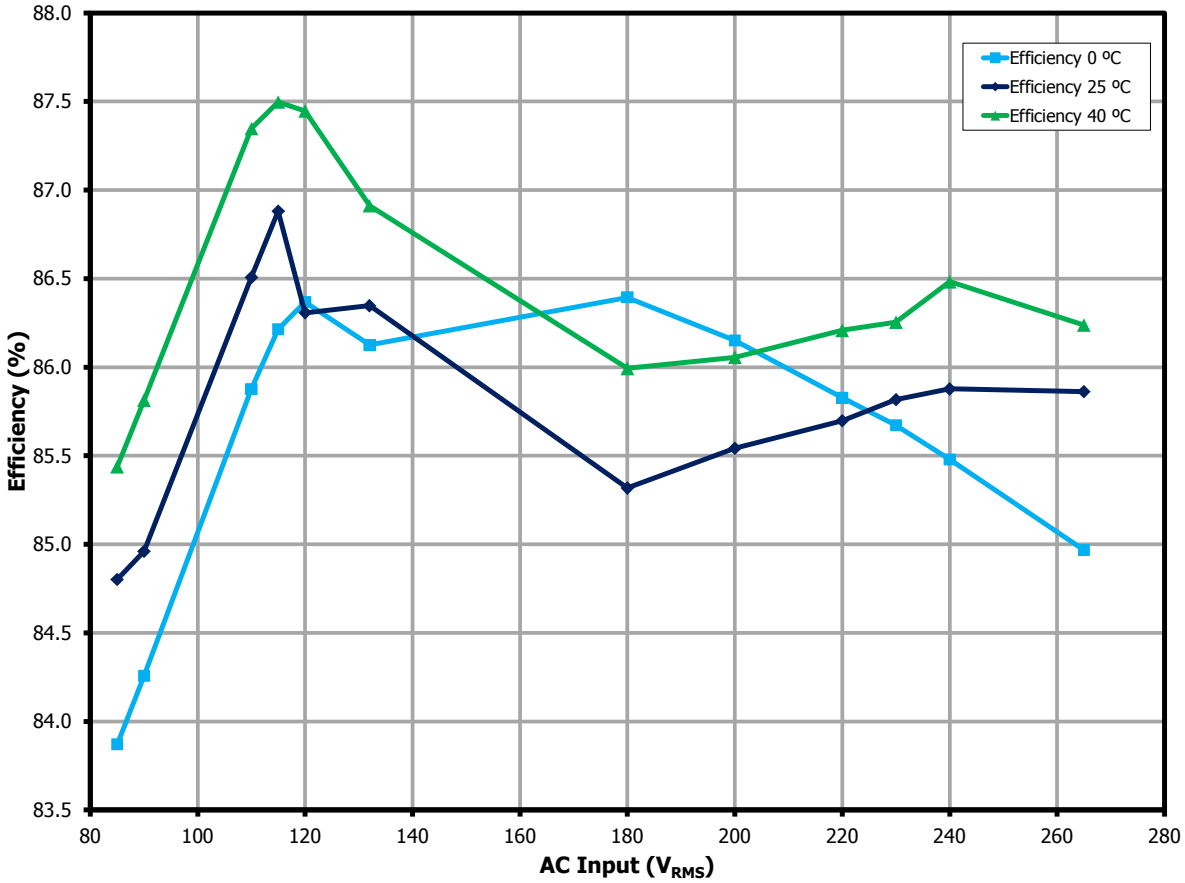


Figure 8 – Full load Efficiency vs. Line Voltage.

8.3 *Efficiency vs. Load*

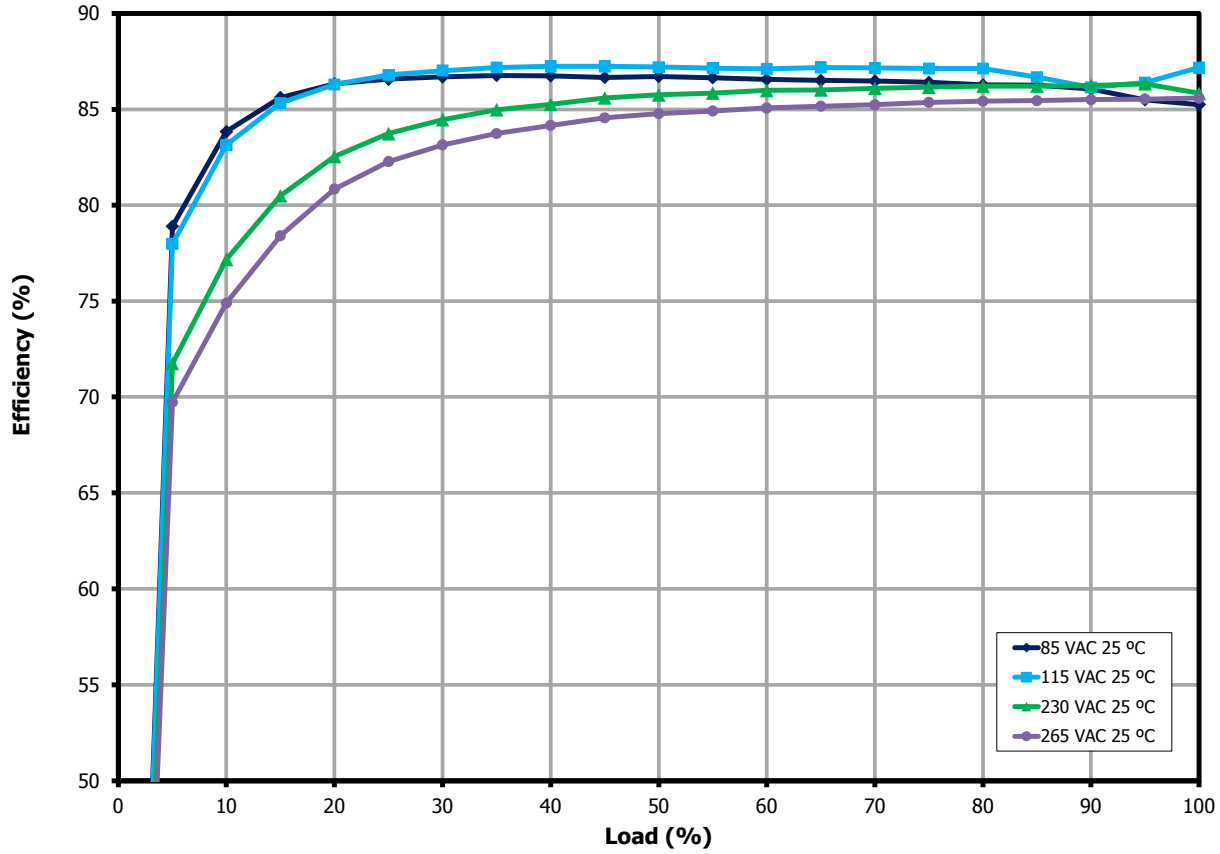


Figure 9 – Efficiency vs. Load, Room Ambient – 25 ºC Temperature.

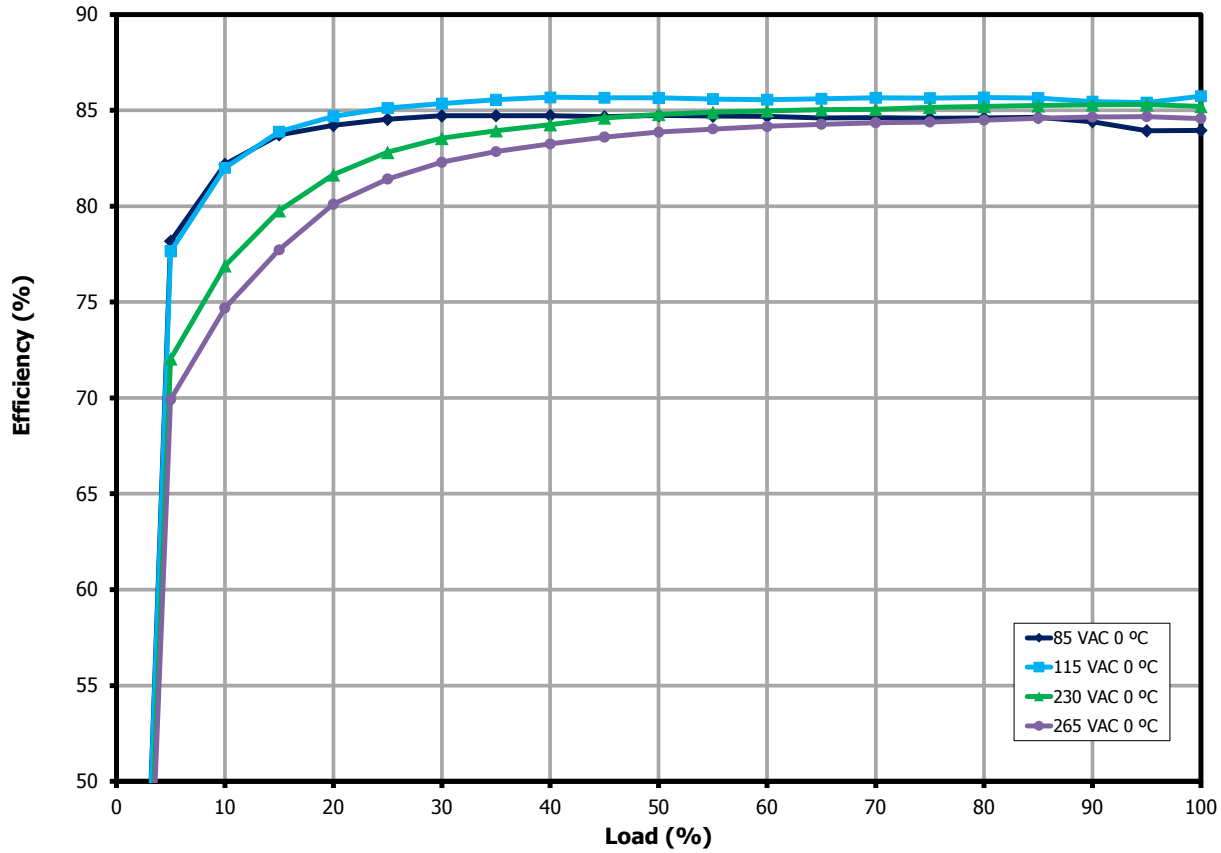


Figure 10 – Efficiency vs. Load, Cold Ambient – 0 ºC Temperature.

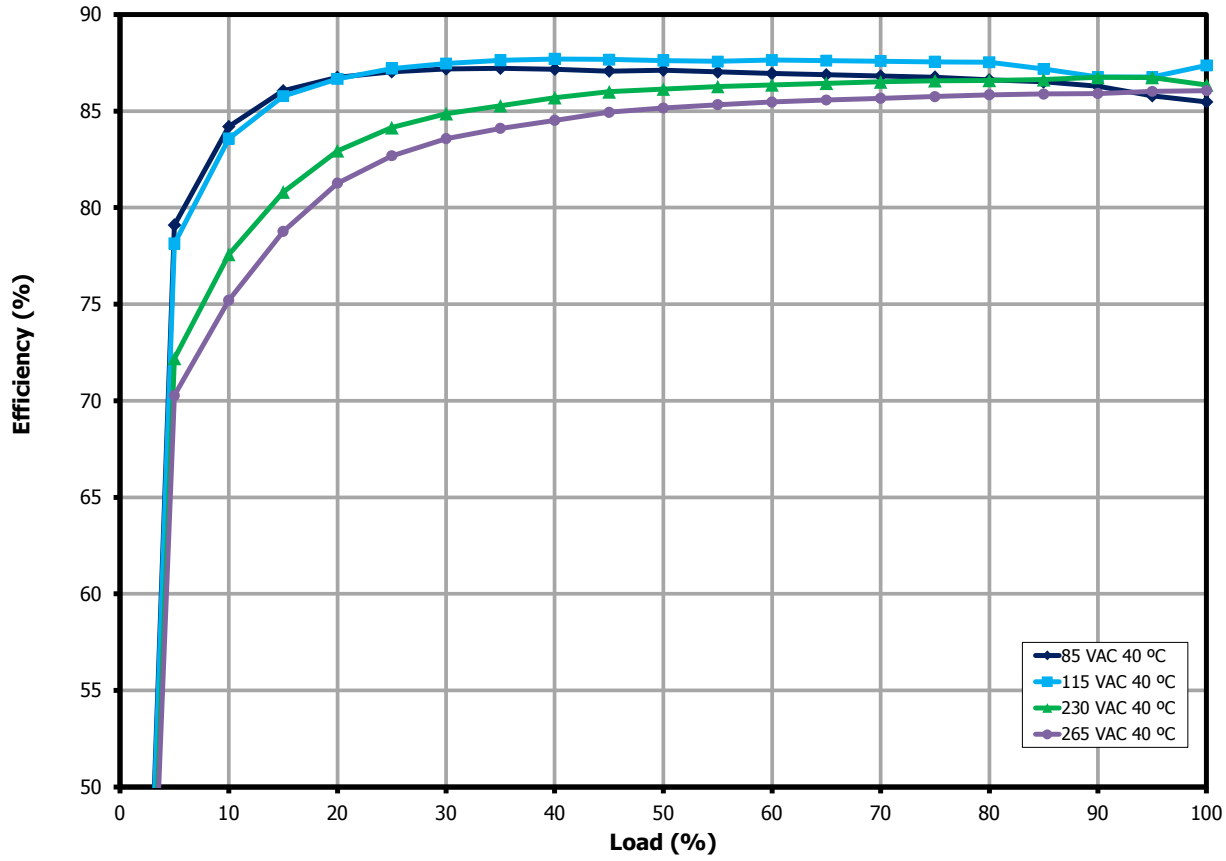


Figure 11 – Efficiency vs. Load, Hot Ambient - 40°C Temperature.

8.4 *No-Load Input Power*

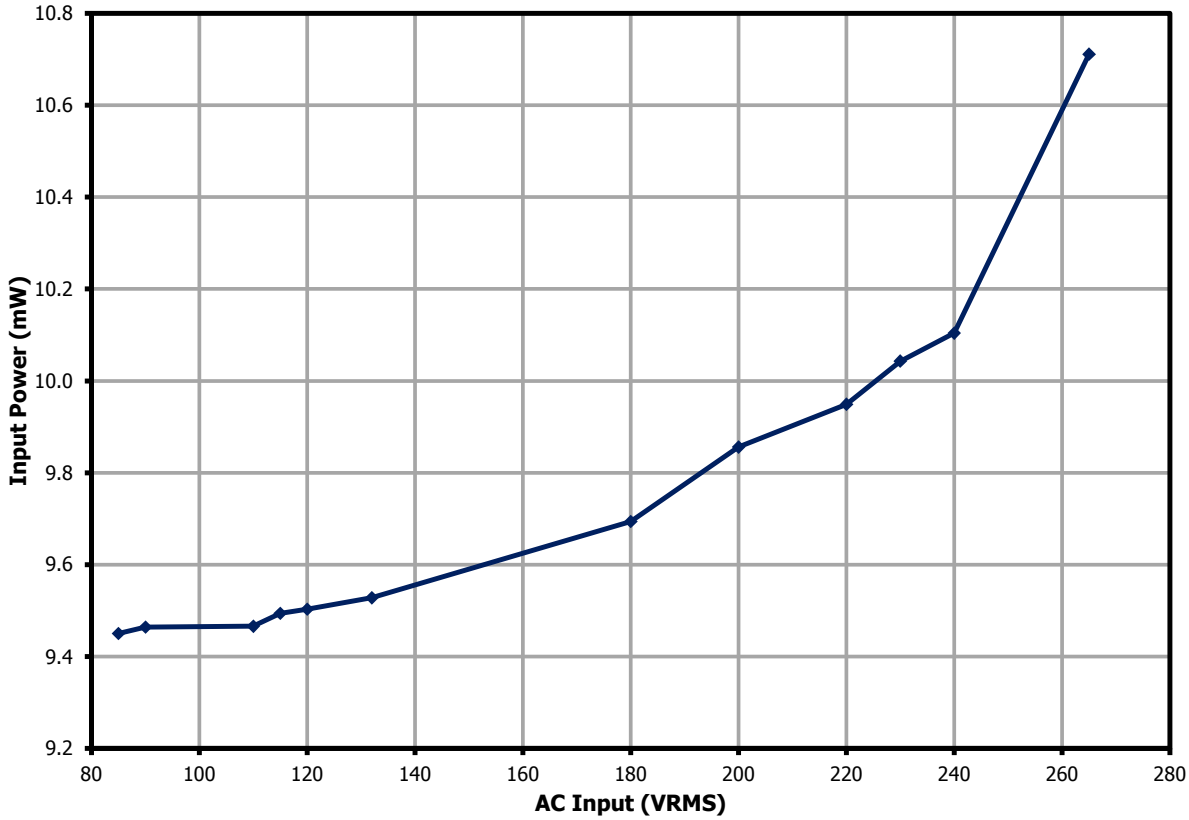


Figure 12 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

8.5 *Standby Power Power (5 V / 30 mA Load, 12 V No-Load)*

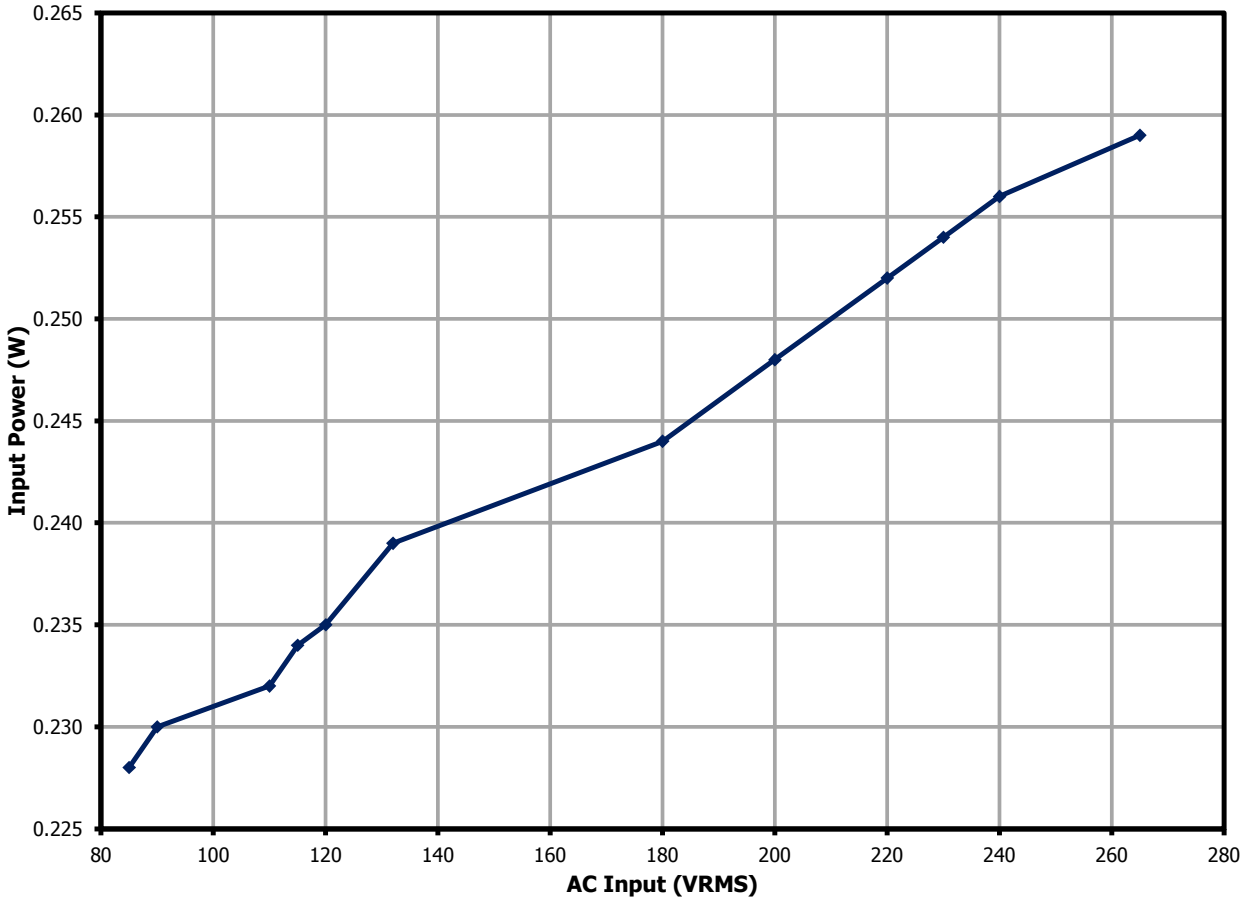


Figure 13 – Standby Power (5 V / 30 mA Load, 12 V No-Load).

8.6 *Line and Load Regulation*

8.6.1 Line Regulation (Full load)

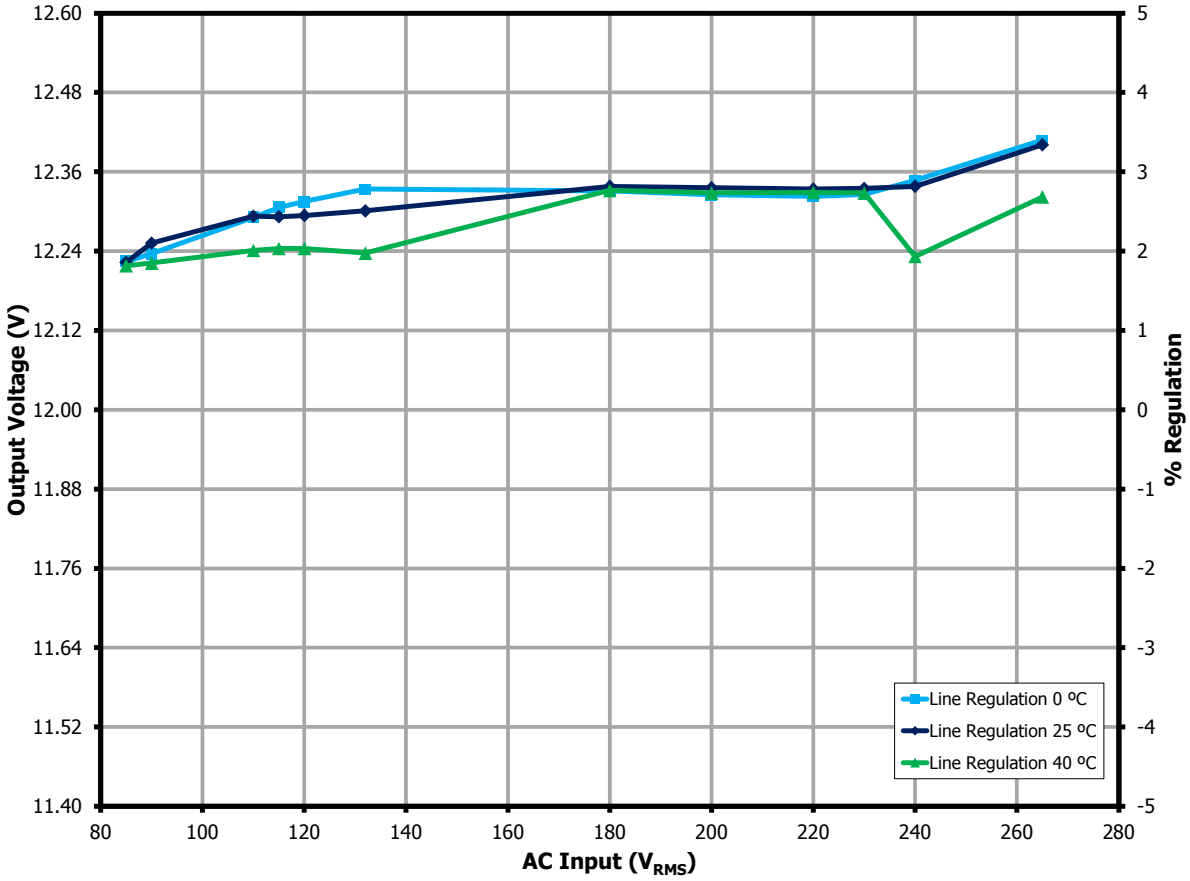


Figure 14 – 12 V Output Voltage vs. Input Line Voltage.

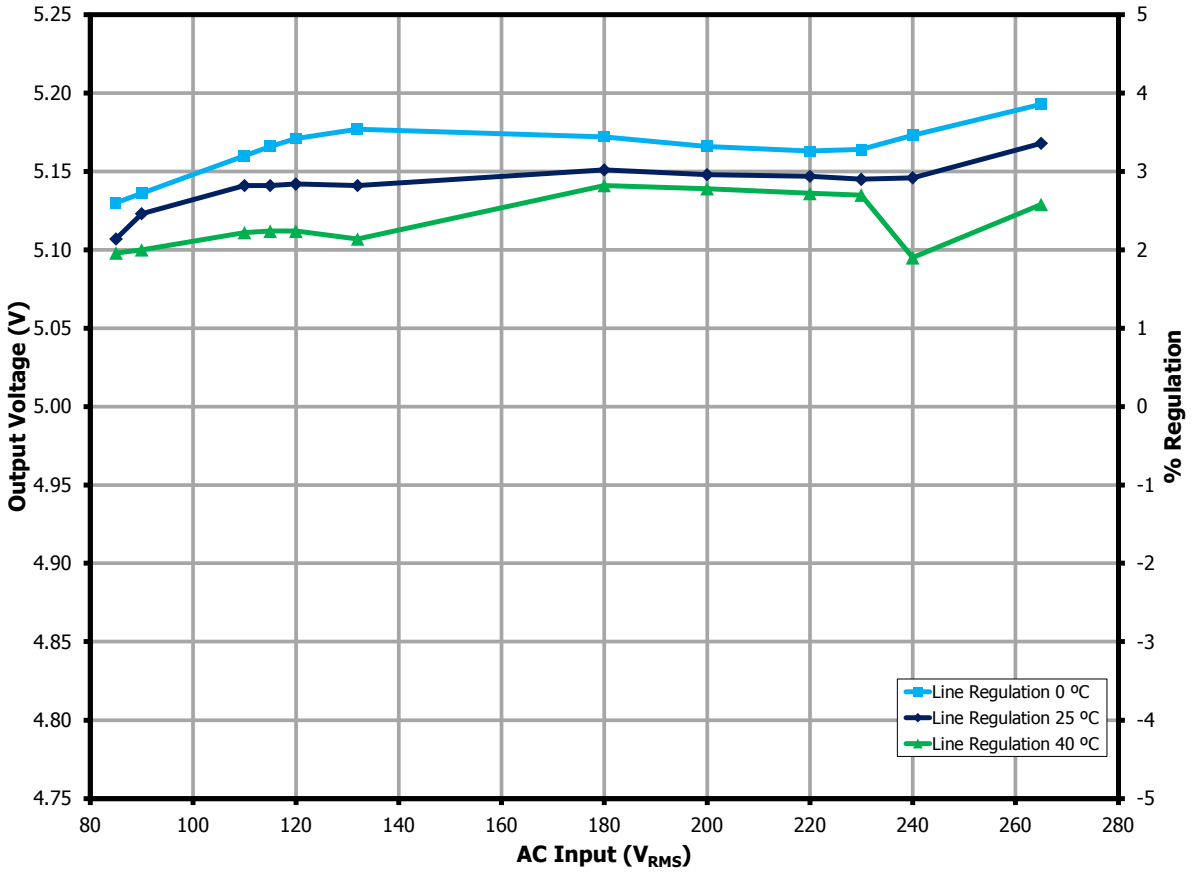


Figure 15 – 5 V Output Voltage vs. Input Line Voltage.

	5 V	12 V
Min.	5.19 V	12.41 V
Max.	5.09 V	12.23 V

8.6.2 5 V Load Regulation

Note: Both 5 V & 12 V outputs are loaded with the same percentage.

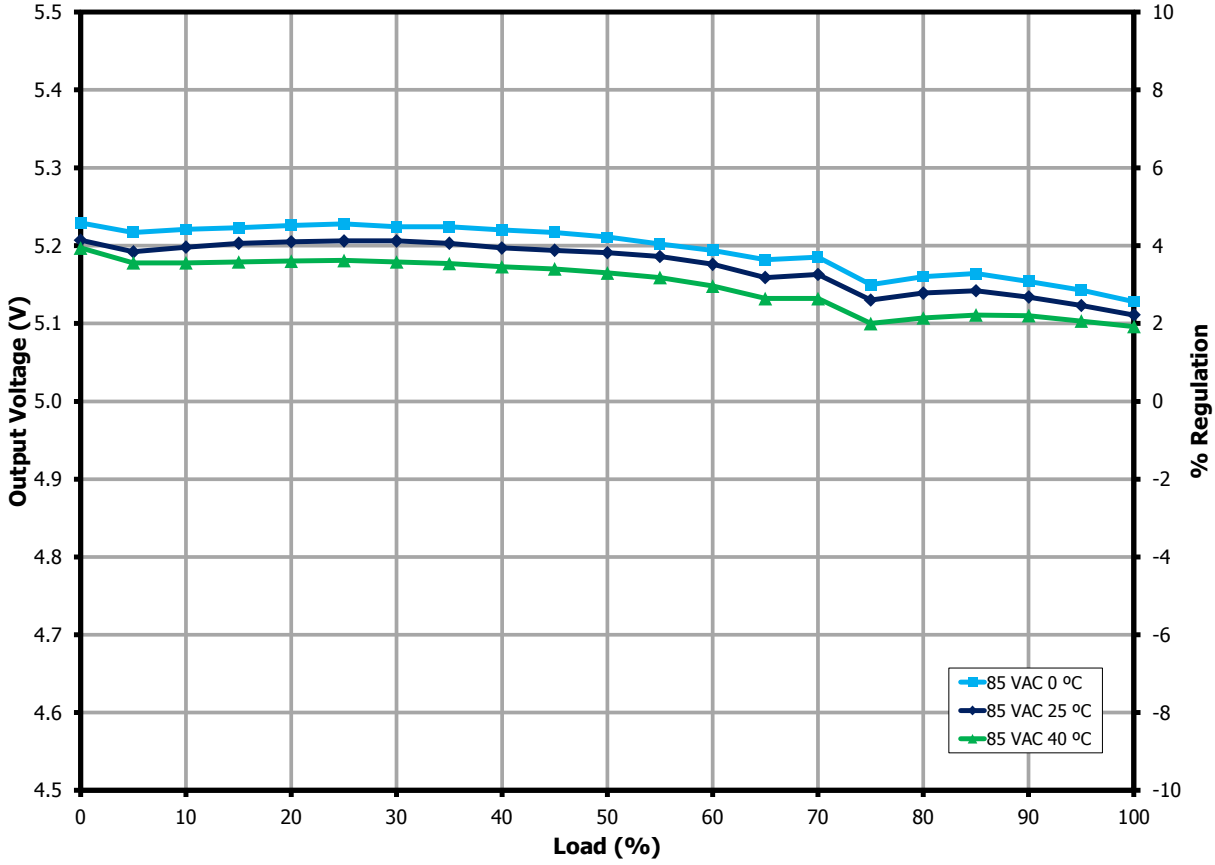


Figure 16 – 5 V Output Voltage vs. Load at 85 VAC.

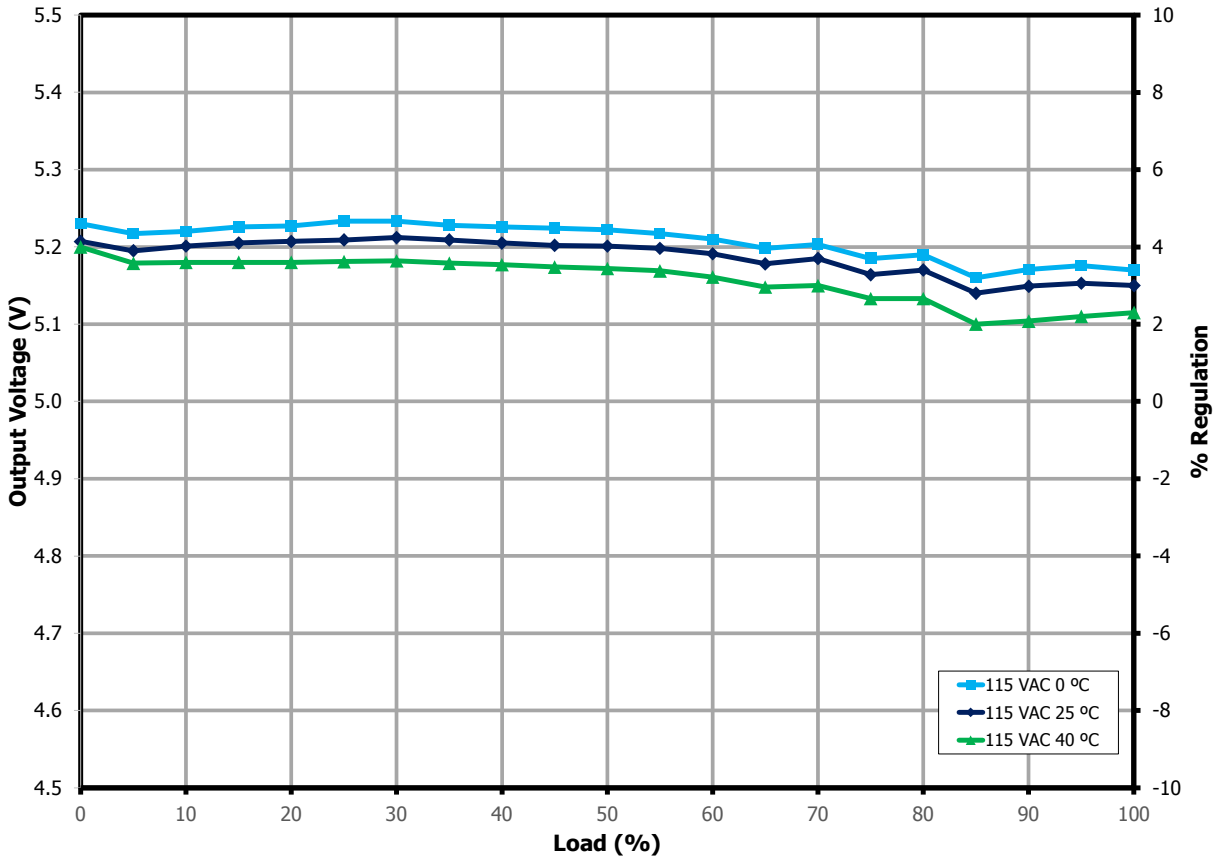


Figure 17 – 5 V Output Voltage vs. Load at 115 VAC.

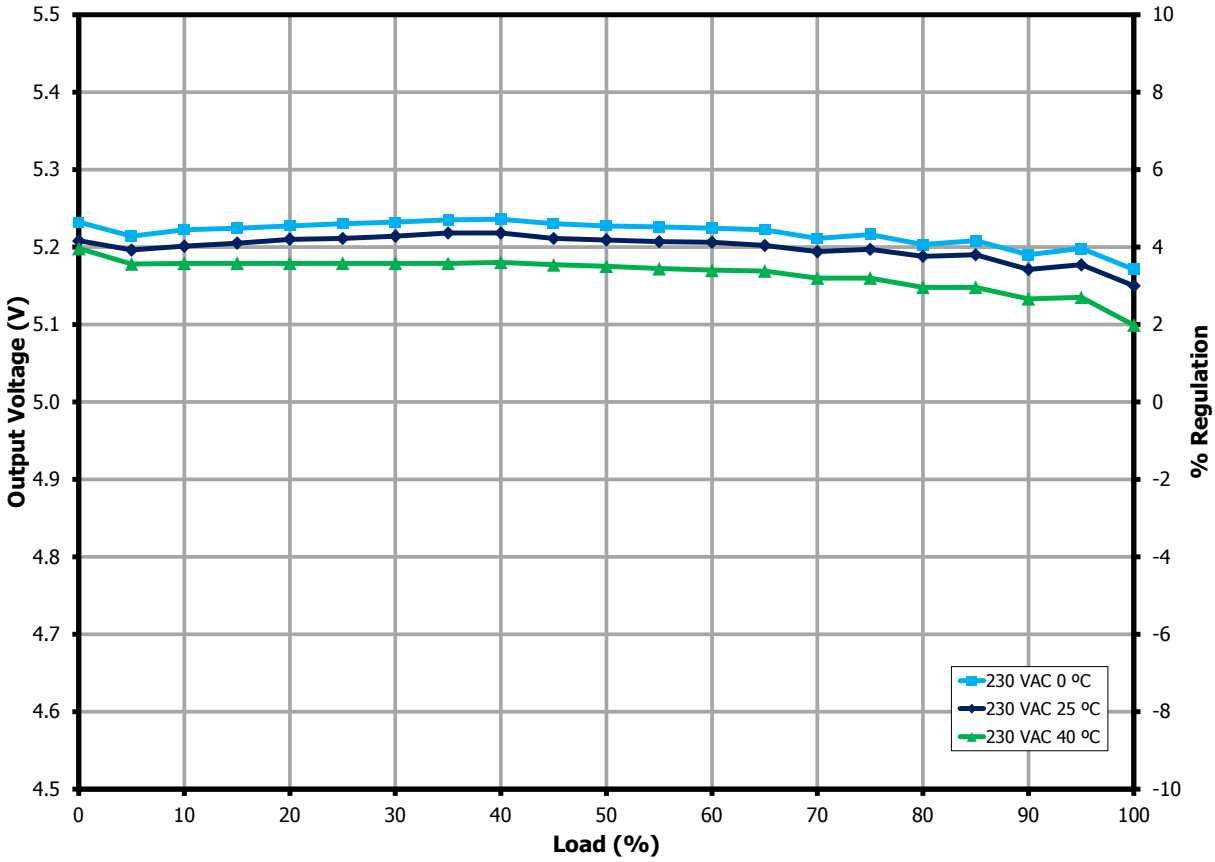


Figure 18 – 5 V Output Voltage vs. Load at 230 VAC.

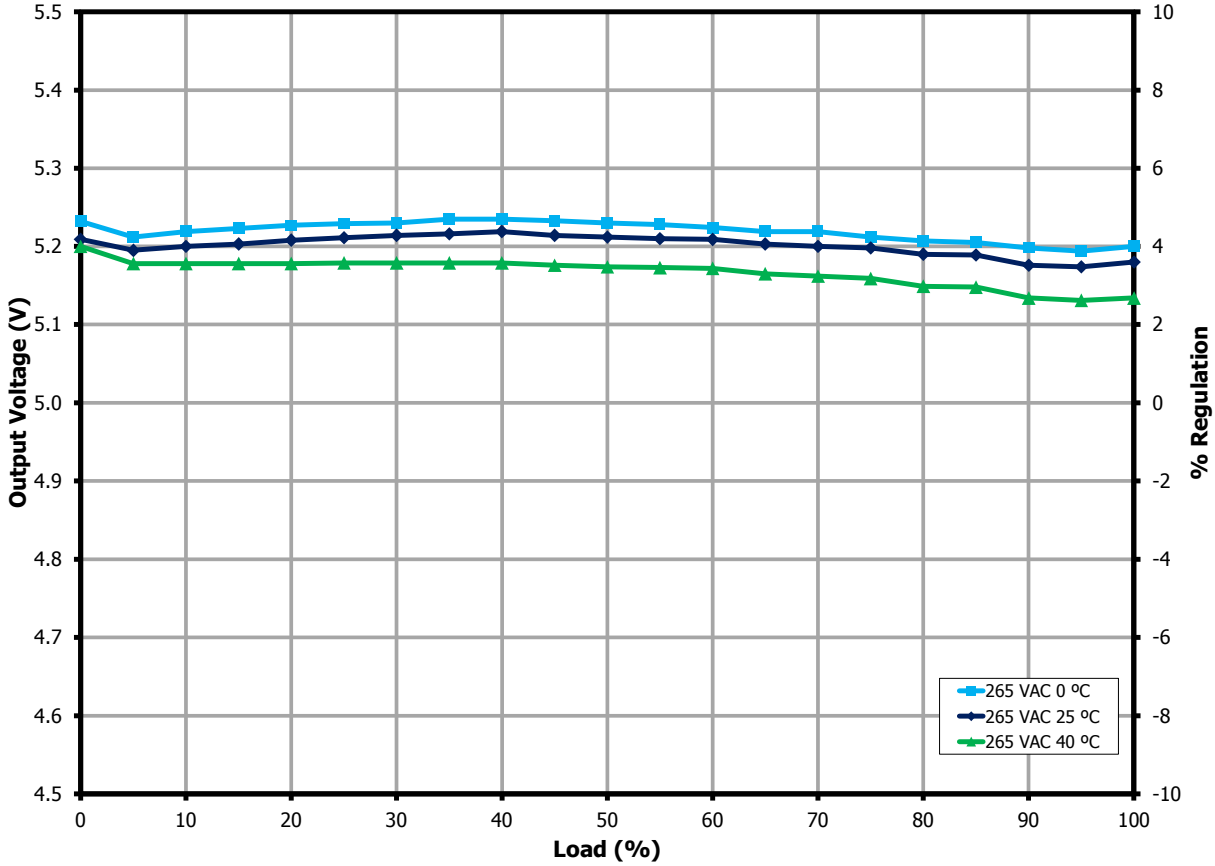


Figure 19 – 5 V Output Voltage vs. Load at 265 VAC.

8.6.3 12 V Load Regulation

Note: Both 5 V and 12 V outputs are loaded with the same percentage.

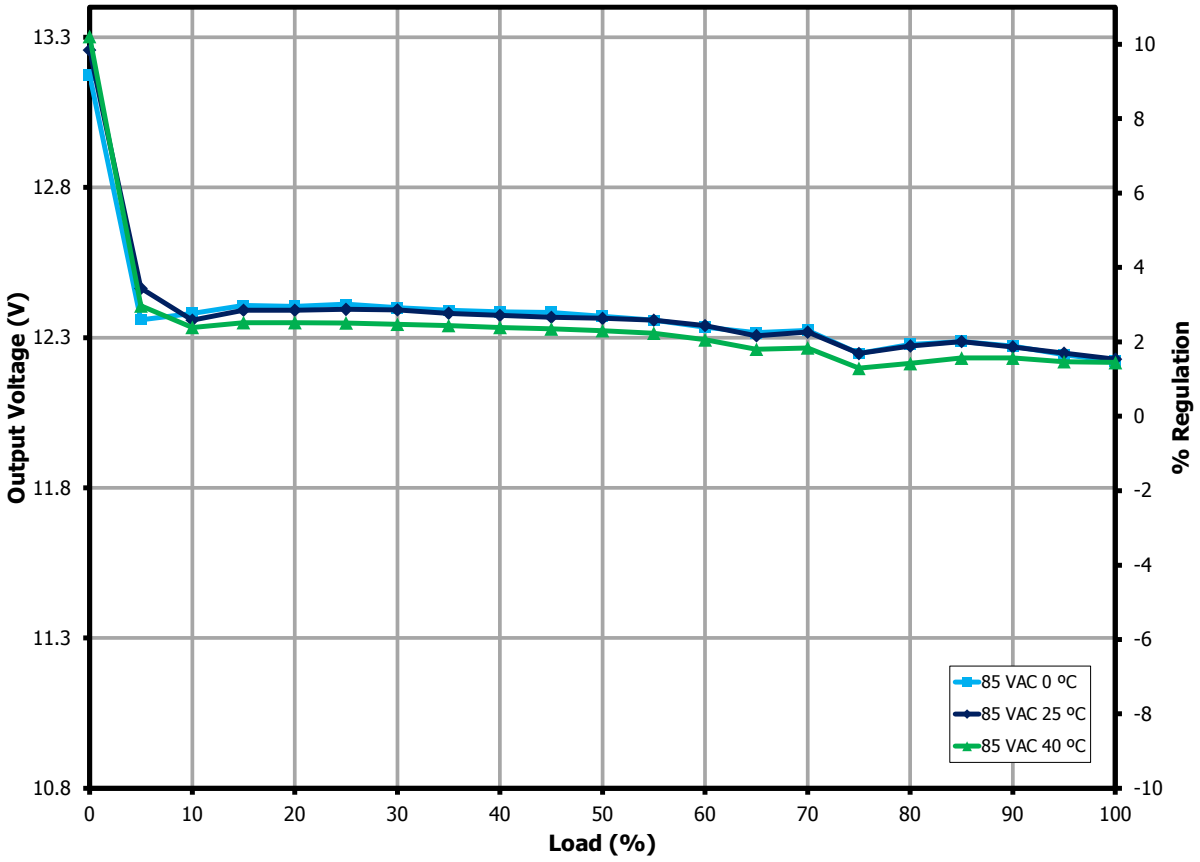


Figure 20 – 12 V Output Voltage vs. Load at 85 VAC.

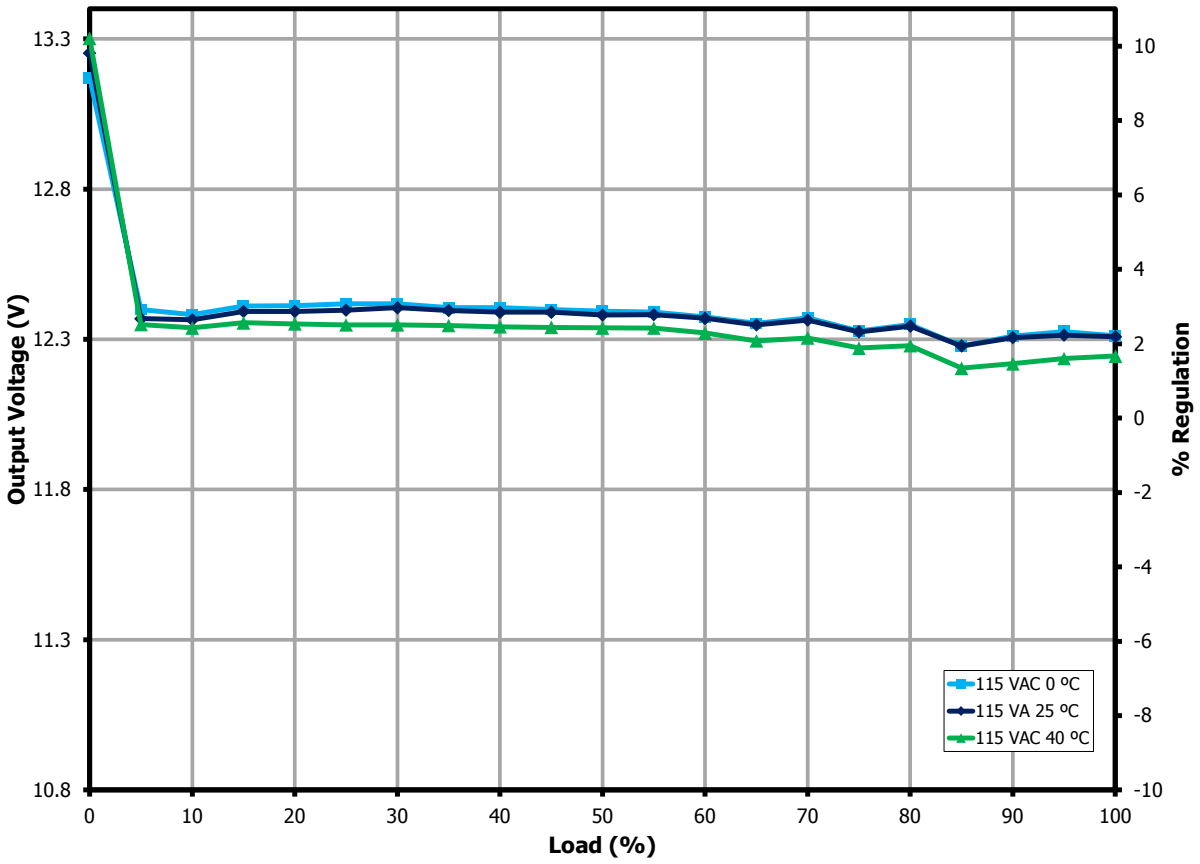


Figure 21 – 12 V Output Voltage vs. Load at 115 VAC.

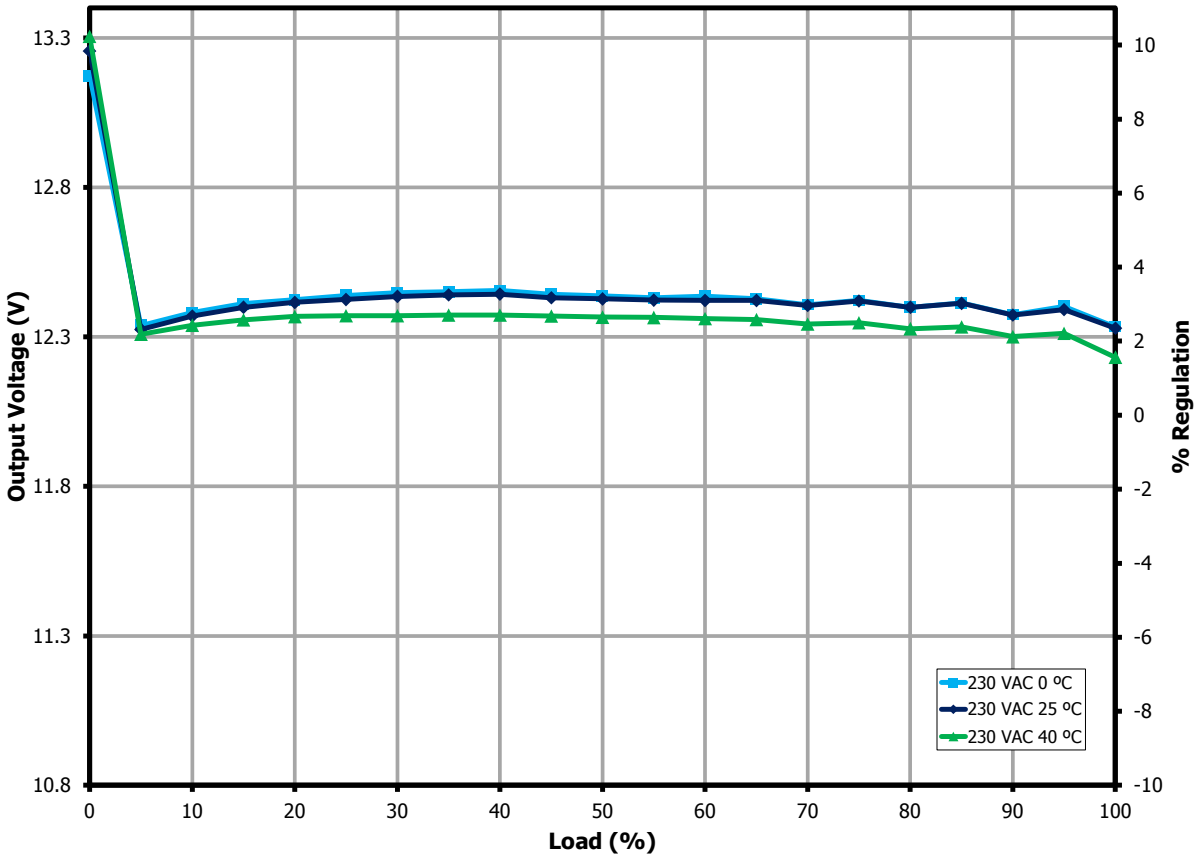


Figure 22 – 12 V Output Voltage vs. Load at 230 VAC.

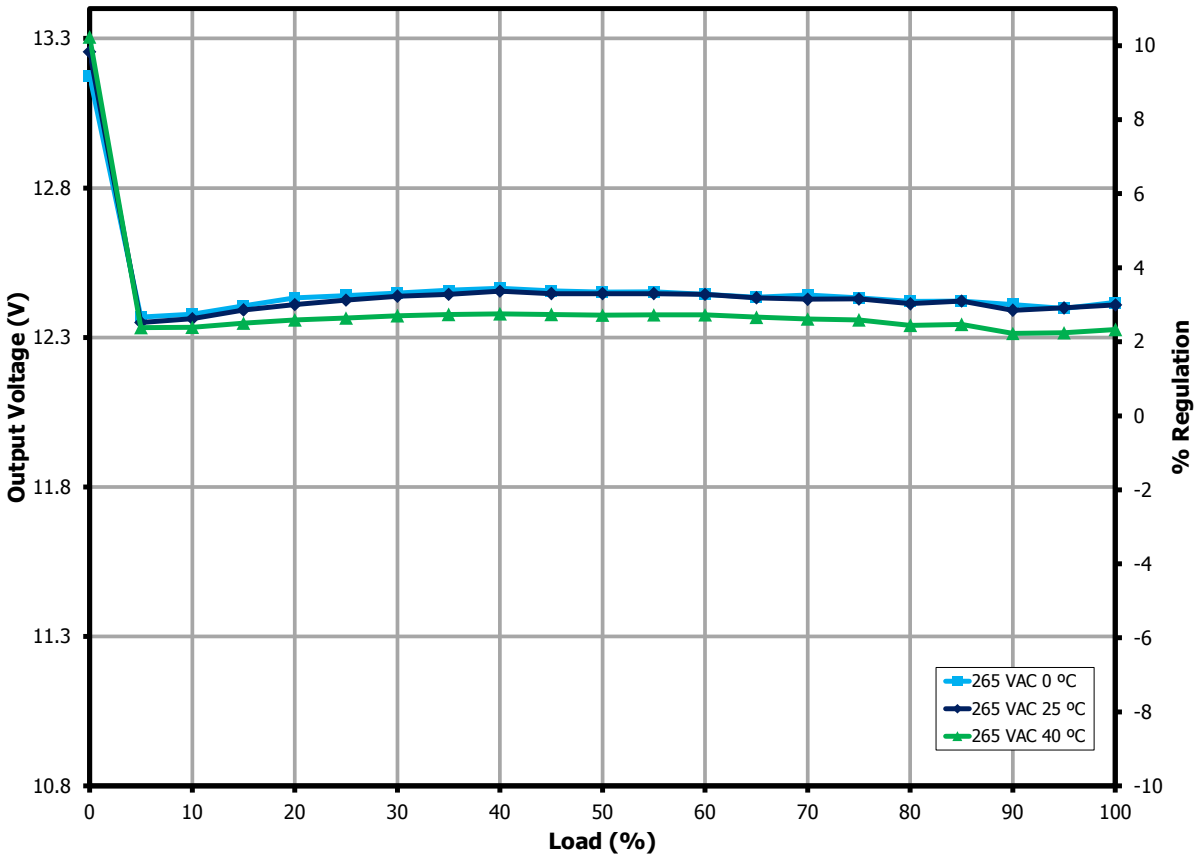


Figure 23 – 12 V Output Voltage vs. Load at 265 VAC.

8.7 *Cross Load Regulation*

8.7.1 12 V Load Change with Full Load on 5 V

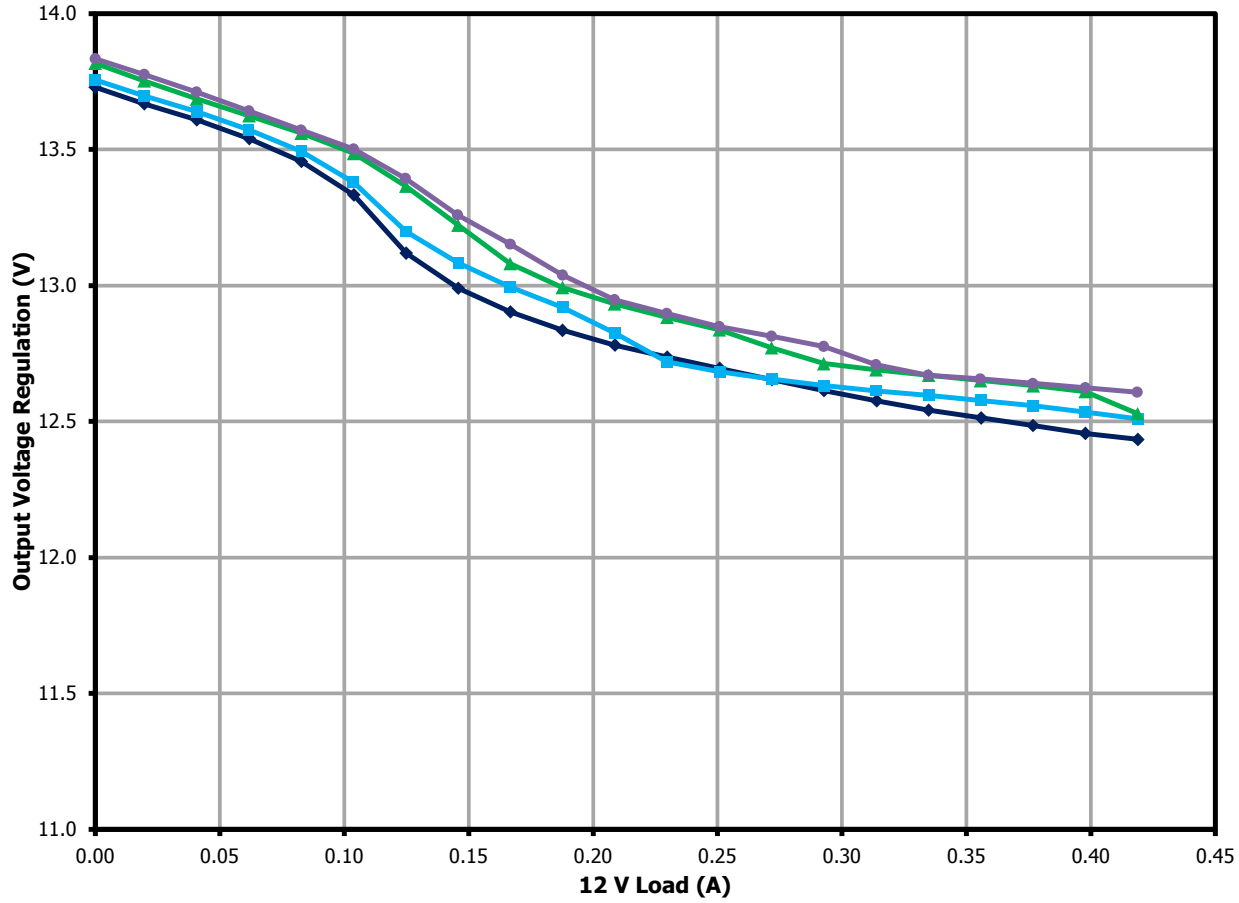


Figure 24 – 12 V Output Voltage vs. Output Load, Room Temperature.

	5 V	12 V
Min	5.14 V	12.43 V
Max	5.25 V	13.83 V

8.7.2 12 V Load Change with No-Load on 5 V

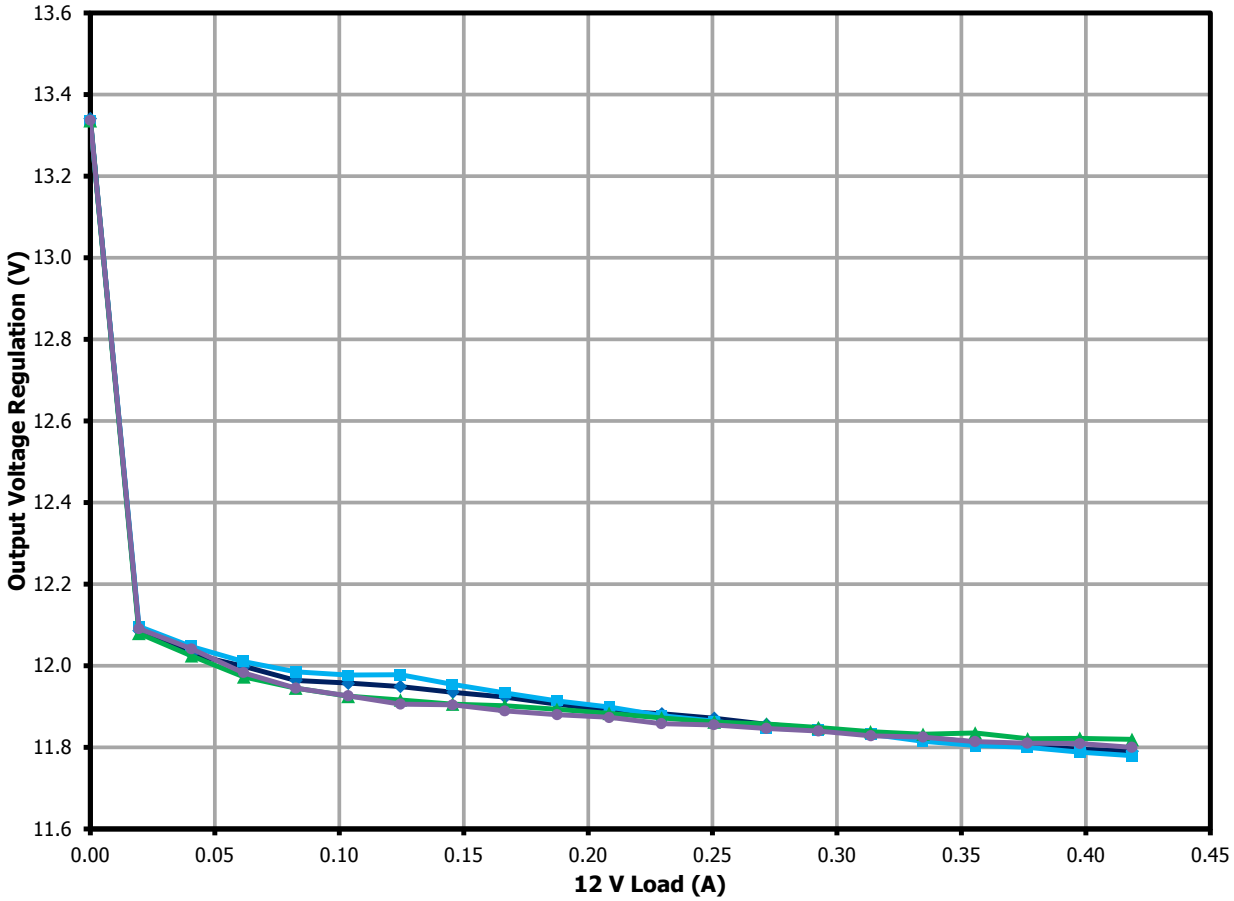


Figure 25 – 12 V Output Voltage vs. Output Load, Room Temperature.

	5 V	12 V
Min	5.26 V	11.77 V
Max	5.30 V	13.33 V

8.7.3 5 V Load Change with Full Load on 12 V

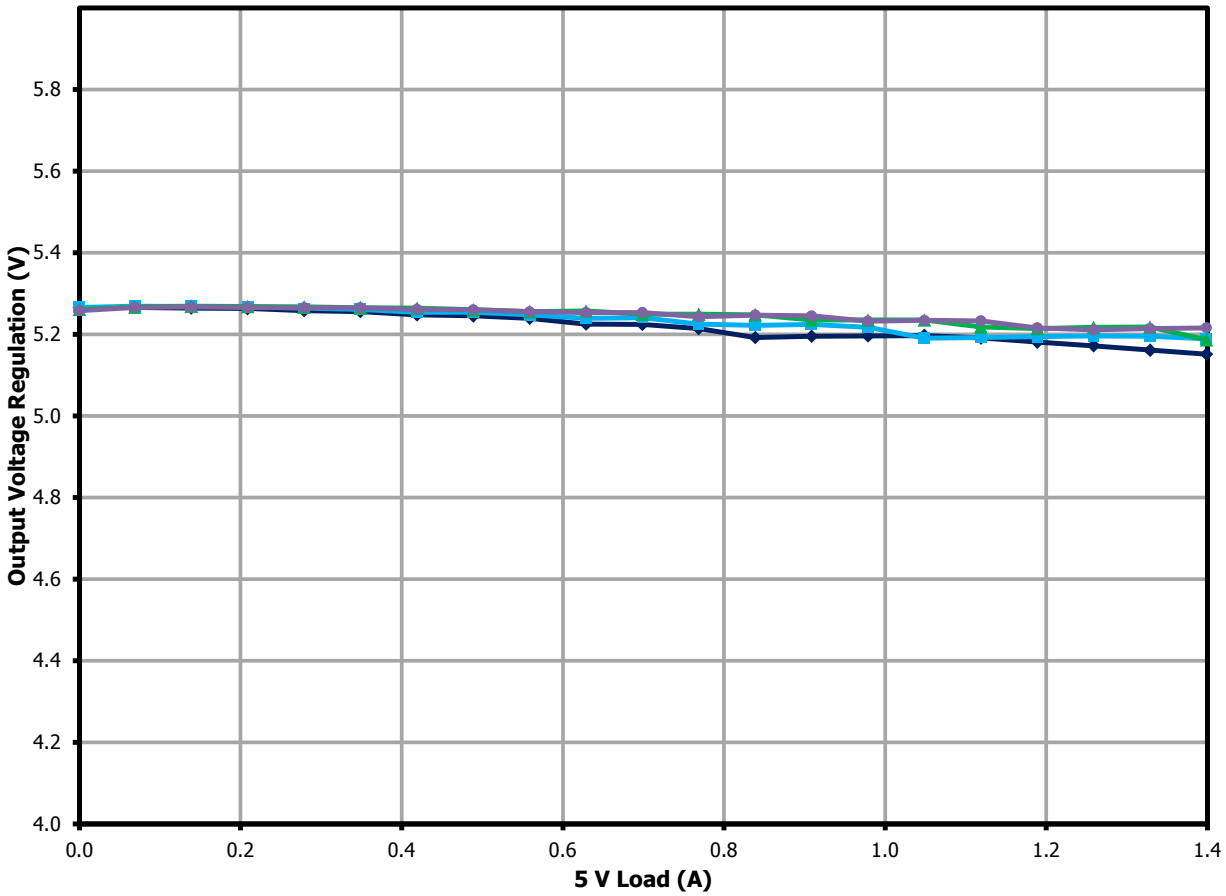


Figure 26 – 5 V Output Voltage vs. Output Load, Room Temperature.

	5 V	12 V
Min	5.15 V	11.77 V
Max	5.21 V	12.60 V

8.7.4 5 V Load Change with No-Load on 12 V

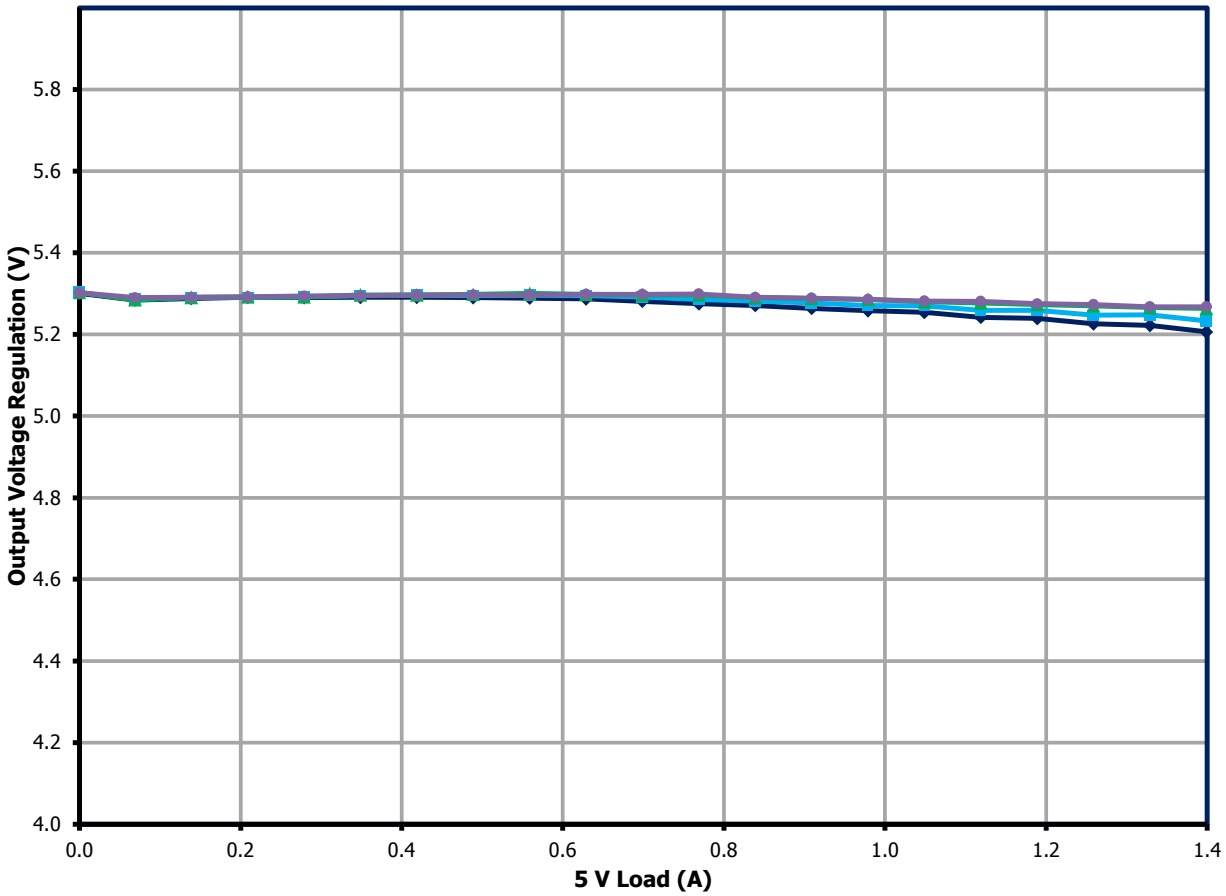


Figure 27 – 5 V Output Voltage vs. Output Load, Room Temperature**.**

	5 V	12 V
Min	4.95 V	11.86 V
Max	5.00 V	13.36 V

9 Thermal Performance

9.1 *85 VAC*

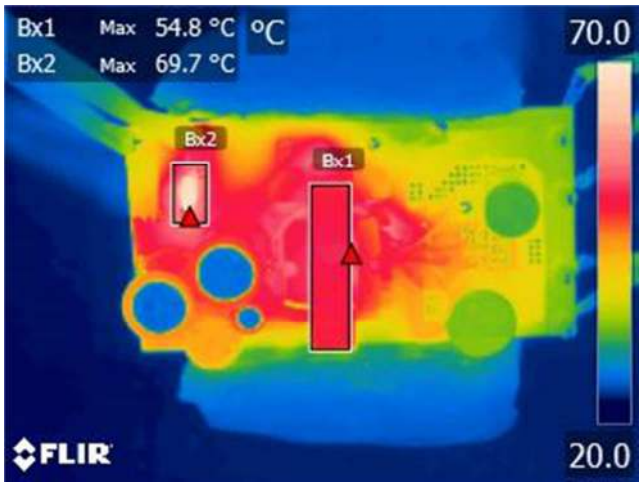


Figure 28 – Transformer Side. 85 VAC, Full Load.

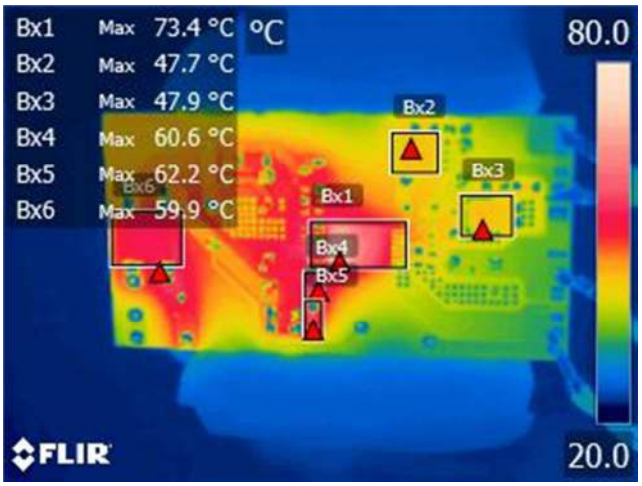


Figure 29 – InnoSwitch3-TN Side. 85 VAC, Full Load.

	Reference	ºC
Ambient		24.9
Transformer	T1	62.6
Thermistor	RT1	59.4

	Reference	ºC
Ambient		24.9
InnoSwitch3-TN	U1	73.4
SR FET Q1	Q1	47.7
Schottky D4	D4	47.9
Clamp Resistor	R2	60.6
Snubber Diode	D1	62.2
Bridge Diode	BR1	59.6

9.2 *265 VAC*

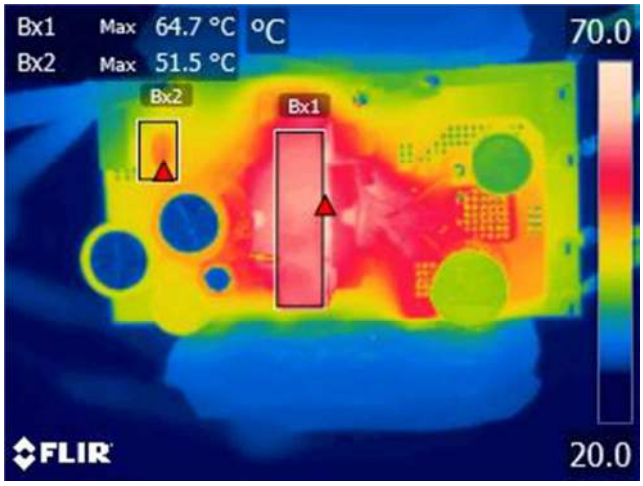


Figure 30 – Transformer Side. 265 VAC, Full Load.

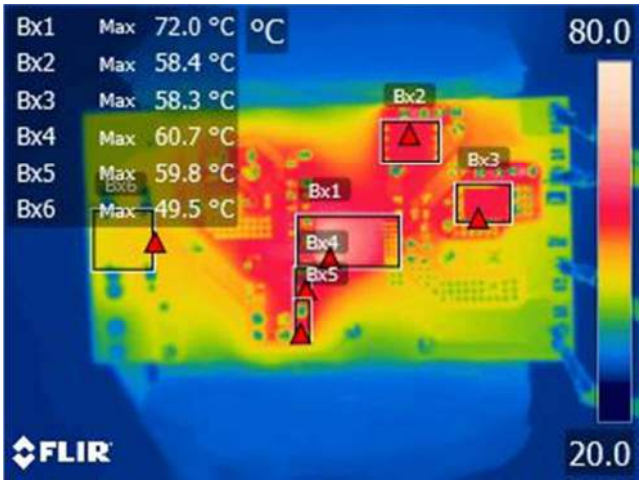


Figure 31 – InnoSwitch3-TN Side. 265 VAC, Full Load.

	Reference	°C
Ambient		27.7
Transformer	T1	64.7
Thermistor	RT1	51.5

	Reference	°C
Ambient		27.7
InnoSwitch3-TN	U1	72.0
SR FET Q1	Q1	58.4
Schottky D4	D4	58.3
Clamp Resistor	R2	60.7
Snubber Diode	D1	59.8
Bridge Diode	BR1	49.5

10 Waveforms

10.1 *Load Transient Response*

10.1.1 12 V Load Transient – No-Load at 5 V Output

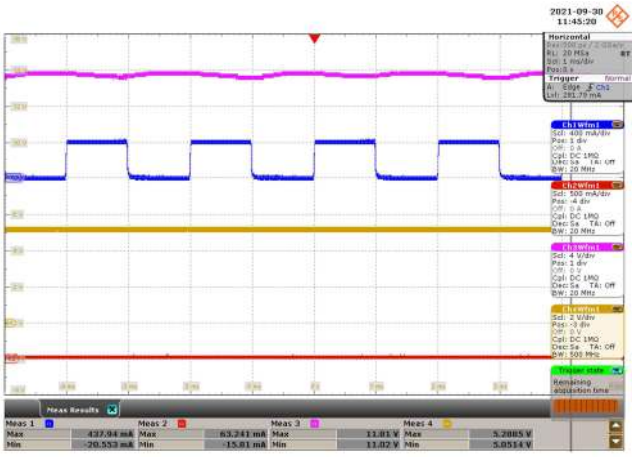


Figure 32 – 0 A – 0.42 A, 12 V Load Step Transient Response, 85 VAC.
5 V_{MIN}: 5.05 V.; 5 V_{MAX}: 5.28 V.
12 V_{MIN}: 11.02 V. 12 V_{MAX}: 11.81 V.
Upper: 12 V_{OUT}, 4 V / div.
Upper Middle: 12 V I_{OUT}. 400 mA / div.
Upper Middle: 5 V_{OUT}, 2 V / div.
Lower: 5 V I_{OUT}, 500 mA / div., 1 ms / div.

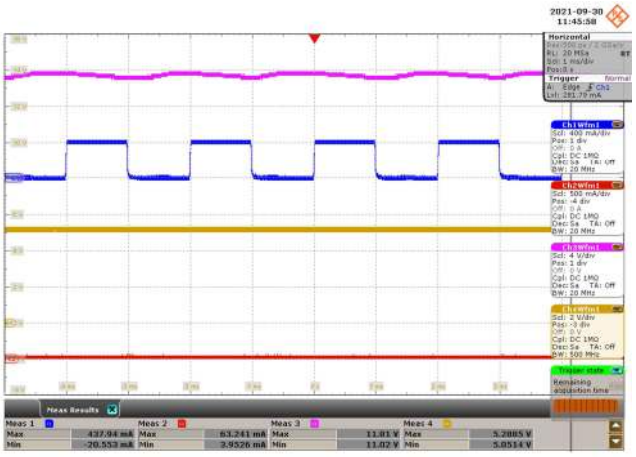


Figure 33 – 0 A – 0.42 A, 12 V Load Step Transient Response. 265 VAC.
5 V_{MIN}: 5.05 V. 5 V_{MAX}: 5.28 V.
12 V_{MIN}: 11.02 V. 12 V_{MAX}: 11.81 V.
Upper: 12 V V_{OUT}, 4 V / div.
Upper Middle: 12 V I_{OUT}. 400 mA / div.
Upper Middle: 5 V_{OUT}, 2 V / div.
Lower: 5 V I_{OUT}, 500 mA / div., 1 ms / div.

10.1.2 5 V Load Transient – No-Load at 12 V Output

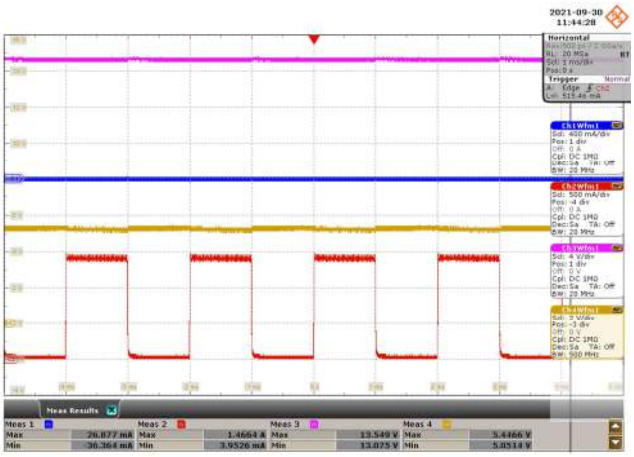


Figure 34 – 0 A – 1.4 A, 5 V Load Step Transient Response, 85 VAC.
5 V_{MIN}: 5.05 V. 5 V_{MAX}: 5.44 V.
12 V_{MIN}: 13.07 V. 12 V_{MAX}: 13.54 V.
Upper: 12 V_{OUT}, 4 V / div.
Upper Middle: 12 V I_{OUT}. 400 mA / div.
Upper Middle: 5 V_{OUT}, 2 V / div.
Lower: 5 V I_{OUT}, 500 mA / div., 1 ms / div.

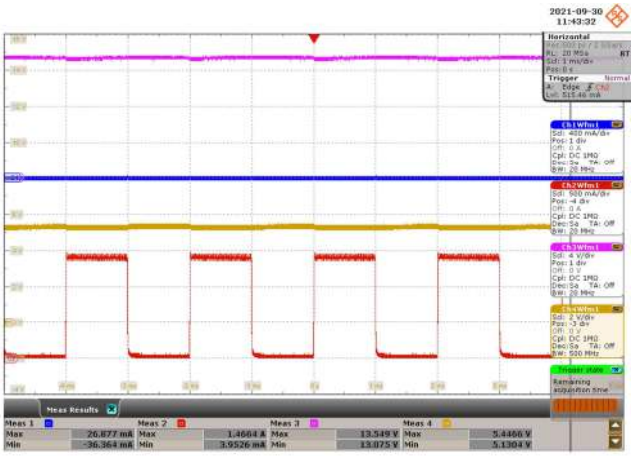


Figure 35 – 0 A – 1.4 A, 5 V Load Step Transient Response. 265 VAC.
5 V_{MIN}: 5.13 V. 5 V_{MAX}: 5.44 V.
12 V_{MIN}: 13.07 V. 12 V_{MAX}: 13.54 V.
Upper: 12 V V_{OUT}, 4 V / div.
Upper Middle: 12 V I_{OUT}. 400 mA / div.
Upper Middle: 5 V_{OUT}, 2 V / div.
Lower: 5 V I_{OUT}, 500 mA / div., 1 ms / div.

10.2 *Switching Waveforms*

10.2.1 InnoSwitch3-TN Waveforms

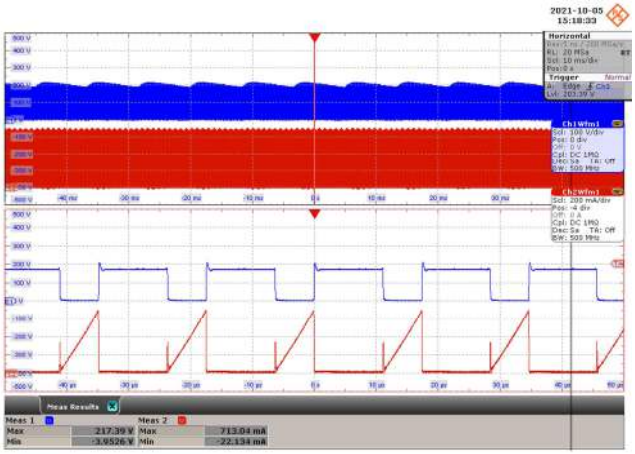


Figure 36 – Drain Voltage and Current Waveforms.
85 VAC Input, Full Load.
Upper: V_{DRAIN}, 100 V / div, 10 ms / div.
Lower: I_{DRAIN}, 200 mA / div, 10 ms / div.
Zoom: 20 µs / div.

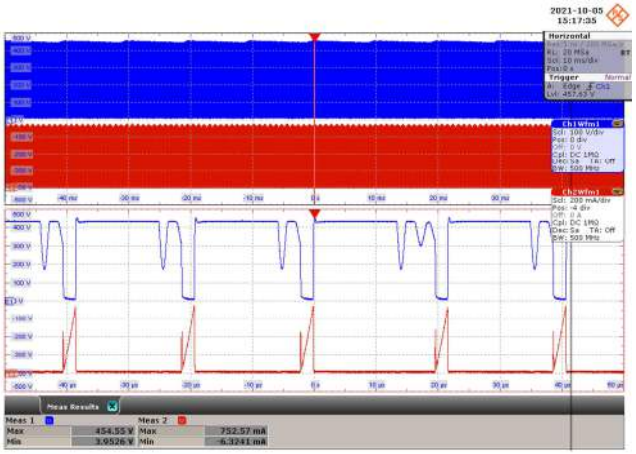


Figure 37 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (454 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div, 10 ms / div.
Lower: I_{DRAIN}, 200 mA / div, 10 ms / div.
Zoom: 20 µs / div.

10.2.2 InnoSwitch3-TN Drain Voltage and Current Waveforms During Start-up

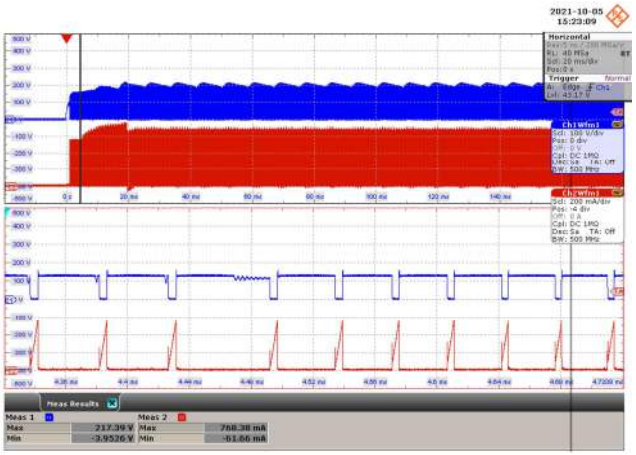


Figure 38 – Drain Voltage and Current Waveforms.
85 VAC Input, Full Load.
Upper: V_{DRAIN}, 100 V / div, 20 ms / div.
Lower: I_{DRAIN}, 200 mA / div, 20 ms / div.
Zoom: 40 µs / div.

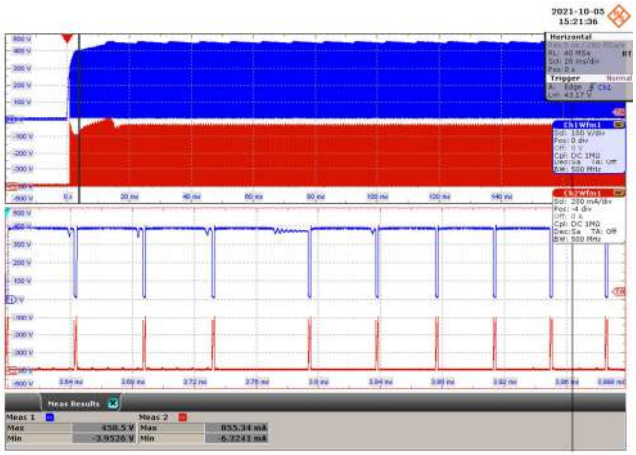


Figure 39 – Drain Voltage and Current Waveforms.
265 VAC Input, Full Load, (458 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div, 20 ms / div.
Lower: I_{DRAIN}, 200 mA / div, 20 ms / div.
Zoom: 40 µs / div.

10.2.3 SR FET Waveforms

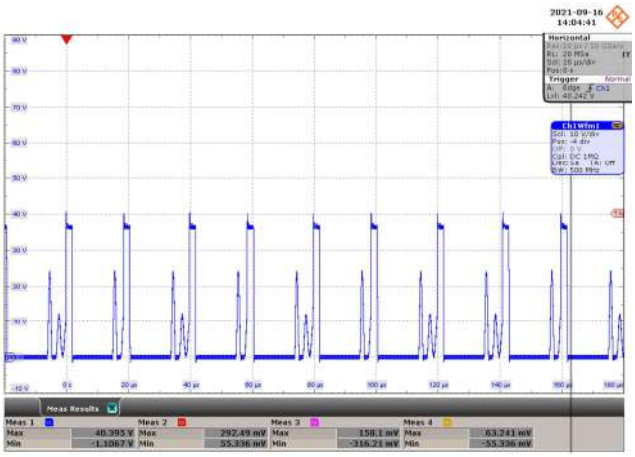


Figure 40 – 5 V SR FET Voltage Waveforms.
265 VAC Input, Full Load.
5 V_{MAX} = 40.39 V.
5 V SRFET V_{MAX}: 10 V / div.
20 µs / div.

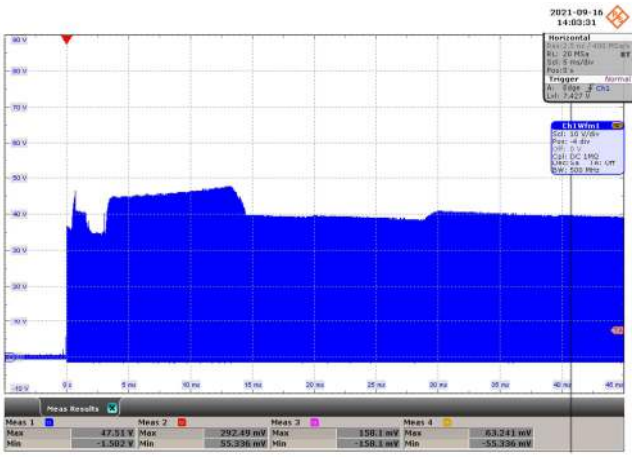


Figure 41 – 5 V FET Voltage Waveforms During Start-Up.
265 VAC Input, Full Load.
5 V_{MAX} = 47.51 V.
5 V SRFET V_{MAX}: 10 V / div.
5 ms / div.

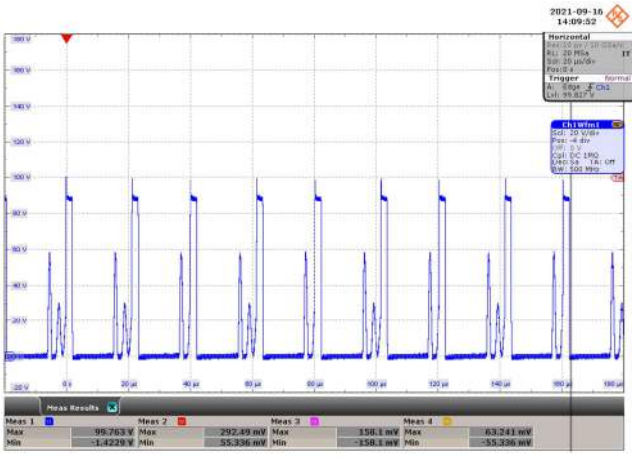


Figure 42 – 12 V Schottky Voltage Waveforms.
265 VAC Input, Full Load.
12 V_{MAX} = 99.76 V.
12 V Schottky V_{MAX}: 20 V / div.
20 µs / div.

Figure 43 – 5 V Schottky Voltage Waveforms During Start-Up.
265 VAC Input, Full Load.
12 V_{MAX} = 103.72 V.
12 V Schottky V_{MAX}: 20 V / div.
5 ms / div.

10.2.4 Output Voltage and Current Waveforms During Start-Up

10.2.4.1 Full load

Figure 44 – Output Voltage and Current Waveforms.
85 VAC Input.
Upper: 5 V_{OUT}, 1 V / div.
Upper Middle: 5 V I_{OUT}, 400 mA / div.
Lower Middle: 12 V V_{OUT}, 4 V / div.
Lower: 12 V I_{OUT}. 400 mA / div.
10 ms / div.

Figure 45 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 5 V_{OUT}, 1 V / div.
Upper Middle: 5 V I_{OUT}, 400 mA / div.
Lower Middle: 12 V V_{OUT}, 4 V / div.
Lower: 12 V I_{OUT}. 400 mA / div.
10 ms / div.

10.2.5 Output Voltage and Current Waveform with Shorted Output (5 V)

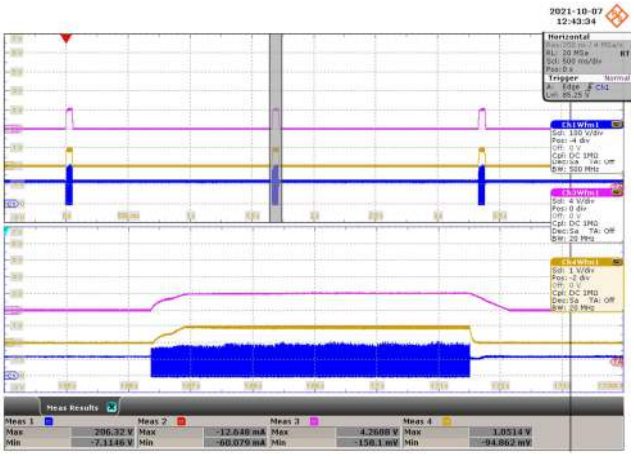


Figure 46 – Output Voltage and Current Waveforms.
85 VAC Input.
Upper: 12 V_{OUT}, 4 V / div.
Middle: 5 V_{OUT}, 1 V / div.
Lower: InnoSwitch3-TN V_{DS}. 100 V / div.
500 ms / div.
Zoom: 10 ms / div.

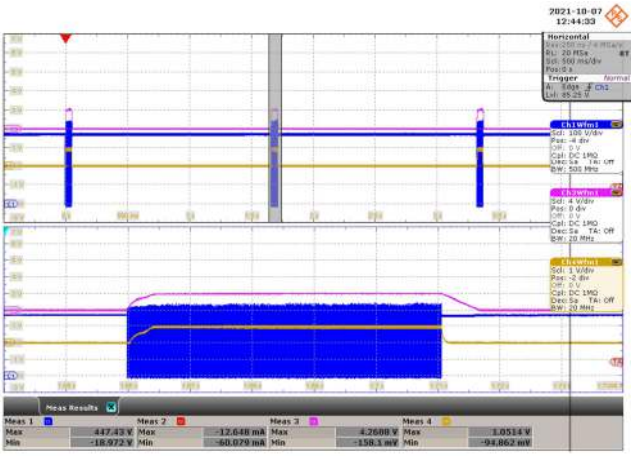


Figure 47 – Output Voltage and Current Waveforms.
265 VAC Input.
Upper: 12 V_{OUT}, 4 V / div.
Middle: 5 V_{OUT}, 1 V / div.
Lower: InnoSwitch3-TN V_{DS}. 100 V / div.
500 ms / div.
Zoom: 10 ms / div.

10.2.6 Overvoltage Protection

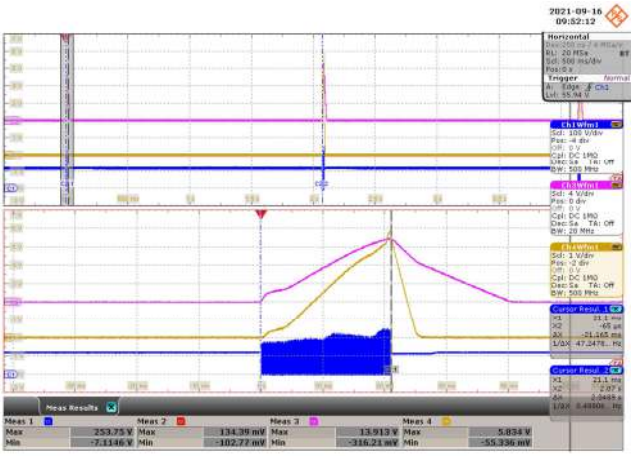


Figure 48 – Output Voltage Waveform. Full Load.
85 VAC Input.
Upper: 12 V_{OUT}, 4 V / div. 12 V_{MAX} = 13.91 V.
Middle: 5 V_{OUT}, 1 V / div. 5 V_{MAX} = 5.83 V.
Lower: InnoSwitch3-TN V_{DS}. 100 V / div.
500 ms / div.
Zoom: 10 ms / div.

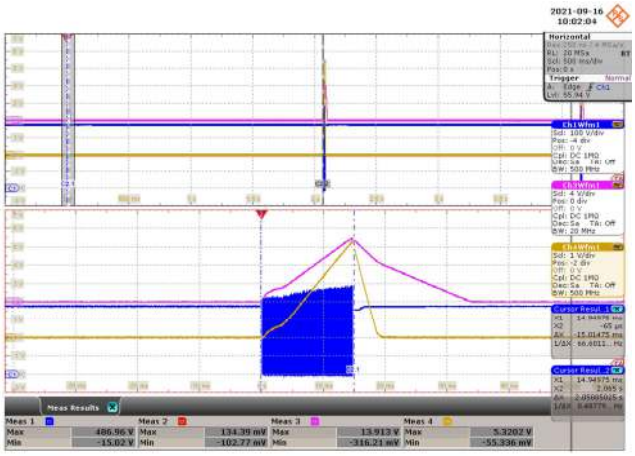


Figure 49 – Output Voltage Waveform. Full Load.
265 VAC Input.
Upper: 12 V V_{OUT}, 4 V / div. 12 V_{MAX} = 13.91 V.
Middle: 5 V_{OUT}, 1 V / div. 5 V_{MAX} = 5.32 V.
Lower: InnoSwitch3-TN V_{DS}. 100 V / div.
500 ms / div.
Zoom: 10 ms / div.

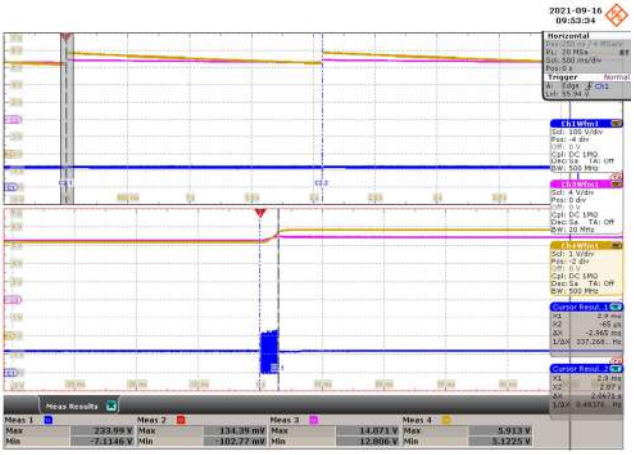


Figure 50 – Output Voltage Waveform. No Load.
85 VAC Input.
Upper: 12 V_{OUT}, 4 V / div. 12 V_{MAX} = 14.07 V.
Middle: 5 V_{OUT}, 1 V / div. 5 V_{MAX} = 5.91 V.
Lower: InnoSwitch3-TN V_{DS}. 100 V / div.
500 ms / div.
Zoom: 10 ms / div.

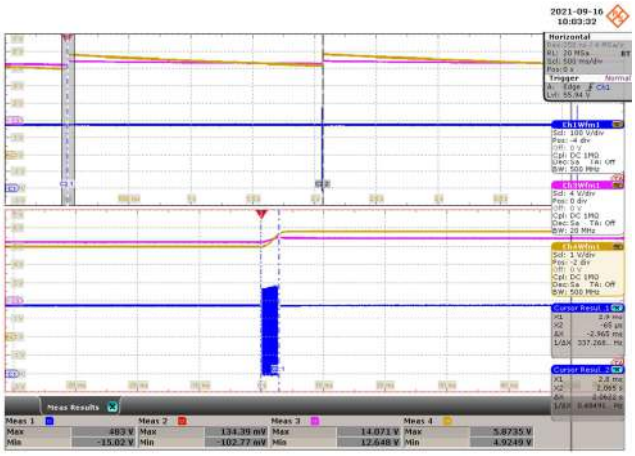


Figure 51 – Output Voltage Waveform. No Load.
265 VAC Input.
Upper: 12 V_{OUT}, 4 V / div. 12 V_{MAX} = 14.07 V.
Middle: 5 V_{OUT}, 1 V / div. 5 V_{MAX} = 5.87 V.
Lower: InnoSwitch3-TN V_{DS}. 100 V / div.
500 ms / div.
Zoom: 10 ms / div.

10.3 ***Output Ripple Measurements***

10.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

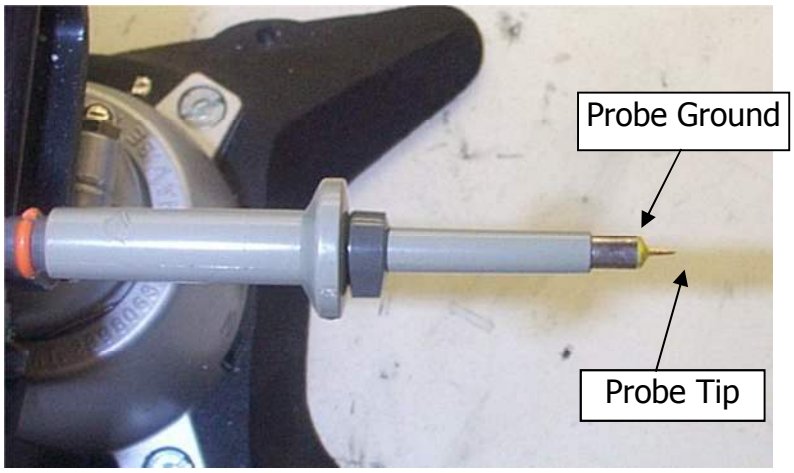


Figure 52 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

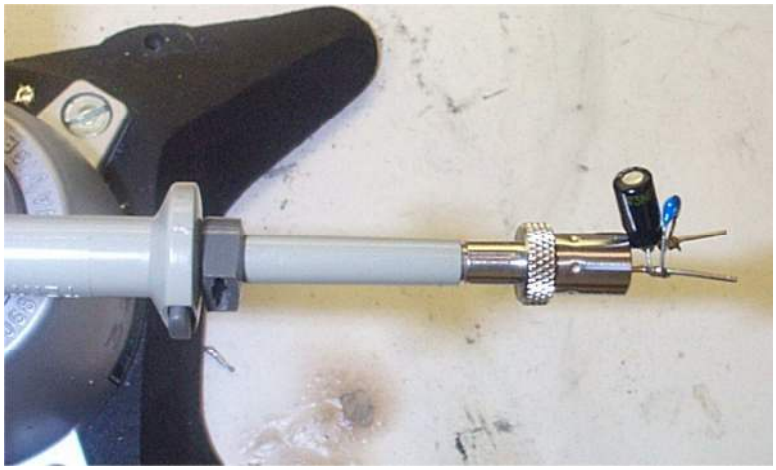


Figure 53 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

10.3.2 Ripple Voltage Waveforms

Note: Both 5V & 12V output are loaded with the same percentage.

10.3.2.1 0% Load

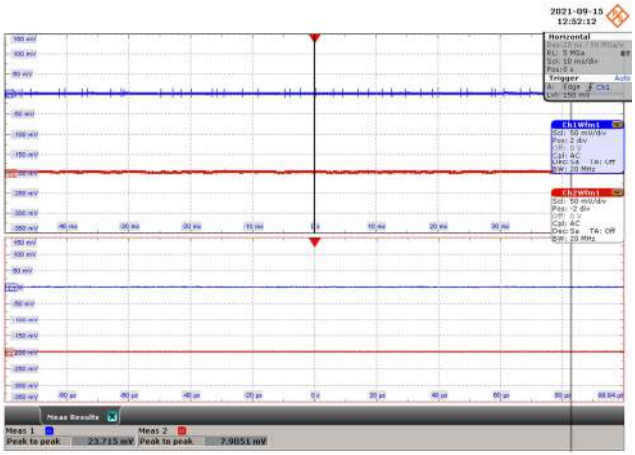


Figure 54 – Output Ripple Voltage Waveforms.
85 VAC Input.
12 V_{PK-PK}: 23.71 mV, 5 V_{PK-PK}: 7.9 mV.
Upper: 12 V_{OUT}, 50 mV / div, 10 ms / div.
Lower: 5 V_{OUT}, 50 mV / div, 10 ms / div.
Zoom: 20 µs / div.

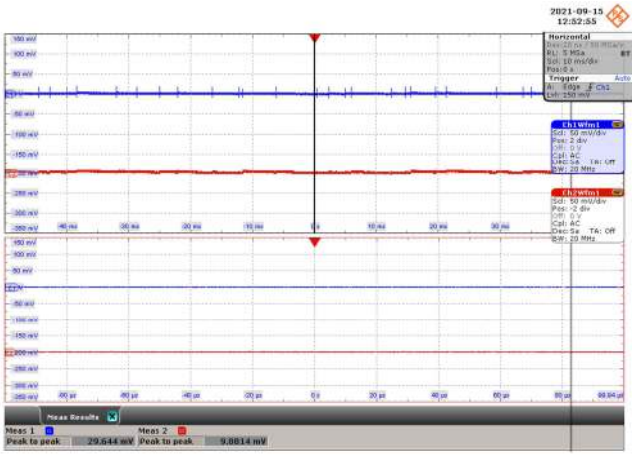


Figure 55 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
12 V_{PK-PK}: 29.64 mV, 5 V_{PK-PK}: 9.88 mV.
Upper: 12 V_{OUT}, 50 mV / div, 10 ms / div.
Lower: 5 V_{OUT}, 50 mV / div, 10 ms / div.
Zoom: 20 µs / div.

10.3.2.2 25% Load

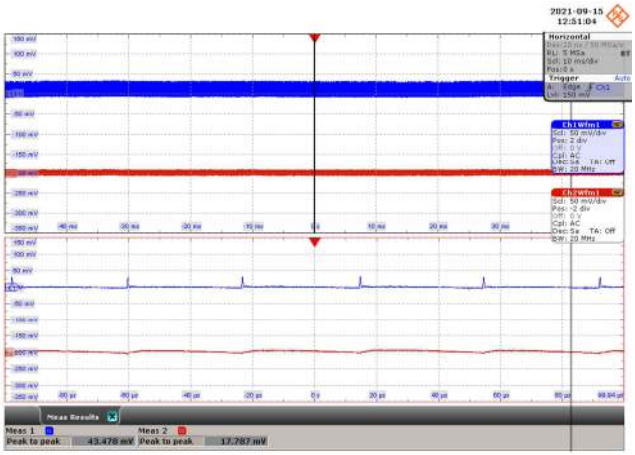


Figure 56 – Output Ripple Voltage Waveforms.
85 VAC Input.
12 V_{PK-PK}: 43.47 mV, 5 V_{PK-PK}: 17.78 mV.
Upper: 12 V_{OUT}, 50 mV / div, 10 ms / div.
Lower: 5 V_{OUT}, 50 mV / div, 10 ms / div.
Zoom: 20 µs / div.

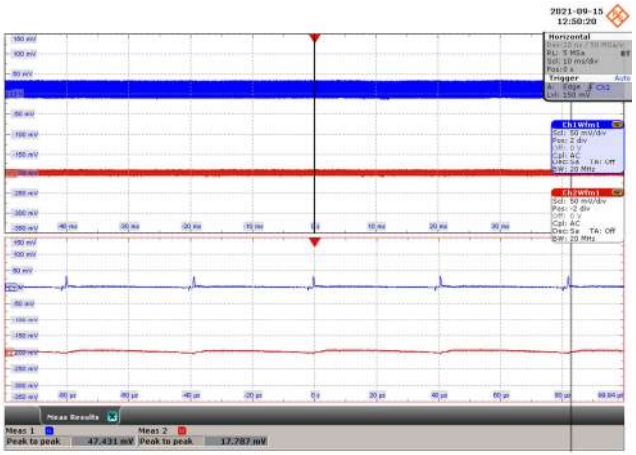


Figure 57 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
12 V_{PK-PK}: 47.43 mV, 5 V_{PK-PK}: 17.78 mV.
Upper: 12 V_{OUT}, 50 mV / div, 10 ms / div.
Lower: 5 V_{OUT}, 50 mV / div, 10 ms / div.
Zoom: 20 µs / div.

10.3.2.3 50% Load

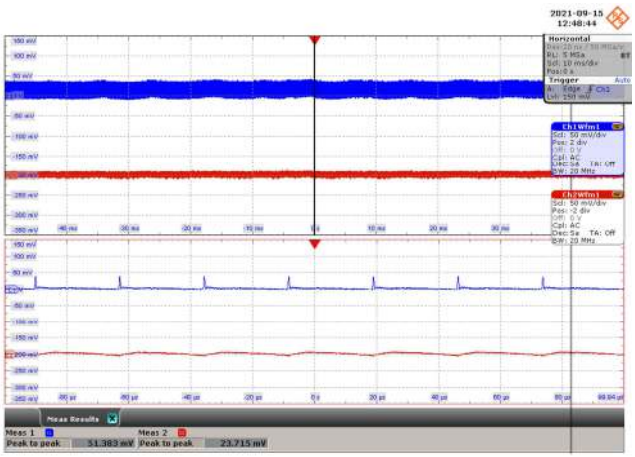


Figure 58 – Output Ripple Voltage Waveforms.
85 VAC Input.
12 V_{PK-PK}: 51.38 mV, 5 V_{PK-PK}: 23.71 mV.
Upper: 12 V_{OUT}, 50 mV / div, 10 ms / div.
Lower: 5 V_{OUT}, 50 mV / div, 10 ms / div.
Zoom: 20 µs / div.

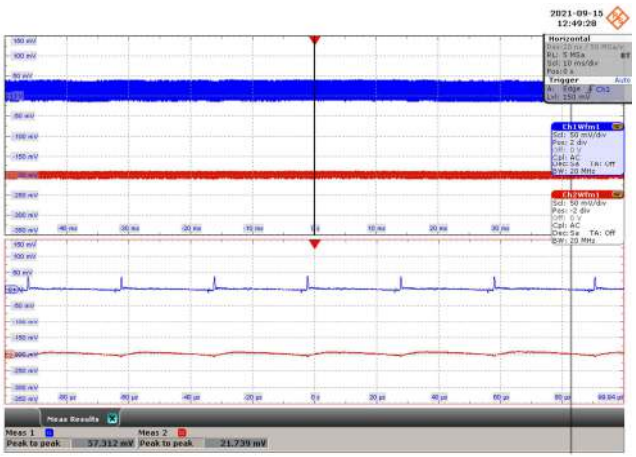


Figure 59 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
12 V_{PK-PK}: 57.31 mV, 5 V_{PK-PK}: 21.73 mV.
Upper: 12 V_{OUT}, 50 mV / div, 10 ms / div.
Lower: 5 V_{OUT}, 50 mV / div, 10 ms / div.
Zoom: 20 µs / div.

10.3.2.4 75% Load

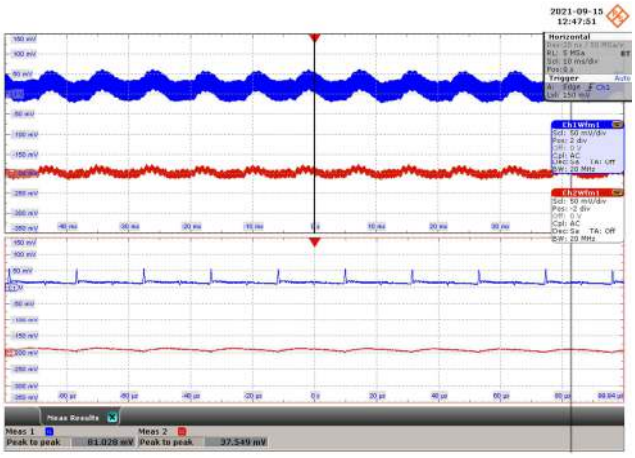


Figure 60 – Output Ripple Voltage Waveforms.
85 VAC Input.
12 V_{PK-PK}: 81.02 mV, 5 V_{PK-PK}: 37.54 mV.
Upper: 12 V_{OUT}, 50 mV / div, 10 ms / div.
Lower: 5 V_{OUT}, 50 mV / div, 10 ms / div.
Zoom: 20 µs / div.

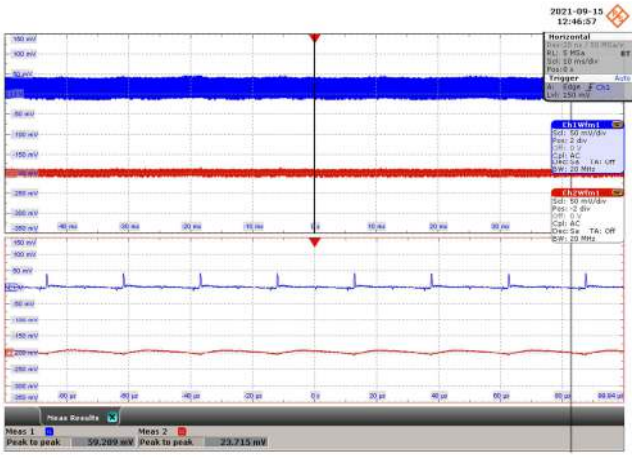


Figure 61 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
12 V_{PK-PK}: 59.28 mV, 5 V_{PK-PK}: 23.7 mV.
Upper: 12 V_{OUT}, 50 mV / div, 10 ms / div.
Lower: 5 V_{OUT}, 50 mV / div, 10 ms / div.
Zoom: 20 µs / div.

10.3.2.5 100% Load

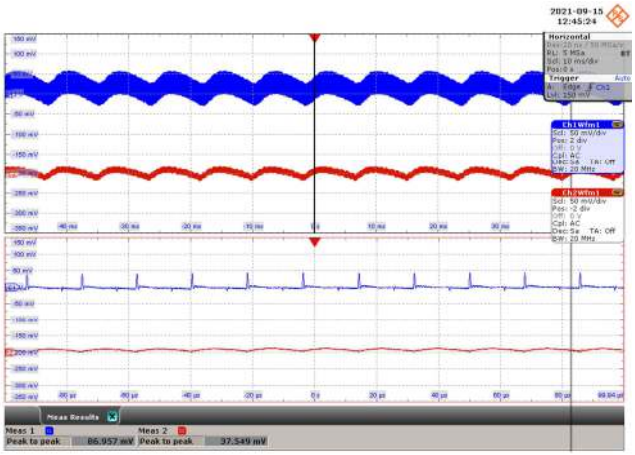


Figure 62 – Output Ripple Voltage Waveforms.
85 VAC Input.
12 V_{PK-PK}: 86.95 mV, 5 V_{PK-PK}: 37.54 mV.
Upper: 12 V_{OUT}, 50 mV / div, 10 ms / div.
Lower: 5 V_{OUT}, 50 mV / div, 10 ms / div.
Zoom: 20 µs / div.

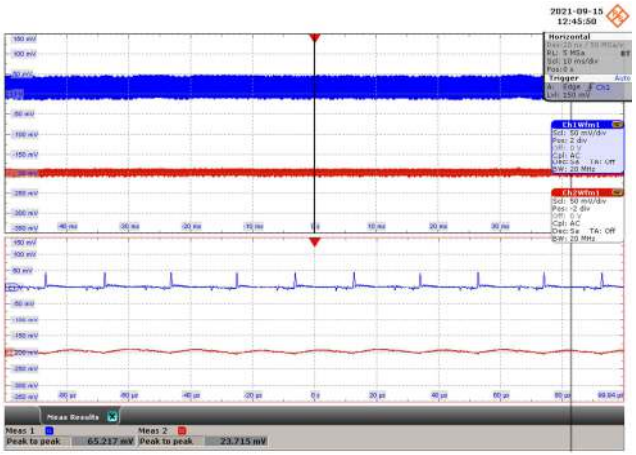


Figure 63 – Output Ripple Voltage Waveforms**.**
265 VAC Input.
12 V_{PK-PK}: 65.21 mV, 5 V_{PK-PK}: 23.71 mV.
Upper: 12 V_{OUT}, 50 mV / div, 10 ms / div.
Lower: 5 V_{OUT}, 50 mV / div, 10 ms / div.
Zoom: 20 µs / div.

10.3.3 Ripple (ATE Measurements)

Note: Both 5V & 12V output are loaded with the same percentage.

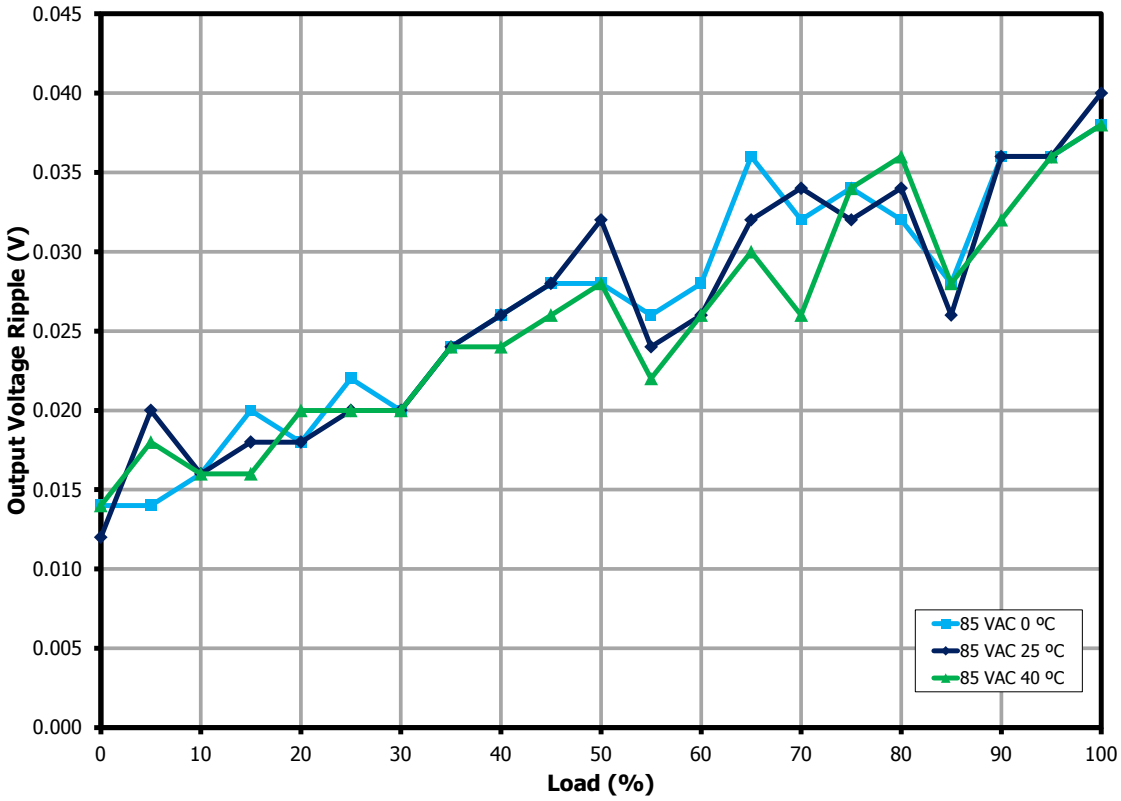


Figure 64 – 5 V Output Voltage Ripple vs. Output Load, 85 VAC Input.

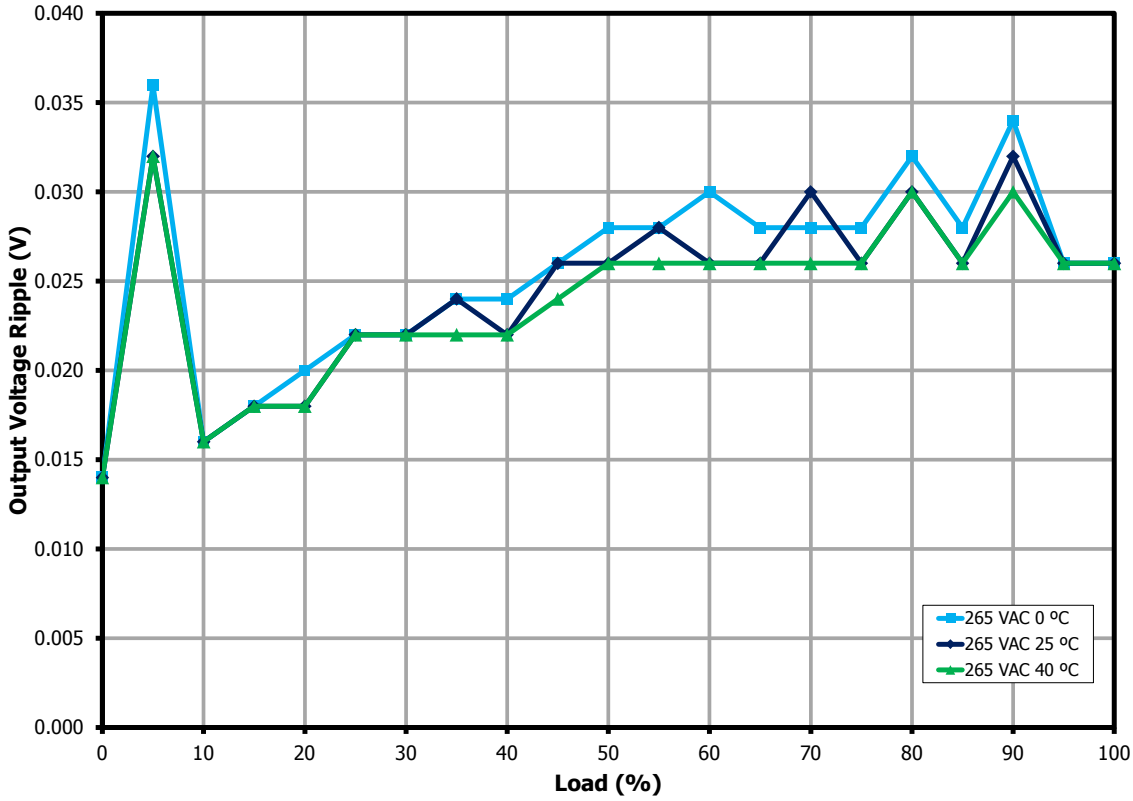


Figure 65 – 5 V Output Voltage Ripple vs. Output Load, 265 VAC Input.

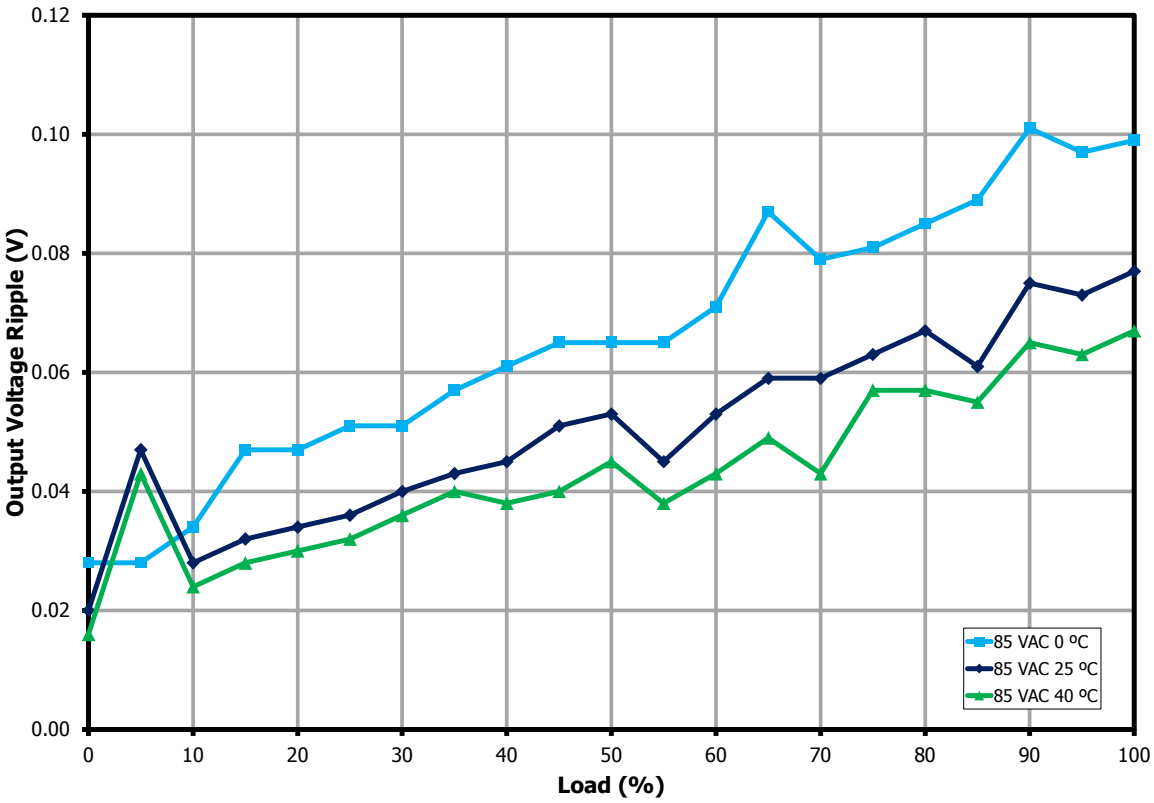


Figure 66 – 12 V Output Voltage Ripple vs. Output Load, 85 VAC Input.

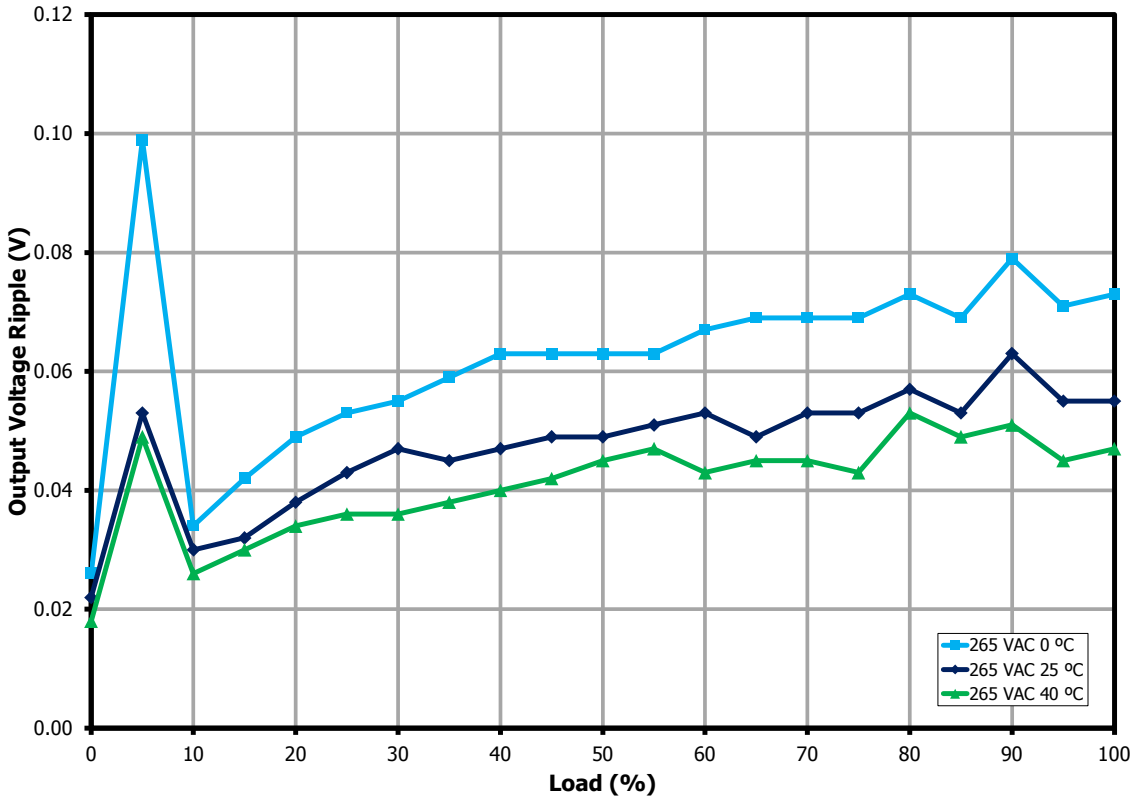


Figure 67 – 12 V Output Voltage Ripple vs. Output Load, 265 VAC Input.

11 EMI

11.1 *Conductive EMI*

11.1.1 Floating Output (QP / AV)

11.1.1.1 115 VAC Input

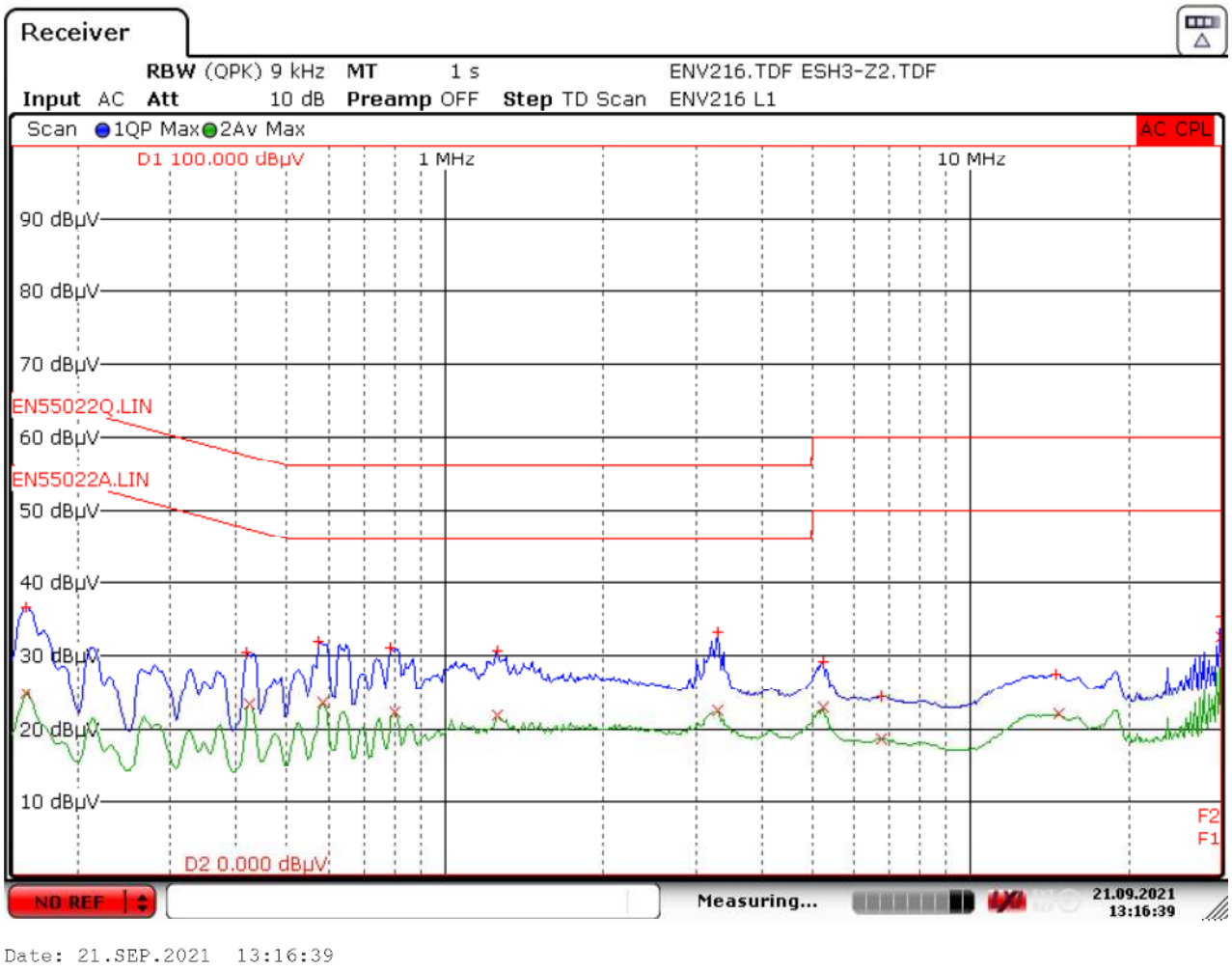


Figure 68 – Floating Ground - 115 VAC Line.

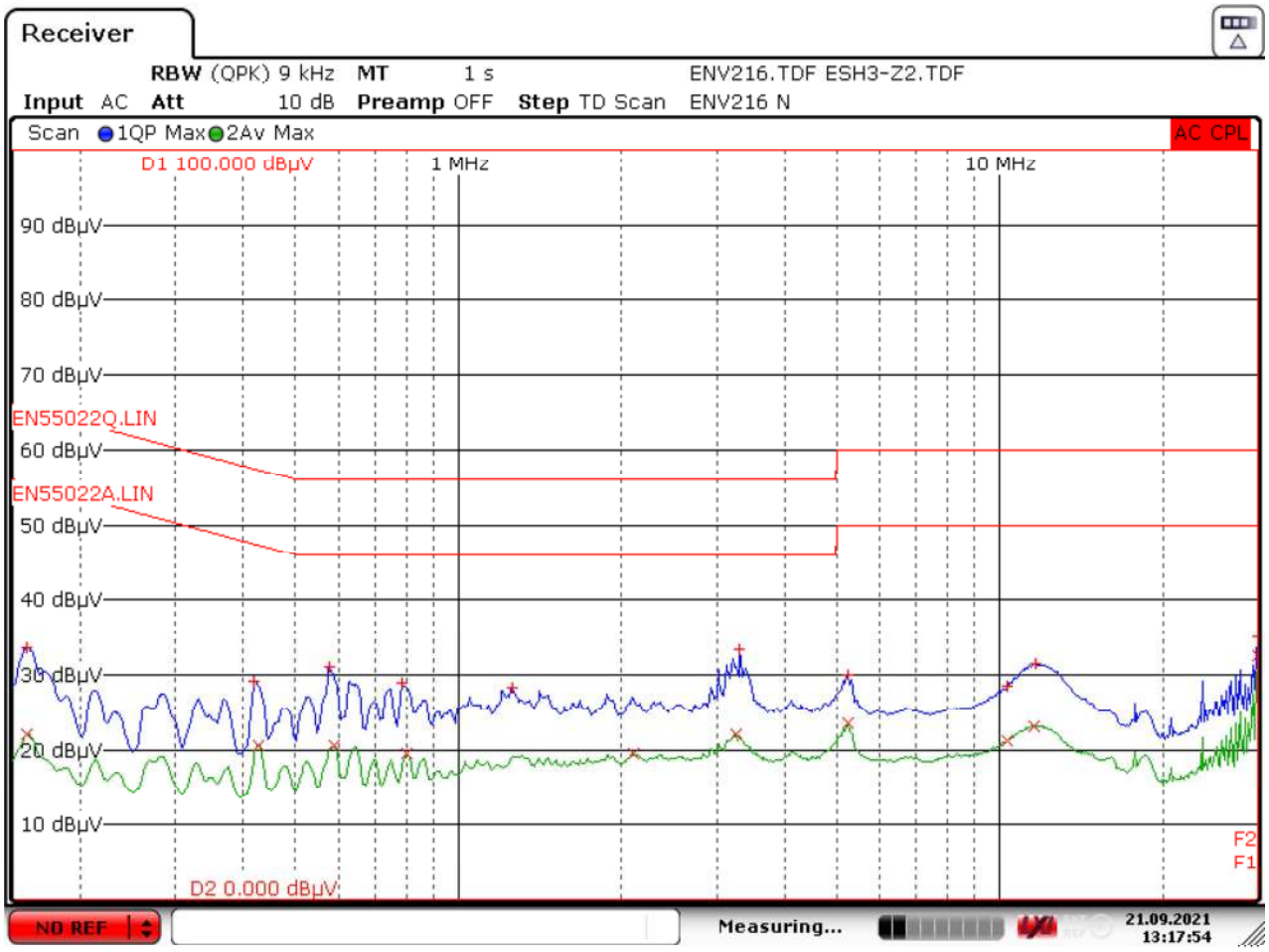


Figure 69 – Floating Ground - 115 VAC Neutral.

11.1.1.2 230 VAC Input

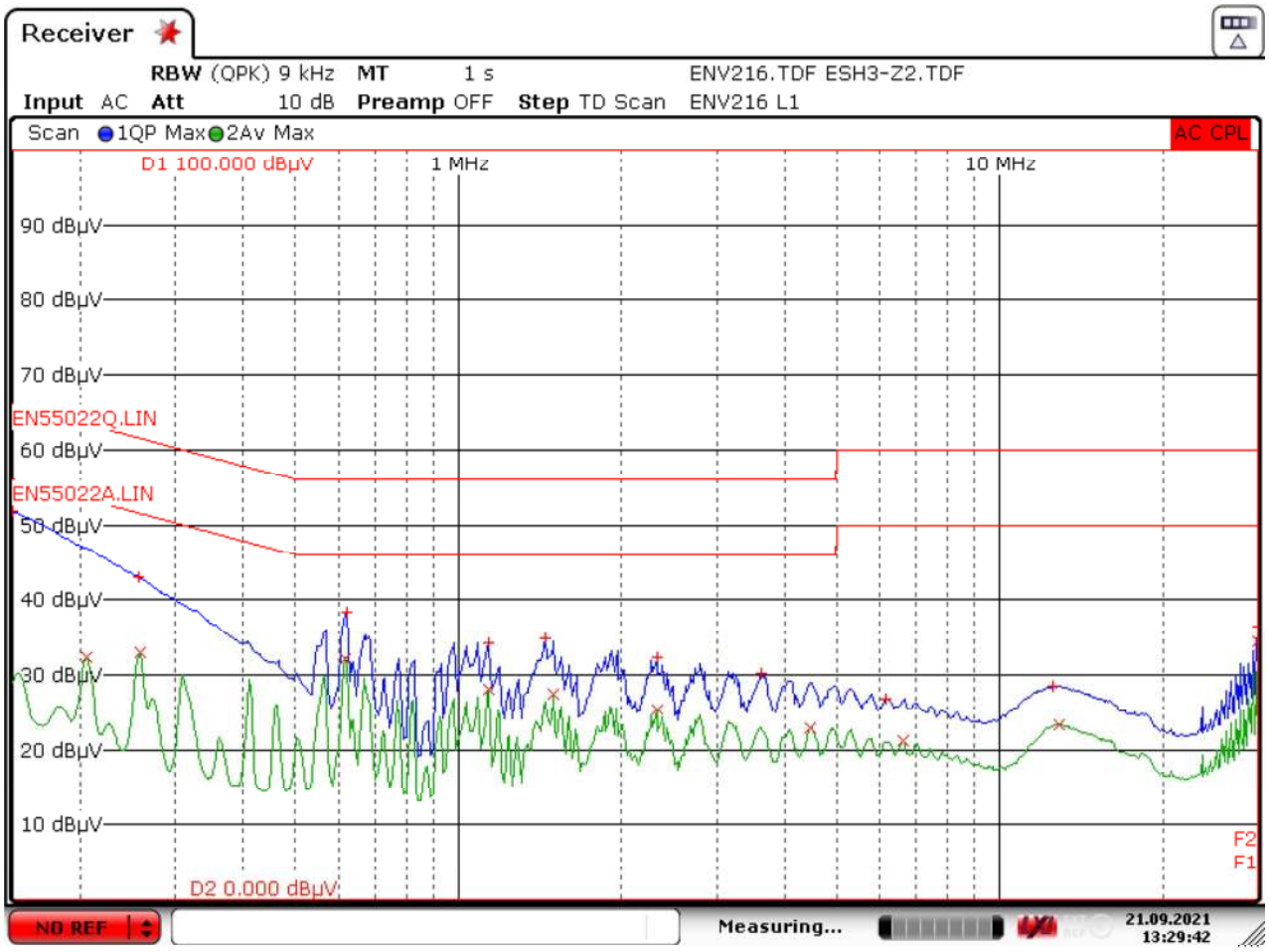


Figure 70 – Floating Ground - 230 VAC Line.

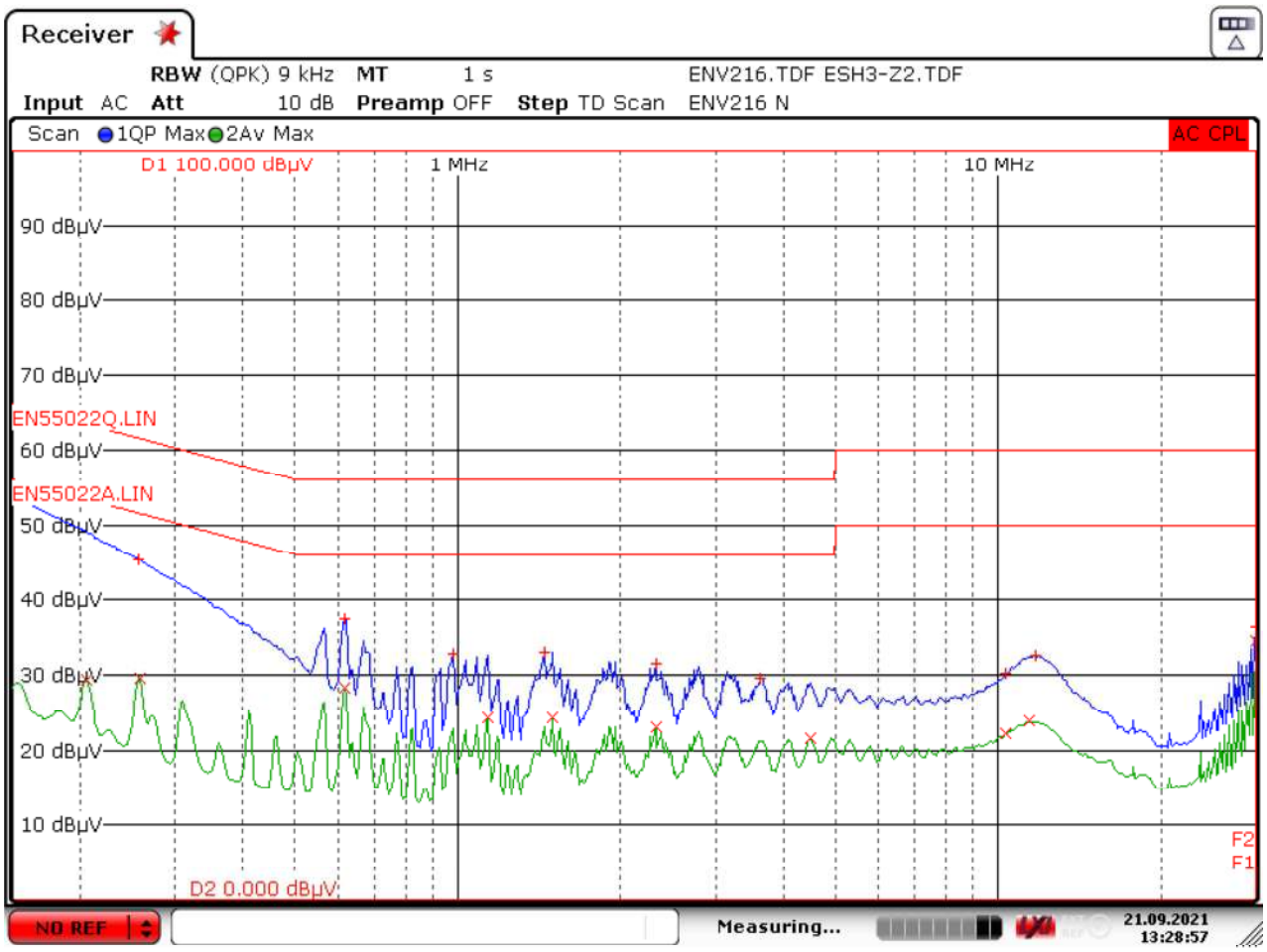


Figure 71 – Floating Ground - 230 VAC Neutral.

12 Lighting Surge Test

12.1 *Differential Mode Test*

Passed ±1 kV, 500 A surge test.

Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Test Result
1	0	L,N	2	10	PASS
-1	0	L,N	2	10	PASS
1	90	L,N	2	10	PASS
-1	90	L,N	2	10	PASS
1	180	L,N	2	10	PASS
-1	180	L,N	2	10	PASS
1	270	L,N	2	10	PASS
-1	270	L,N	2	10	PASS

12.2 *Common Mode Test*

Passed ±6 kV, ring wave test.

Ring Wave Voltage (kV)	Phase Angle (°)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Test Result
2	0	L,N-PE	12	10	PASS
-2	0	L,N-PE	12	10	PASS
2	90	L,N-PE	12	10	PASS
-2	90	L,N-PE	12	10	PASS
2	180	L,N-PE	12	10	PASS
-2	180	L,N-PE	12	10	PASS
2	270	L,N-PE	12	10	PASS
-2	270	L,N-PE	12	10	PASS
4	0	L,N-PE	12	10	PASS
-4	0	L,N-PE	12	10	PASS
4	90	L,N-PE	12	10	PASS
-4	90	L,N-PE	12	10	PASS
4	180	L,N-PE	12	10	PASS
-4	180	L,N-PE	12	10	PASS
4	270	L,N-PE	12	10	PASS
-4	270	L,N-PE	12	10	PASS
6	0	L,N-PE	12	10	PASS
-6	0	L,N-PE	12	10	PASS
6	90	L,N-PE	12	10	PASS
-6	90	L,N-PE	12	10	PASS
6	180	L,N-PE	12	10	PASS
-6	180	L,N-PE	12	10	PASS
6	270	L,N-PE	12	10	PASS
-6	270	L,N-PE	12	10	PASS

12.3 **EFT**

Passed ±2 kV, EFT test.

EFT Surge Voltage (kV)	Phase Angle (°)	IEC Coupling	Frequency	T-Burst	T-Rep	Test Result
2	0	L,N-PE	5 kHz	15 ms	120 s	PASS
-2	0	L,N-PE	5 kHz	15 ms	120 s	PASS
2	90	L,N-PE	5 kHz	15 ms	120 s	PASS
-2	90	L,N-PE	5 kHz	15 ms	120 s	PASS
2	180	L,N-PE	5 kHz	15 ms	120 s	PASS
-2	180	L,N-PE	5 kHz	15 ms	120 s	PASS
2	270	L,N-PE	5 kHz	15 ms	120 s	PASS
-2	270	L,N-PE	5 kHz	15 ms	120 s	PASS
2	0	L,N-PE	100 kHz	750 us	120 s	PASS
-2	0	L,N-PE	100 kHz	750 us	120 s	PASS
2	90	L,N-PE	100 kHz	750 us	120 s	PASS
-2	90	L,N-PE	100 kHz	750 us	120 s	PASS
2	180	L,N-PE	100 kHz	750 us	120 s	PASS
-2	180	L,N-PE	100 kHz	750 us	120 s	PASS
2	270	L,N-PE	100 kHz	750 us	120 s	PASS
-2	270	L,N-PE	100 kHz	750 us	120 s	PASS

13 Revision History

Date	Author	Revision	Description & Changes	Reviewed
26-Oct-21	MA	1.0	Initial Release.	Apps & Mktg
10-Nov-21	KM	1.1	Updated BOM	Apps & Mktg

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