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March 2014

## FQP12N60C

## N-Channel QFET® MOSFET

600 V, 12 A, 650 mΩ

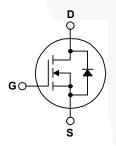
## **Description**

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.

#### **Features**

- 12 A, 600 V,  $R_{DS(on)}$  = 650 m $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D$  = 6 A
- · Low Gate Charge (Typ. 48 nC)
- · Low Crss (Typ. 21 pF)
- · 100% Avalanche Tested





## Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQP12N60C	Unit	
V <sub>DSS</sub>	Drain-Source Voltage		600	V	
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)		12 7.4	A A	
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	48	A	
V <sub>GSS</sub>	Gate-Source voltage		± 30	V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		870	mJ	
I <sub>AR</sub>	Avalanche Current (Note 1)		12	A	
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)		22.5	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns	
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C		225 1.78	W W/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C	
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C	

<sup>\*</sup>Drain current limited by maximum junction temperature

#### **Thermal Characteristics**

Symbol	Parameter	FQP12N60C	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.56	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W	

## **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP12N60C	FQP12N60C	TO-220	Tube	N/A	N/A	50 units

## **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Off Charac	teristics			II.		
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_J = 25^{\circ}\text{C}$	600			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.5		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°			1 10	μ <b>Α</b> μ <b>Α</b>
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	-		100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	-		-100	nA
On Charac	teristics					•
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6 A		0.53	0.65	Ω
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 6 A		13		S
Dynamic C	Characteristics			I.		
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$	\	1760	2290	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		182	235	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	21	28	pF
Switching	Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 12 A		30	70	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$		85	180	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			140	280	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		90	190	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 12 A		48	63	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V	-/	8.5		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)		21		nC
Drain-Sour	rce Diode Characteristics and Maximur	n Ratings			/	
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				12	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				48	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 12 A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 12 A		420		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dl <sub>F</sub> /dt = 100 A/μs		4.9		μС

#### NOTES:

<sup>1.</sup> Repetitive rating: pulse-width limited by maximum junction temperature.

<sup>2.</sup> L = 11 mH, I $_{AS}$  = 12 A, V $_{DD}$  = 50 V, R $_{G}$  = 25  $\Omega$ , starting T $_{J}$  = 25°C.

 $<sup>3.</sup>I_{SD} \le 12$  A, di/dt  $\le 200$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ , starting  $T_J$  = 25°C.

<sup>4.</sup> Essentially independent of operating temperature typical characteristics.

## **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

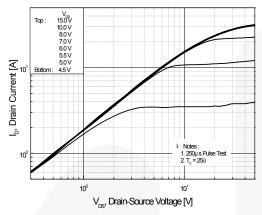


Figure 3. On-Resistance Variation vs. **Drain Current and Gate Voltage** 

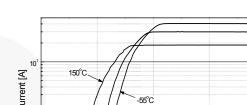
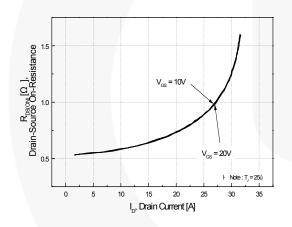


Figure 2. Transfer Characteristics

I<sub>D</sub>, Drain Current [A] Notes : 1. V<sub>DS</sub> = 40V 2. 250µ s Pulse Test 10<sup>-1</sup> 2 V<sub>cs</sub>, Gate-Source Voltage [V]

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue



Reverse Drain Current [A] I Notes: 1. V<sub>GS</sub> = 0V 2. 250µs Pulse Test 0.4 V<sub>sp</sub>, Source-Drain voltage [V]

Figure 5. Capacitance Characteristics

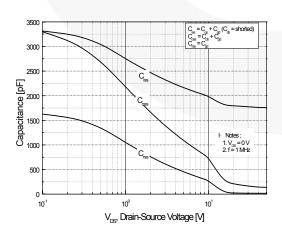
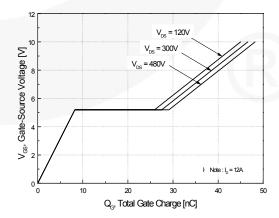


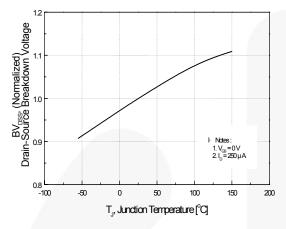
Figure 6. Gate Charge Characteristics



## **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On-Resistance Variation vs. Temperature



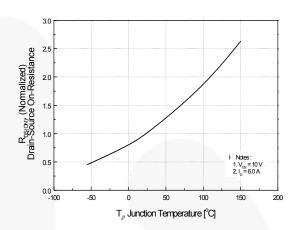
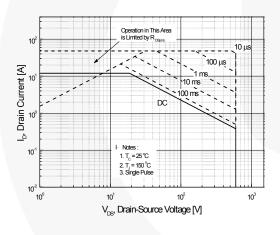


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature



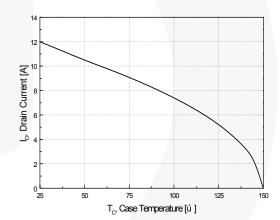
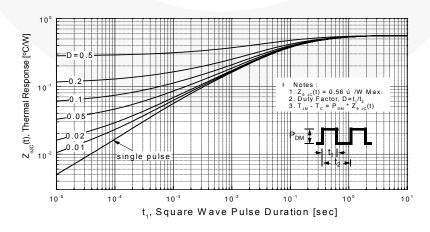


Figure 11. Transient Thermal Response Curve



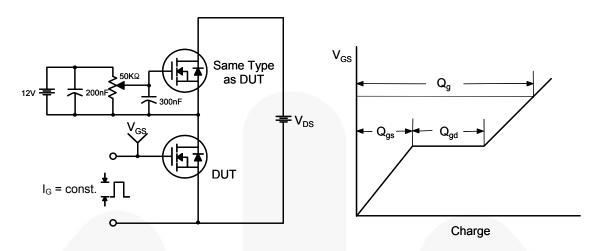


Figure 12. Gate Charge Test Circuit & Waveform

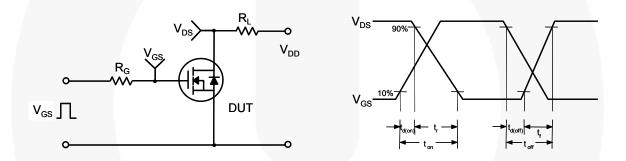


Figure 13. Resistive Switching Test Circuit & Waveforms

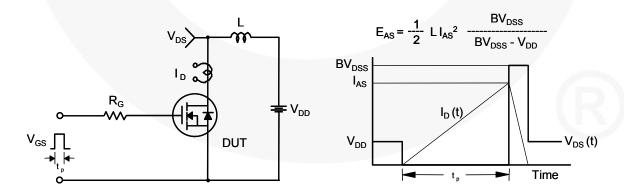


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

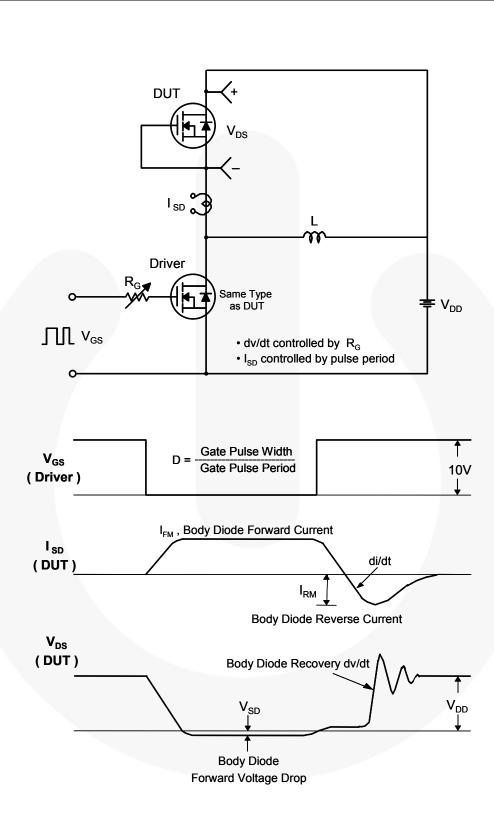


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

### **Mechanical Dimensions**

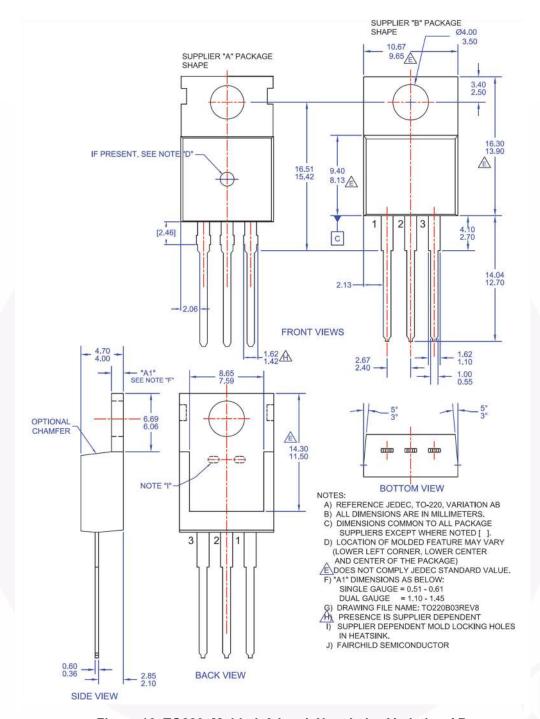


Figure 16. TO220, Molded, 3-Lead, Non Jedec Variation AB

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