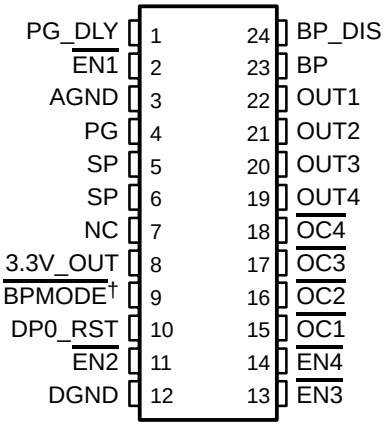
- **Complete USB Hub Power Solution**
- **Meets USB Specifications 1.1 and 2.0**
- **Independent Thermal and Short-Circuit Protection**
- **3.3-V Regulator for USB Hub Controller**
- **Overcurrent Logic Outputs**
- **4.5-V to 5.5-V Operating Range**
- **CMOS- and TTL-Compatible Enable Inputs**
- **185 μA Bus-Power Supply Current**
- **Available in 24-Pin SSOP Package**
- **–40°C to 85°C Ambient Temperature Range**

DB PACKAGE
(TOP VIEW)



NC – No internal connection
† Pin 9 is active low (BPMODE) for TPS2074 and active high (BPMODE) for TPS2075.

description

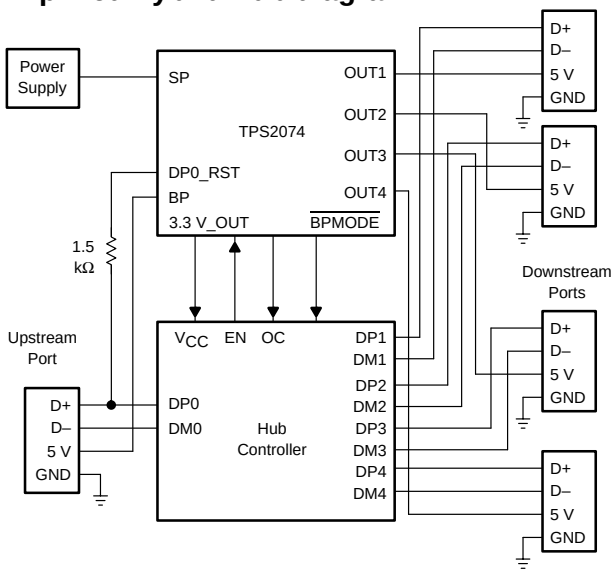
The TPS2074 and TPS2075 provide a complete USB hub power solution by incorporating three major functions: current-limited power switches for four ports, a 3.3-V 100-mA regulator, and a DP0 line control to signal attach/detach of the hub.

These devices are designed to meet bus-powered and self-powered hub requirements. These devices are also designed for hybrid hub implementations and allow for automatic switching from self-powered mode to bus-powered mode if loss of self-power is experienced. This feature can be disabled by applying a logic high to the BP_DIS input

Each port has a current-limited 100-mΩ N-channel MOSFET high-side power switch for 500 mA self-powered operation. Each port also has a current-limited 500-mΩ N-channel MOSFET high-side power switch for 100-mA bus-powered operation. All the N-channel MOSFETs are designed without parasitic diodes, preventing current backflow into the inputs.

For applications where a 5-V regulator is needed, use the TPS2070 or TPS2071 device.

simplified hybrid-hub diagram‡



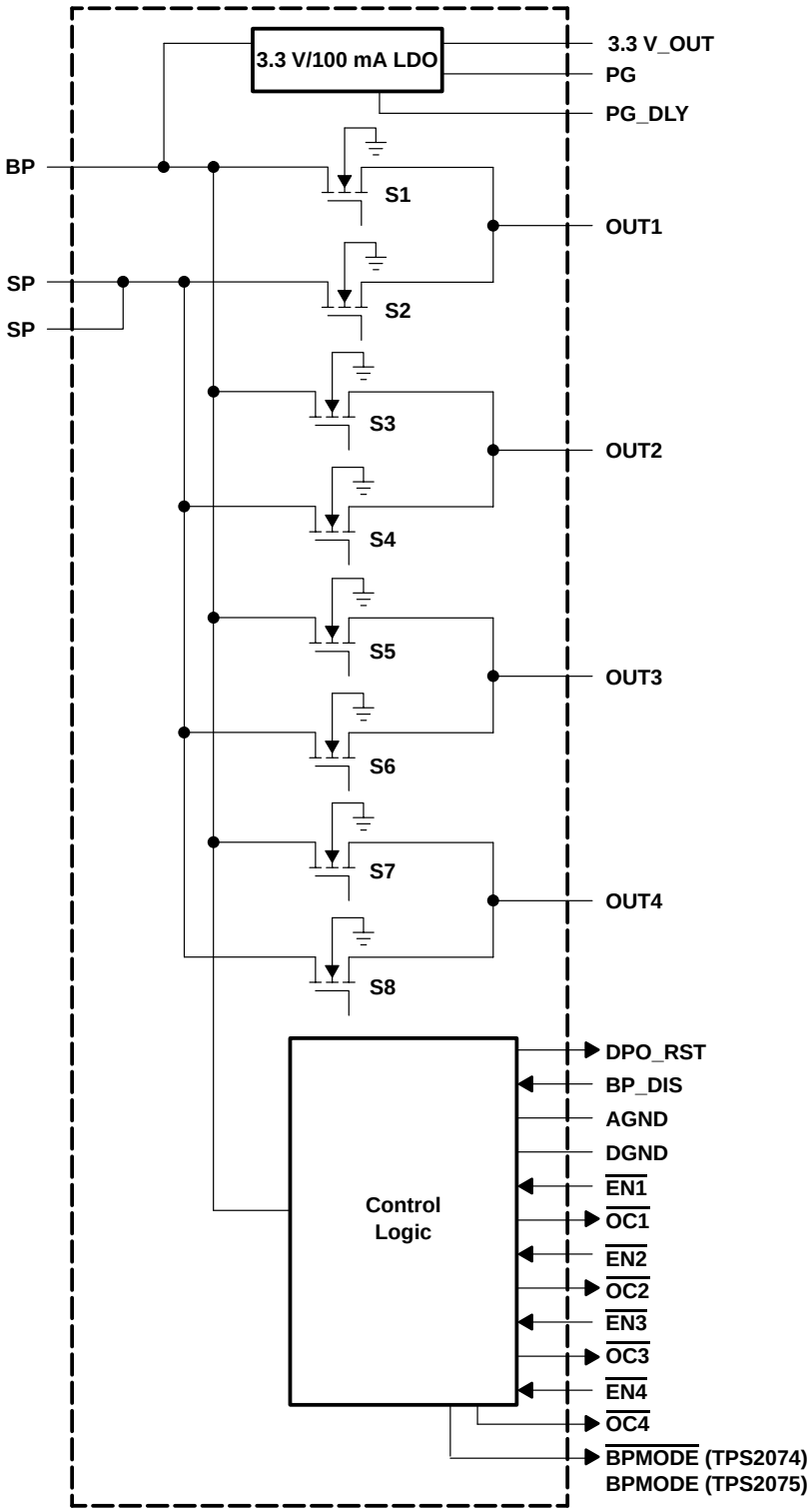
‡ See Figure 33 for complete implementation.

SELECTION GUIDE

T_A	USB HUB POWER CONTROLLERS	PACKAGED DEVICES			
		PIN COUNT	BPMODE	HTSSOP (DAP)	SSOP (DB)†
–40°C to 85°C	Four-port with internal LDO controller	32	Active low	TPS2070DAP	—
			Active high	TPS2071DAP	—
	Four-port without internal LDO controller	24	Active low	—	TPS2074DB
			Active high	—	TPS2075DB

† The DB package is available taped and reeled. Add an R suffix to the device type (e.g., TPS2074DBR).

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PG_DLY†	1		Adjusts the PG time delay with a capacitor to ground. Adjust the pulse width to fit the application.
$\overline{\text{EN1}}$	2	I	Active-low enable for OUT1
AGND	3		Analog ground
PG	4	O	Logic output, power good
SP	5	I	Self-power voltage input, connects to local power supply
SP	6	I	Self-power voltage input, connects to local power supply
NC	7		No internal connection
3.3V_OUT	8	O	3.3-V internal voltage regulator output
$\overline{\text{BPMODE}}$‡	9	O	A logic signal that indicates if the outputs source from the bus-powered supply, $\overline{\text{BPMODE}}$ (TPS2074) or BPMODE (TPS2075), can be used to signal the hub controller.
DP0_RST	10	O	Connects to DP signal from upstream hub/host through an external 1.5-kΩ resistor
$\overline{\text{EN2}}$	11	I	Active-low enable for OUT2
DGND	12		Digital ground
$\overline{\text{EN3}}$	13	I	Active-low enable for OUT3
$\overline{\text{EN4}}$	14	I	Active-low enable for OUT4
$\overline{\text{OC1}}$	15	O	Logic output, overcurrent response for OUT1
$\overline{\text{OC2}}$	16	O	Logic output, overcurrent response for OUT2
$\overline{\text{OC3}}$	17	O	Logic output, overcurrent response for OUT3
$\overline{\text{OC4}}$	18	O	Logic output, overcurrent response for OUT4
OUT4	19	O	Power switch output for downstream ports
OUT3	20	O	Power switch output for downstream ports
OUT2	21	O	Power switch output for downstream ports
OUT1	22	O	Power switch output for downstream ports
BP	23	I	Bus power voltage input, connect to V_{BUS}
BP_DIS	24	I	Active-high logic input, disables autoswitch to bus power when self power is disconnected. Connect to BP or GND

† Use the following formula to calculate the capacitance needed;
C = (desired pulse width $\times$ 3 $\times$ 10^{-6} / 1.22

‡ Pin 9 is active low for TPS2074 and active high for TPS2075.

detailed description

BP

The bus-powered supply input (BP) serves as the source for the internal 3.3-V LDO and for all logic functions in the device. In bus-powered mode, BP also serves as the source for all the outputs (OUTx). If BP is below the undervoltage threshold, all power switches will turn off and the LDO will be disabled. BP must be connected to a voltage source in order for the device to operate.

SP

The self-powered supply input (SP) serves as the source for all the outputs (OUTx) in self-powered mode. The enable logic for the SP switches requires that BP be connected to a voltage source.

OUT1, OUT2, OUT2, OUT4

OUTx are the outputs of the integrated power switches.

3.3V_OUT

The internal 3.3-V LDO output can be used to supply up to 100 mA current to low-power functions, such as hub controllers.

DP0_RST

DP0_RST functions as a hub reset when a 1.5-kΩ resistor is connected between DP0_RST and the upstream DP0 data line in a hub system. To provide a clean attach signal on DP0 data line, the DP0_RST output goes low momentarily (because of the upstream pulldown resistor) to discharge any parasitic charge on the cable, then goes to 3-state and finally outputs a high signal. The low and Hi-Z pulse widths are adjustable using a capacitor between PG_DLY and ground, and are approximately 50% of the power-good time delay. Detachment is signaled by a Hi-Z on DP0_RST. Both DP0_RST and PG will transition high at the same time.

Power Good (PG)

The power good (PG) function serves as a reset for a USB hub controller. PG is asserted low when the output voltage on the internal voltage regulator is below a fixed threshold. A time delay to ensure a stable output voltage before PG goes high is adjustable using a small-value ceramic capacitor from PG_DLY to ground.

PG_DLY

PG_DLY connects to an external capacitor to adjust the time delay for PG and DP0_RST. For USB applications, a 0.1 μF capacitor is recommended, however, reference the USB hub controller data sheet to determine the needed pulse width criteria.

BP_DIS

BP_DIS is used to enable or disable the autoswitching function between bus-powered mode and self-powered mode. When BP_DIS is connected low and the voltage on SP is greater than the undervoltage-lockout (UVLO) threshold, the device will switch to self-powered operation automatically; if the SP voltage falls lower than the UVLO threshold, the device will switch to bus-powered operation. When BP_DIS is connected high, the autoswitching function is disabled and the device will not autoswitch to bus-powered operation if the SP voltage is below the UVLO threshold.

$\overline{\text{BPMODE}}$ or BPMODE

$\overline{\text{BPMODE}}$ (TPS2074) or BPMODE (TPS2075) is an output that signals when the device is in bus-powered mode. The logic state is set according to the voltages on BP, SP, and BP_DIS. For the TPS2074, $\overline{\text{BPMODE}}$ outputs a low signal to indicate bus-powered mode or a high signal to indicate self-powered mode. For the TPS2075, BPMODE outputs a high signal to indicate bus-powered mode or a low signal to indicate self-powered mode. This output can be used to inform a USB hub controller to configure for bus-powered mode or self-powered mode.

detailed description (continued)

$\overline{OC1}$, $\overline{OC2}$, $\overline{OC3}$, $\overline{OC4}$

$\overline{OCx}$ is an output signal that is asserted (active low) when an overcurrent or overtemperature condition is encountered for the corresponding channel. $\overline{OCx}$ will remain asserted until the overcurrent or overtemperature condition is removed.

$\overline{EN1}$, $\overline{EN2}$, $\overline{EN3}$, $\overline{EN4}$,

The active-low logic input $\overline{ENx}$ enables or disables the power switches in the device. The enable input is compatible with both TTL and CMOS logic levels. The switches will not turn on until 3.3V_OUT is above the PG threshold.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

Input voltage range: $V_{I(BP)}$, $V_{I(SP)}$, $V_{I(\overline{ENx})}$, $V_{I(BP\_DIS)}$ . . . . . –0.3 V to 6 V
Output voltage range: $V_{O(OUTx)}$ . . . . . –0.3 V to 6 V
$V_{O(3.3V\_OUT)}$, $V_{O(PG\_DLY)}$, $V_{O(\overline{OCx})}$, $V_{O(\overline{BPMODE})}$,
$V_{O(DP0\_RST)}$, $V_{O(PG)}$ . . . . . –0.3 V to $V_{O\ (3.3V\_OUT)}$ 0.3 V
Continuous output current: $I_{O(\overline{OUTx})}$, $I_{O(3.3V\_OUT)}$ . . . . . internally limited
Maximum output current: $I_{O(BPMODE)}$ or $I_{O(BPMODE)}$, $I_{O(DP0\_RST)}$, $I_{O(PG)}$, $I_{O(OCx)}$ . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
24 DB	889.7 mW	8.9 mW/°C	489.3 mW	355.9 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage	$V_{I(BP)}$	4.5	5.5	V
	$V_{I(SP)}$	0	5.5	
	$V_{I(BP\_DIS)}$	0	5.5	
	$V_{I(\overline{ENx})}$	0	5.5	
Continuous output current, I_O	BP to OUTx (per switch)		100	mA
	SP to OUTx (per switch)		500	
	BP to 3.3V_OUT		100	
Operating virtual junction temperature, T_J		-40	125	°C

electrical characteristics over recommended operating junction temperature range, $4.5\ V \le V_{I(BP)} \le 5.5\ V$, $4.85\ V \le V_{I(SP)} \le 5.5\ V$, $\overline{ENx} = 0\ V$, BP_DIS = 0 V (unless otherwise noted)

input current

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
$I_{I(BP)}$	Input current at BP, switches disabled	No load on OUTx and 3.3V_OUT, $\overline{ENx} = V_{I(BP)}$	$V_{I(SP)}$ = Hi-Z		185	240	µA
			$V_{I(SP)}$ = 0 V		185	240	
			$V_{I(SP)}$ = 5 V		175	210	
	Input current at BP, switches enabled	No load on OUTx and 3.3V_OUT, $\overline{ENx}$ = 0 V	$V_{I(SP)}$ = Hi-Z		185	240	µA
			$V_{I(SP)}$ = 0 V		185	240	
			$V_{I(SP)}$ = 5 V		175	210	
$I_{I(SP)}$	Input current at SP, switches disabled	No load on OUTx and 3.3V_OUT, $\overline{ENx} = V_{I(SP)}$	$V_{I(BP)}$ = Hi-Z		90	115	µA
			$V_{I(BP)}$ = 0 V		90	115	
			$V_{I(BP)}$ = 5 V		115	140	
	Input current at SP, switches enabled	No load on OUTx and 3.3V_OUT, $\overline{ENx}$ = 0 V	$V_{I(BP)}$ = Hi-Z		90	115	µA
			$V_{I(BP)}$ = 0 V		90	115	
			$V_{I(BP)}$ = 5 V		115	140	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

power switches

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance	SP to OUTx	$V_{I(SP)} = V_{I(BP)} = 5\ V$, $I_{Ox} = 0.5\ A$	T_A = 25°C		100		mΩ
				T_A = 70°C		110	150	
		BP to OUTx	$V_{I(BP)} = 4.5\ V$, $V_{I(SP)}$ = Open, $I_{Ox} = 0.1\ A$	T_A = 25°C		500		
				T_A = 70°C		600	900	
$I_{lkg(OUTx)}$	Leakage current at OUTx (no load on 3.3V_OUT)		$\overline{ENx} = V_{I(BP)} = 5.5\ V$, $V_{I(SP)}$ = Hi-Z, OUTx connected to ground, $V_{I(VIN)}$ = Hi-Z	T_J = 25°C		0.5	10	µA
			$\overline{ENx} = V_{I(BP)} = V_{I(SP)} = 5.5\ V$, OUTx connected to ground	T_J = 25°C		0.5	10	
			$\overline{ENx}$ = $V_{I(BP)}$ = Hi-Z or 0 V, $V_{I(SP)} = V_{I(OUTx)} = 5.5\ V$	T_J = 25°C		0.5	10	
			$\overline{ENx} = V_{I(BP)} = V_{I(SP)}$ = Hi-Z or 0 V, $V_{I(OUTx)} = 5.5\ V$	T_J = 25°C		0.5	10	
	Short-circuit current (per output)†		$V_{I(BP)} = V_{I(SP)} = 5\ V$, OUTx connected to GND, Device enabled into short circuit		0.6	0.9	1.2	A
			$V_{I(BP)} = 5\ V$, $V_{I(SP)}$ = open, OUTx connected to GND, device enabled into short circuit		0.12	0.2	0.3	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

NOTE: All BP to OUTx , SP to OUTx switches and the internal 3.3-V voltage regulator are loaded to the recommended continuous current rating of 100 mA, 500 mA and 100 mA, respectively, for the static drain-source on-state resistance measurements.

input signals ($\overline{ENx}$, BP_DIS)

PARAMETER				TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	
I_I	Input current	Pullup	$\overline{ENx}$ (active low)	$V_{I(\overline{ENx})} = 0\ V$			5	µA
		Pulldown	BP_DIS (active high)	$V_{I(BP\_DIS)} = 5\ V$			5	

electrical characteristics over recommended operating junction temperature range, $4.5\ V \le V_{I(BP)} \le 5.5\ V$, $4.85\ V \le V_{I(SP)} \le 5.5\ V$, $\overline{EN}x = 0\ V$, BP_DIS = 0 V (unless otherwise noted) (continued)

output signals (BPMODE or $\overline{BPMODE}$, $\overline{OC}x$, DPO_RST)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{BPMODE}$	$4.25\ V \le V_{I(BP)} \le 5.5\ V$, $4.5\ V \le V_{I(SP)} \le 5.5\ V$	I_O = 2 mA	2.4			V
		BPMODE	$4.25\ V \le V_{I(BP)} \le 5.5\ V$, $V_{I(SP)} < 4\ V$		2.4			
		$\overline{OC}x$	$4.25\ V \le V_{I(BP)} \le 5.5\ V$, $V_{I(\overline{EN}x)}$ = 3.3 V or Hi-Z		2.4			
		DPO_RST	$4.25\ V \le V_{I(BP)} \le 5.5\ V$, $V_{I(PG\_DLY)}$ = 3.3 V		2.4			
V_{OL}	Low-level output voltage	$\overline{BPMODE}$	$4.25\ V \le V_{I(BP)} \le 5.5\ V$, $V_{I(SP)} < 4\ V$	I_O = 3.2 mA			0.4	V
		BPMODE	$4.25\ V \le V_{I(BP)} \le 5.5\ V$, $4.5\ V \le V_{I(SP)} \le 5.5\ V$				0.4	
		$\overline{OC}x$	$4.25\ V \le V_{I(BP)} \le 5.5\ V$, OUTx = 0 V	$I_{O(\overline{OC})}$ = 3.2 mA			0.4	
$V_{I(BP)}$	Minimum input voltage at BP for low-level output		I_O = 300 µA,	$V_{O(\overline{BPMODE})} \le 0.4\ V$			1.5	V
			I_O = 300 µA, $V_{I(SP)}$ = 5 V	$V_{O(BPMODE)} \le 0.4\ V$,			1.5	
I_{lkg}	Hi-Z leakage current at DP0_RST		$0\ V \le V_{I(DPO\_RST)} \le 3.3\ V$, $V_{I(SP)}$ = 0 V, $V_{I(BP)}$ = 5.5 V, $V_{I(PG\_DLY)}$ = 0.9 V		–5		5	µA
t_d	Overcurrent response delay time (see Note 1)				1		10	ms

NOTE 1: Specified by design, not tested in production.

undervoltage lockout (SP and BP)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Start threshold	SP				4.5	V
		BP	$V_{I(SP)}$ = Hi-Z			4.25	
	Stop threshold	SP		4			V
		BP		3.75			
V_{hys}	Hysteresis voltage (see Note 1)	SP		300			mV
		BP		300			

NOTE 1: Specified by design, not tested in production.

electrical characteristics over recommended operating junction temperature range, $4.5\ V \le V_{I(BP)} \le 5.5\ V$, $4.85\ V \le V_{I(SP)} \le 5.5\ V$, $\overline{EN}x = 0\ V$, BP_DIS = 0 V, $C_{L(3.3V\_OUT)} = 10\ \mu F$ (unless otherwise noted)

internal voltage regulator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage, dc	$V_{I(BP)}$ = 4.25 V to 5.5 V, I_O= 5 mA to 100 mA	3.2	3.3	3.4	V
	Dropout voltage	I_O = 100 mA		0.6		V
	Line regulation	$V_{I(BP)}$ = 4.25 V to 5.25 V, I_O= 5 mA			0.1	%/v
	Load regulation	$V_{I(BP)}$ = 4.25 V, I_O= 5 mA to 100 mA			0.6%	
I_{OS}	Short-circuit current limit†	$V_{I(BP)}$ = 4.25 V, 3.3V_OUT connected to GND	0.12	0.2	0.3	A
	Pulldown transistor at 3.3V_OUTPUT (see Note 1)	$V_{I(3.3V\_OUT)}$ = 3.3 V	10			mA
		$V_{I(3.3V\_OUT)}$ = 1 V	5			
PSRR	Power-supply ripple rejection (see Note 1)	F = 1 kHz, $C_{L(3.3V\_OUT)}$=4.7 µF, ESR=0.25 Ω, I_O=5 mA, $V_{I(BP)PP}$=100 mV	40			dB
	Low-level trip threshold voltage at PG		2.88	2.94	3	V
V_{hys}	Hysteresis voltage at PG (see Note 1)		50		100	mV
V_{OH}	High-level output voltage at PG	4.25 V ≤ $V_{I(BP)}$ ≤ 5.25 V, I_O = 2 mA	2.4			V
V_{OL}	Low-level output voltage at PG	4.25 V ≤ $V_{I(BP)}$ ≤ 5.25 V, I_O = 3.2 mA			0.4	V
V_{ref}	Reference voltage at PG_DLY			1.22		V
	Charge current at PG_DLY			3		µA
t_d	Delay time at PG (see Notes 1 and 2)	$C_{L(PG\_DLY)}$ = 0.47 µF		190		ms

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

NOTES: 1. Specified by design, not tested in production.

2. The PG delay time (t_d) is calculated using the PG_DLY reference voltage and charge current:

$$t_d = \frac{C_{L(PG\_DLY)} \times V_{ref}}{\text{Charge Current}}$$

power switch timing requirements

PARAMETER			TEST CONDITIONS†‡	MIN	TYP	MAX	UNIT
t_{on}	Turnon time (see Note 1)	BP to OUTx switch	$V_{I(BP)}$ = 5 V, $V_{I(SP)}$ = open, T_A = 25°C, C_L = 100 µF, R_L = 50 Ω		4.5		ms
		SP to OUTx switch	$V_{I(SP)}$ = $V_{I(BP)}$ = 5 V, T_A = 25°C, C_L = 100 µF, R_L = 10 Ω		4.5		
t_{off}	Turnoff time (see Note 1)	BP to OUTx switch	$V_{I(BP)}$ = 5 V, $V_{I(SP)}$ = open, T_A = 25°C, C_L = 100 µF, R_L = 50 Ω		15		ms
		SP to OUTx switch	$V_{I(SP)}$ = $V_{I(BP)}$ = 5 V, T_A = 25°C, C_L = 100 µF, R_L = 10 Ω		10		
t_r	Rise time, output (see Note 1)	BP to OUTx switch	$V_{I(BP)}$ = 5 V, $V_{I(SP)}$ = open, T_A = 25°C, C_L = 100 µF, R_L = 50 Ω		4		ms
		SP to OUTx switch	$V_{I(SP)}$ = $V_{I(BP)}$ = 5 V, T_A = 25°C, C_L = 100 µF, R_L = 10 Ω		3		
t_f	Fall time, output (see Note 1)	BP to OUTx switch	$V_{I(BP)}$ = 5 V, $V_{I(SP)}$ = open, T_A = 25°C, C_L = 100 µF, R_L = 50 Ω		10		ms
		SP to OUTx switch	$V_{I(SP)}$ = $V_{I(BP)}$ = 5 V, T_A = 25°C, C_L = 100 µF, R_L = 10 Ω		3		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

‡ All BP to OUTx , SP to OUTx switches and the internal 3.3-V voltage regulator are loaded to the recommended continuous current rating of 100 mA, 500 mA and 100 mA, respectively, for the static drain-source on-state resistance measurements.

NOTE 1. Specified by design, not tested in production.

thermal shutdown

PARAMETER			MIN	TYP	MAX	UNIT
T_J	Thermal shutdown	First		140		°C
		Second		150		
	Hysteresis	First		15		°C
		Second		25		

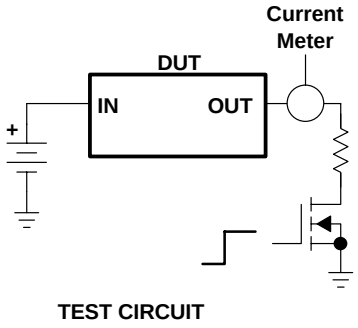


Figure 1. Current Limit Response

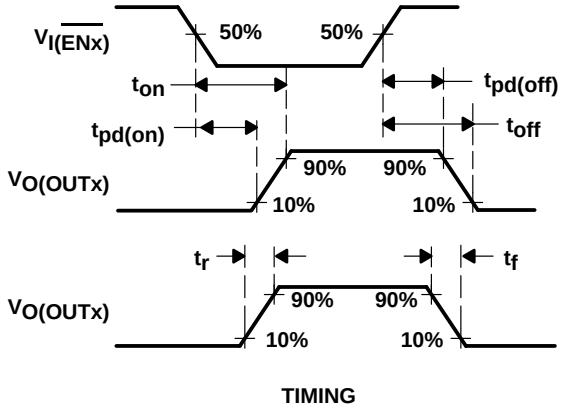


Figure 2. Timing and Internal Voltage Regulator Transition Waveforms

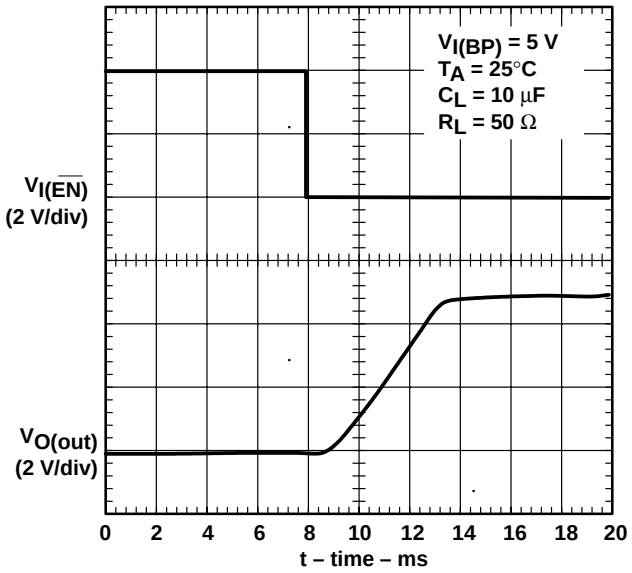


Figure 3. Turnon Delay and Rise Time (BP Switch)

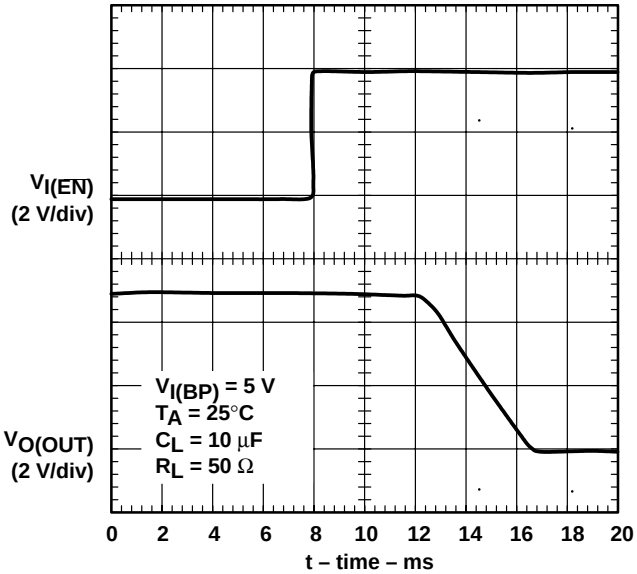


Figure 4. Turnoff Delay and Fall Time (BP Switch)

PARAMETER MEASUREMENT INFORMATION

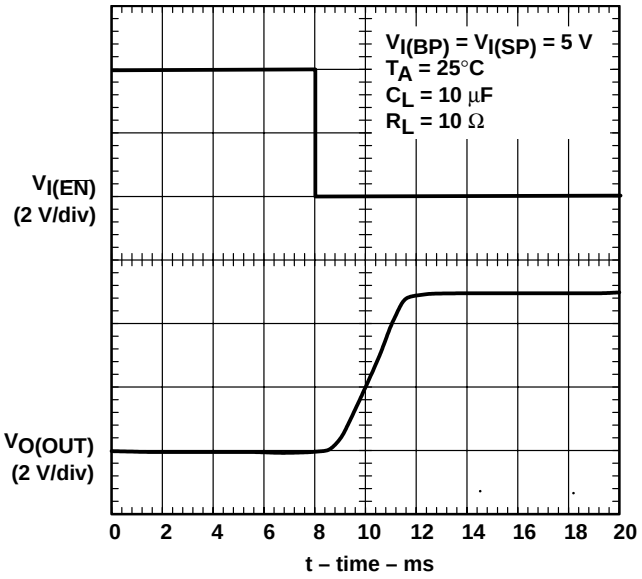


Figure 5. Turnon Delay and Rise Time (SP Switch)

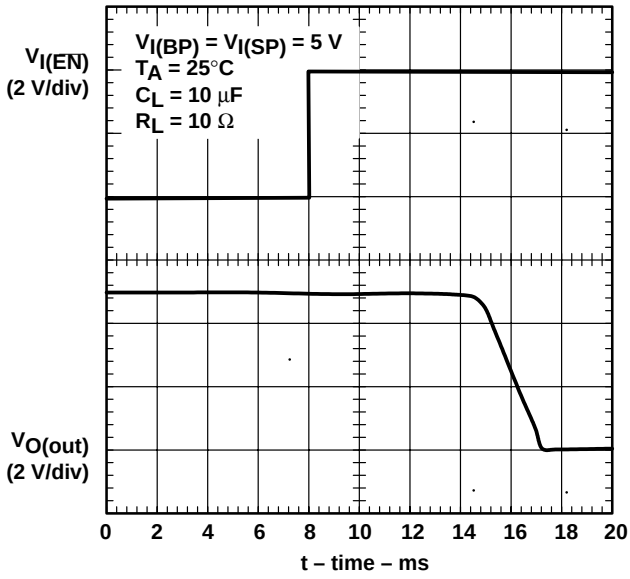


Figure 6. Turnoff Delay and Fall Time (SP Switch)

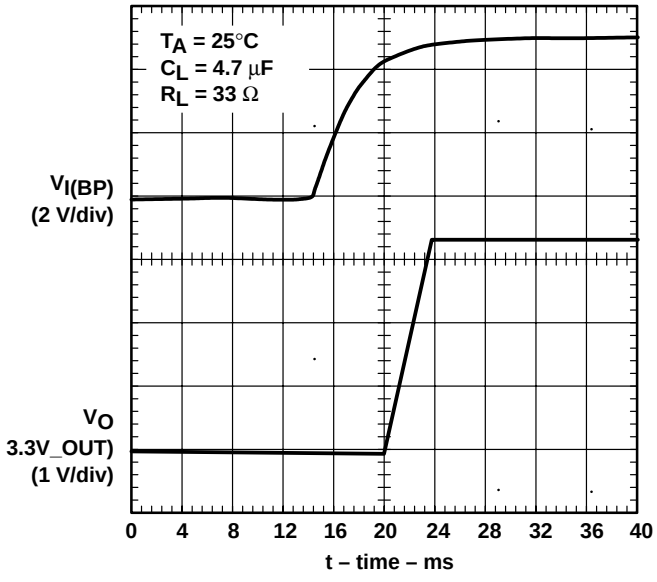


Figure 7. Turnon Delay and Rise Time (3.3V_OUT)

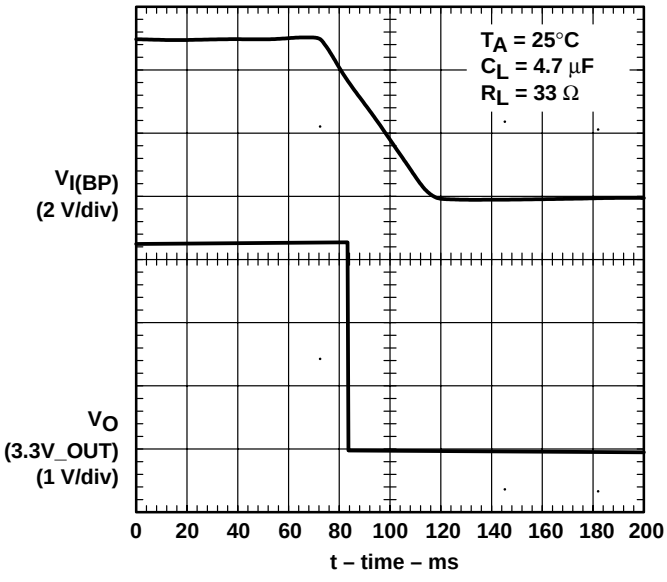


Figure 8. Turnoff Delay and Fall Time (3.3V_OUT)

PARAMETER MEASUREMENT INFORMATION

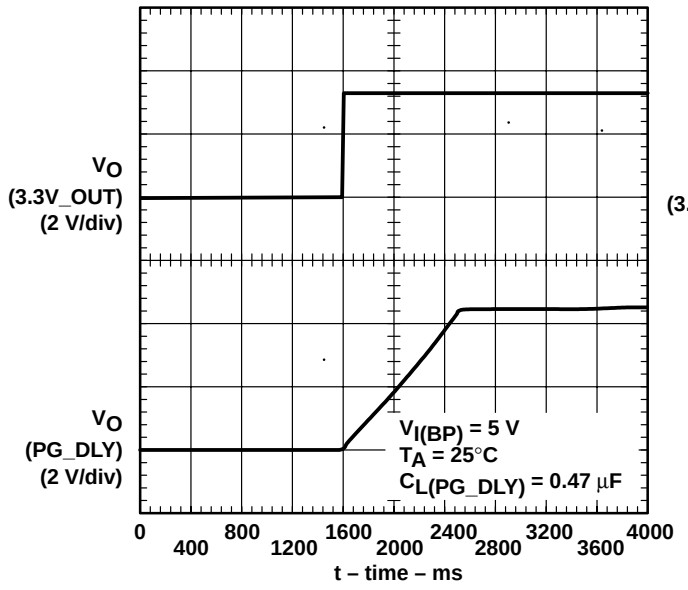


Figure 9. PG_DLY Rise Time With a 0.47-μF Capacitor

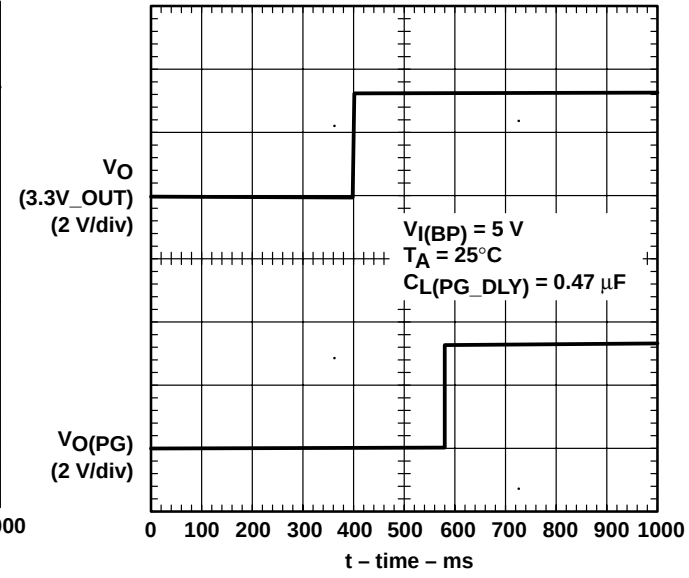


Figure 10. Turnon Delay (3.3V_OUT to PG)

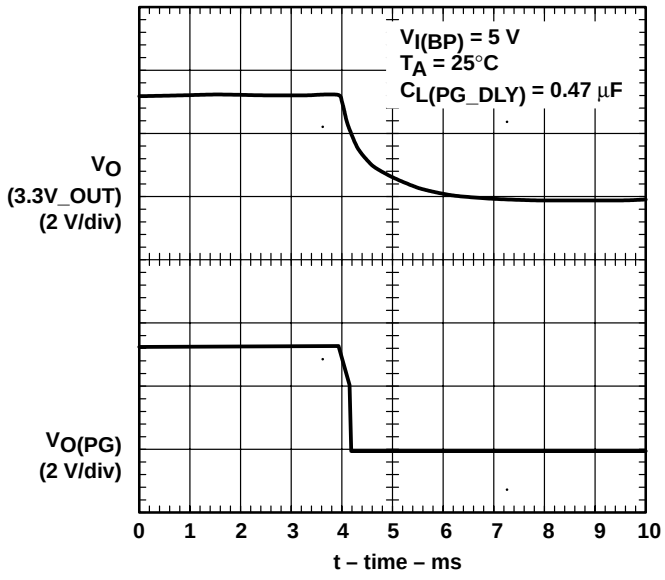


Figure 11. Turnoff Time (3.3V_OUT to PG)

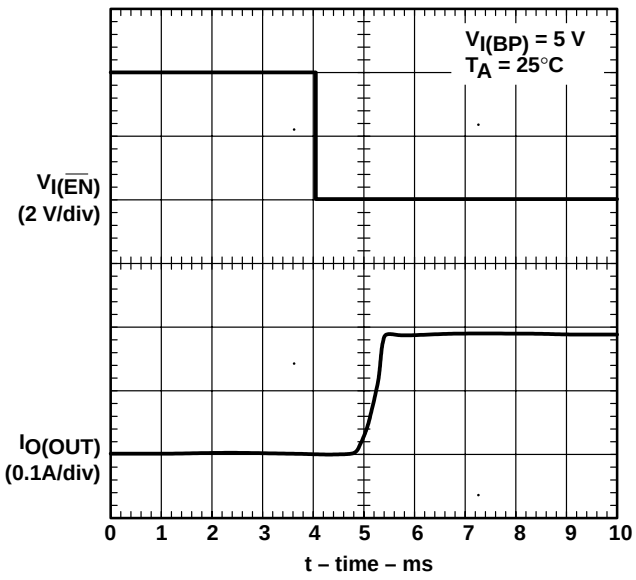


Figure 12. Short-Circuit Current (BP Switch), Device Enabled Into Short

PARAMETER MEASUREMENT INFORMATION

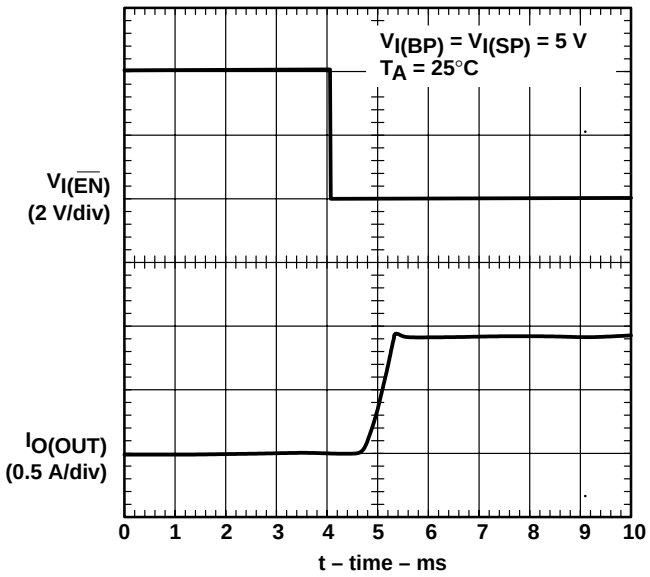


Figure 13. Short-Circuit Current (SP Switch), Device Enabled Into Short

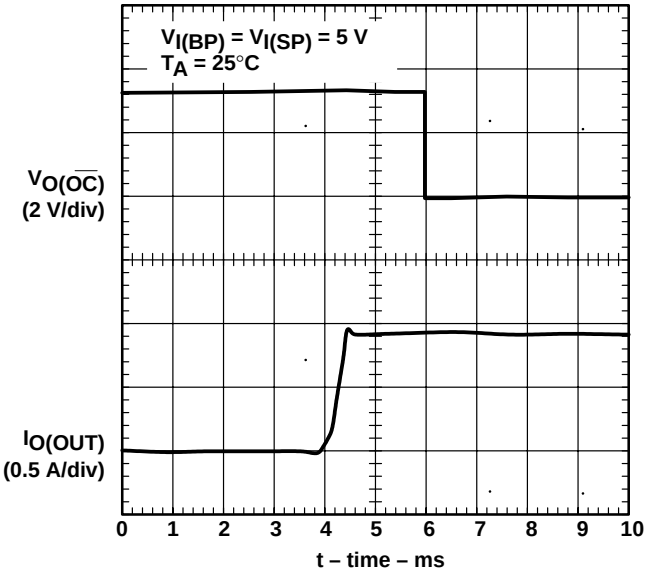


Figure 14. $\overline{OC}$ Response (SP Switch), Device Enabled Into Short

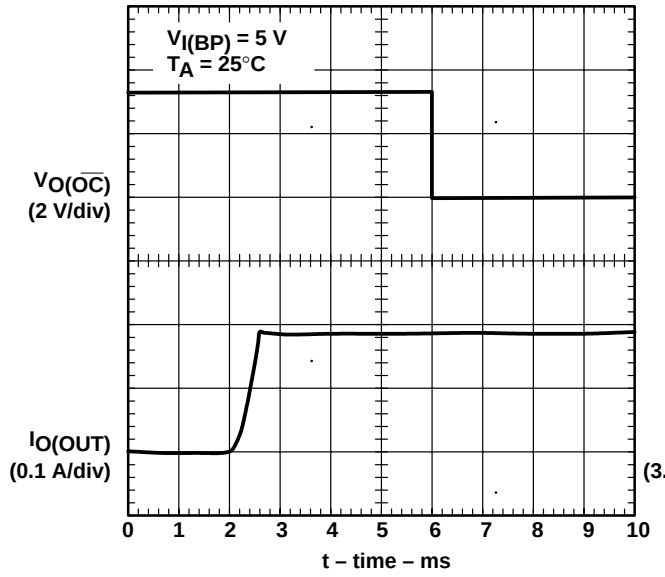


Figure 15. $\overline{OC}$ Response (BP Switch), Device Enabled Into Short

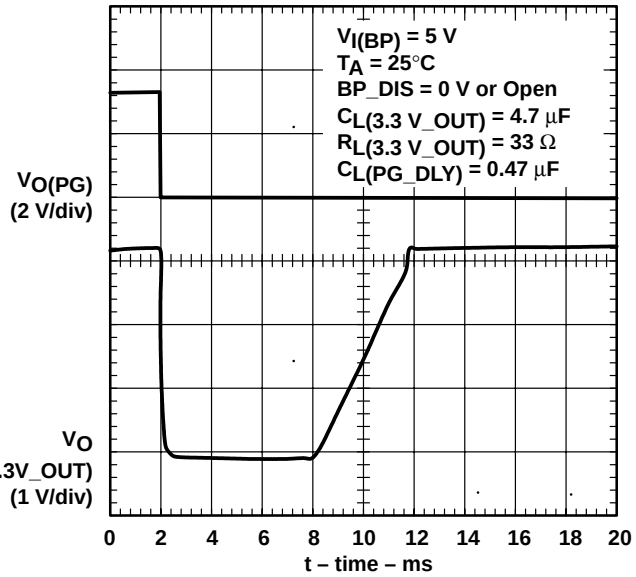


Figure 16. SP to BP Automatic Switchover Enabled

PARAMETER MEASUREMENT INFORMATION

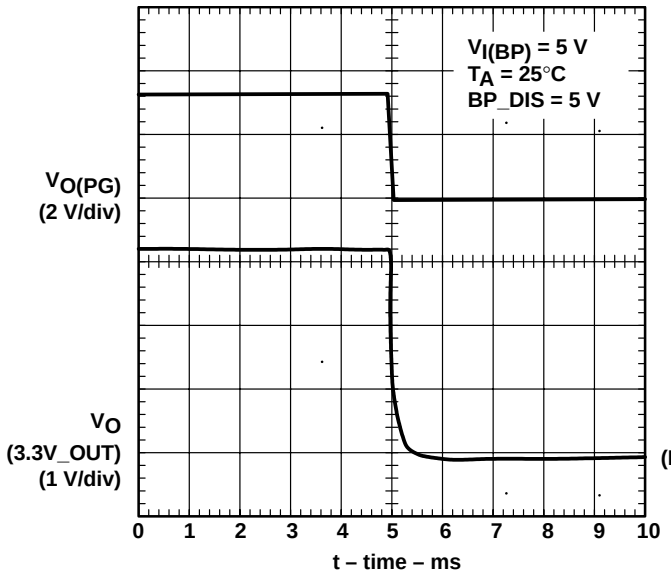


Figure 17. SP to BP Automatic Switchover Disabled

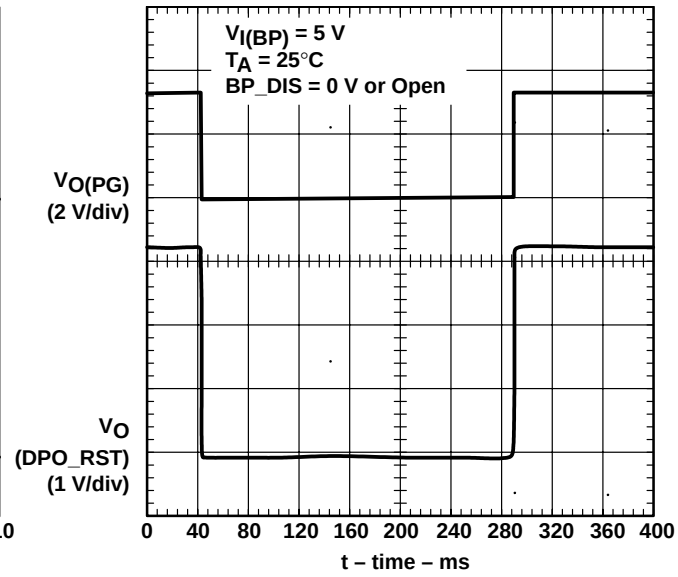


Figure 18. SP to BP Automatic Switchover Enabled

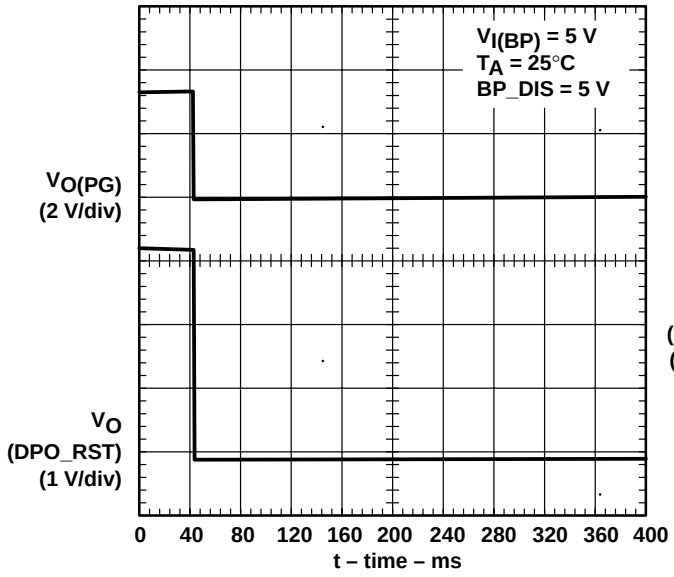


Figure 19. SP to BP Automatic Switchover Disabled

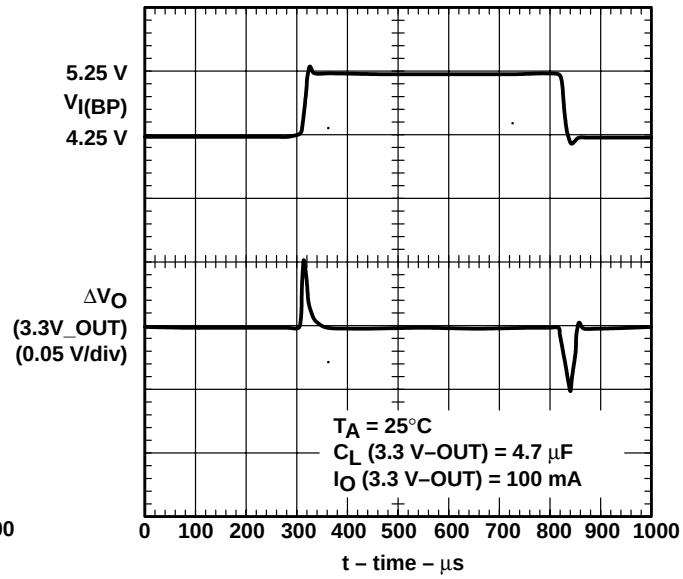


Figure 20. Line Transient Response

PARAMETER MEASUREMENT INFORMATION

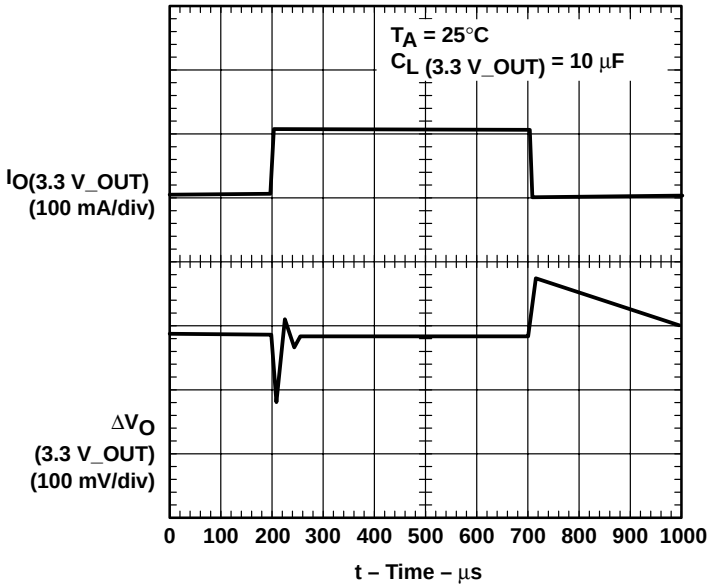


Figure 21. Load Transient Response

TYPICAL CHARACTERISTICS

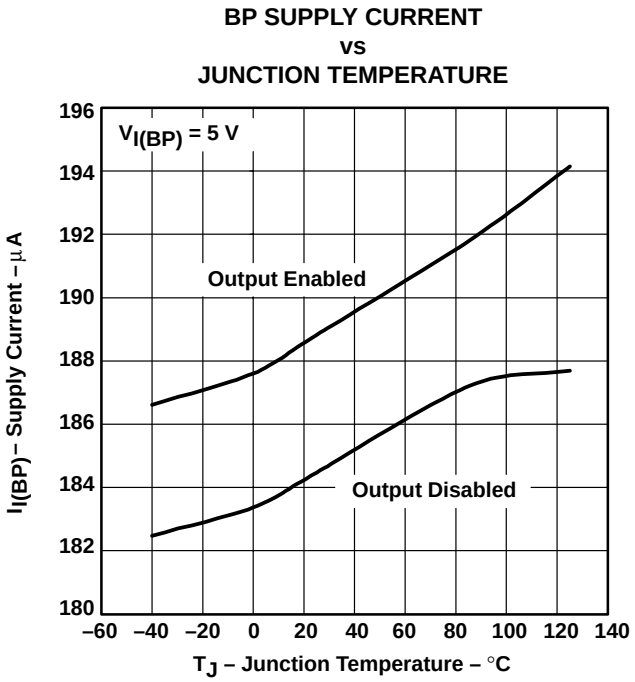


Figure 22

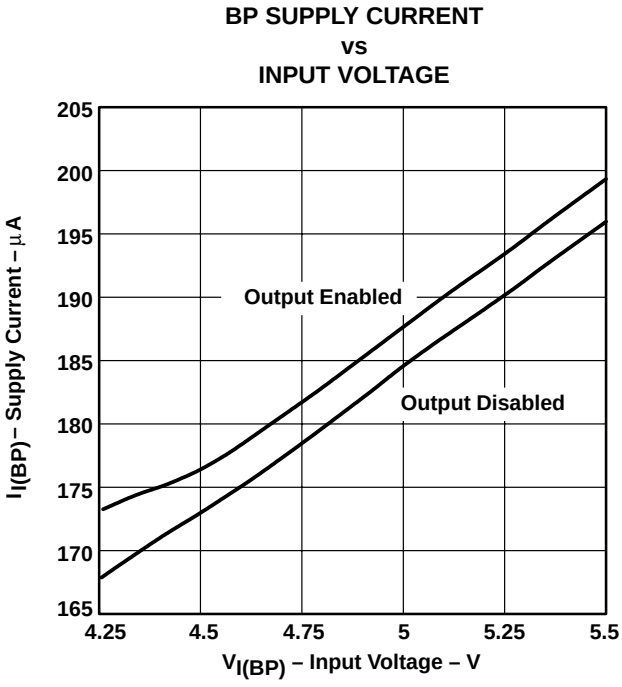


Figure 23

TYPICAL CHARACTERISTICS

SP SUPPLY CURRENT vs JUNCTION TEMPERATURE

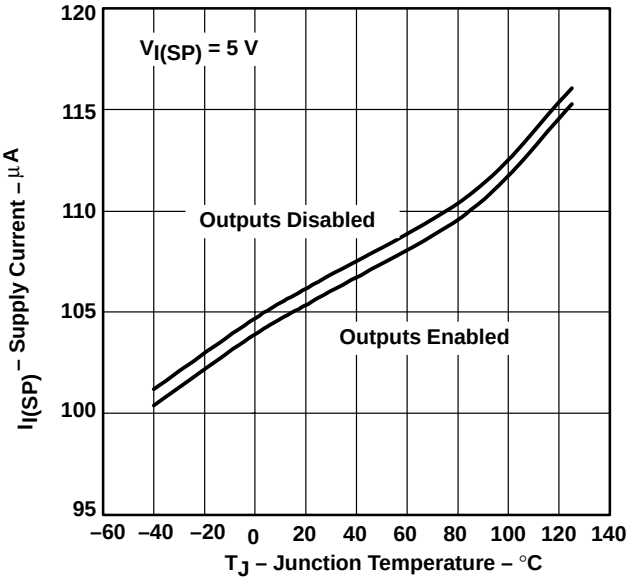


Figure 24

SP SUPPLY CURRENT vs INPUT VOLTAGE

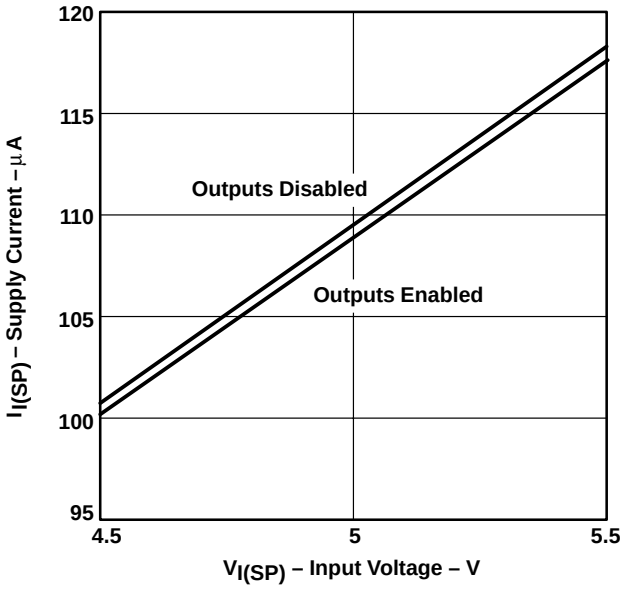


Figure 25

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE (SELF-POWER SWITCHES)

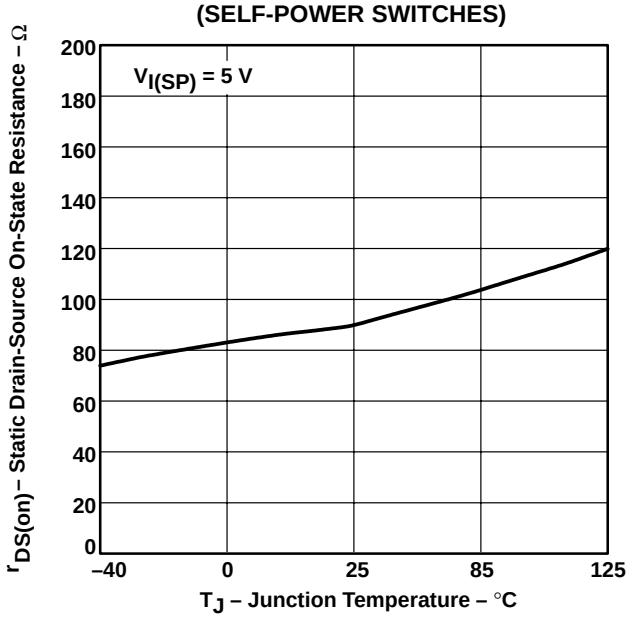


Figure 26

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE (BUS POWER SWITCHES)

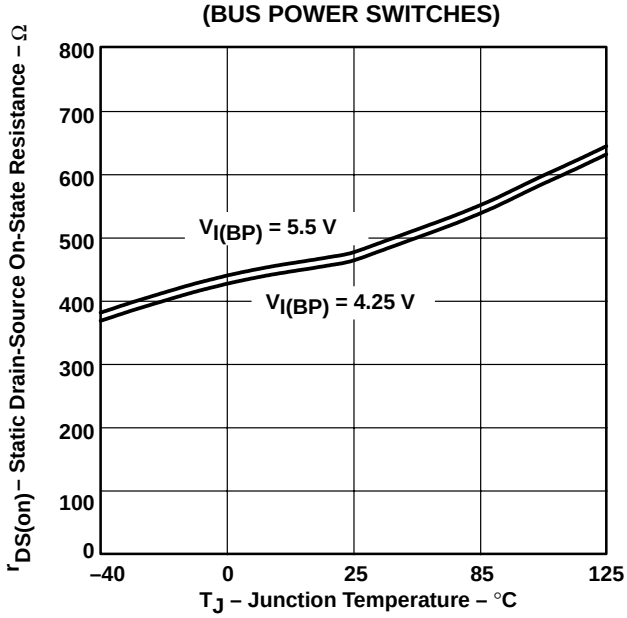


Figure 27

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE (BUS-POWER SWITCHES)

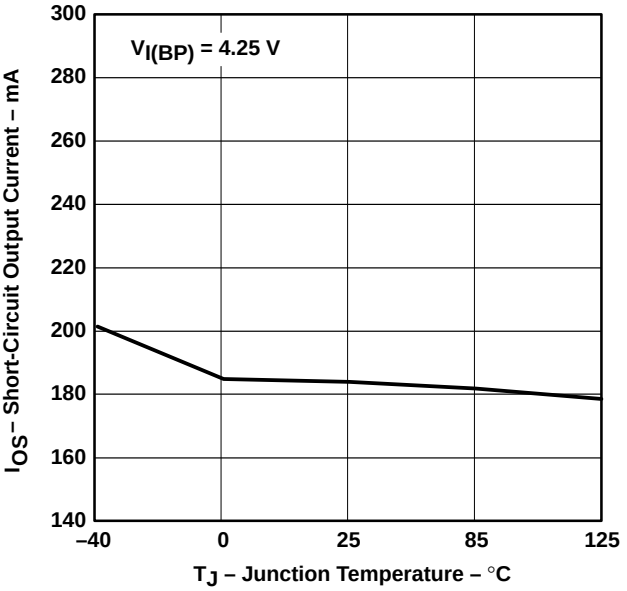


Figure 28

SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE (BUS-POWER SWITCHES)

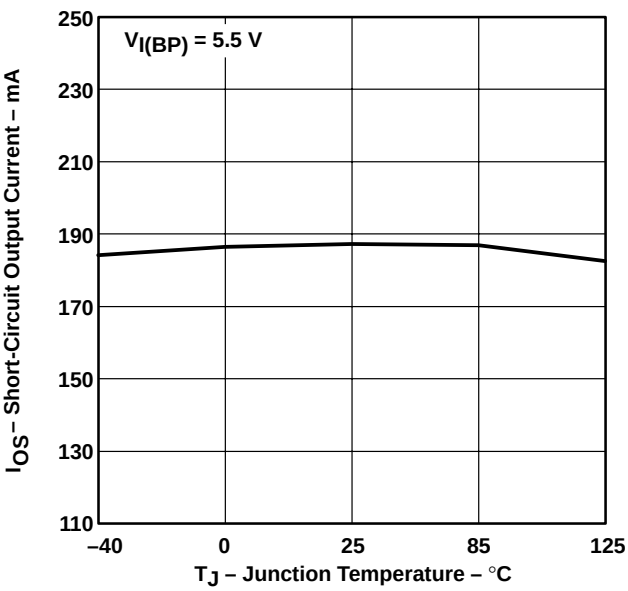


Figure 29

SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE (SELF-POWER SWITCHES)

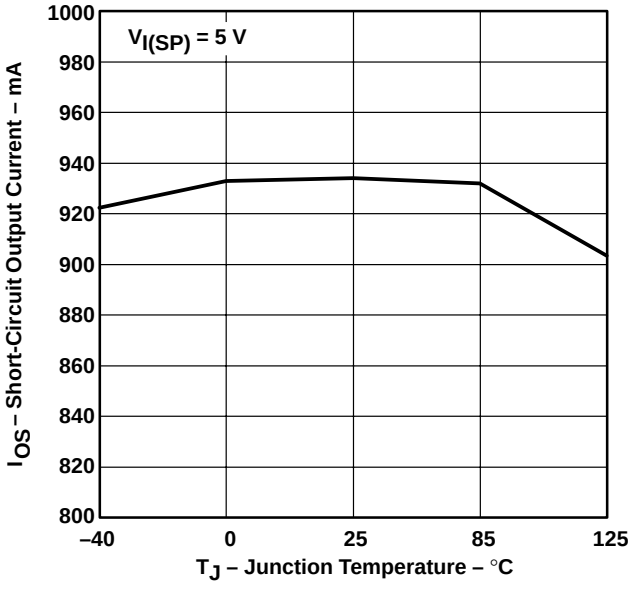


Figure 30

INPUT VOLTAGE (BP UNDERVOLTAGE LOCKOUT) vs JUNCTION TEMPERATURE

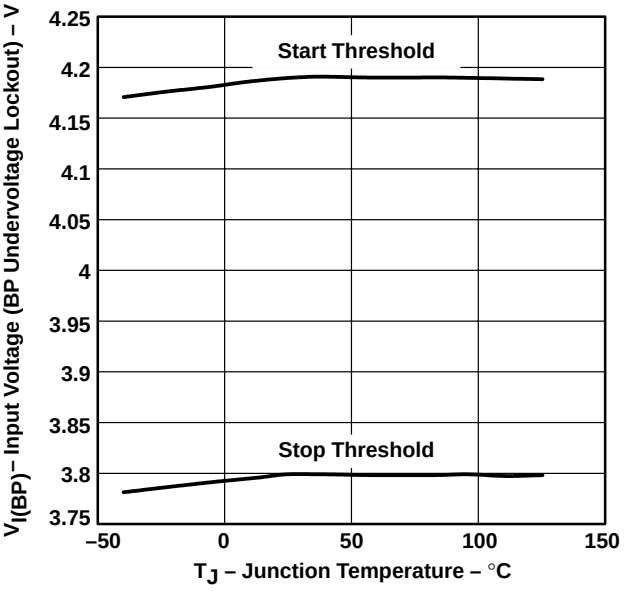


Figure 31

TYPICAL CHARACTERISTICS

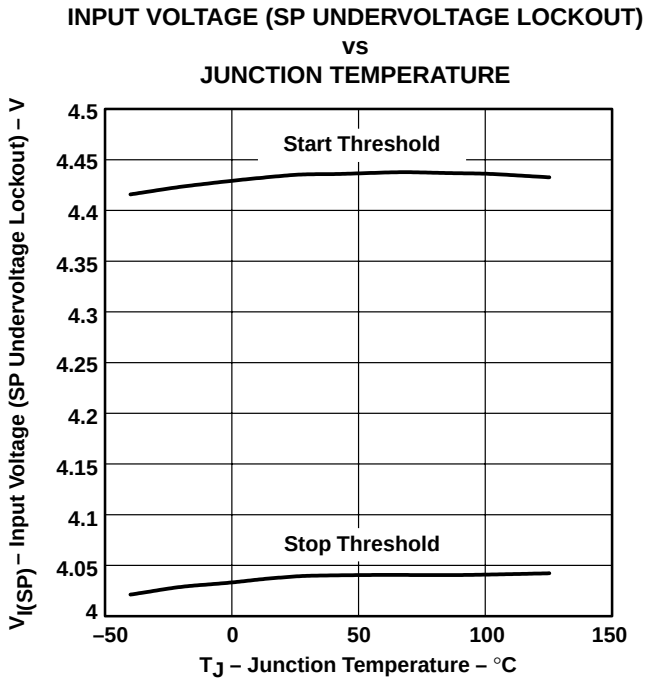


Figure 32

APPLICATION INFORMATION

external capacitor requirements

A 0.1-µF ceramic bypass capacitor and a 10-µF bulk capacitor between BP and AGND, close to the device, are recommended. Similarly, a 0.1-µF ceramic and a 68-µF bulk capacitor, from SP to AGND, and from VEXT to AGND if an external 5-V LDO is required, are recommended because of much higher current in the self-powered mode.

From each of the outputs (OUTx) to ground, a 33-µF or higher valued bulk capacitor is recommended when the output load is heavy. This precaution reduces power-supply transients. Additionally, bypassing the outputs with a 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

An output capacitor connected between 3.3V_OUT and GND is required to stabilize the internal control loop. The internal LDO is designed for a capacitor range of 4.7 µF to 33 µF with an ESR of 0.2 Ω to 10 Ω. Solid tantalum-electrolytic, aluminum-electrolytic, and multilayer ceramic capacitors are all suitable.

Ceramic capacitors have different types of dielectric material, each exhibiting different temperature and voltage variations. The most common types are X5R, X7R, Y5U, Z5U, and NPO. The NPO type ceramic capacitors are generally the most stable over temperature. However, the X5R and X7R are also relatively stable over temperature (with the X7R being the more stable of the two) and are therefore acceptable for use. The Y5U and Z5U types provide high capacitance in a small geometry, but exhibit large variations over temperature. For this reason, the Y5U and Z5U are not generally recommended.

APPLICATION INFORMATION

external capacitor requirements (continued)

A transient condition occurs because of a sudden increase in output current. The output capacitor reduces the transient effect by providing the additional current needed by the load. Depending on the current demand at the output, a voltage drop will occur across the internal resistance, ESR, of the capacitor. Using a low ESR capacitor will help minimize this voltage drop. A larger capacitor will also reduce the voltage drop by supplying the current demand for a longer time, versus that provided by a smaller capacitor.

overcurrent

An internal sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before BP and SP have been applied. The TPS2074 and TPS2075 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a very short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS2074 and TPS2075 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ response

The $\overline{\text{OCx}}$ output is asserted (active low) when an overcurrent or overtemperature condition is encountered and will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device and charging the downstream capacitor. The TPS2074 and TPS2075 are designed to reduce false overcurrent reporting by implementing an internal deglitch circuit. This circuit eliminates the need for an external filter, which requires extra components. Also, using low-ESR electrolytic capacitors on the outputs can reduce erroneous overcurrent reporting by providing a low-impedance energy source to lower the inrush current flow through the device during hot-plug events. The $\overline{\text{OCx}}$ outputs are logic outputs thereby requiring no pullup or pulldown resistors.

APPLICATION INFORMATION

power dissipation and junction temperature

The major source of power dissipation for the TPS2074 and TPS2075 comes from the internal voltage regulator and the N-channel MOSFETs. Checking the power dissipation and junction temperature is always a good design practice. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET according to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the graphs shown under the typical characteristics section of this data sheet. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by four to get the total power dissipation coming from the N-channel MOSFETs.

The power dissipation for the internal voltage regulator is calculated using:

$$P_D = \left(V_{I(BP)} - V_{O(min)}\right) \times I_{O(OUT)}$$

The total power dissipation for the device becomes:

$$P_{D(total)} = P_{D(\text{voltage regulator})} + \left(4 \times P_{D(switch)}\right)$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = ambient temperature °C

$R_{\theta JA}$ = Thermal resistance °C /W, equal to inverting of derating factor found on the power dissipation table in this data sheet.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods. The faults force the TPS2074 and TPS2075 into constant-current mode at first, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels.

The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2074 and TPS2075 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. Once the die temperature rises to approximately 140°C, the internal thermal-sense circuitry determines which power switch is in an overcurrent condition and turns only that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. If the die temperature exceeds the first thermal trip point of 140°C and reaches 150°C, the device turns off. The $\overline{OC}$ output is asserted (active low) when overtemperature or overcurrent occurs.

APPLICATION INFORMATION

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the device (LDO and switches) is in the off state at power up. The UVLO will also keep the device from being turned on until the power supply has reached the start threshold (see undervoltage lockout table), even if the switches are enabled. The UVLO will activate whenever the input voltage falls below the stop threshold as defined in the undervoltage lockout table. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switches before input power is removed. Upon reinsertion, the power switches will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

self-power to bus-power or bus-power to self-power transition

An autoswitching function between bus-powered mode and self-powered mode is a feature of the TPS2074 and TPS2075. When this feature is enabled (BP_DIS is inactive) and SP is removed or applied, a transition will be initiated. The transition sequence begins with the internal LDO being turned off and its external capacitance discharged. Any enabled switches are also turned off and the external capacitors discharged. Once the LDO and switch outputs are low, the internal logic will turn the LDO back on. This entire sequence occurs whenever power to the SP input is removed or applied, regardless of the source of power, i.e., an external power supply or the use of the external regulator.

universal serial bus (USB) applications

The universal serial bus (USB 1.1) interface is a 12-Mb/s, 1.5-Mb/s, or 480 Mb/s (USB 2.0), multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V-level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub or across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2074 and TPS2075 can provide power-distribution solutions for hybrid hubs that need switching between BPH and SPH according to power availability and application requirements.

APPLICATION INFORMATION

USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
  - Output 5.25 V to 4.75 at 500 mA
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
  - Output 5.25 V to 4.4 at 100 mA
  - Not send power back upstream
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA
  - Not send power back upstream (SP functions)

The feature set of the TPS2074 and TPS2075 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the needs of both input and output ports on hubs, as well as the input ports for bus-powered functions

USB hybrid hub

A USB hybrid hub can be simply implemented using the TPS2075 USB power controller and a TUSB2046 USB hub controller as shown in Figure 33. The TPS2075 USB power controller provides all the power needs to the four downstream ports and meets all the USB power specifications for both self-powered hubs and bus-powered hubs. The power controllers integrated 3.3-V LDO is used to provide power for the hub controller and any other local functions (e.g. transient suppressor SN75240), which saves board space and cost. The TPS2075 also provides the hub controller with a power good (PG) signal that connects to the $\overline{\text{RESET}}$ input of the hub controller to automatically reinitialize the hub when switching between self-powered mode and bus-powered mode whenever the self-power supply is connected or disconnected. The amount of time in which the hub controller is kept in a reset state is controlled by a capacitor connected between the PG_DLY pin of the power controller and ground.

APPLICATION INFORMATION

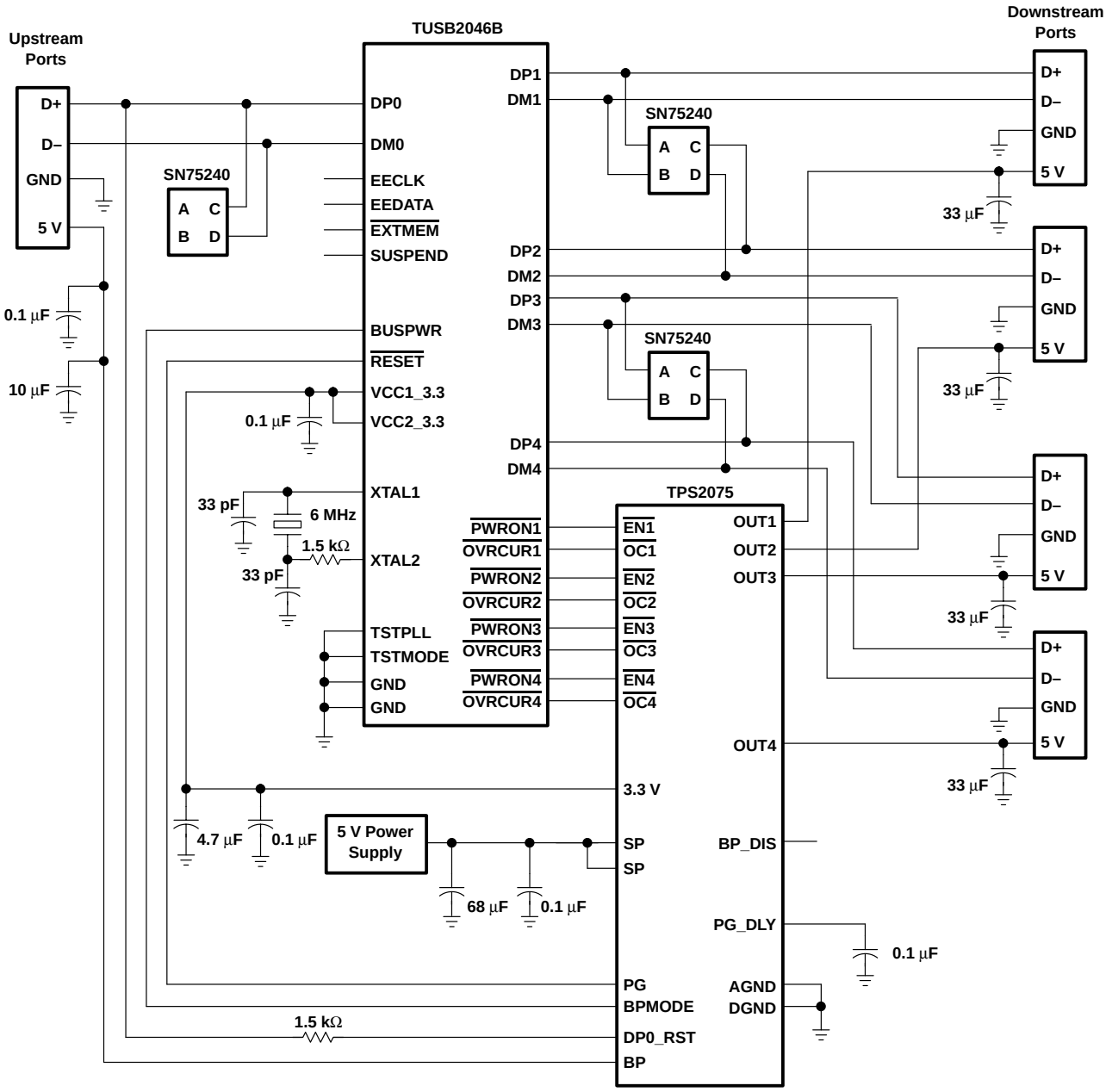
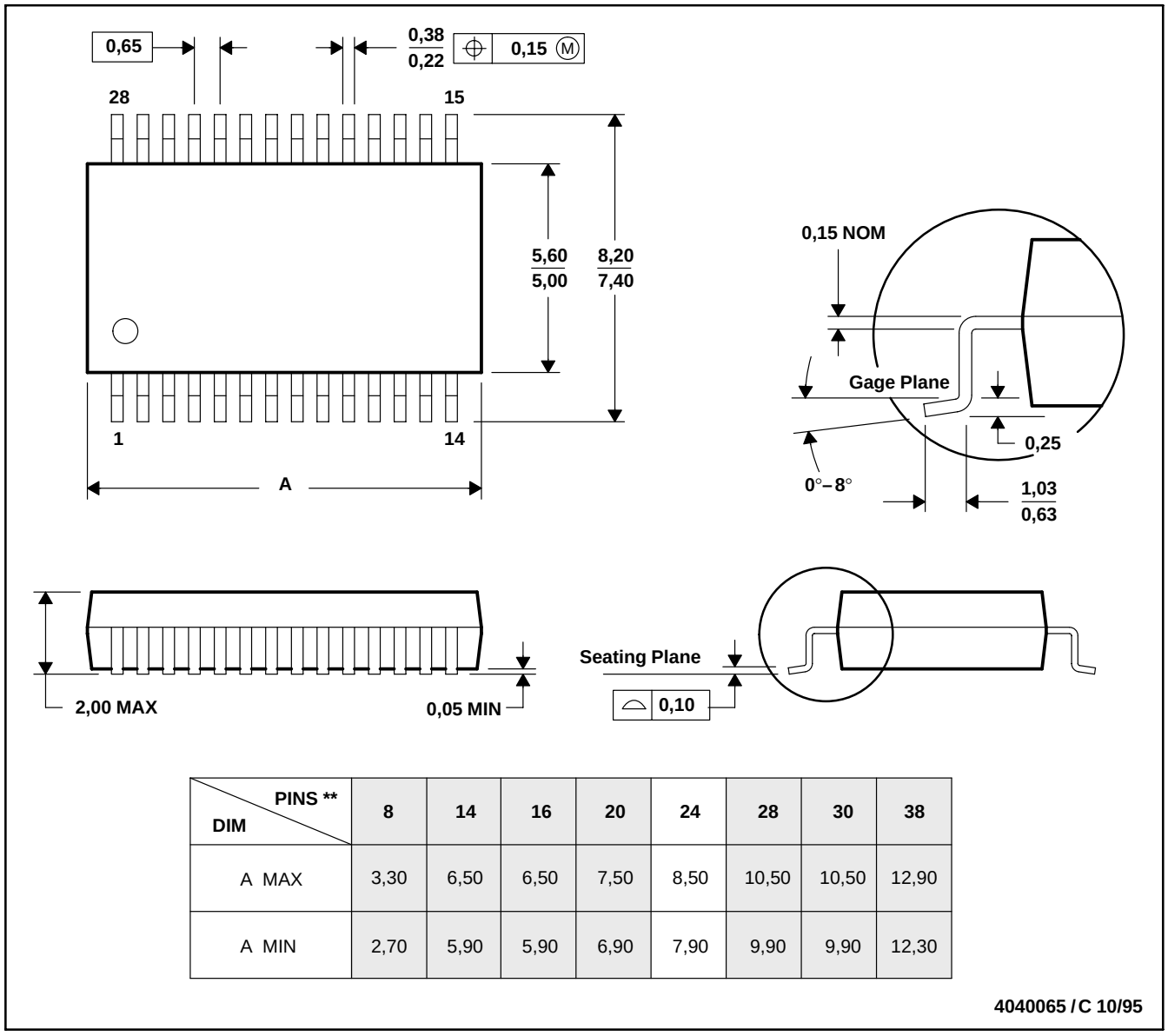


Figure 33. USB Hybrid Hub Using TPS2075 Power Controller and TUSB2046 Hub Controller

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / C 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2074DB	ACTIVE	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS2074	Samples
TPS2075DB	ACTIVE	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS2075	Samples
TPS2075DBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPS2075	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

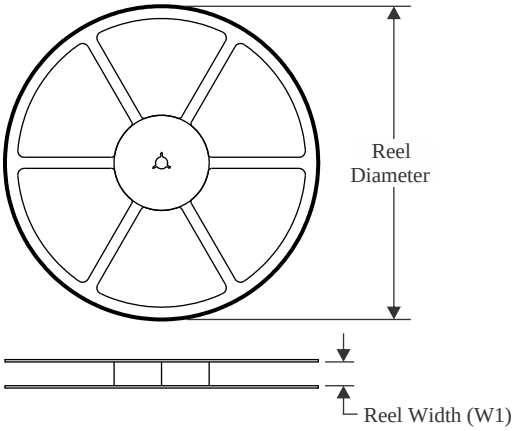
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

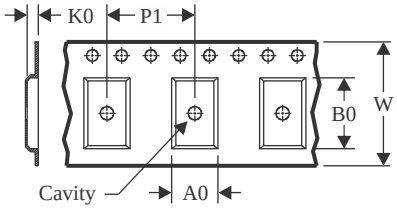
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

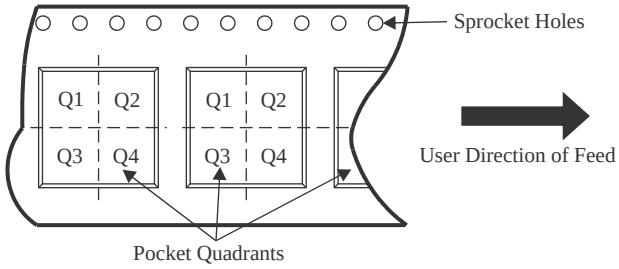


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

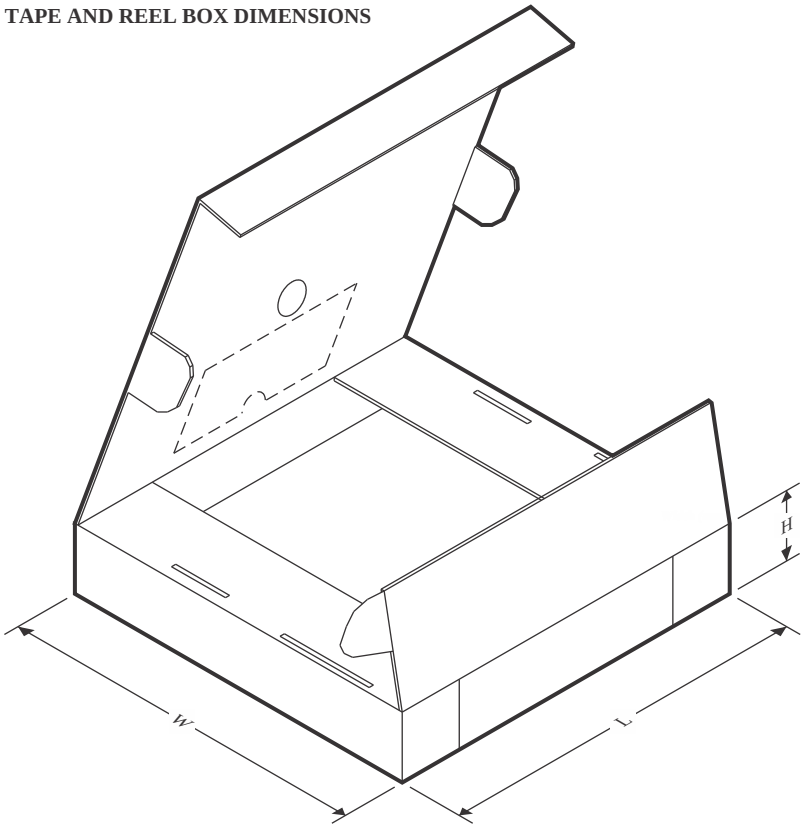
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2075DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1

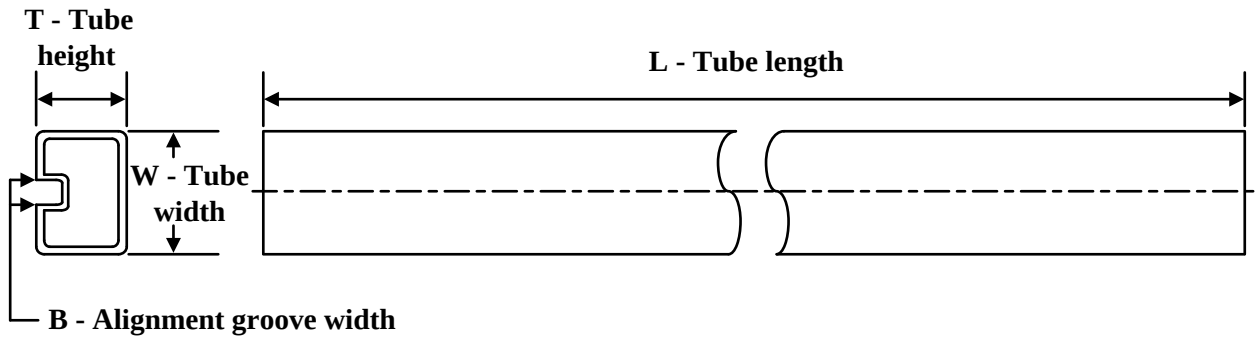
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2075DBR	SSOP	DB	24	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2074DB	DB	SSOP	24	60	530	10.5	4000	4.1
TPS2075DB	DB	SSOP	24	60	530	10.5	4000	4.1

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