AOZ5276QI

High-Current, High-Performance Smart Power Stage

General Description

The AOZ5276QI is a general-purpose Smart Power Stage (SPS) consisting of two asymmetrical MOSFETs and an integrated driver for high current, high frequency DC-DC converters.

The AOZ5276QI provides an output voltage signal (IMON), which represents the real-time module current with a gain of 5mV/A. The IMON signal can be directly used to replace inductor DCR sensing or resistor sensing in multiphase voltage regulator systems without the need for temperature compensation.

The AOZ5276QI also includes an accurate module temperature monitor (TMON). TMON is a voltage sourced signal with a gain of 8mV/°C.

The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High-Side (HS) MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low-Side (LS) MOSFET has ultra-low ON resistance to minimize conduction loss. The standard 5mm x 6mm QFN package is optimally designed to minimize parasitic inductance for minimal EMI signature.

Features

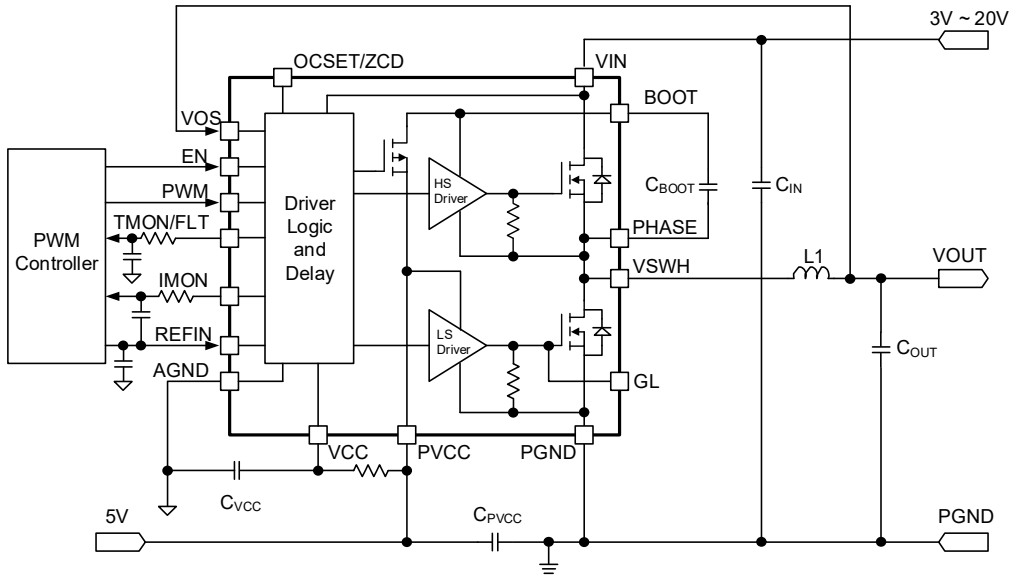
- 3V to 20V power supply range
- 30V HS MOSFET provides better system ruggedness
- 90A continuous output current
  - Up to 100A for 10ms on pulse
  - Up to 150A for 10µs on pulse
- Optimized for switching frequency up to 1MHz
- Integrated current monitor (5mV/A) with 5% accuracy over temperature
- Integrated temperature monitor (8mV/°C) with 2% accuracy
- Fault Indicator
- Under-Voltage LockOut (UVLO) on VCC
- Under-Voltage LockOut (UVLO) on VIN
- High-Side MOSFET Over-Current and Short-Circuit Protection
- Zero Current Detect Function (ZCD)
- Over Temperature Protection (OTP)
- Standard QFN5x6-39L package

Applications

- Server systems
- High end CPU/GPU power stage
- Communications Infrastructure

Green Product

Typical Application Circuit

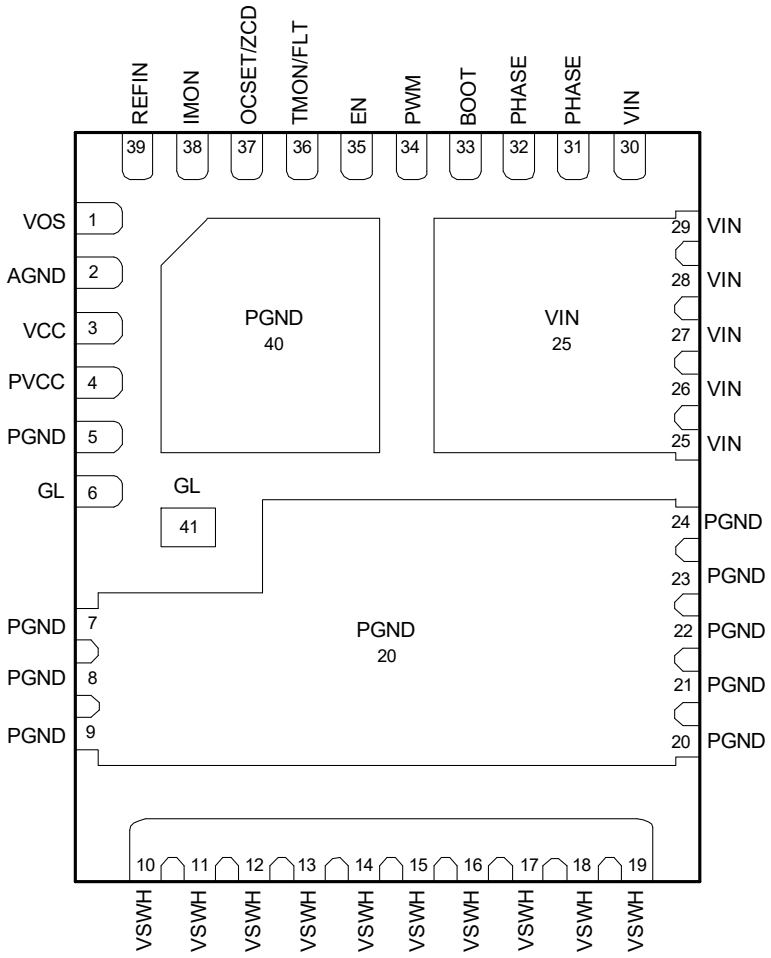


Ordering Information

Part Number	Junction Temperature Range	Package	PreOVP	Environmental
AOZ5276QI	-40°C to 125°C	QFN5x6-39L	Active	RoHS
AOZ5276QI-01	-40°C to 125°C	QFN5x6-39L	Disabled	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

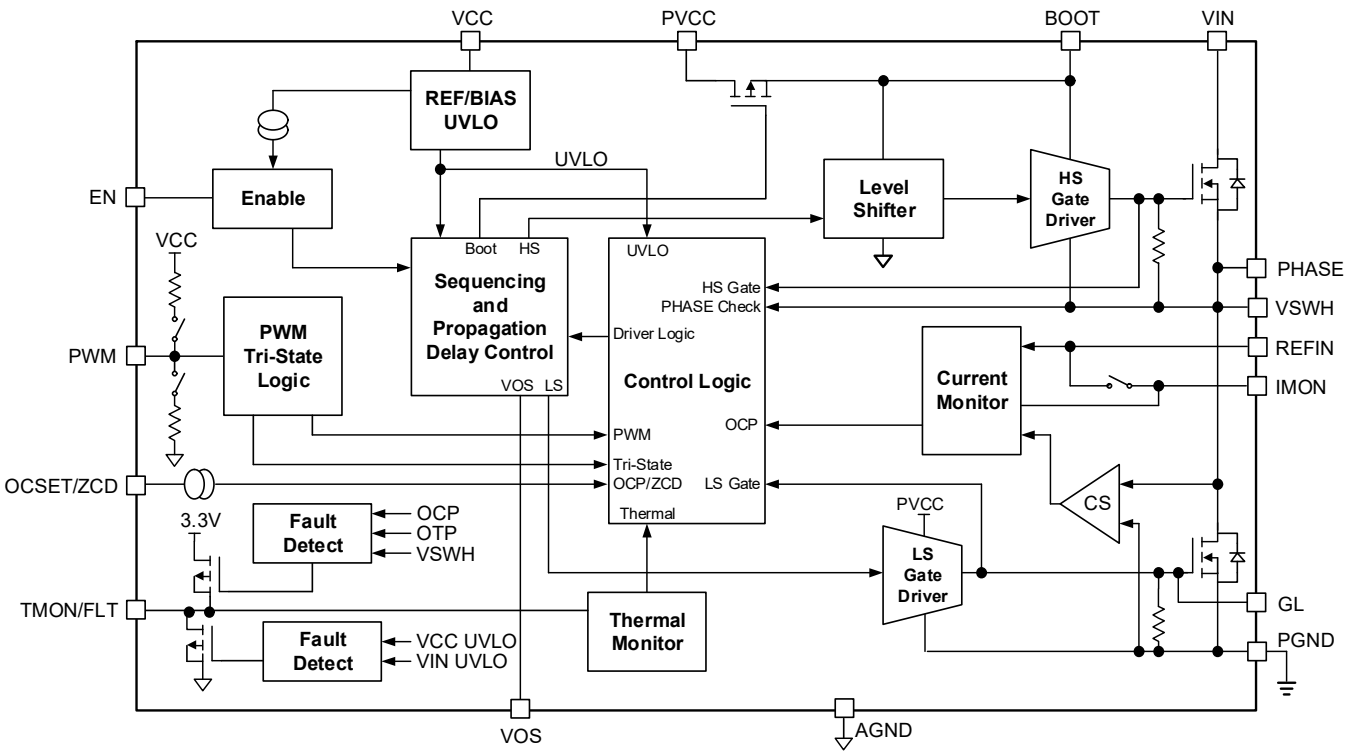


QFN5x6-39L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VOS	Output voltage sense.
2	AGND	Signal Ground.
3	VCC	5 V Bias for Internal Logic Blocks. Ensure to position a 1 µF MLCC directly between VCC and AGND (Pin 2).
4	PVCC	5 V Power Rail for High-Side and Low-Side MOSFET Drivers. Ensure to position a 1 µF MLCC directly between PVCC and PGND (Pin 5).
5, 40	PGND	Power Ground for High-Side and Low-Side MOSFET Gate Drivers. Ensure to connect 1 µF MLCC directly between PGND and PVCC (Pin 4).
6, 41	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
7, 8, 9, 20, 21, 22, 23, 24	PGND	Power Ground pin for power stage (Source connection of Low-Side MOSFET).
10, 11, 12, 13, 14, 15, 16, 17, 18, 19	VSWH	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET.
25, 26, 27, 28, 29, 30	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).
31, 32	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 33).
33	BOOT	High-Side MOSFET Gate Driver supply rail. Connect a 100 nF ceramic capacitor between BOOT and the PHASE (Pin 31 and 32).
34	PWM	PWM input signal from Controller IC. This input is compatible with 3.3V and 5V Tri-State logic levels.
35	EN	Output enable pin. When this pin is pulled to a logic low level, the IC disables most blocks. EN=HIGH enables all blocks inside IC and requires 4 µs power up time.
36	TMON/FLT	Temperature Monitor and Fault Flag Pin. TMON/FLT will be pulled HI (~ 3.3 V) or LOW (0 V) to indicate a fault condition (see Table 5). For multi-phase application, the TMON/FLT pin can be connected together as a common bus. The highest voltage representing the highest temperature among all phases will be sent to the PWM controller. No more than 470 pF total capacitance can be directly connected across TMON/FLT and AGND (Pin 2). A higher capacitance load is allowed with a series resistor (~ 1 kΩ) for up to 1 nF. At 0 °C and in normal operation, the output voltage is 0.6 V with a temperature coefficient value of 8 mV/°C. There is an internal pull up source to 3.3V when a fault condition occurs.
37	OCSET/ZCD	Setting control for OCP limit threshold and Zero Cross Detect function (ZCD). OCP limit threshold is detected and latched 120 µs after device enabled. Refer to Table 3 for the resistor value for each current limit threshold level. After 120 µs, the OCP limit is set and this pin becomes ZCD control only. ZCD is active when this pin is floating or pulled HI.
38	IMON	Current Monitor output signal referenced to REFIN (Pin 39). Connect the IMON output to the appropriate Current Sense input of the controller. No more than 47 pF capacitance can be directly connected across IMON and REFIN pins. With a 100 Ω series resistor, up to 470 pF may be used.
39	REFIN	Input for external reference voltage for IMON (Pin 38). This voltage should be between 0.7 V and 2.0 V. Nominal value is 1.2 V. Place a low ESR ceramic capacitor (~ 0.1 µF) from this pin to AGND (Pin 2). Connect REFIN to the appropriate Current Sense Reference output from the controller.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC, PVCC)	-0.3V to 6V
High Voltage Supply (VIN)	-0.3V to 25V
Control Inputs (PWM, EN, REFIN, OCSET/ZCD, VOS)	-0.3V to (VCC+0.3V)
Output (TMON/FLT, IMON)	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 31V
Bootstrap Voltage Transient(1) (BOOT-PGND)	-8V to 40V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3V to 6V
BOOT Voltage Transient(1) (BOOT-PHASE/VSWH)	-0.3V to 9V
Switch Node Voltage DC (PHASE/VSWH)	-0.3V to 25V
Switch Node Voltage Transient(1) (PHASE/VSWH)	-8V to 33V
Low-Side Gate Voltage DC (GL)	(PGND-0.3V) to (PVCC+0.3V)
Low-Side Gate Voltage Transient(2) (GL)	(PGND-2.5V) to (PVCC+0.3V)
VSWH Current DC	90A
VSWH Current 10ms Pulse	100A
VSWH Current 10µs Pulse	150A
Storage Temperature (T_S)	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
ESD Rating(3)	±2kV HBM ±1 kV CDM

Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Peak voltages can be applied for 20ns per switching cycle.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	3V to 20V
Low Voltage/ MOSFET Driver Supply (VCC, PVCC)	4.5V to 5.5V
Control Inputs (PWM, EN, OCSET/ZCD, VOS)	0V to VCC
Output (TMON/FLT, IMON)	0V to 3.3V
Control Inputs (REFIN)	0.7V to 2.0V
Operating Frequency	200 kHz to 1MHz

Electrical Characteristics[4]

T_J = 25 °C to 125 °C. Typical values reflect 25°C junction temperature; VIN = 12V, VCC = PVCC = EN = 5V, unless otherwise specified. Min/Max values are guaranteed by test, design, or statistical correlation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
V_{IN}	Power Stage Power Supply		3		20	V
V_{CC}	Low Voltage Bias Supply	PVCC = VCC	4.5		5.5	V
$R_{\theta JC}$[5]	Thermal Resistance	PCB Temp = 100 °C		1.8		°C/W
$R_{\theta JA}$[5]		Fsw=600 kHz, V_{OUT}=1 V		12.5		°C/W
Input Supply and UVLO						
V_{CC_UVLO}	VCC Under-Voltage Lockout	VCC Rising	3.4	3.8	4.2	V
V_{CC_HYST}		VCC Hysteresis		400		mV
t_{VCC_DEL}	VCC Power On Delay	From VCC UVLO release			200	µs
V_{IN_UVLO}	VIN Under-Voltage Lockout	VIN Rising	2.2	2.4	2.6	V
V_{IN_HYST}	VIN Hysteresis			400		mV
I_{VCC}	Control Circuit Bias Current	EN=0V, PWM= Floating		600	800	µA
		EN=5V, PWM= Floating		5	7	mA
I_{PVCC}	Drive Circuit Operating Current	PWM = 300kHz, 20% Duty Cycle		15		mA
		PWM = 600kHz, 20% Duty Cycle		30		mA
PWM Input						
V_{PWM_H}	Logic High Input Voltage				2.7	V
V_{PWM_L}	Logic Low Input Voltage		0.65			V
R_{PWM_DOWN}	PWM Pin Input Resistance	Pull Down		10		kΩ
R_{PWM_UP}		Pull Up		23		kΩ
V_{TRI}	PWM Tri-State Window		1.1		2.1	V
V_{PMW_FLOAT}	PWM Tri-State Voltage Clamp	PWM = Floating		1.5		V
t_{PMW_SKIP}	Minimum PWM Pulse Detection				10	ns
t_{PWMH_MIN}	Forced Minimum On Pulse			30		ns
t_{PWML_SKIP}	Forced Minimum Off Pulse			50		ns
EN Input						
V_{EN_ON}	Output Enable Threshold				2.4	V
V_{EN_OFF}	Output Disable Threshold		0.8			V
R_{EN}	EN Input Resistance	Pull-Down Resistor		100		kΩ
t_{PD_ENH}	Propagation Delay for EN: L → H	PWM= GND, Delay from EN (L → H) to GL (L → H)		30		µs
t_{PD_ENL}	Propagation Delay for EN: H → L	PWM=GND, Delay from EN (H → L) to GL (H → L)		50		ns
Gate Driver Timing						
t_{PDLU}	PWM to High-Side Gate	PWM: H→L, VSWH: H→L		25		ns
t_{PDLL}	PWM to Low-Side Gate	PWM: L→ H, GL: H→ L		25		ns
t_{PDHU}	Low-side to High-Side Gate Deadtime	GL: H→ L, GH[6]: L→ H		10		ns
t_{PDHL}	High-Side to Low-side Gate Deadtime	VSWH: H → 1V, GL: L → H		10		ns
t_{TSSHD}	Tri-State Shutdown Delay	PWM: L → V_{TRI}, GL: H → L and PWM: H → V_{TRI}, VSWH: H → L	40		80	ns
t_{TSEXIT}	Tri-State Propagation Delay	PWM: V_{TRI} → H, VSWH: L → H PWM: V_{TRI} → L, GL: L → H			30	ns
t_{LGMIN}	Low-Side Minimum On-Time	ZCD enables		150		ns

Electrical Characteristics[4]

T_J = 25°C to 125°C. Typical values reflect 25°C junction temperature; VIN = 12V, VCC = PVCC = EN = 5V, unless otherwise specified. Min/Max values are guaranteed by test, design, or statistical correlation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IMON Timing and Operating Range						
t_{FALL_BLK}	VSWH Falling Blanking Time			250		ns
t_{PRO_DEL}	IMON to IL Propagation Delay	L=150nH, Freq=600kHz, VOUT=1.8VIMON Valley to IL Valley		60	75	ns
BW_{IMON}	IMON Gain Bandwidth		5	7.5		MHz
V_{REFIN}	REFIN Voltage Range		0.7	1.2	2.0	V
V_{IMON}	IMON Voltage Range		0.3		3	V
C_{IMON}	Max IMON Output Capacitance Allowed	Across IMON and REFIN	10		47	pF
		With 100Ω resistor in series			470	pF
IMON Accuracy						
A_{IMON}	IMON Gain			5		mV/A
V_{IMON_ACC}	IMON Accuracy	-20A ≤ I_{OUT} ≤ 20A	-1		1	A
		20A ≤ I_{OUT} ≤ 60A	-5		5	%
Zero Cross Detect Threshold (When OCSET/ZCD = Open)						
I_{ZCD_OFS}	ZCD Current Threshold Offset	PWM=0V		2		A
I_{ZCD_BLK}	ZCD Blanking Time	PWM=0V		300		ns
TMON Operating Range and Over-Temperature Threshold						
A_{TMON_SLP}	TMON Slope Gain	No Load	7.8	8	8.2	mV/°C
V_{TMON_25C}	TMON Voltage at 25°C	$V(T_{JCT})$=0.6 V + (8mV x T_{JCT})	0.776	0.8	0.824	V
V_{TMON_125C}	TMON Voltage at 125°C	$V(T_{JCT})$=0.6 V + (8mV x T_{JCT})	1.56	1.6	1.64	V
I_{TMON_SOUR}	TMON Sourcing Current	TMON = 0V		800		µA
I_{TMON_SINK}	TMON Sinking Current	TMON = 3.3V		90		µA
T_{OTP}	Over-Temperature Threshold	Temperature Rising	135	140	145	°C
T_{OTP_HYST}	Over-Temperature Hysteresis			15		°C
Current Limit and Low Side Negative Current Limit						
t_{OCP_SETUP}	Current Limit Threshold Setup Time to Latch after the IC power-up			120		µs
I_{LIM_DEF}	Default Current Limit	R_{OCSET}=Open		120		A
I_{LIM_1}	Current Limit 1	R_{OCSET}= 80kΩ. See Table 3		100		A
I_{LIM_2}	Current Limit 2	R_{OCSET}= 25kΩ. See Table 3		85		A
I_{LIM_HYS}	OCP Hysteresis			10		A
N_{OC_COUNT}	OC Counts before Reporting Fault and HS Latches Off			9		counts
I_{NEG_OCP}	Negative OCP Threshold	Negative Turbo Mode		-60		A
Fault Output Indicator						
$I_{TMON/FLT}$	TMON/FLT Output Current at Fault Conditions	TMON = 2.5V		10		mA
$I_{TMON/FLT}$	TMON/FLT Fault Report Time				100	ns
Preliminary Over-Voltage Protection (AOZ5276 Only)						
V_{POVP}	Over-Voltage Protection Threshold			2.8		V

Notes:

4. All voltages are specified with respect to the corresponding AGND pin.
5. Characterization value. Not tested in production.
6. GH is an internal pin.

Timing Diagram

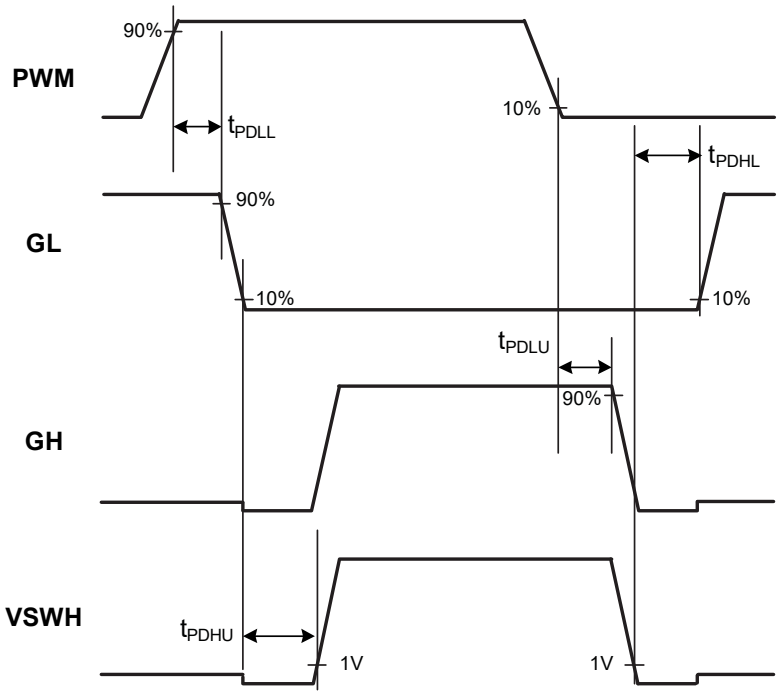


Figure 1. PWM Logic Input Timing Diagram

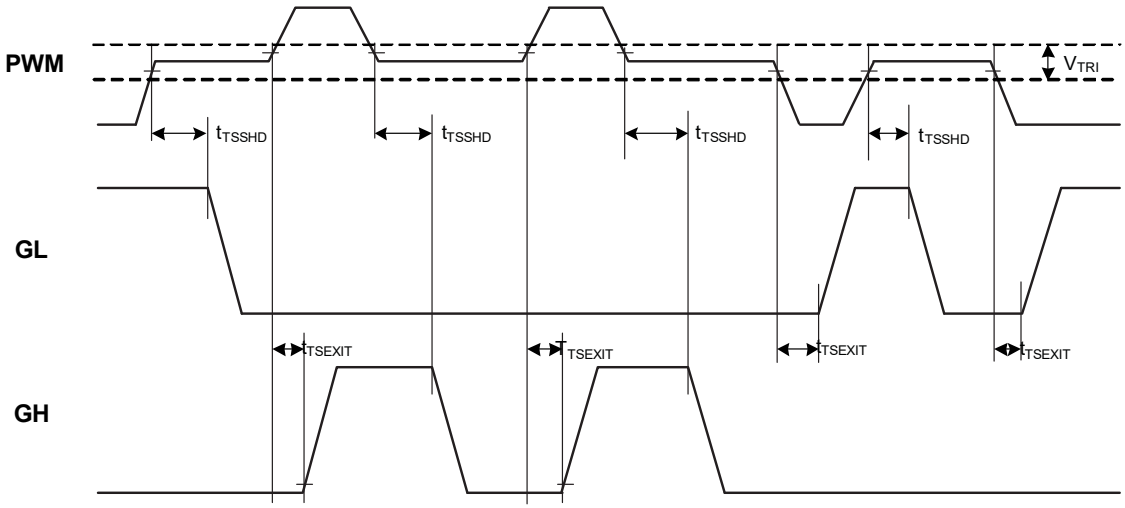


Figure 2. PWM Tri-State Hold Off and Exit Timing Diagram

Typical Performance Characteristics

T_A = 25°C, VIN = 12V, vOUT = 1V, VCC = PVCC = EN = 5V, unless otherwise specified.

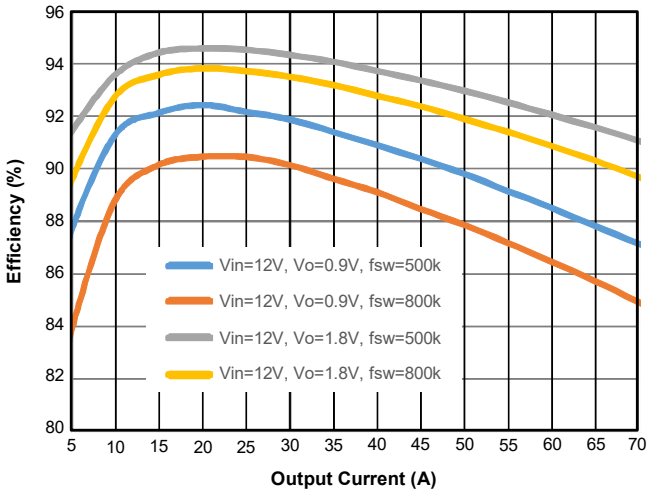


Figure 3. Efficiency vs. Output Current

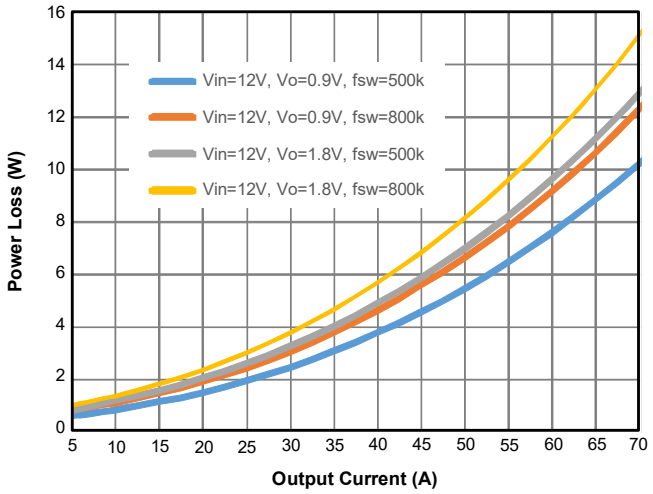


Figure 4. Power Loss vs. Output Current

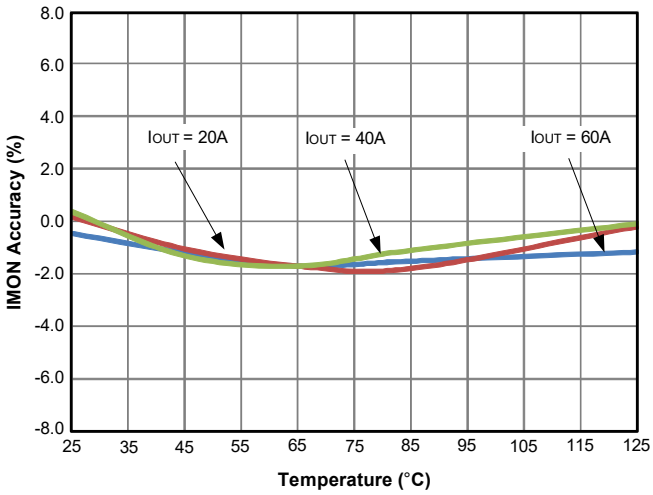


Figure 5. IMON Accuracy (I_{VCC}) vs. Temperature

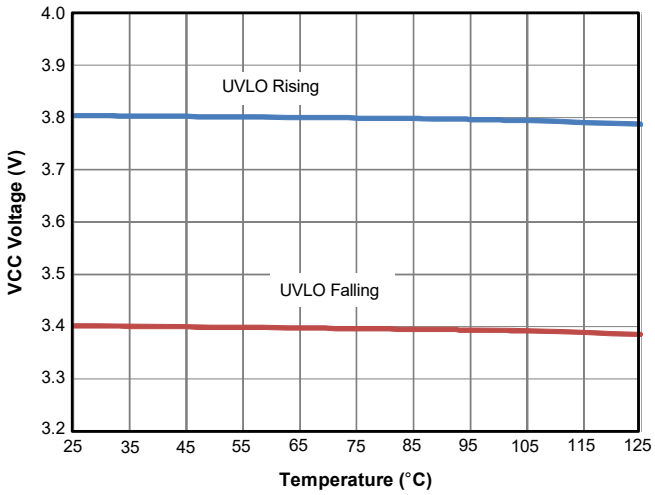


Figure 6. UVLO (VCC) Threshold vs. Temperature

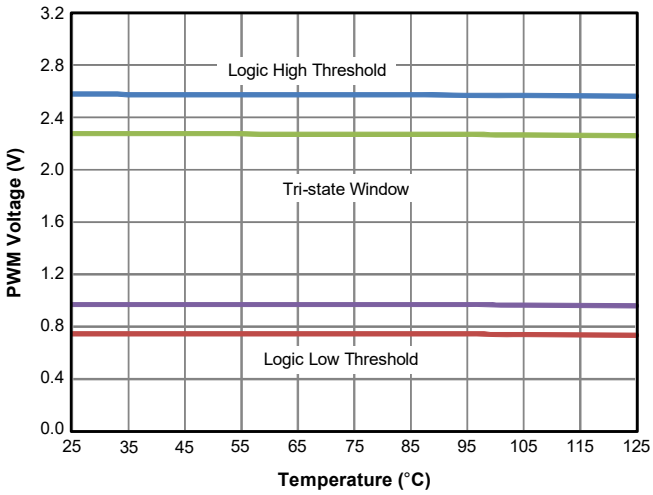


Figure 7. PWM Threshold vs. Temperature

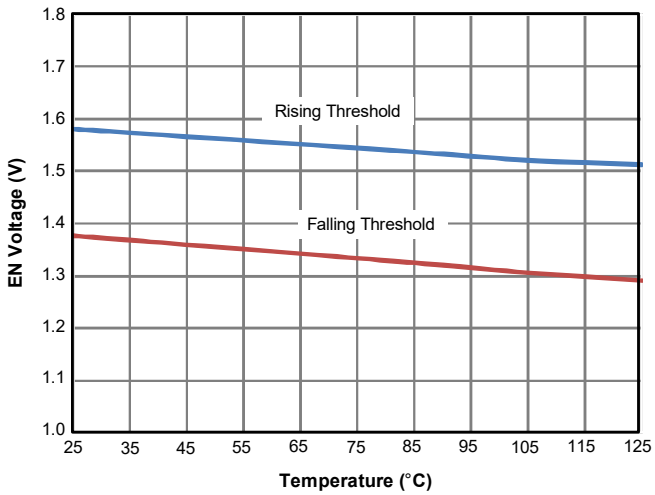


Figure 8. EN Threshold vs. Temperature

Application Information

AOZ5276QI is a fully integrated smart power module designed to work over an input voltage range of 3V to 20V with 5V supplies for gate drive and internal control circuits.This smart power stage module features accurate current monitoring (IMON) which provides both High-Side and Low-Side MOSFET current information in both constant current and diode emulated mode operation. It also features temperature monitoring (TMON) which provides continuous thermal reading of the module temperature. Additional features such as, Power Input (VIN) Under-Voltage Lock-Out (UVLO), Control Circuit Input Voltage (VCC) UVLO, and light load efficiency control. A bootstrap capacitor "auto-refresh" feature ensures the boot capacitor is sufficiently charged before the High-Side MOSFET is being turned on.

The High-Side and Low-Side MOSFETs are combined into a single package with the pin configuration optimized for power routing with minimum parasitic inductance. The MOSFETs are individually tailored for efficient operation in low duty cycle synchronous buck converter applications. In addition, a high current driver is also included in the package to minimize the gate drive loop delay resulting in extremely fast switching.

Powering the Module and the Gate Drives

An external 5V supply (PVCC) is required for driving the MOSFETs. The MOSFETs are designed with low gate thresholds so that lower drive voltage can be used to reduce the switching and drive losses without compromising the conduction losses. The integrated gate driver is capable of supplying high peak current into the gate of Low-Side MOSFET to achieve extremely fast switching. A ceramic bypass capacitor of 1µF or higher is recommended from PVCC to PGND. For effective filtering it is strongly recommended to have a direct connection from this capacitor to PGND.

The bootstrap supply for driving the High-Side MOSFET is generated by connecting a small capacitor between BOOT pin and the switching node (PHASE). It is recommended that this capacitor *Cboot* should be connected as close as possible to the device across PHASE (Pin 32) and BOOT (Pin 33). Pin 31 (PHASE) connection is optional as Pin 32 connection is sufficient. *Rboot* is an optional external resistor that can be used by designers to slow down the turn-on speed of the High-Side MOSFET. Selecting the *Rboot* value is a compromise between switching speed and the amplitude of power switching node (VSWH) voltage spikes. Typical values of *Rboot* are between 1Ω and 5Ω.

Power-On Reset (POR)

During initial start-up, both VCC and VIN voltage rise is monitored. Once the rising VCC voltage exceeds 3.8V (V_{CC_UVLO}) and VIN voltage exceeds 2.4V (V_{IN_UVLO}) for 120µs, normal operation of the driver is enabled. The PVCC voltage is not being monitored as it should be connected to VCC. Both VCC and VIN POR are gated to the TMON/FLT pin, which resumes normal TMON operation 120µs after both VCC and VIN are above their POR levels and no other faults occur. For UVLO function detail, see Table 5.

The AOZ5276QI must be powered up before the PWM input is applied. During start-up it is necessary for the PWM signal to go through a proper soft start sequence to minimize inrush current in the converter. Powering the module with a full duty cycle PWM signal applied may lead to a number of undesirable consequences.

PWM Input

The AOZ5276QI is compatible with 3.3V PWM input logic and supports Tri-State PWM. When the input is high impedance or left open, both the gate drive outputs will be turned off and the Low-Side and High-Side gates are actively held low. The PWM Threshold in Table 1 lists the thresholds for high-level and low-level logic, as well as Tri-State operation.

Table 1. PWM Input and Tri-State Thresholds

Parameters	V_{PWMH}	V_{PWML}	$V_{TRI(L)}$	$V_{TRI(H)}$
Thresholds	2.70V	0.65V	1.1V	2.1V

The AOZ5276QI is compatible with standard multiphase controllers as well as other controller IC's utilizing 3.3V PWM logic. If the PWM input is being pulled into and remains in the tri-state window for a set hold-off time (t_{TSSHD}), the driver will force both MOSFETs to their off state. When the PWM signal moves outside the tri-state window, the driver immediately resumes operation and drives the MOSFETs according to the PWM input.

This feature allows the controller to use PWM as a method of forcing both MOSFETs to be off. For the condition that the PWM input is floating, the pin will be pulled into the Tri-State Clamp Voltage (V_{PWM_FLOAT}) internally, thus forcing both MOSFETs to a safe off state. Table 2 shows the logic truth table for PWM and EN inputs.

Table 2. GH and GL Operation Truth Table

PWM	EN	GH[7]	GL	High-Side MOSFET	Low-Side MOSFET
Tri-State	X	0	0	OFF	OFF
0	1	0	1	OFF	OFF
1	1	1	0	ON	OFF
X	0	0	0	OFF	OFF

Note:

7. GH signal is not available on package level.

Current Monitoring (IMON)

An accurate Current Sense Amplifier monitors the current through the Low-Side MOSFET. A voltage signal proportional to that current appears at the IMON (Pin 38), relative to REFIN (Pin 39), with current sense gain of 5mV/A. Both IMON and REFIN should be connected to the appropriate current sense inputs of the controller. This IMON signal effectively eliminates the needs of using external sense resistor or inductor DCR sensing.

Figure 9 shows the Low-Side MOSFET current sense mechanism. After the falling edge of the PWM, there are two delays:

1. The expected propagation delay from PWM to VSWH (t_{PDLU})
2. The blanking delay to allow time for the transition to settle (t_{FALL_BLK})

The IMON signal emulates the actual inductor current waveform.

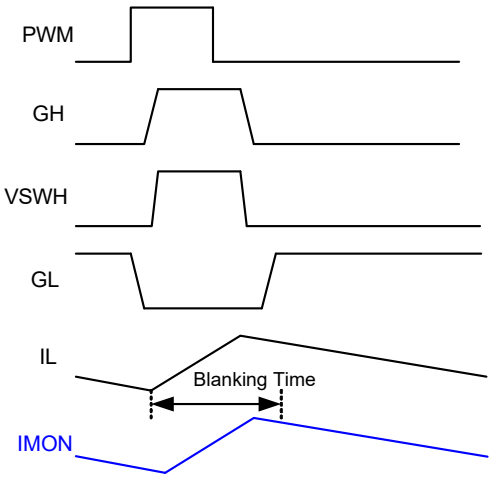


Figure 9. Commutating Current Re-Construction at IMON

Temperature Monitoring (TMON/FLT)

AOZ5276QI monitors its internal temperature and provides a signal proportional to that temperature on the TMON/FLT pin. TMON/FLT has a voltage of 600mV at 0°C and temperature gain of 8mV/°C (A_{TMON_SLP}). Figure 10 shows a simplified functional representation. The top section represents the protection fault that will pull the output high. The mid-section shows the symbolic sensor and the output buffer. The bottom section will set the initial state of TMON/FLT before the module is active. The TMON/FLT pin is configured internally such that a user can tie multiple pins together externally and the resulting TMON/FLT bus will assume the voltage of the highest contributor (representing the highest temperature).

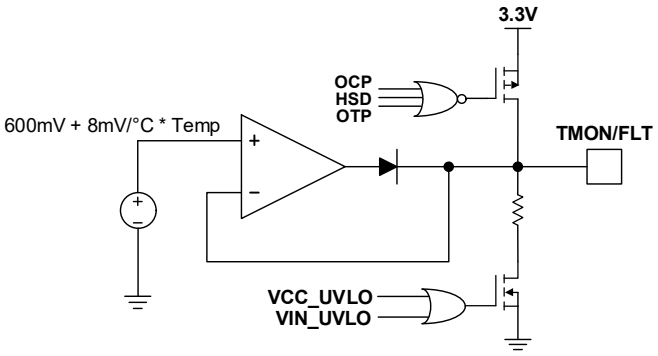


Figure 10. Temperature Monitor Internal Circuit

Zero Cross Detect (ZCD)

OCSET/ZCD pin controls the functions of ZCD. When OCSET/ZCD pin is left open or pulled up, ZCD function is being enabled.

ZCD will detect the valley current when Low-Side MOSFET is on. If the current is less than 2A (I_{ZCD_OFS}), the MOSFET will be turned off independent of PWM logic level. This is an automatic light load mechanism and suitable for most analog PWM controllers.

See Table 5 for details of ZCD function.

Negative Current Protection (NCP)

OCSET/ZCD pin also controls the function of NCP. When OCP threshold is set to any level with a resistor from OCSET/ZCD to AGND, NCP function becomes active.

For NCP function, the MOSFET will be turned off independent of PWM logic level if the current is less than -60 A (I_{NEG_OCP}). This is to protect the Low-Side MOSFET recovering from very high negative current. NCP will be released when negative current is less than 50A.

See Table 5 for details of NCP function.

Over Temperature Protection (OTP)

If the internal temperature exceeds the Over-Temperature threshold (T_{OTP}), the TMON/FLT (Pin 36) is pulled to 3.3V after 100ns ($t_{TMON/FLT}$) delay. Both High-Side and Low-Side MOSFETs are turned off under OTP condition. The TMON/FLT will remain in the fault mode until the junction temperature drops below the hysteresis threshold (T_{OTP_HYST}). At that point, the TMON/FLT and IMON pins resume normal operation. See Table 5 for OTP function detail.

Over Current Protection (OCP)

An Over Current Production (OCP) fault is detected when the current running through the power stage exceeds 120A (I_{LIM_DEF}). The OCP level can be set by using external resistor at OCSET/ZCD (Pin 37). During the initial 120µs (t_{OCP_SETUP}) after the part is enabled, the resistor value is detected and latched within the system to store the OCP threshold level. After OCP level is latched, the OCSET/ZCD pin will function as ZCD/NCP control only. If the OCP event is trigged 9 times (N_{OC_COUNT}) consecutively, TMON/FLT (Pin 36) will be internally pulled to 3.3V to indicate a fault condition.

The FAULT flag will be released by a power reset or the output current is 10A less than the OCP threshold. For OCP function detail, refer to Table 5.

OCSET/ZCD pin control 3 functions:

1. Zero Cross Detect (ZCD)
2. Negative Current Protection (NCP)
3. OCP Threshold Setting

See Table 3 for the OCSET/ZCD setting and corresponding functions.

Table 3. OCSET/ZCD Setting for OCP Level, ZCD and NCP Function

OCSET/ ZCD	Within 120µs after power-up	After 120µs since IC power-up	
	OCP Level	ZCD	NCP
Open	120A	Enable	Not Active
80kΩ	100A	Not Active	Enable
<25kΩ	85A	Not Active	Enable

High-Side Short Detect (HSD)

When Low-Side MOSFET is on, the voltage across the High-Side MOSFET is monitored. A High-Side short condition is detected if the voltage is higher than the HSD threshold. The TMON/FLT pin will be pulled high to indicate a fault condition. The power module will not change the High-Side and Low-Side MOSFET status until the fault condition is released by power cycling.

Pre-Over Voltage Protection (Pre-OVP)

AOZ5276QI monitors VOUT (VOS) during the power up period. If an abnormally high VOUT is detected during this time, the SPS will turn on the LS FET until the FAULT clears. Pre-OVP is active when the SPS is enabled or disabled. The fault will be released when VOUT falls below 2.3 V. See Table 5 for Pre-OVP function detail.

FAULT Reporting

These 3 protection functions will trigger the fault reporting at TMON/FLT (Pin 36):

1. VCC and VIN Under-Voltage Lock-Out (UVLO)
2. Over-Current Protection (OCP)
3. Over-Temperature Protection (OTP)
4. High-Side Short Detect (HSD)

For UVLO function, TMON/FLT will be pulled down to ground to indicate under voltage fault condition.

For OCP, OTP and HSD functions, TMON/FLT will be pulled high to 3.3 V to indicate the fault condition. For OTP, both High-Side and Low-Side MOSFETs will be turned off to protect the module from over-heating. The PWM controller should quickly recognize when it is outside normal operating conditions.

All of the above faults are summarized in Table 4 and 5.

Table 4. Fault Reporting Summary

Fault	Response
VCC and VIN UVLO	Fault Flag pulled down only
OCP	Fault Flag pulled to 3.3V after 9 consecutive occurrences
OTP	Fault Flag pulled to 3.3V Both MOSFETs are off
HSD	Fault Flag pulled to 3.3V only

Table 5. Protection Feature and Function Summary

Protection	Entry Condition	Action	Release
Over Current Protection (OCP) See Protection Case	• IMON peak sensing • 9 consecutive occurrences of over current condition • Current level setting with OCSET using external resistor: 120A (Default) / 100A / 85A	• TMON/FLT pull up to 3.3V • IMON continues to generate current information	• Power reset (UVLO_VCC or UVLO_VIN) or • 3 consecutive cycles of load current below OCP falling threshold or • PWM to tri-state for 2µs
Negative Current Protection (NCP)	• IMON valley sensing • Blanking time (LS on state) is 100ns	• LS off until NCP release	• 10 A higher than NCP
Zero Current Detection (ZCD)	• OCSET/ZCD is floating or pulled high • IMON valley sensing • Inductor current <2A (as reported by IMON) • Blanking time of (LS on state) is 100 ns	• LS off until next cycle	• PWM rising
High-Side Short Detection (HSD)	• PHASE sensing • PHASE voltage above 200 mV during LS on state • Blanking time of (LS on state) is 65ns	• TMON/FLT pull up to 3.3V • No change in HS and LS ON/OFF status until fault is cleared	• Power reset (UVLO_VCC or UVLO_VIN)
Pre-OVP Protection (POVP) (AOZ5276QI ONLY)	• VOUT(VOS) sensing • VOUT voltage above 2.8V • POVP is active when the SPS is enabled or disabled	• LS on	• VOUT voltage below 2.3V (0.5V hysteresis)
Over Temperature Protection (OTP)	• TMON sensing • TMON voltage above 1720mV (140°C)	• Turn off both HS and LS • TMON/FLT pull up to 3.3V	• TMON voltage below 1600mV (125°C)
Power Stage Supply UVLO (VIN_UVLO)	• VIN sensing • VIN voltage below 2V	• HS, LS, TMON & IMON are disabled • TMON/FLT pull low	• VIN voltage above 2.4V (400mV Hysteresis)
Driver IC Supply UVLO (VCC_UVLO)	• VCC sensing • VCC voltage below 3.4V • No PVCC sensing	• HS, LS, TMON & IMON are disabled • TMON/FLT pull low • IMON shorted to REFIN	• VCC voltage above 3.8V (400 mV Hysteresis)

PCB Layout Guideline

AOZ5276QI is a high current module rated for operation up to 1MHz. This requires fast switching speed to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package eliminates driver-to-MOSFET gate pad parasitics of the package or PCB.

While excellent switching speed is achieved, correspondingly high levels of dv/dt and di/dt will be observed throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout the critical requirement is to minimize the area of the primary switching current loop, formed by the VIN, VSWH and the input bypass capacitor CVIN. The PCB design is simplified because of the optimized pin out in AOZ5276QI. The bulk of VIN and PGND pins are located adjacent to each other and the input capacitors should be placed as close as possible to these pins (as shown in Figure 11). The area of the secondary switching loop, formed by Low Side MOSFET, output inductor and output capacitor COUT is the next critical parameter and requires the second layer or “Inner 1” to be the PGND plane. Via should be placed near input capacitors’ PGND pads.

While AOZ5276QI is optimally efficient, it still requires attention to thermal design in order to achieve maximum power dissipation. MOSFETs in the package are directly attached to individual exposed pads to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal relief pads should be placed correspondingly to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the high voltage system input, is desirable and VIAs should be provided near the device to connect the VIN pads to the power plane. Significant amount of heat is dissipated through multiple PGND pins. A large copper area connected to the PGND pins in addition to the system ground plane through VIAs will further improve thermal dissipation.

As shown in Figure 11, the top most layer of the PCB should comprise of wide and exposed copper area for the primary AC current loop that runs along VIN pad originating from the input capacitors that are mounted to a large PGND pad. They serve as thermal relief as heat flows down to the VIN exposed pad that fan out to a wider area. Adding VIAs will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

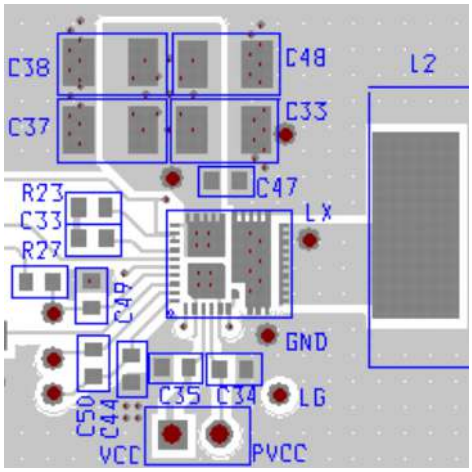


Figure 11. Top Layer of Demo Board, VIN, VSWH and PGND Copper Pads

As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spike appear at the VSWH terminal which are caused by the large internal di/dt produced by the in-package parasitic. To minimize the effects of this interference, the VSWH terminal at which the main inductor L is mounted to, is sized just so the inductor can physically fit. The goal is to employ the least amount of copper area for this VSWH terminal just enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH pad or Inductor terminal, is voided and the shape of this void is replicated descending down through the rest of the layers. Refer to Figure 12.

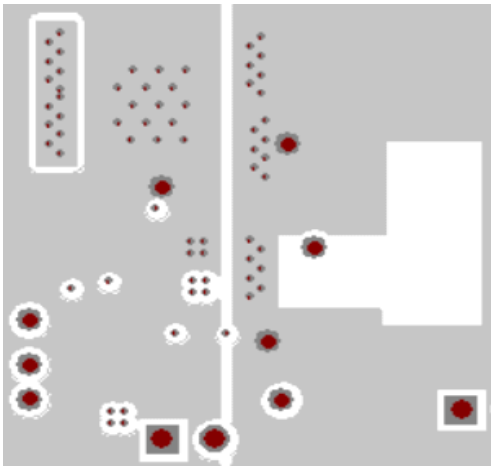
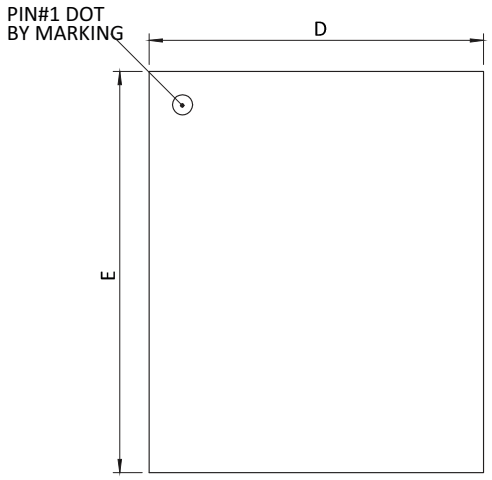


Figure 12. Bottom Layer of PCB

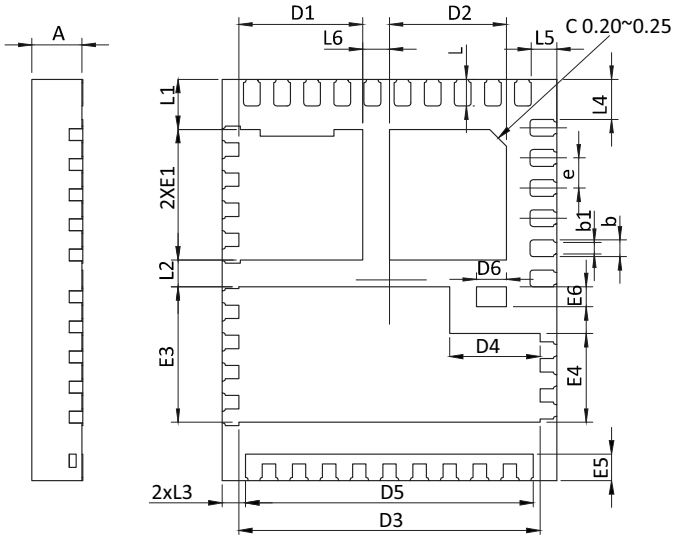
Positioning VIAs through the landing pattern of the VIN and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer. (See RECOMMENDED LANDING PATTERN AND VIA PLACEMENT section).

The exposed pads dimensional footprint of the 5x6 QFN package is shown on the package dimensions page. For optimal thermal relief, it is recommended to fill the PGND and VIN exposed landing pattern with 10mil diameter VIAs. 10mil diameter is a commonly used via diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127µm) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.

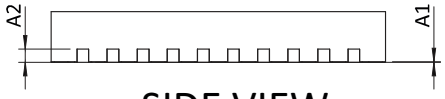
Package Dimensions, QFN5x6-39L



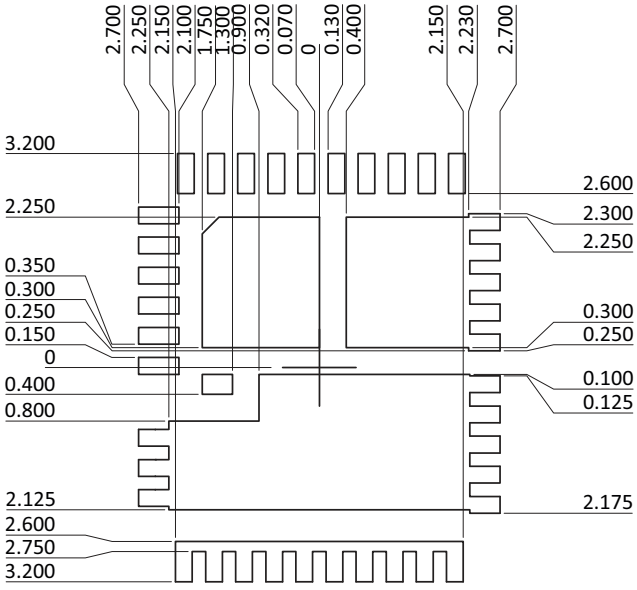
FRONT VIEW



SIDE VIEW BOTTOM VIEW



SIDE VIEW



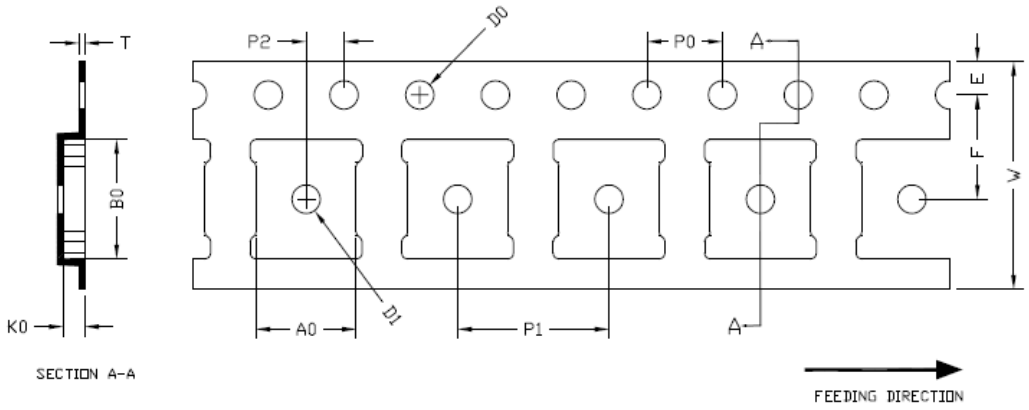
RECOMMANDED LAND PATTERN

SYMBOLS	DIMENSION IN MM.			DIMENSION IN INCH.		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20REF			0.008REF		
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	1.75	1.85	1.95	0.069	0.073	0.077
D2	1.65	1.75	1.85	0.065	0.069	0.073
D3	4.40	4.50	4.60	0.173	0.177	0.181
D4	1.26	1.36	1.46	0.050	0.054	0.057
D5	4.20	4.30	4.40	0.165	0.169	0.173
D6	0.35	0.45	0.55	0.014	0.018	0.022
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	1.85	1.95	2.05	0.073	0.077	0.081
E3	1.93	2.03	2.13	0.076	0.080	0.084
E4	1.20	1.30	1.40	0.047	0.051	0.055
E5	0.30	0.40	0.50	0.012	0.016	0.020
E6	0.20	0.30	0.40	0.008	0.012	0.016
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.65	0.75	0.85	0.026	0.030	0.033
L2	0.30	0.40	0.50	0.012	0.016	0.020
L3	0.25	0.35	0.45	0.010	0.014	0.018
L4	0.50	0.60	0.70	0.020	0.024	0.028
L5	0.28	0.38	0.48	0.011	0.015	0.019
L6	0.30	0.40	0.50	0.012	0.016	0.020
b	0.15	0.25	0.35	0.006	0.010	0.014
b1	0.08	0.18	0.28	0.003	0.007	0.011
e	0.45BSC			0.018BSC		

NOTE
1.CONTROLLING DIMENSION IS MILLIMETER.
2.CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN5x6-39L

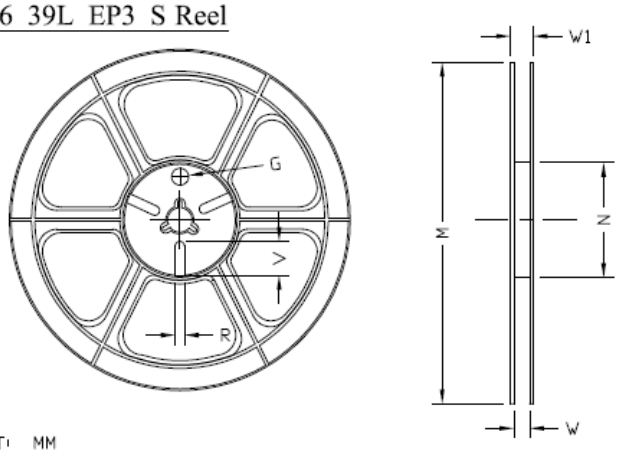
QFN5x6_39L_EP3_S Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	W	E	F	P0	P1	P2	T
QFN5X6	5.30 ±0.10	6.30 ±0.10	1.15 ±0.10	ø1.50 +0.10 −0.00	ø1.50 +0.20 −0.00	12.00 +0.30 −0.10	1.75 ±0.10	5.50 ±0.05	4.00 ±0.10	8.00 ±0.10	2.00 ±0.05	0.30 ±0.03

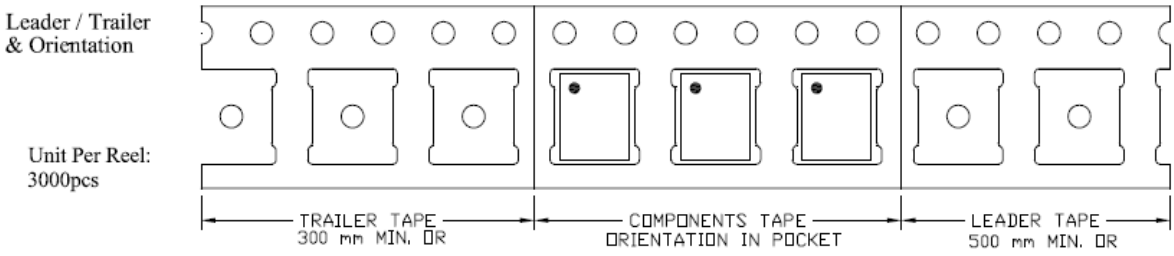
QFN5x6_39L_EP3_S Reel



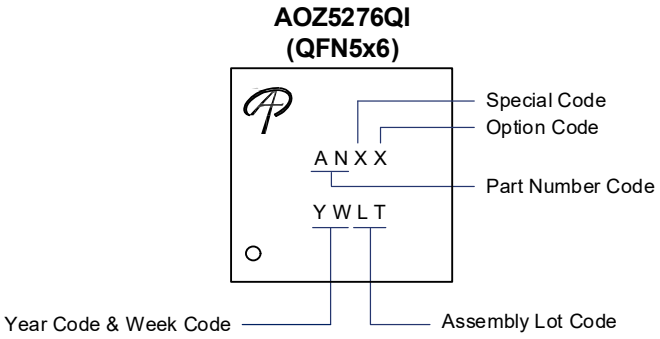
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330 ±0.50	ø97.00 ±0.10	13.0 ±0.30	17.40 ±1.00	ø13.0 +0.5 −0.2	10.6	2.00 ±0.50	---	---	---

QFN5x6_39L_EP3_S Tape



Part Marking



Part Number	Code
AOZ5276QI	AN00
AOZ5276QI-01	AN01